

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The 2SK3326 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

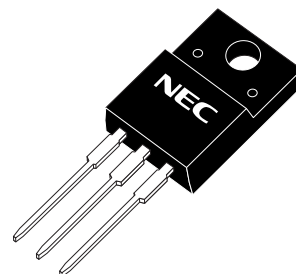
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3326	Isolated TO-220

FEATURES

- Low gate charge :
Q_G = 22 nC TYP. (V_{DD} = 400 V, V_{GS} = 10 V, I_D = 10 A)
- Gate voltage rating : ±30 V
- Low on-state resistance :
R_{DS(on)} = 0.85 Ω MAX. (V_{GS} = 10 V, I_D = 5.0 A)
- Avalanche capability ratings
- Isolated TO-220(MP-45F) package

(Isolated TO-220)

**ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)**

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	500	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS(AC)}	±30	V
Drain Current (DC)	I _{D(DC)}	±10	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±40	A
Total Power Dissipation (T _C = 25°C)	P _T	40	W
Total Power Dissipation (T _A = 25°C)	P _T	2.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	10	A
Single Avalanche Energy ^{Note2}	E _{AS}	10.7	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

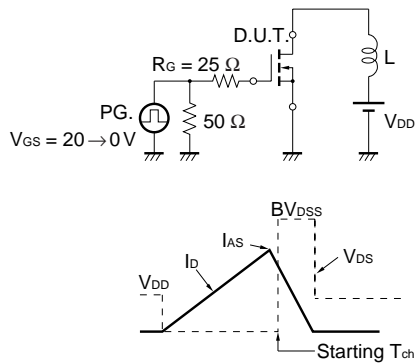
2. Starting T_{ch} = 25 °C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

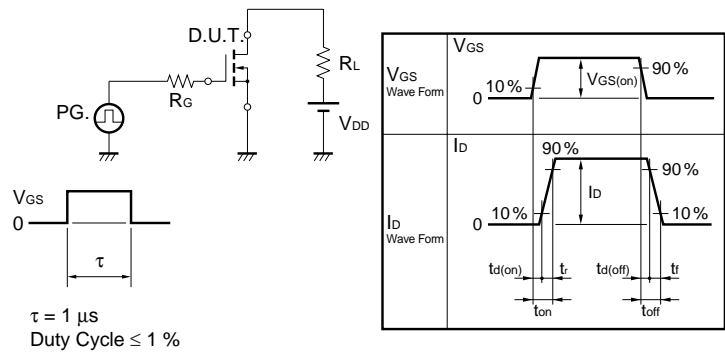
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Leakage Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V			100	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 5.0 A	2.0	4.0		S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 5.0 A		0.68	0.85	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		1200		pF
Output Capacitance	C _{oss}			190		pF
Reverse Transfer Capacitance	C _{rss}			10		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 5.0 A, V _{GS(on)} = 10 V, R _G = 10 Ω, R _L = 60 Ω		21		ns
Rise Time	t _r			11		ns
Turn-off Delay Time	t _{d(off)}			40		ns
Fall Time	t _f			9.5		ns
Total Gate Charge	Q _G	V _{DD} = 400 V, V _{GS} = 10 V, I _D = 10 A		22		nC
Gate to Source Charge	Q _{GS}			6.5		nC
Gate to Drain Charge	Q _{GD}			7.5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V, di/dt = 50 A/μs		0.5		μs
Reverse Recovery Charge	Q _{rr}			2.6		μC

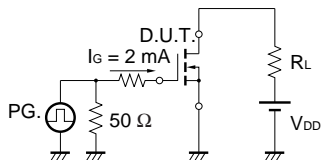
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS(T_A = 25 °C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

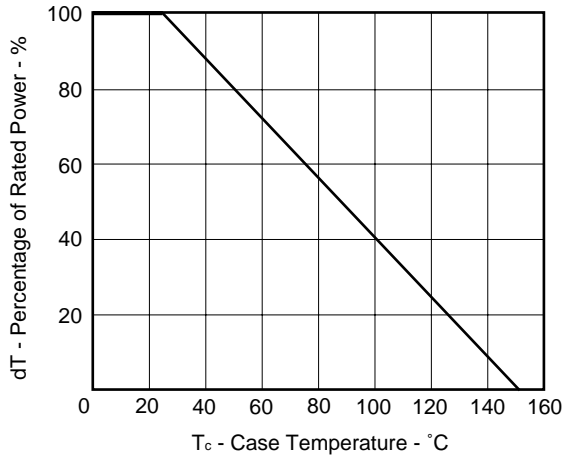


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

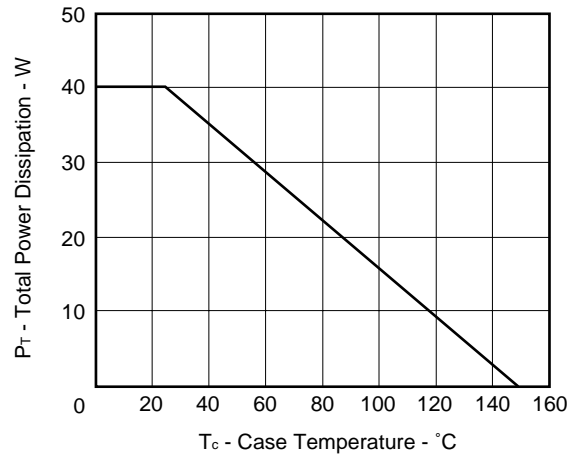


Figure3. FORWARD BIAS SAFE OPERATING AREA

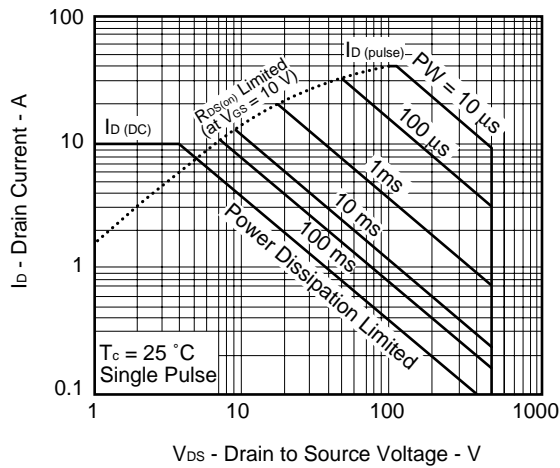


Figure4. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

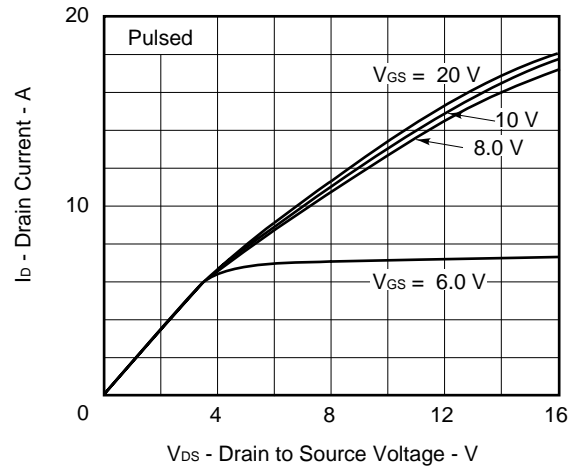


Figure5. DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE

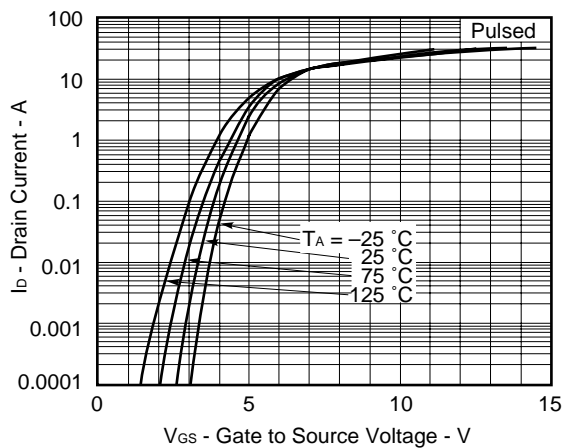


Figure6. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

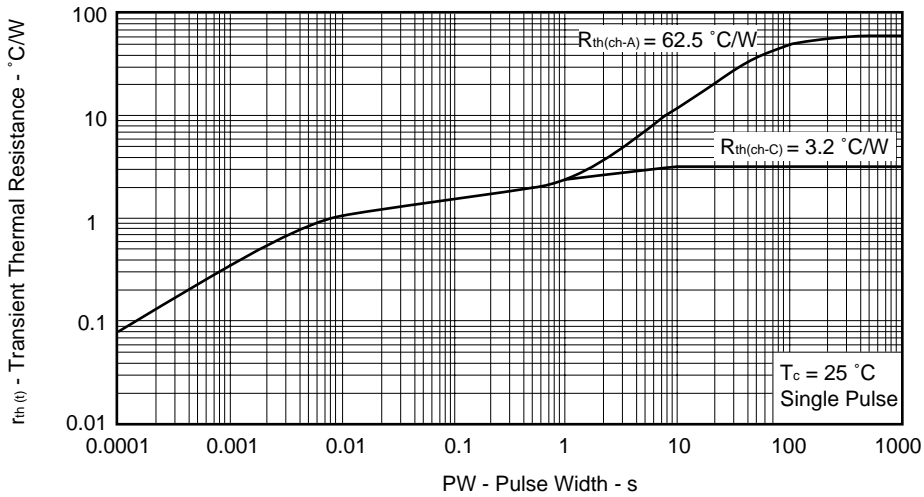


Figure7. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

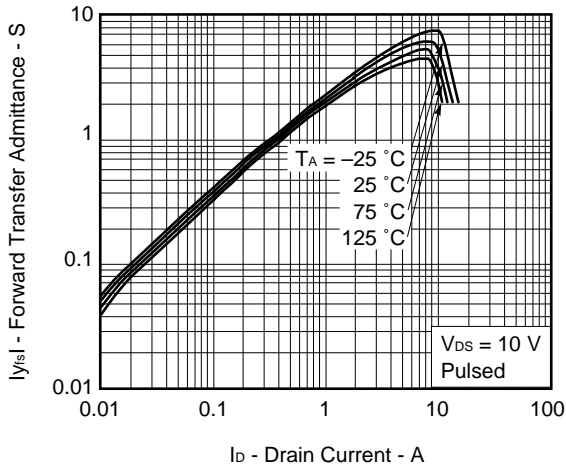


Figure8. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

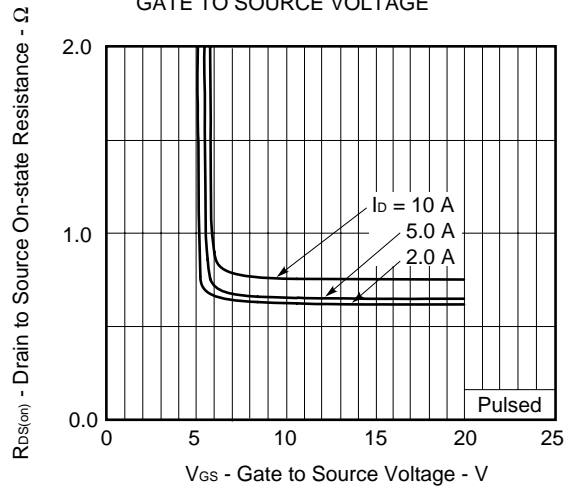


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

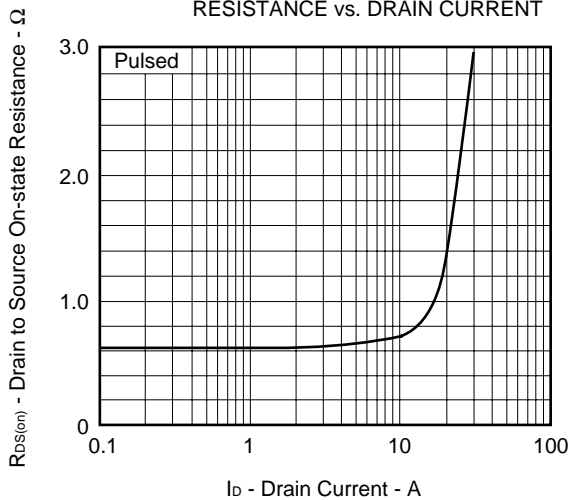


Figure10. GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

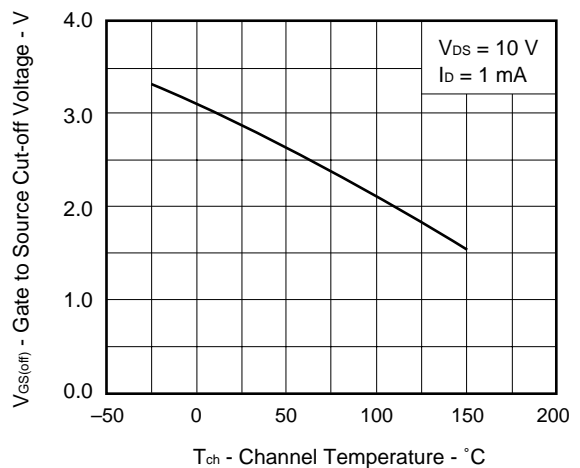


Figure11. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

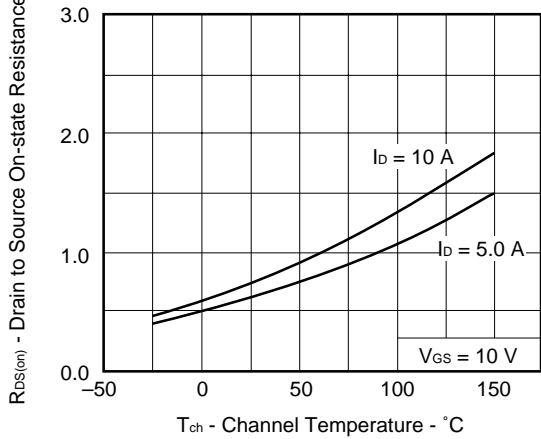


Figure12. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

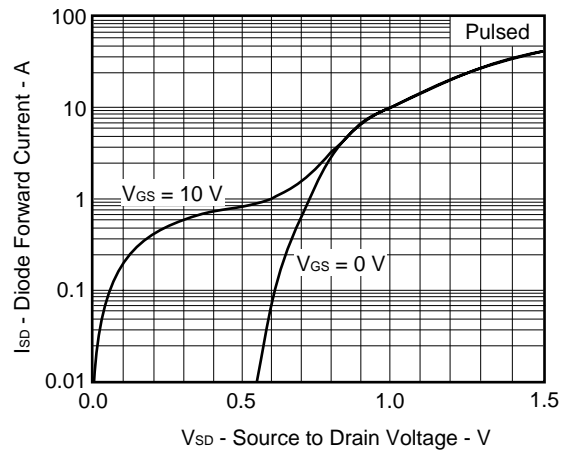


Figure13. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

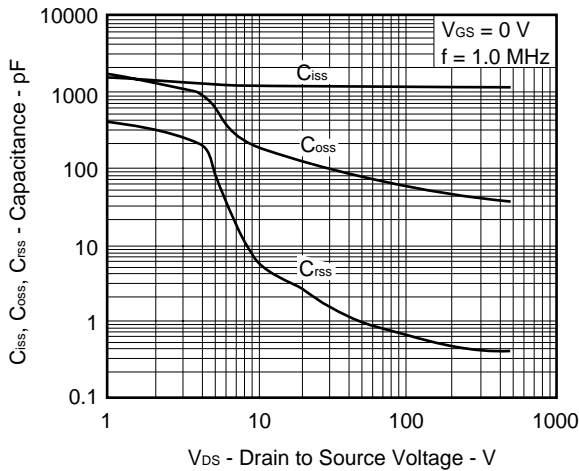


Figure14. SWITCHING CHARACTERISTICS

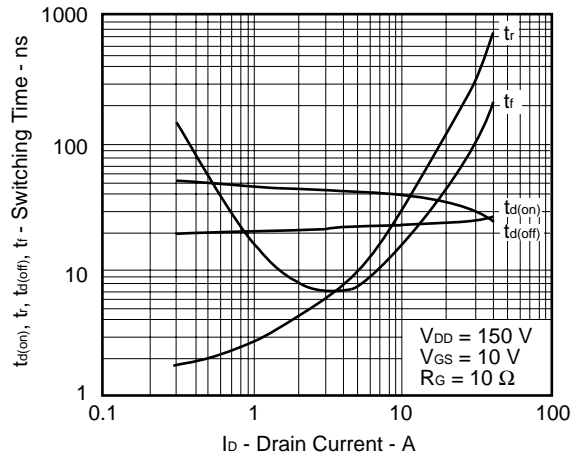


Figure15. REVERSE RECOVERY TIME vs. DRAIN CURRENT

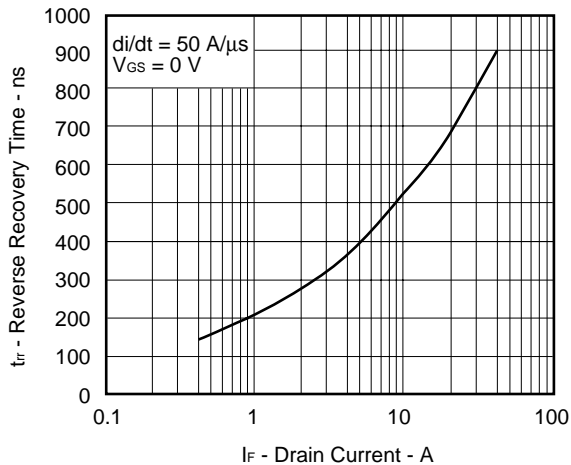


Figure16. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

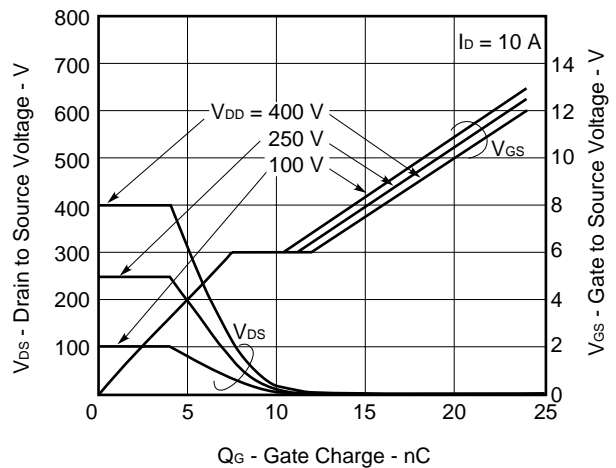


Figure17. SINGLE AVALANCHE ENERGY vs STARTING CHANNEL TEMPERATURE

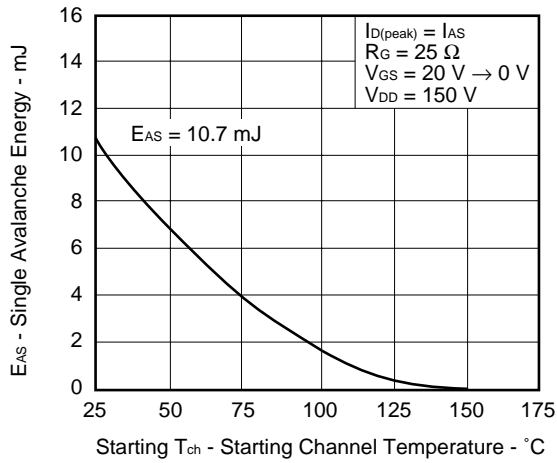
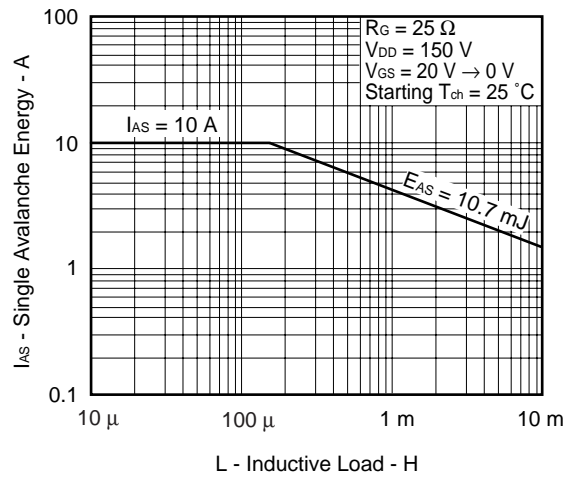
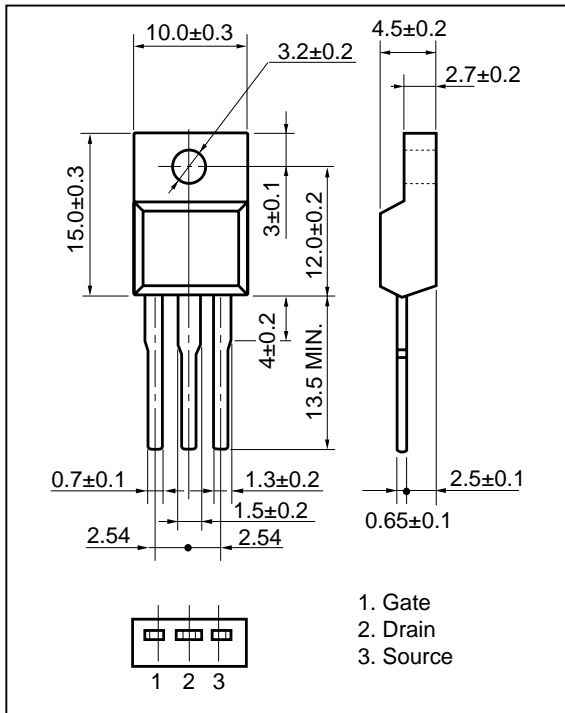


Figure18. SINGLE AVALANCHE ENERGY vs INDUCTIVE LOAD

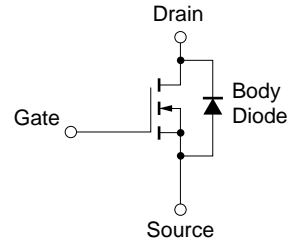


PACKAGE DRAWING (Unit: mm)

Isolated TO-220(MP-45F)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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