To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS FIELD EFFECT TRANSISTOR
2SK3365

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3365 is N-Channel MOS Field Effect Transistor designed for DC/DC converters application of notebook computers.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3365	TO-251 (MP-3)
2SK3365-Z	TO-252 (MP-3Z)

FEATURES

- Low on-resistance
  $R_{DS(on)1}$ = 14 mΩ (MAX.) (V_{GS} = 10 V, I_D = 15 A)
  $R_{DS(on)2}$ = 21 mΩ (MAX.) (V_{GS} = 4.5 V, I_D = 15 A)
  $R_{DS(on)3}$ = 29 mΩ (MAX.) (V_{GS} = 4.0 V, I_D = 15 A)
- Low C_{iss} : C_{iss} = 1300 pF (TYP.)
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±30	A
Drain Current (Pulse) **Note**	$I_{D(pulse)}$	±120	A
Total Power Dissipation (T_C = 25 °C)	P_T	36	W
Total Power Dissipation (T_A = 25 °C)	P_T	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

Note PW ≤ 10 μs, Duty cycle ≤ 1%

THERMAL RESISTANCE

Channel to case Thermal Resistance	$R_{th(ch-C)}$	3.48	°C/W
Channel to ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

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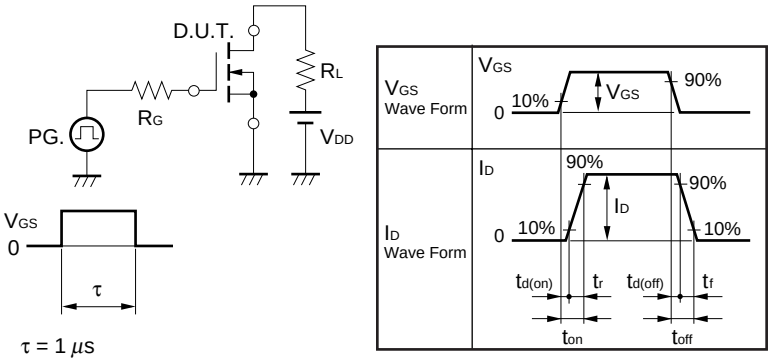
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

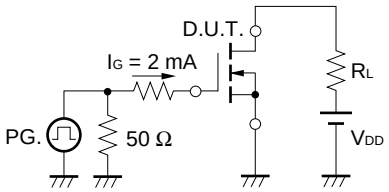
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 15 A		11.5	14	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 15 A		15.2	21	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.0 V, I_D = 15 A		18	29	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 15 A	8.0	16.0		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		1300		pF
Output Capacitance	C_{oss}			405		pF
Reverse Transfer Capacitance	C_{rss}			190		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 15 A, V_{GS} = 10 V, V_{DD} = 15 V,		37		ns
Rise Time	t_r	R_G = 10 Ω		500		ns
Turn-off Delay Time	$t_{d(off)}$			75		ns
Fall Time	t_f			95		ns
Total Gate Charge	Q_G	I_D = 30 A, V_{DD} = 24 V, V_{GS} = 10 V		25		nC
Gate to Source Charge	Q_{GS}			4.5		nC
Gate to Drain Charge	Q_{GD}			7.0		nC
Body Diode forward Voltage	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V		35		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		32		nC

TEST CIRCUIT 1 SWITCHING TIME



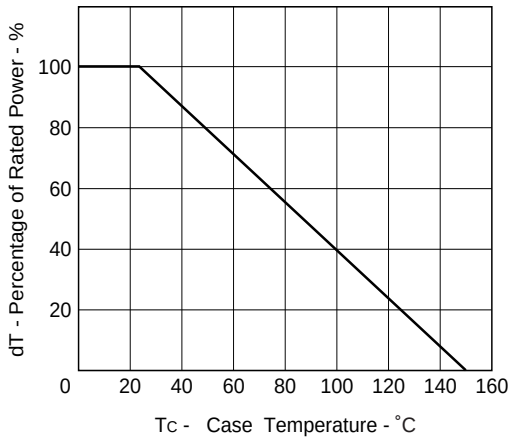
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

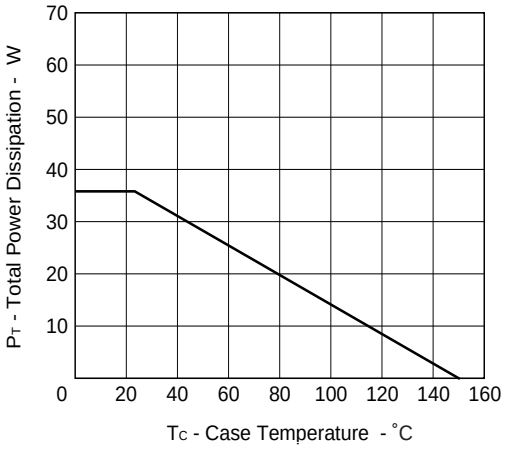


TYPICAL CHARACTERISTICS (T_A = 25°C)

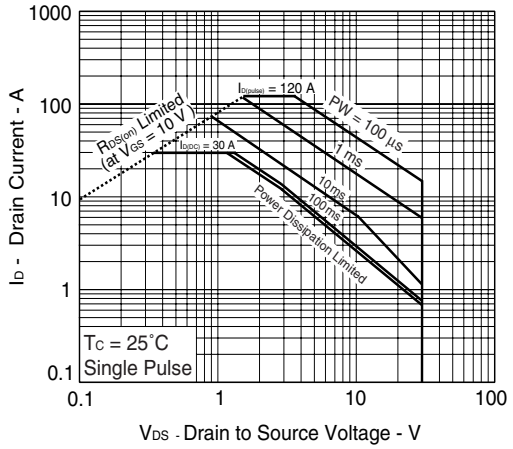
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



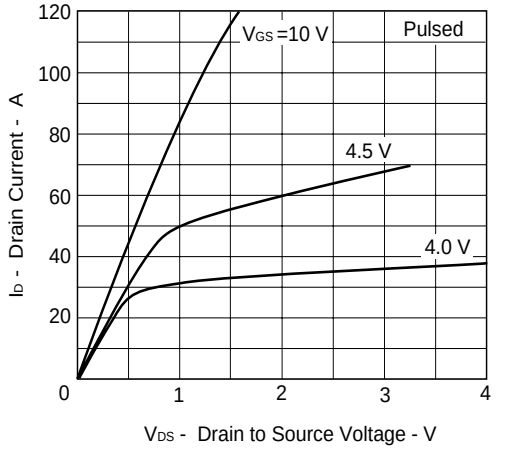
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



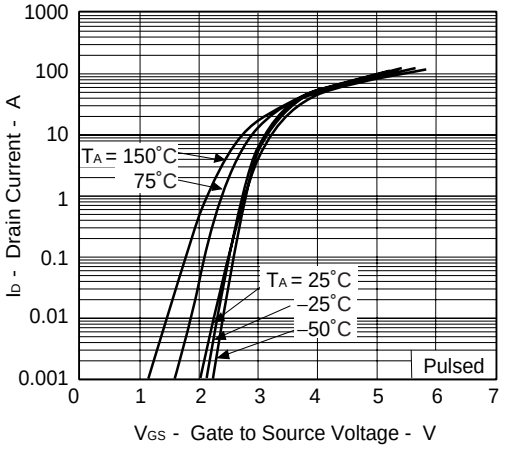
FORWARD BIAS SAFE OPERATING AREA



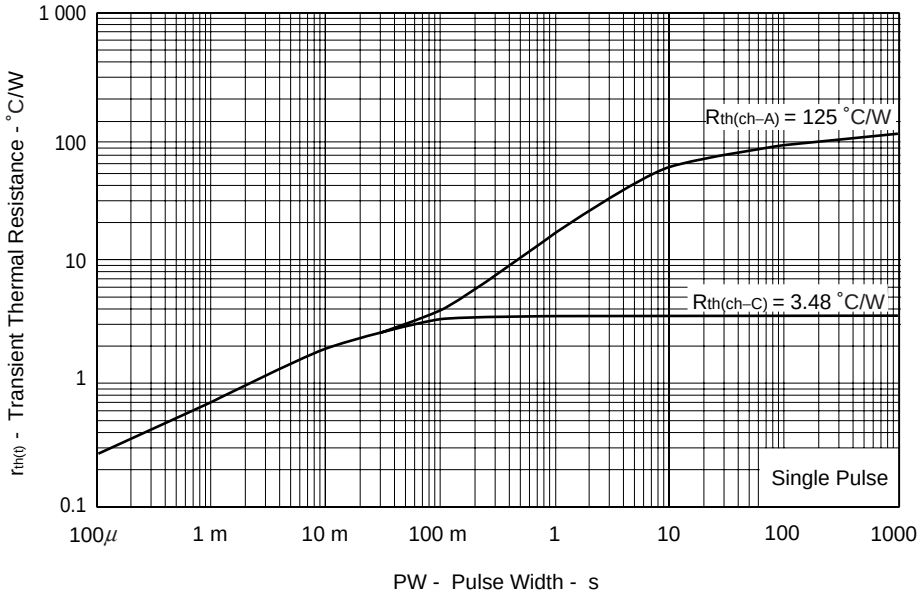
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



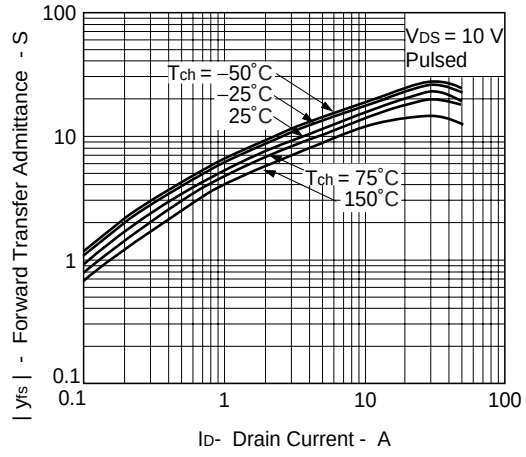
FORWARD TRANSFER CHARACTERISTICS



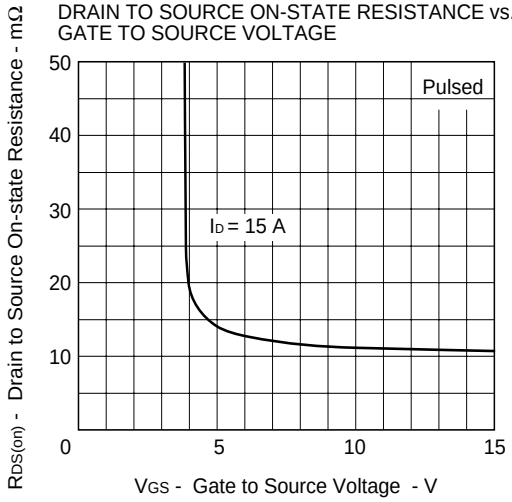
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



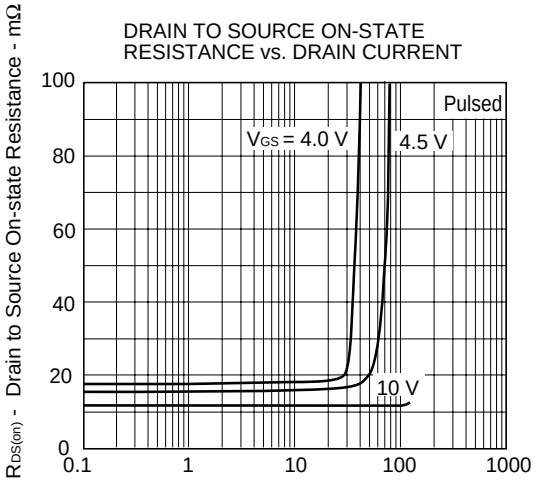
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



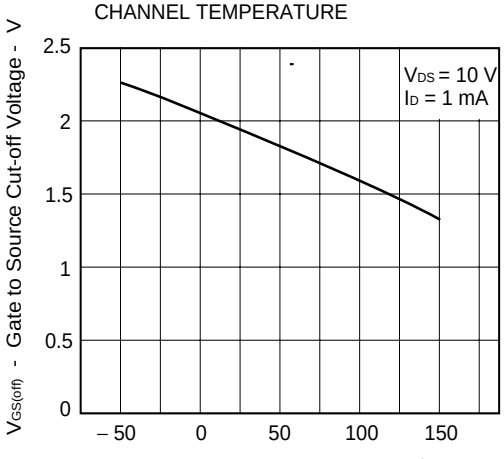
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



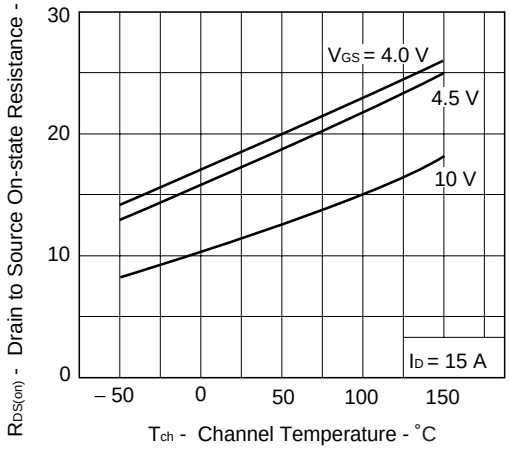
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



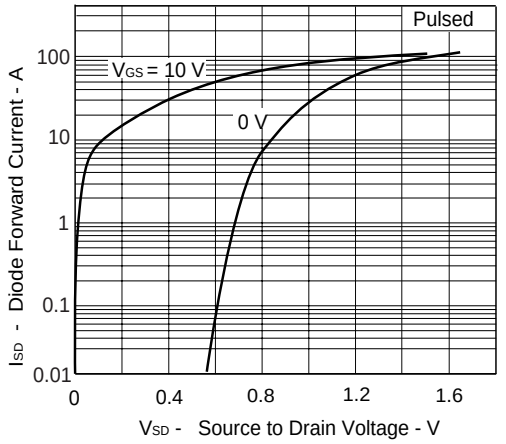
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



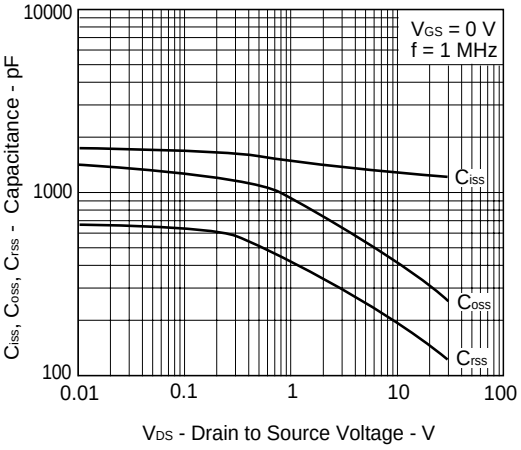
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



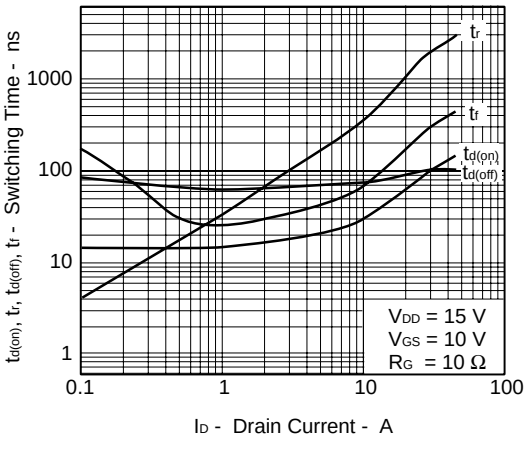
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



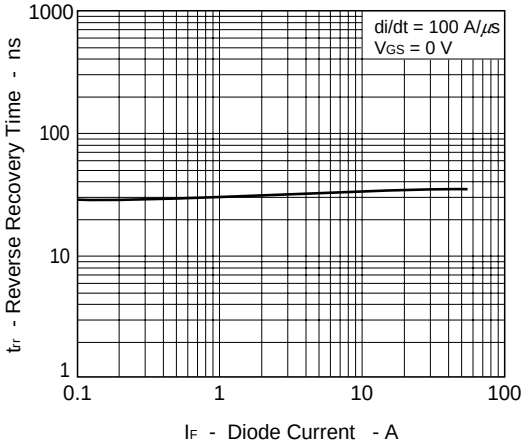
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



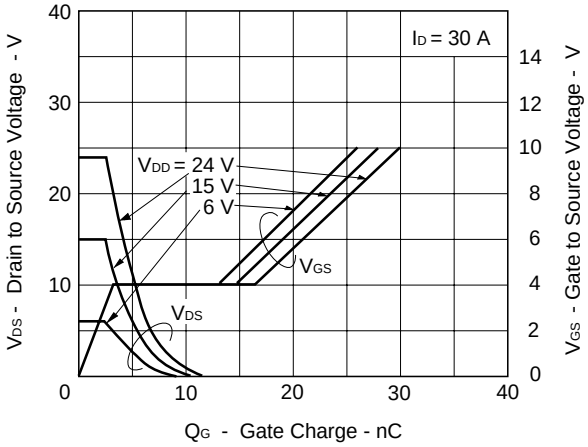
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

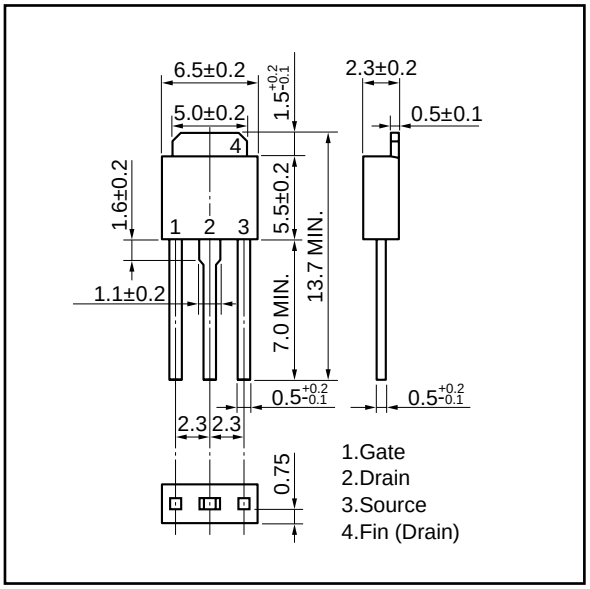


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

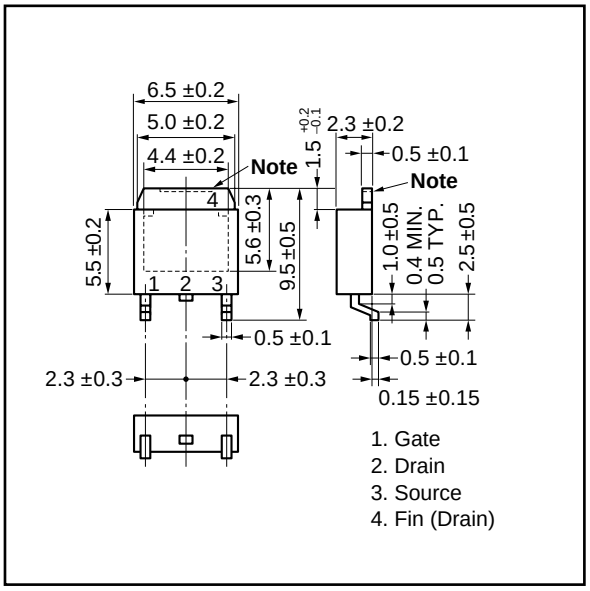


PACKAGE DRAWINGS (Unit: mm)

1) TO-251 (MP-3)

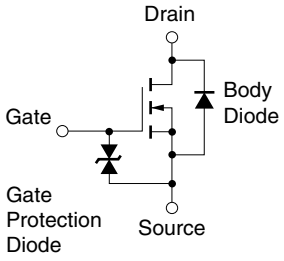


<R> 2) TO-252 (MP-3Z)



Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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