

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR

# 2SK3385

## SWITCHING

## N-CHANNEL POWER MOS FET

### DESCRIPTION

The 2SK3385 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

### FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 28 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 15 \text{ A)}$   
 $R_{DS(on)2} = 45 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 15 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1500 \text{ pF TYP.}$
- Built-in gate protection diode
- TO-251/TO-252 package

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 30$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 100$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	36	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current <sup>Note2</sup>	$I_{AS}$	22	A
Single Avalanche Energy <sup>Note2</sup>	$E_{AS}$	48	mJ

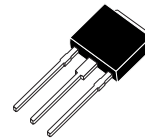
**Notes 1.**  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

**2.** Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = 30 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

### ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3385	TO-251 (MP-3)
2SK3385-Z	TO-252 (MP-3Z)

(TO-251)



(TO-252)



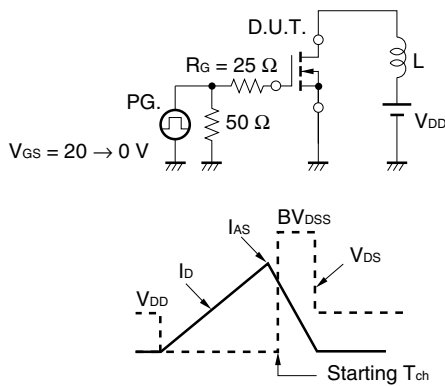
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

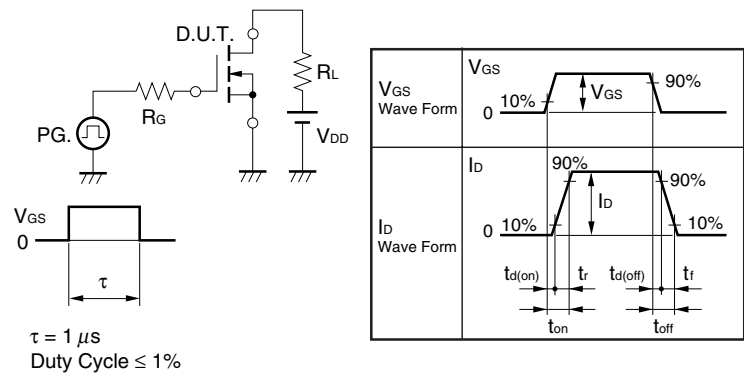
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance <b>Note</b>	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A	8	16		S
Drain to Source On-state Resistance <b>Note</b>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		22	28	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 15 A		31	45	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		1500		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		250		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		130		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 15 A		22		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V		250		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		77		ns
Fall Time	t <sub>f</sub>			77		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 48 V		30		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = 10 V		4.8		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 30 A		8.6		nC
Body Diode Forward Voltage <b>Note</b>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		1.0		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		44		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		79		nC

**Note** Pulsed

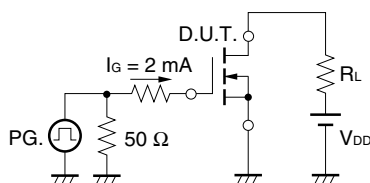
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

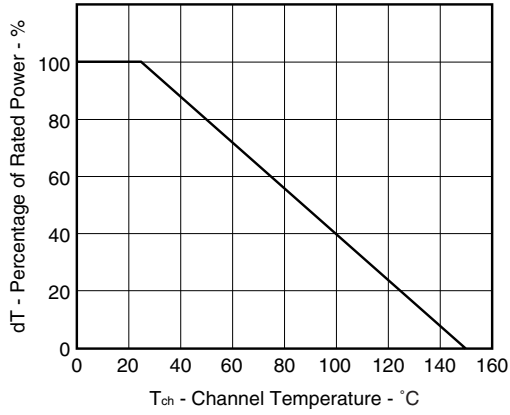


**TEST CIRCUIT 3 GATE CHARGE**

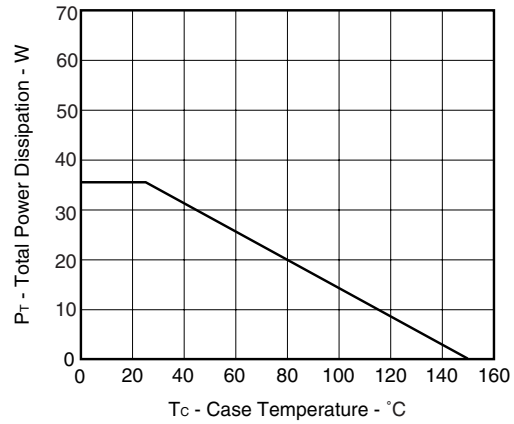


TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

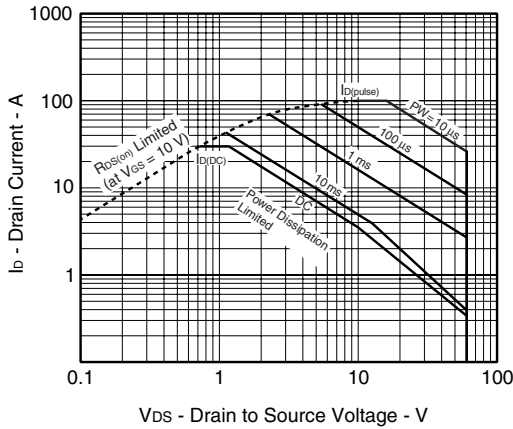
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



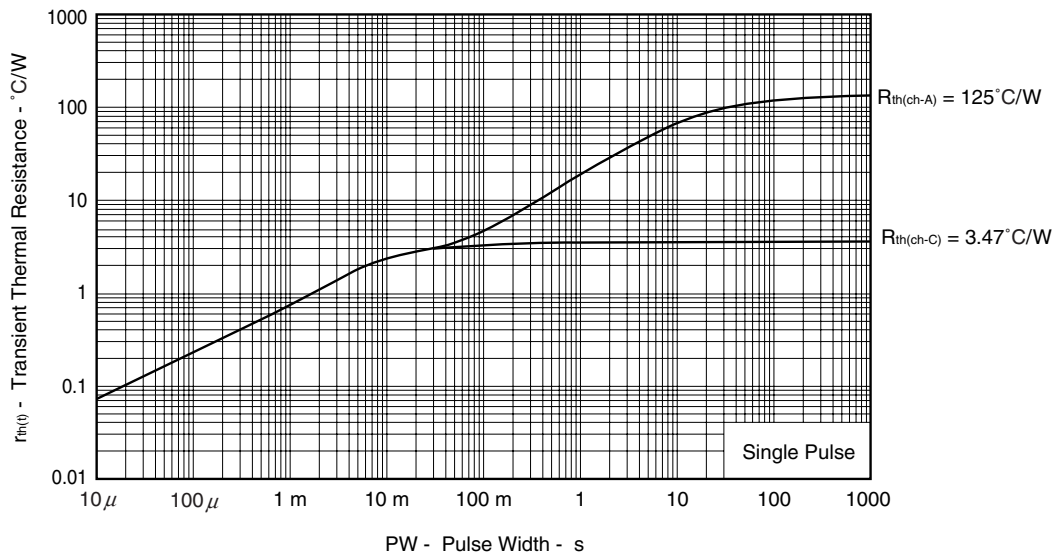
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



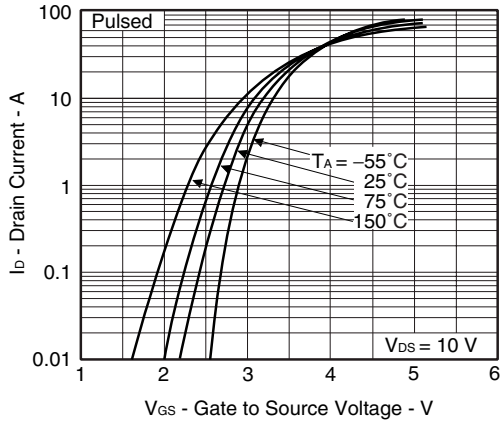
FORWARD BIAS SAFE OPERATING AREA



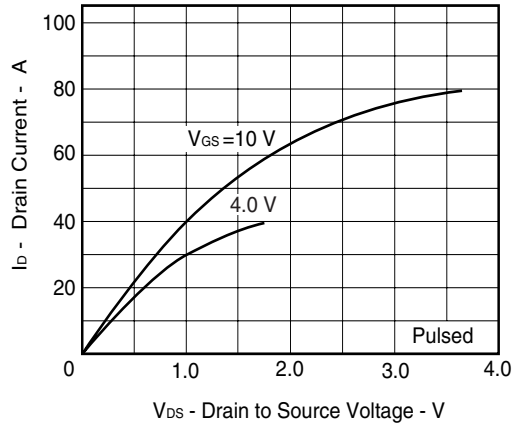
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



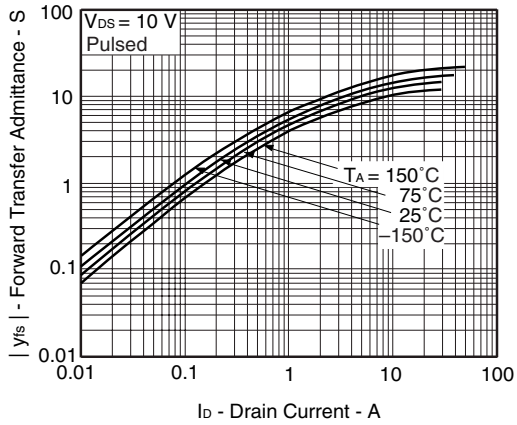
FORWARD TRANSFER CHARACTERISTICS



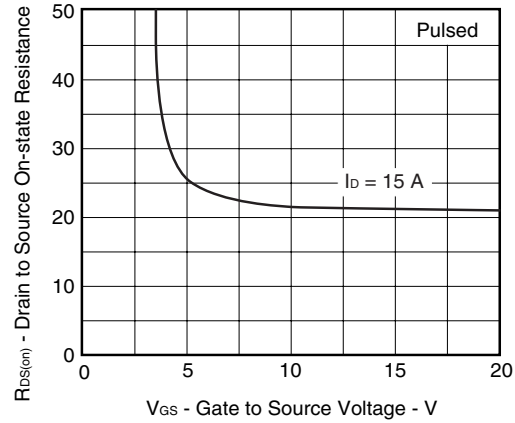
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



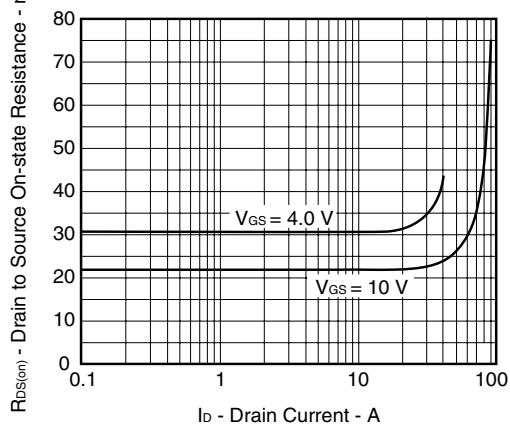
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



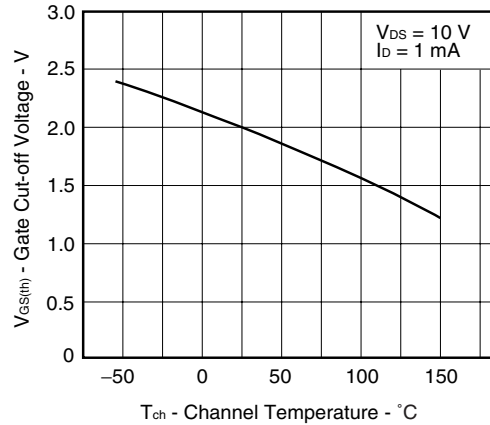
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



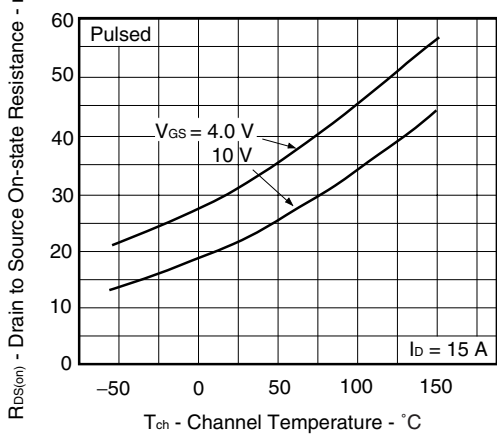
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



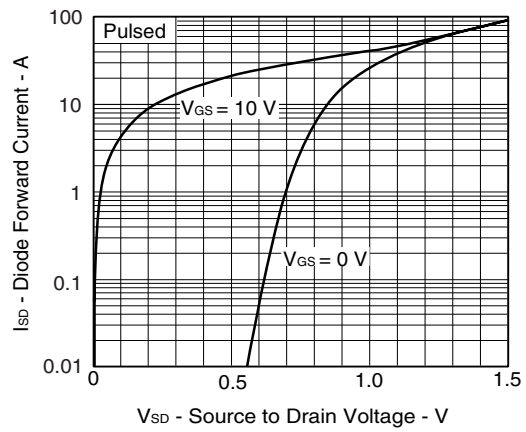
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



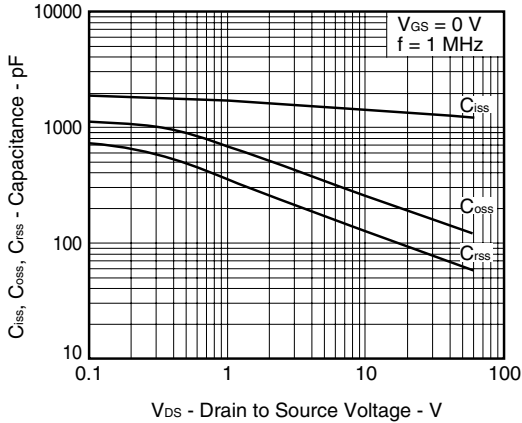
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



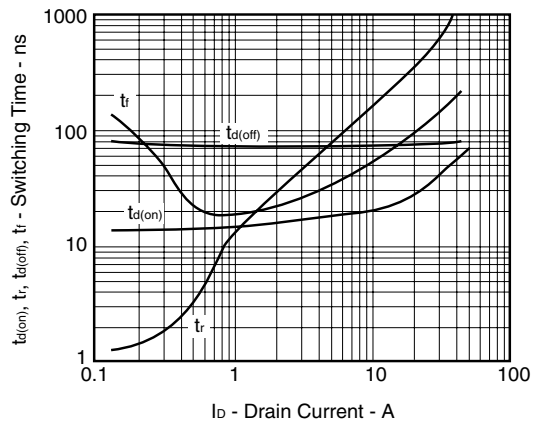
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



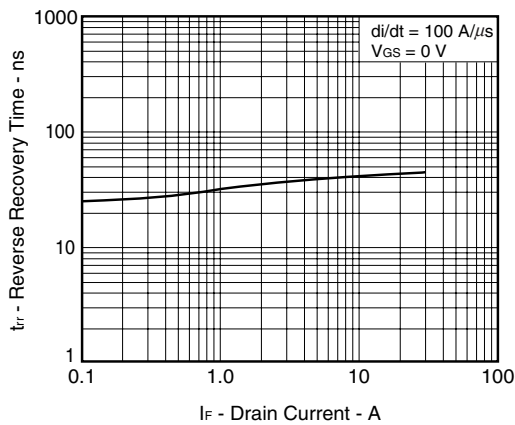
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



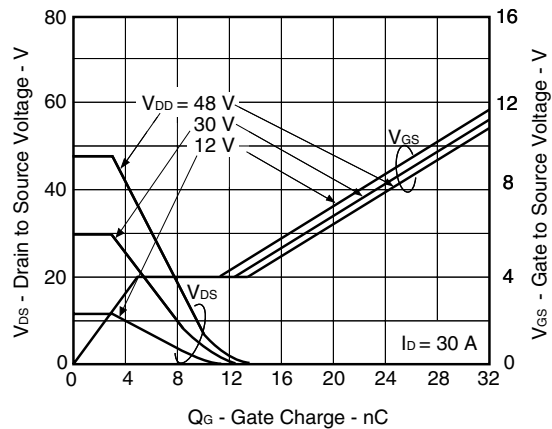
SWITCHING CHARACTERISTICS

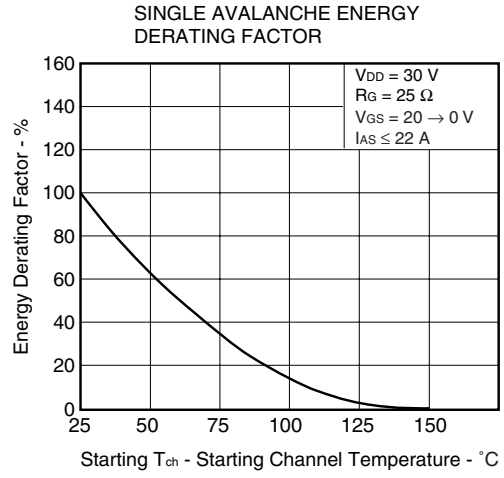
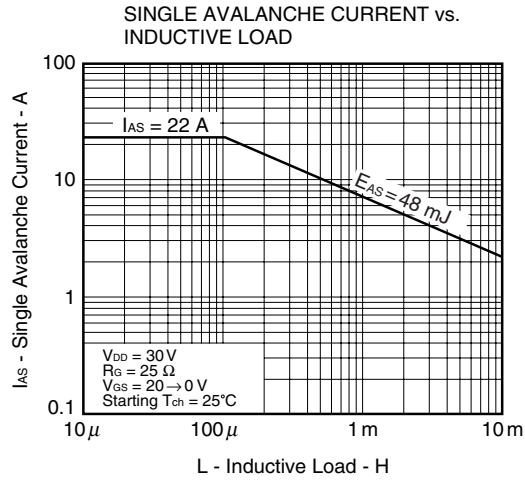


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



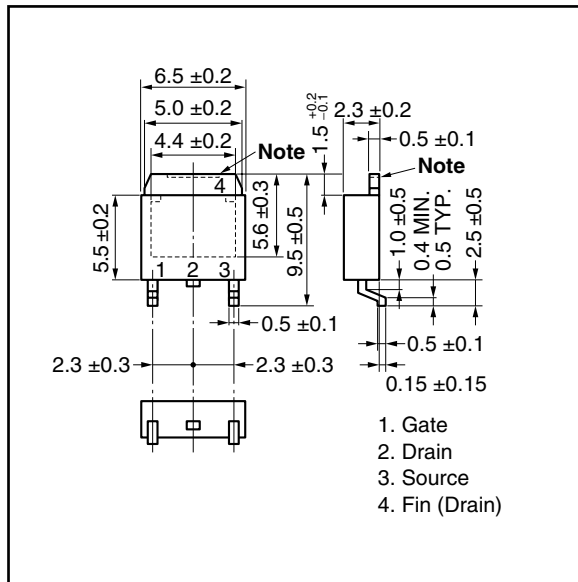
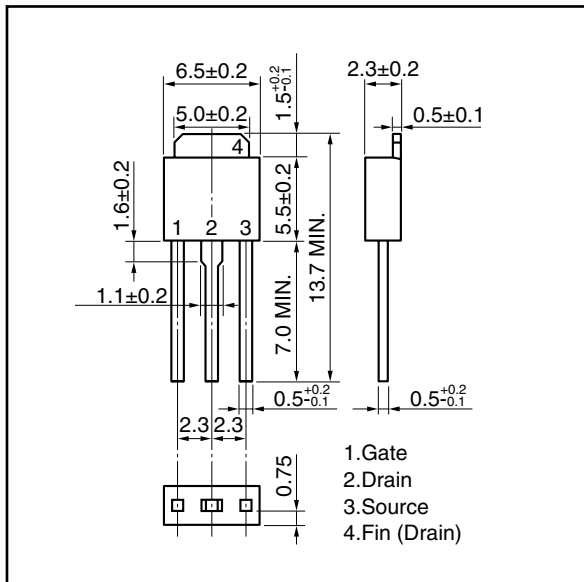




PACKAGE DRAWINGS (Unit: mm)

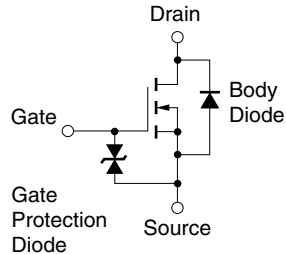
1) TO-251 (MP-3)

<R> 2) TO-252 (MP-3Z)



**Note** The depth of notch at the top of the fin is from 0 to 0.2 mm.

EQUIVALENT CIRCUIT



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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