To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

2SK3455

Phase-out/Discontinued

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3455 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3455	Isolated TO-220

FEATURES

- Low gate charge
  Q_G = 30 nC TYP. (V_{DD} = 400 V, V_{GS} = 10 V, I_D = 12 A)
- Gate voltage rating ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.60 Ω MAX. (V_{GS} = 10 V, I_D = 6.0 A)
- Avalanche capability ratings
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	500	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±12	A
Drain Current (Pulse) Note1	$I_{D(pulse)}$	±36	A
Total Power Dissipation (T_A = 25°C)	P_{T1}	2.0	W
Total Power Dissipation (T_C = 25°C)	P_{T2}	50	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	12	A
Single Avalanche Energy Note2	E_{AS}	103	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

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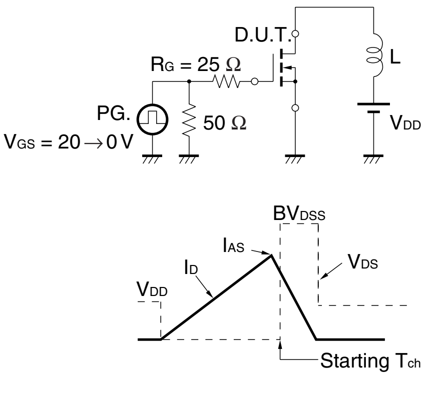
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

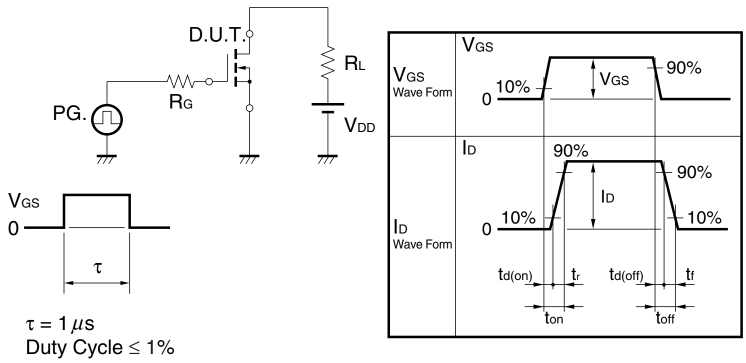
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 6.0 A	2.0			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 6.0 A		0.50	0.60	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		1620		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		10		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 6.0 A		24		ns
Rise Time	t_r	V_{GS} = 10 V		18		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		50		ns
Fall Time	t_f			15		ns
Total Gate Charge	Q_G	V_{DD} = 400 V		30		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		9		nC
Gate to Drain Charge	Q_{GD}	I_D = 12 A		11		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 12 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 12 A, V_{GS} = 0 V		1.5		μs
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/ μs		11		μC

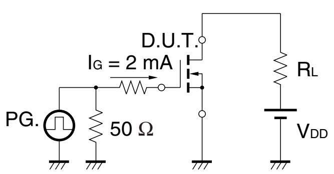
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

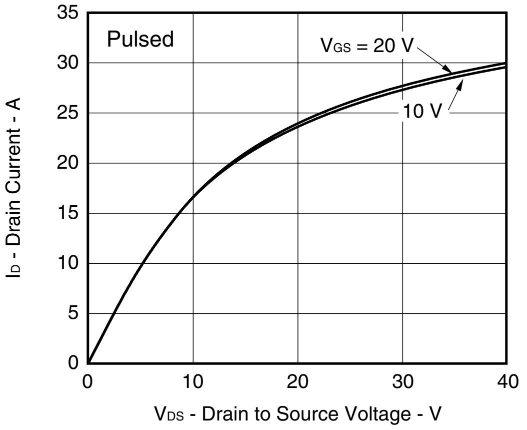


TEST CIRCUIT 3 GATE CHARGE

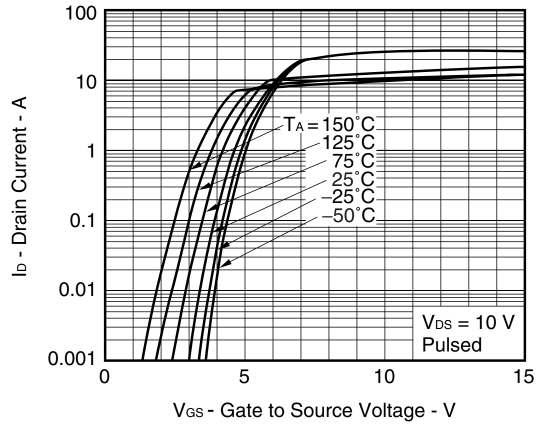


TYPICAL CHARACTERISTICS (T_A = 25°C)

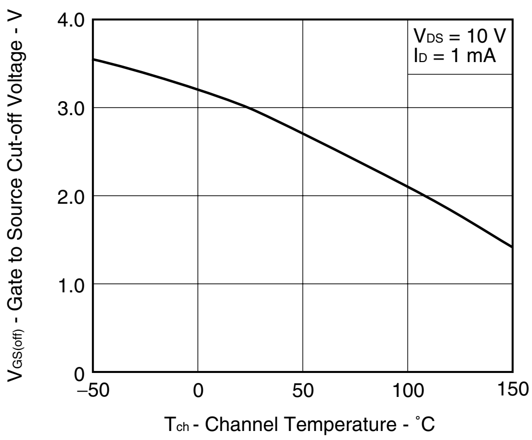
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



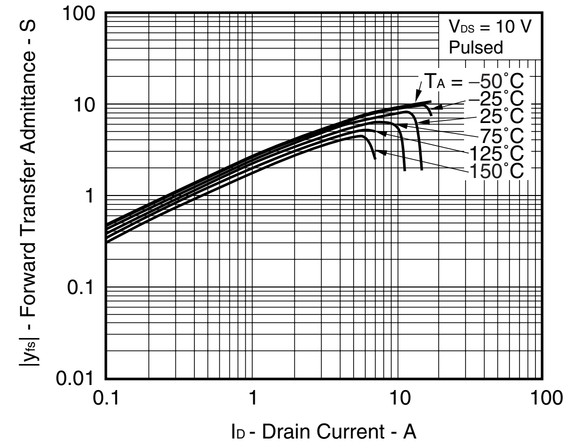
FORWARD TRANSFER CHARACTERISTICS



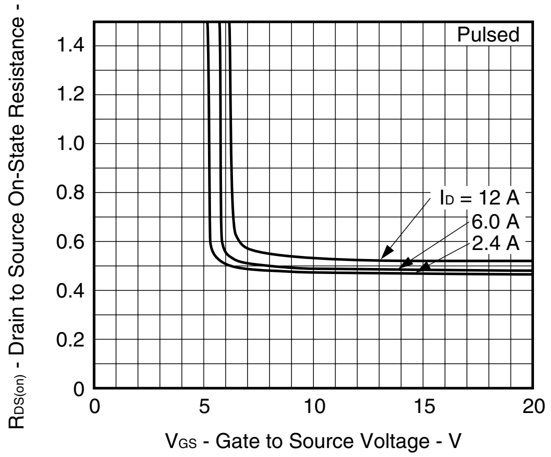
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



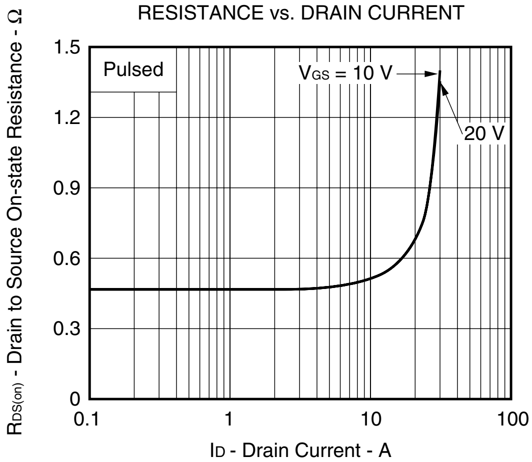
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



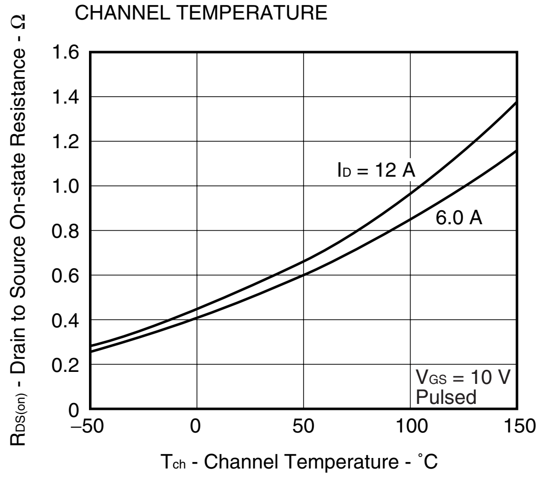
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



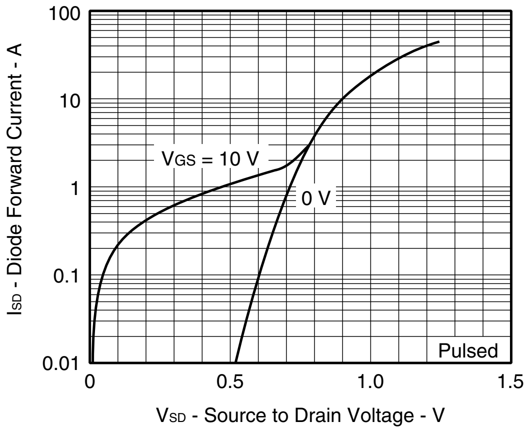
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



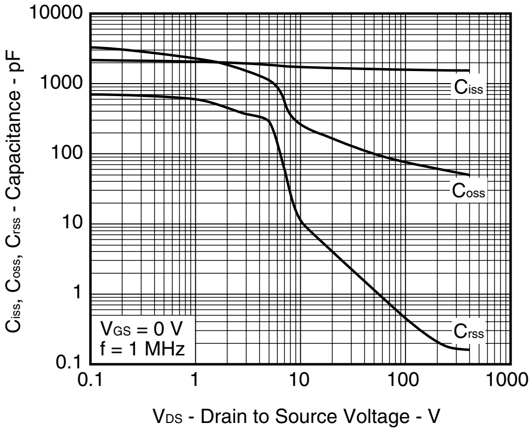
<R> DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



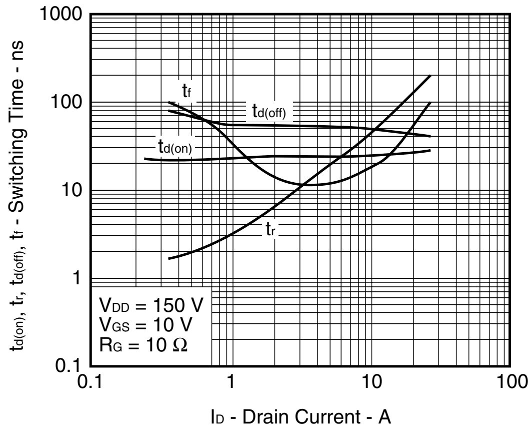
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



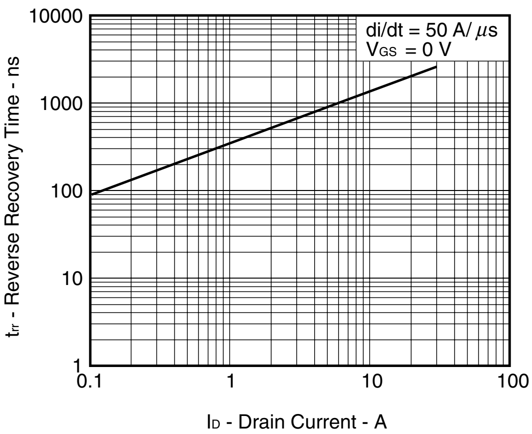
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



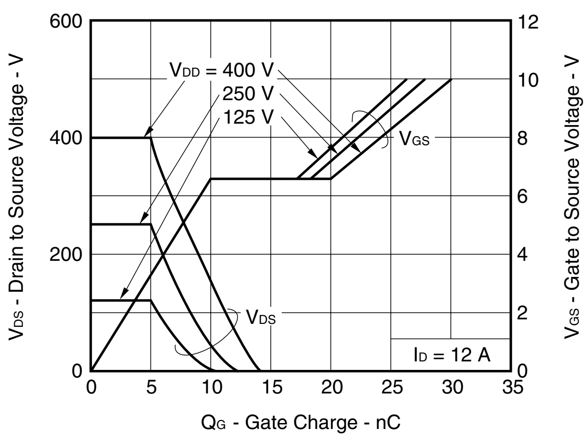
SWITCHING CHARACTERISTICS



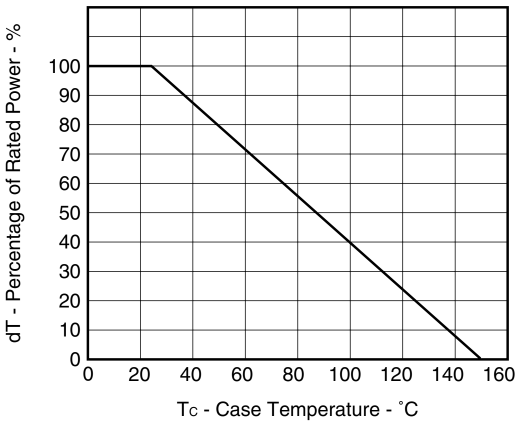
REVERSE RECOVERY TIME vs. DRAIN CURRENT



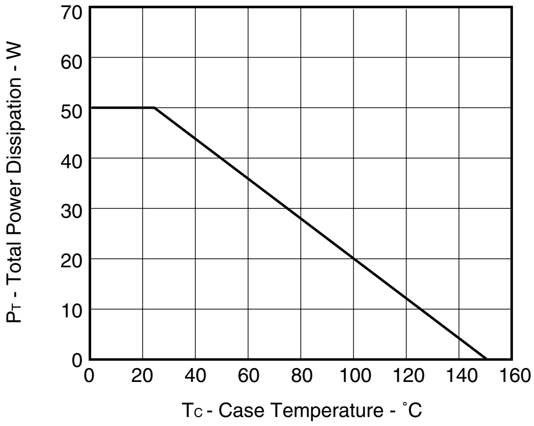
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



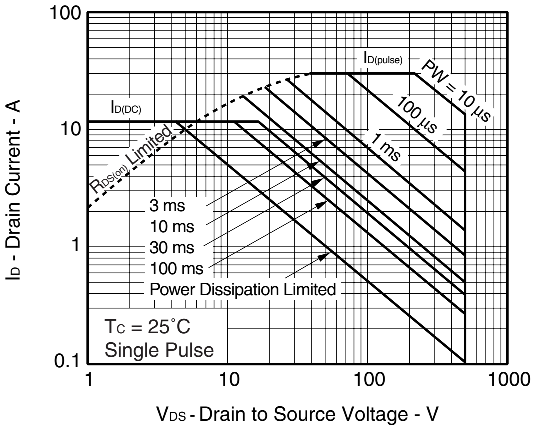
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



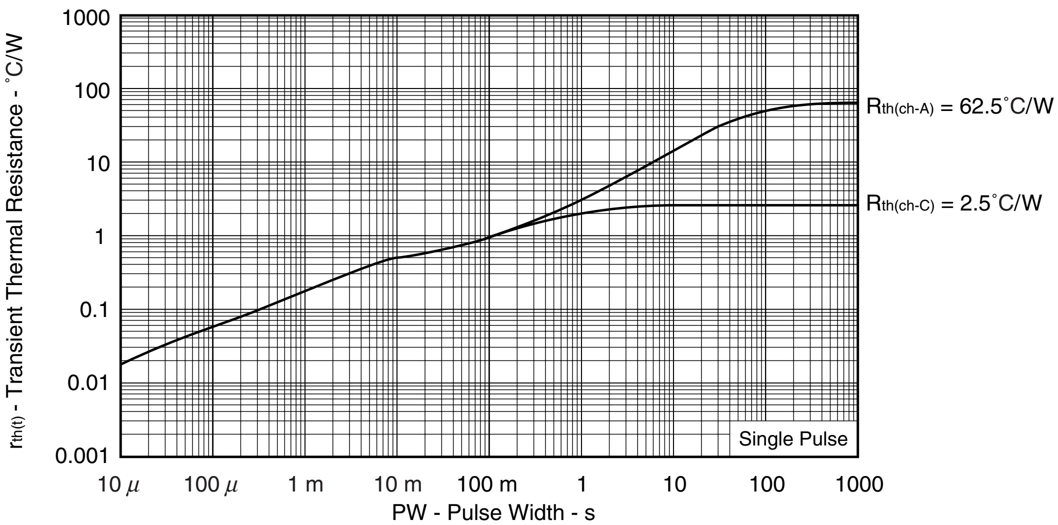
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



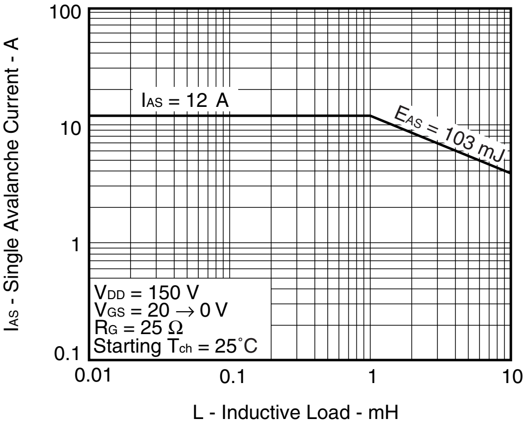
FORWARD BIAS SAFE OPERATING AREA



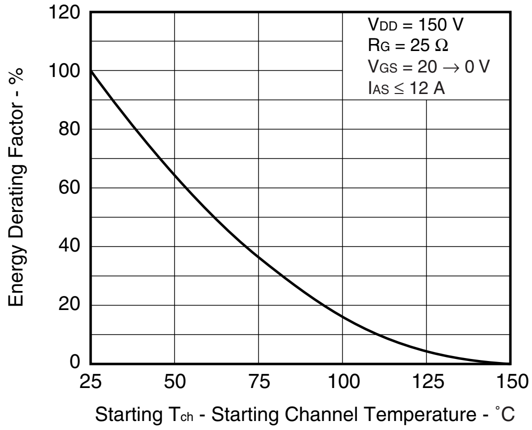
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

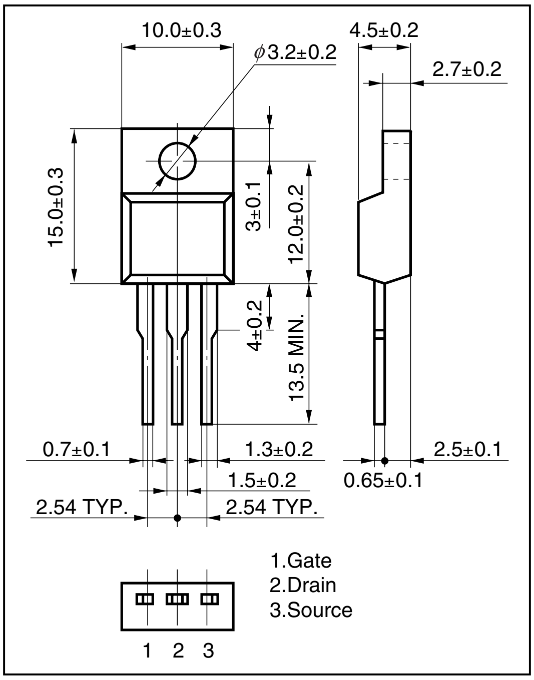


SINGLE AVALANCHE ENERGY
DERATING FACTOR

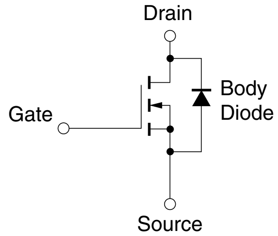


PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.