

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3668 is N-channel DMOS FET device that features a low on-state resistance, low charge and excellent switching characteristics, designed for high voltage applications such as high intensity discharge lamp drive.

FEATURES

- Low gate charge
 $Q_G = 26 \text{ nC TYP. (} V_{DD} = 320 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 10 \text{ A)}$
- Gate voltage rating: $\pm 30 \text{ V}$
- Low on-state resistance
 $R_{DS(on)} = 0.55 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 5.0 \text{ A)}$
- Surface mount package available

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	400	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 34	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	1.5	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	100	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	10	A
★ Single Avalanche Energy ^{Note2}	E_{AS}	8	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

★ **2.** Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 150 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

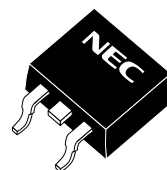
THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.25	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistane	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3668-ZK	TO-263 (MP-25ZK)

(TO-263)



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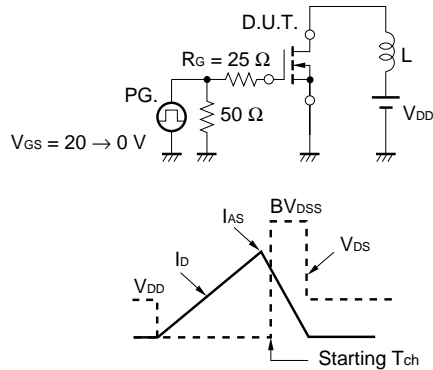
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

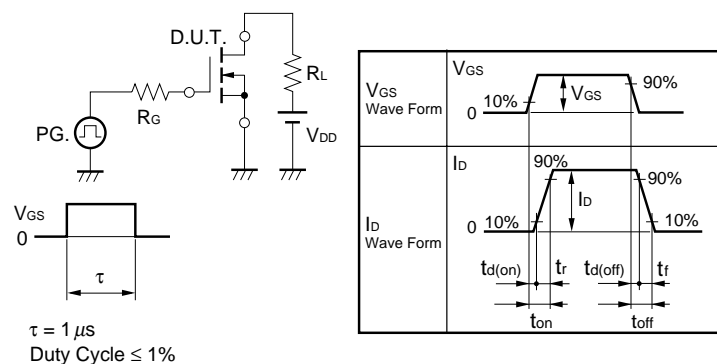
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	2.5		3.5	V
★ Forward Transfer Admittance Note	y _{fs}	V _{DS} = 10 V, I _D = 5.0 A	3.0	5.6		S
★ Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 5.0 A		0.40	0.55	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		1320		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		230		pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		13		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 5.0 A		18		ns
Rise Time	t _r	V _{GS} = 10 V		8		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		44		ns
Fall Time	t _f			4		ns
Total Gate Charge	Q _G	V _{DD} = 320 V		26		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		7		nC
Gate to Drain Charge	Q _{GD}	I _D = 10 A		11		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 10 A, V _{GS} = 0 V		0.90		V
Reverse Recovery Time	t _{rr}	I _F = 10 A, V _{GS} = 0 V		350		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		2.7		μC

Note Pulsed: PW ≤ 800 μs, Duty Cycle ≤ 2%

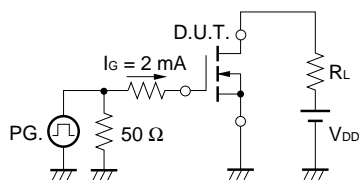
TEST CIRCUIT 1 AVALANCHE CAPABILITY



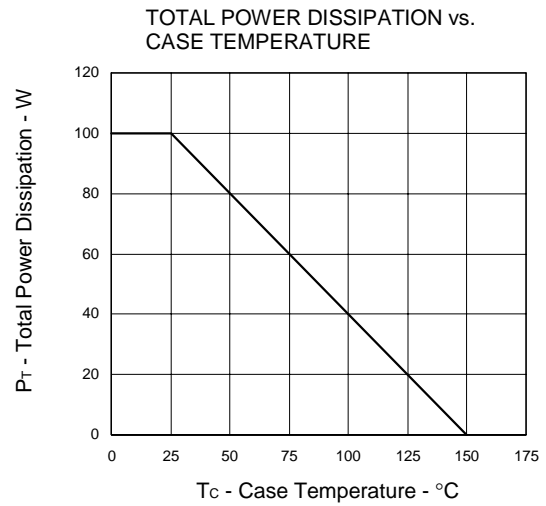
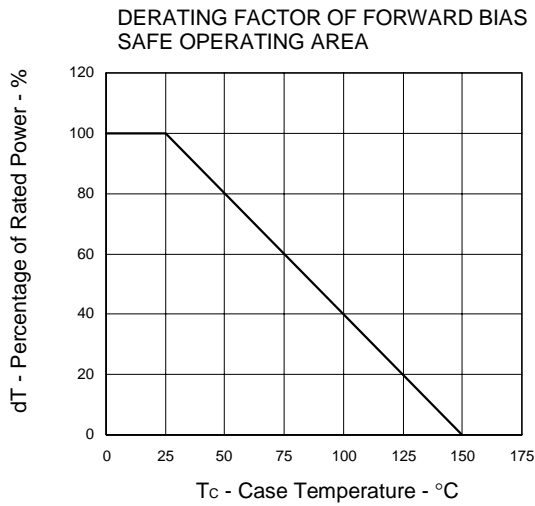
TEST CIRCUIT 2 SWITCHING TIME



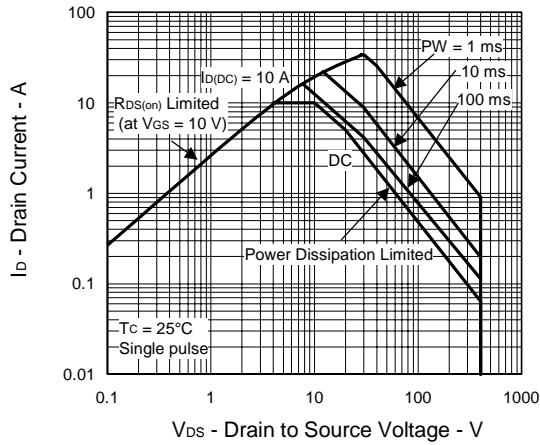
TEST CIRCUIT 3 GATE CHARGE



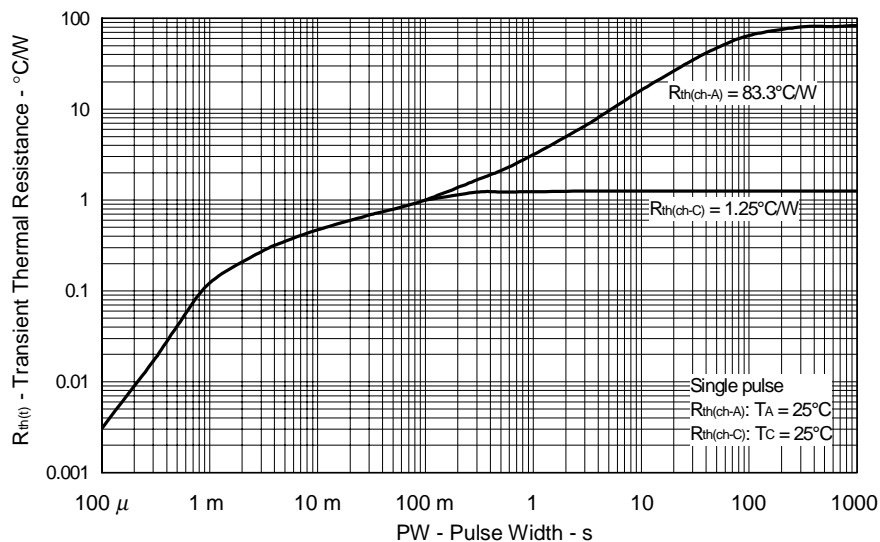
TYPICAL CHARACTERISTICS (T_A = 25°C)



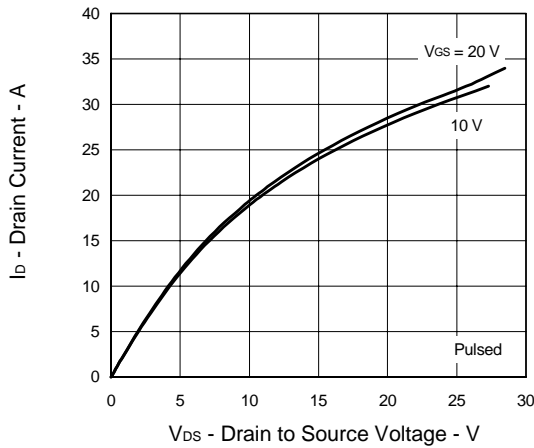
★ **FORWARD BIAS SAFE OPERATING AREA**



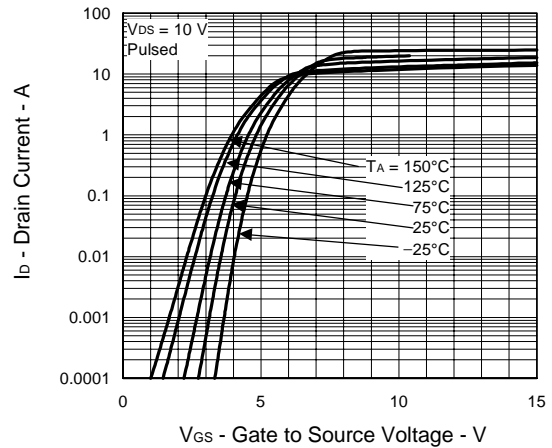
★ **TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH**



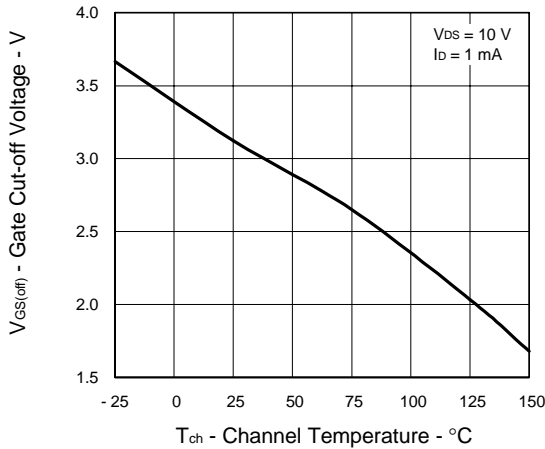
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



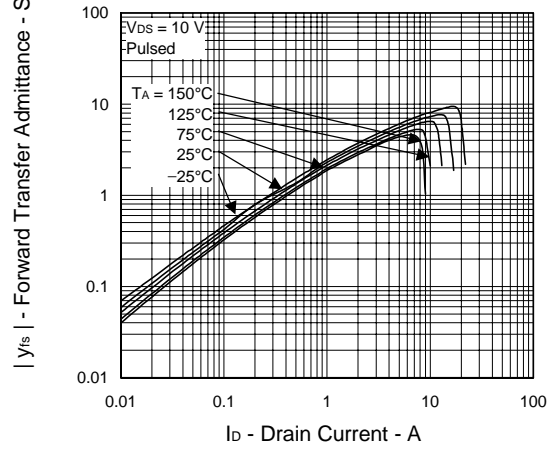
FORWARD TRANSFER CHARACTERISTICS



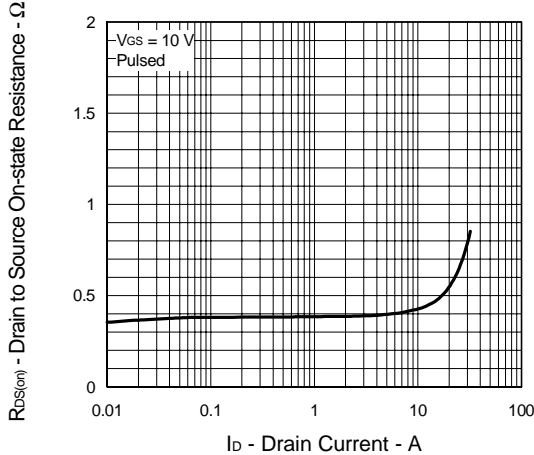
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



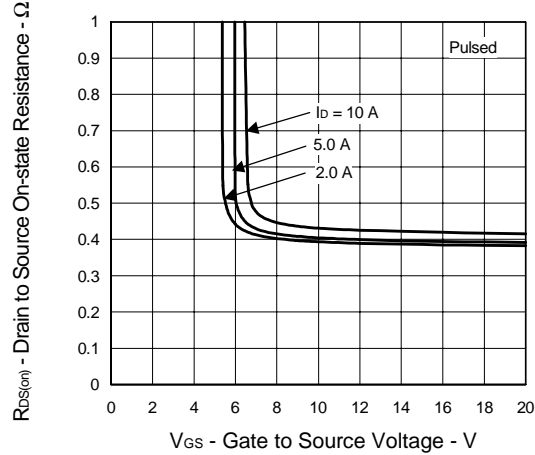
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



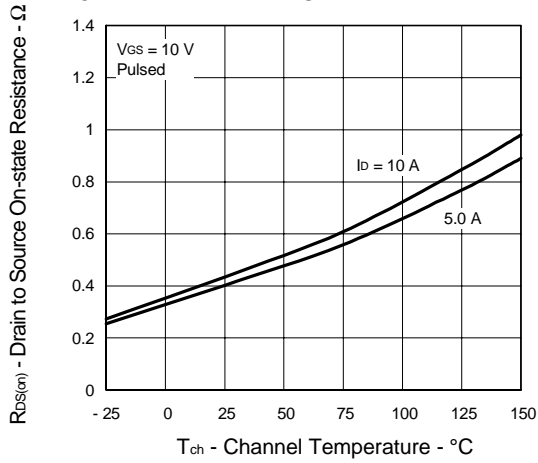
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



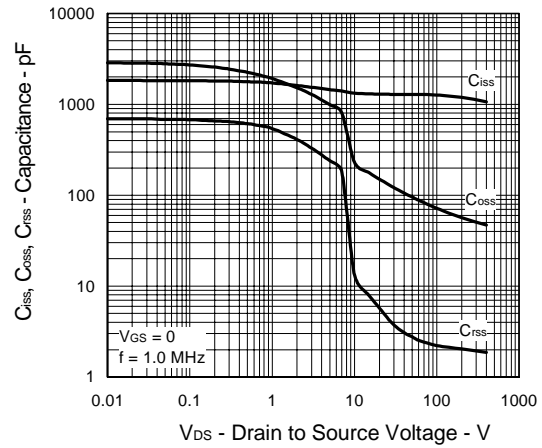
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



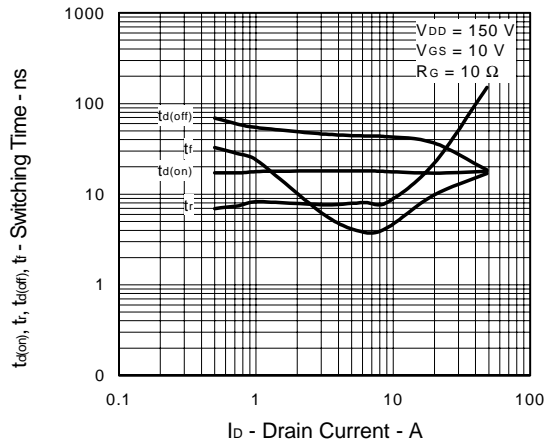
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



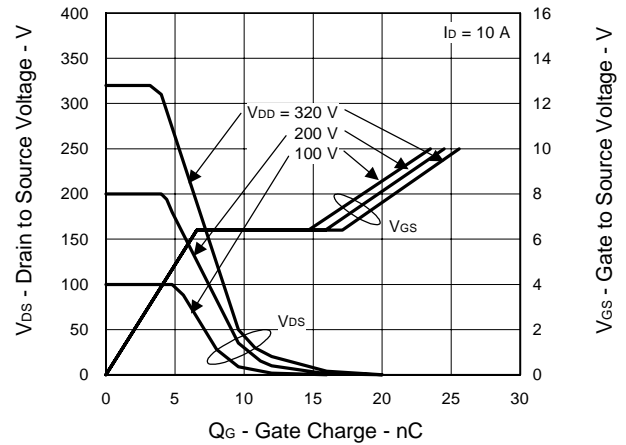
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



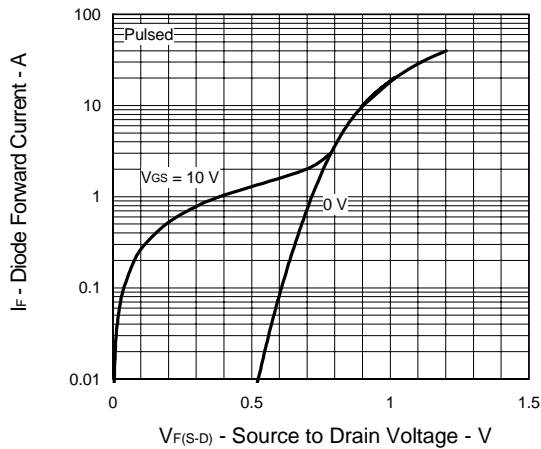
SWITCHING CHARACTERISTICS



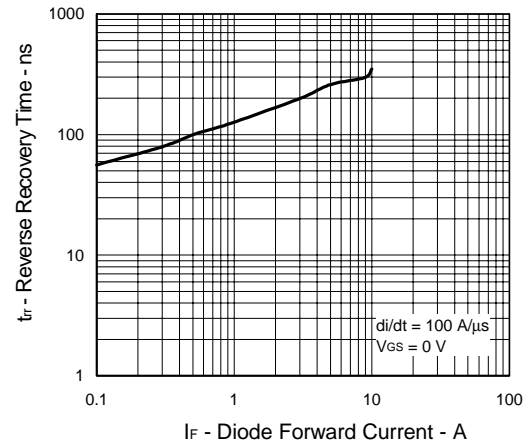
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



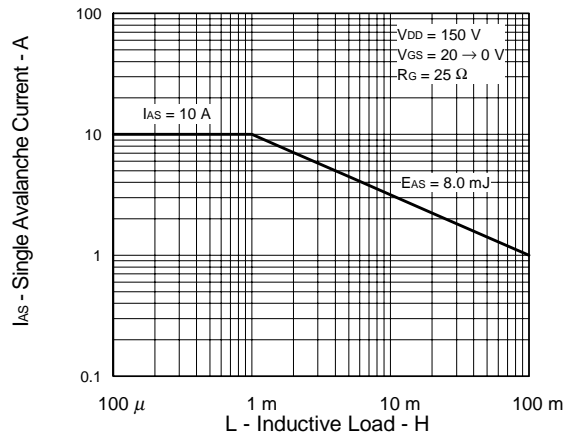
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



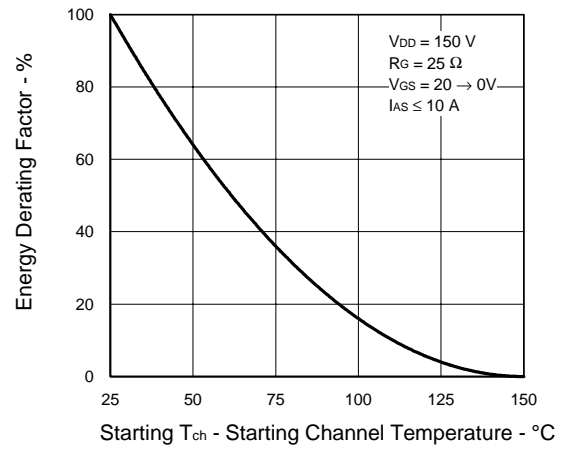
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



★ SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

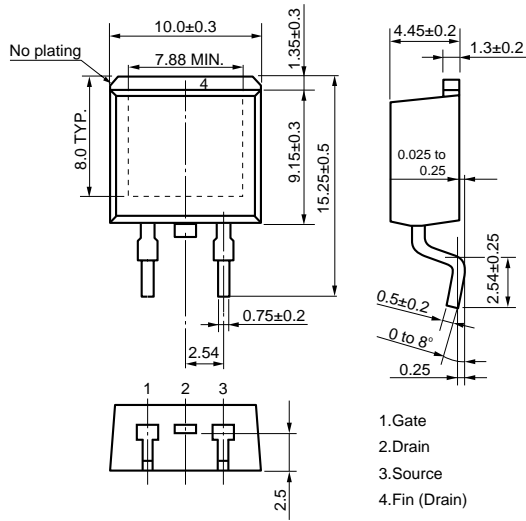


SINGLE AVALANCHE ENERGY DERATING FACTOR

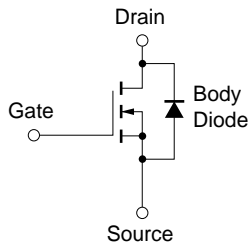


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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