5P49V60B

VersaClock® 6E Programmable Clock Generator

The 5P49V60B is a Renesas sixth-generation, commercial, programmable clock generator (VersaClock 6E) supporting automotive applications. The 5P49V60B is Quality Managed (QM) with the following characteristics:

- AEC-Q100 Grade 2 (-40°C to +105°C)
- IATF 16949
- PPAP support

Configurations may be stored in on-chip One-Time Programmable (OTP) memory or loaded from an I^2C interface. Two select pins allow up to four different configurations to be accessible using processor GPIOs or bootstrapping. The different selections may be used for different operating modes (full function, partial function, partial power-down), regional standards (US, Japan, Europe) or system production margin testing. Frequencies are generated from a single reference clock. The reference clock can come from one of the two redundant clock inputs. A glitch-less manual switchover function allows selection of either clock during normal operation.

Applications

- Automotive infotainment
- Dashboard systems
- Audio/Video applications
- Camera applications
- Active antennas
- In-vehicle networking

Features

- Flexible 1.8V, 2.5V, or 3.3V power-rails
- High-performance, low phase noise PLL, < 0.5ps RMS typical phase jitter on outputs
- Four banks of internal OTP memory
  - In-system or factory programmable
  - Two select pins accessible with processor GPIOs or bootstrapping
- I^2C serial programming interface
  - 0xD0 or 0xD4 I^2C address options allows multiple devices configured in a same system
- LVCMOS reference clock output
- Four universal output pairs individually configurable:
  - Differential (LVPECL, LVDS or HCSL)
  - Two LVCMOS in-phase or 180 degrees out of phase
  - I/O VDDs can be mixed and matched, supporting 1.8V (LVDS and LVCMOS), 2.5V, or 3.3V
- Output frequency ranges:
  - Single-ended clock outputs: 1MHz to 200MHz
  - Differential clock outputs: 1MHz to 350MHz
- Redundant clock input with manual switchover
- Programmable output enable or power-down mode
- 4.0 × 4.0 mm 24-VFQFPN wettable flank package

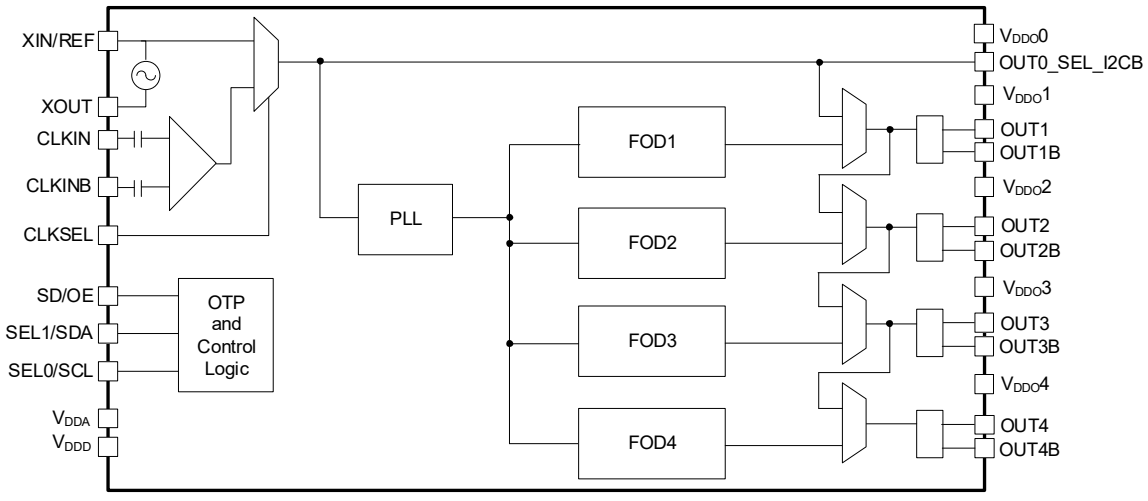


Figure 1. Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments

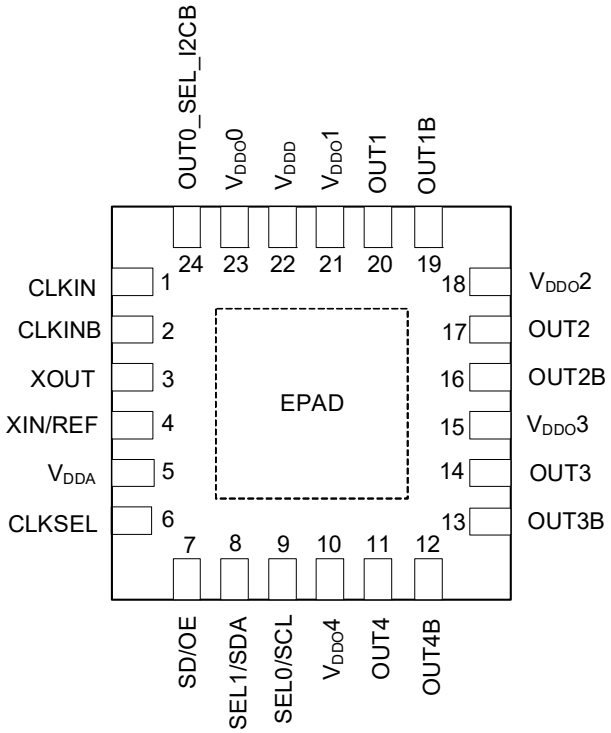


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Internal Pull-down	Differential clock input. Weak 100kΩ internal pull-down.
2	CLKINB	Input	Internal Pull-down	Complementary differential clock input. Weak 100kΩ internal pull-down.
3	XOUT	Output		Crystal oscillator interface output.
4	XIN/REF	Input		Crystal oscillator interface input, or single-ended LVCMOS clock input. Ensure that the input voltage is between 500mV and 1.2V. Refer to the section <Hyperlink>Driving XIN/REF with a CMOS Driver.
5	V_{DDA}	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
6	CLKSEL	Input	Internal Pull-down	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default). 1 = CLKIN, CLKINB. See <Hyperlink>Table 15 for more details.
7	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD).
8	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I^2C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull-down resistor.

Number	Name	Type		Description
9	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I^2C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull-down resistor.
10	$V_{DDO}4$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT4/OUT4B.
11	OUT4	Output		Output clock 4. Refer to the <Hyperlink>Output Drivers section for more details.
12	OUT4B	Output		Complementary output clock 4. Refer to the <Hyperlink>Output Drivers section for more details.
13	OUT3B	Output		Complementary output clock 3. Refer to the <Hyperlink>Output Drivers section for more details.
14	OUT3	Output		Output clock 3. Refer to the <Hyperlink>Output Drivers section for more details.
15	$V_{DDO}3$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3/OUT3B.
16	OUT2B	Output		Complementary output clock 2. Refer to the <Hyperlink>Output Drivers section for more details.
17	OUT2	Output		Output clock 2. Refer to the <Hyperlink>Output Drivers section for more details.
18	$V_{DDO}2$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
19	OUT1B	Output		Complementary output clock 1. Refer to the <Hyperlink>Output Drivers section for more details.
20	OUT1	Output		Output clock 1. Refer to the <Hyperlink>Output Drivers section for more details.
21	$V_{DDO}1$	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.
22	V_{DDD}	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. V_{DDA} and V_{DDD} should have the same voltage applied.
23	$V_{DDO}0$	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0_SEL_I2CB	Input/ Output	Internal Pull-down	Latched input/LVCMOS output. At power-up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull-up (10kΩ) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull-down (10kΩ) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I^2C interface. After power-up, the pin acts as an LVCMOS reference output.
-	EPAD	GND		Connect to ground pad.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 5P49V60B at absolute maximum ratings is not implied. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Item	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.9V
XIN/REF Input	1.2V
CLKIN, CLKINB Input	V_{DDO0}, 1.2V voltage swing
I^2C Loading Current	10mA.
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Rating–Human Body Model (Tested per JS-001-2017)	2000V
ESD Rating–Charged Device Model (AECQ100)	750V
Latch Up (AECQ100)	±100mA

2.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power Supply Voltage for Supporting 1.8V Outputs	V_{DDOx}	1.71	1.8	1.89	V
Power Supply Voltage for Supporting 2.5V Outputs		2.375	2.5	2.625	V
Power Supply Voltage for Supporting 3.3V Outputs		3.135	3.3	3.465	V
Power Supply Voltage for Core Logic Functions	V_{DDD}	1.71	-	3.465	V
Analog Power Supply Voltage. Use filtered analog power supply.	V_{DDA}	1.71	-	3.465	V
Operating Temperature (Grade 2), ambient	T_A	-40	-	105	°C
Maximum Load Capacitance (3.3V LVCMOS only)	C_L	-	-	15	pF
Power-up Time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	t_{PU}	0.05	-	5	ms

2.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Theta J_A. Junction to air thermal impedance (0mps)	θ_{JA}	42	°C/W
Theta J_B. Junction to board thermal impedance (0mps)	θ_{JB}	2.35	°C/W
Theta J_C. Junction to case thermal impedance (0mps)	θ_{JC}	41.8	°C/W

2.4 Electrical Specifications

Table 1. Current Consumption [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Core Supply Current	I_{DDCORE} [2]	100MHz on all outputs, 25MHz REFCLK (3.3V)	-	32	42	mA
		100MHz on all outputs, 25MHz REFCLK (2.5V)	-	32	42	
		100MHz on all outputs, 25MHz REFCLK (1.8V)	-	31	42	
Output Buffer Supply Current	I_{DDOx}	LVPECL, 350MHz, 3.3V V_{DDOx}	-	48	63	mA
		LVPECL, 350MHz, 2.5V V_{DDOx}	-	41	54	mA
		LVDS, 350MHz, 3.3V V_{DDOx}	-	26	32	mA
		LVDS, 350MHz, 2.5V V_{DDOx} (same setting as 3.3V)	-	25	30	mA
		LVDS, 350MHz, 1.8V V_{DDOx}	-	23	27	mA
		HCSL, 250MHz, 3.3V V_{DDOx} [3]	-	39	48	mA
		HCSL, 250MHz, 2.5V V_{DDOx} [3]	-	37	46	mA
		LVCMOS, 50MHz, 3.3V, V_{DDOx} [3][4]	-	23	27	mA
		LVCMOS, 50MHz, 2.5V, V_{DDOx} [3][4]	-	20	24	mA
		LVCMOS, 50MHz, 1.8V, V_{DDOx} [3][4]	-	18	21	mA
		LVCMOS, 200MHz, 3.3V V_{DDOx} [3][4]	-	45	58	mA
		LVCMOS, 200MHz, 2.5V V_{DDOx} [3][4]	-	34	45	mA
		LVCMOS, 200MHz, 1.8V V_{DDOx} [3][4]	-	24	33	mA
Power Down Current	I_{DDPD}	SD asserted, I^2C programming (3.3V)	-	10	12	mA
		SD asserted, I^2C programming (2.5V)	-	10	12	
		SD asserted, I^2C programming (1.8V)	-	10	12	

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. $I_{DDCORE} = I_{DDA} + I_{DDD}$, no loads.
3. Measured into a 5” 50Ω trace with 2pF load.
4. Single CMOS driver active.

Table 2. AC Timing Characteristics [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Frequency	f_{IN} [2]	Input frequency limit (crystal)	8	-	40	MHz
		Input frequency limit (CLKIN,CLKINB)	1	-	350	MHz
		Input frequency limit (single-ended over XIN)	1	-	200	MHz
Output Frequency	f_{OUT} [3]	Single-ended clock output limit (LVCMOS)	1	-	200	MHz
		Differential clock output limit (LVPECL/LVDS/HCSL)	1	-	350	
Output Duty Cycle	t_{DC} [4]	Measured at $V_{DD}/2$, all outputs except reference output, V_{DDOX} = 2.5V or 3.3V	45	50	55	%
		Measured at $V_{DD}/2$, all outputs except reference output, V_{DDOX} = 1.8V	40	50	60	%
		Measured at $V_{DD}/2$, reference output OUT0 (5MHz–150.1MHz) with 50% duty cycle input	40	50	60	%
		Measured at $V_{DD}/2$, reference output OUT0 (150.1MHz–200MHz) with 50% duty cycle input	30	50	70	%
Output Skew	t_{SKEW}	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns	-	75	-	ps
Startup Time	$t_{STARTUP}$ [5][6]	Measured after all V_{DD}s have risen above 90% of their target value [7]	-	-	30	ms
		PLL lock time from shutdown mode	-	3	4	ms

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. Practical lower frequency is determined by loop filter settings.
3. A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.
4. Duty cycle is only guaranteed at maximum slew rate settings.
5. Actual PLL lock time depends on the loop configuration.
6. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.
7. Power-up with temperature calibration enabled; contact Renesas if shorter lock-time is required in system.

Table 3. Input Characteristics [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Capacitance	C_{IN}	CLKIN,CLKINB,CLKSEL,SD/OE,SEL1/SDA, SEL0/SCL	-	3	7	pF
Pull-down Resistor	R_{PD}	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB	100	-	350	kΩ
Input High Voltage	V_{IH}	CLKSEL, SD/OE	0.7 × V_{DDD}	-	V_{DDD} + 0.3	V
Input Low Voltage	V_{IL}	CLKSEL, SD/OE V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V and 2.5V	GND - 0.3	-	0.3 × V_{DDD}	V
		CLKSEL, SD/OE V_{DDA}, V_{DDD}, V_{DDO0} = 1.8V	GND - 0.3	-	0.4	V
Input High Voltage	V_{IH}	OUT0_SEL_I2CB	0.7 × V_{DDO}	-	V_{DDO0} + 0.3	V
Input Low Voltage	V_{IL}	OUT0_SEL_I2CB	GND - 0.3	-	0.4	V
Input High Voltage	V_{IH}	XIN/REF	0.5	-	1.2	V
Input Low Voltage	V_{IL}	XIN/REF	GND - 0.3	-	0.4	V
Input Rise/Fall Time	T_R/T_F	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL	-	-	300	ns

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.

Table 4. CLKIN Electrical Characteristics [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Amplitude – CLKIN, CLKINB	V_{SWING}	Peak to peak value, single-ended	200	-	1200	mV
Input Slew Rate – CLKIN, CLKINB	dv/dt	Measured differentially	0.4	-	8	V/ns
Input Leakage Low Current	I_{IL}	V_{IN} = GND	-5	-	5	µA
Input Leakage High Current	I_{IH}	V_{IN} = 1.7V	-	-	30	µA
Input Duty Cycle	DC_{IN}	Measurement from differential waveform	45	-	55	%

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.

Table 5. Electrical Characteristics – CMOS Outputs [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output High Voltage	V_{OH}	I_{OH} = -15mA (3.3V), -12mA (2.5V), -8mA (1.8V) V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V and 2.5V V_{DDA}, V_{DDD}, V_{DDO0} = 1.8V	0.7 × V_{DDO} 0.5 × V_{DDO}	-	V_{DDO} V_{DDO}	V
Output Low Voltage	V_{OL}	I_{OL} = 15mA (3.3V), 12mA (2.5V), 8mA (1.8V)	-	-	0.45	V
Output Driver Impedance	R_{OUT}	CMOS output driver	-	17	-	Ω

Table 5. Electrical Characteristics – CMOS Outputs [1] (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate, SLEW[1:0] = 00	T_{SR} [2]	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) V_{DDOX} = 3.3V	1.0	2.2	-	V/ns
Slew Rate, SLEW[1:0] = 01			1.2	2.3	-	
Slew Rate, SLEW[1:0] = 10			1.3	2.4	-	
Slew Rate, SLEW[1:0] = 11			1.7	2.7	-	
Slew Rate, SLEW[1:0] = 00		Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) V_{DDOX} = 2.5V	0.6	1.3	-	
Slew Rate, SLEW[1:0] = 01			0.7	1.4	-	
Slew Rate, SLEW[1:0] = 10			0.6	1.4	-	
Slew Rate, SLEW[1:0] = 11			1.0	1.7	-	
Slew Rate, SLEW[1:0] = 00		Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of V_{DDO} (output load = 5pF) V_{DD} = 1.8V	0.3	0.7	-	
Slew Rate, SLEW[1:0] = 01			0.4	0.8	-	
Slew Rate, SLEW[1:0] = 10			0.4	0.9	-	
Slew Rate, SLEW[1:0] = 11			0.7	1.2	-	
Output Leakage Current (OUT1–4)	I_{OZDD}	Tri-state outputs	-	-	5	µA
Output Leakage Current (OUT0)		Tri-state outputs	-	-	30	µA

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.

Table 6. Electrical Characteristics – LVDS Outputs [1]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Differential Output Voltage for the TRUE Binary State	V_{OT} (+)	247	-	454	mV
Differential Output Voltage for the FALSE Binary State	V_{OT} (-)	-454	-	-247	mV
Change in V_{OT} between Complimentary Output States	ΔV_{OT}	-	-	50	mV
Output Common Mode Voltage (Offset Voltage) at 3.3 V ±5%, 2.5V ±5%	V_{OS}	1.125	1.25	1.375	V
Output Common Mode Voltage (Offset Voltage) at 1.8V ±5%		0.8	0.875	0.96	V
Change in V_{OS} between Complimentary Output States	ΔV_{OS}	-	-	50	mV
Outputs Short Circuit Current, V_{OUT}+ or V_{OUT} - = 0V or V_{DDO}	I_{OS}	-	9	24	mA
Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT} -	I_{OSD}	-	6	12	mA
LVDS Rise Time 20%–80%	T_R	-	300	-	ps
LVDS Fall Time 80%–20%	T_F	-	300	-	ps

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.

Table 7. Electrical Characteristics – LVPECL Outputs [1]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Output Voltage High, Terminated through 50Ω tied to V_{DD} - 2V	V_{OH}	V_{DDO} - 1.19	-	V_{DDO} - 0.69	V
Output Voltage Low, Terminated through 50Ω tied to V_{DD} - 2V	V_{OL}	V_{DDO} - 1.94	-	V_{DDO} - 1.4	V
Peak-to-Peak Output Voltage Swing	V_{SWING}	0.55	-	0.993	V
LVPECL Rise Time 20%–80%	T_R	-	400	-	ps
LVPECL Fall Time 80%–20%	T_F	-	400	-	ps

1. V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, $V_{DDO[1:4]}$ = 3.3V ±5%, 2.5V ±5%, T_A = -40°C to +105°C unless otherwise specified.

Table 8. Electrical Characteristics – HCSL Outputs [1][2]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate	dV/dt	Scope averaging on [3] [4]	1	-	4	V/ns
Slew Rate Matching	ΔdV/dt	Scope averaging on [4]	-	-	20	%
Maximum Voltage	V_{MAX}	Measurement on single-ended signal using absolute value (scope averaging off)	-	-	1150	mV
Minimum Voltage	V_{MIN}		-300	-	-	mV
Voltage Swing	V_{SWING}	Scope averaging off [3][5]	300	-	-	mV
Crossing Voltage Value	V_{CROSS}	Scope averaging off [5][6]	250	-	550	mV
Crossing Voltage Variation	ΔV_{CROSS}	Scope averaging off [7]	-	-	140	mV

1. V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, $V_{DDO[1:4]}$ = 3.3V ±5%, 2.5V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. Confirmed by design and characterization. Not 100% tested in production.
3. Measured from differential waveform.
4. Slew rate is measured through the V_{SWING} voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.
5. Measured from single-ended waveform.
6. V_{CROSS} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
7. The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of V_{CROSS} min/max (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.

Table 9. Spread Spectrum Generation Specifications [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Spread Frequency	f_{SSOUT}	Output frequency range for spread spectrum	5	-	300	MHz
Mod Frequency	f_{MOD}	Modulation frequency	30 to 63			kHz
Spread Value	f_{SPREAD}	Amount of spread value (programmable)–center spread	±0.25% to ±2.5%			$\%f_{OUT}$
		Amount of spread value (programmable)–down spread	-0.5% to -5%			

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.

3. I²C Bus Characteristics

Table 10. I²C Bus DC Characteristics [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
I²C Bus Voltage	V_{BUS}	SEL1/SDA pin and SEL0/SCL pin.	V_{DDD}	-	3.6	V
Input High Level [2]	V_{IH}	SEL1/SDA pin and SEL0/SCL pin.	0.7 × V_{DDD}	-	V_{BUS}	V
Input Low Level	V_{IL}	SEL1/SDA pin and SEL0/SCL pin.	-	-	0.3 × V_{DDD}	V
Hysteresis of Inputs	V_{HYS}	-	0.05 × V_{DDD}	-	-	V
Input Leakage Current	I_{IN}	-	-	-	36	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA	-	-	0.45	V

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. I²C inputs are 3.3V tolerant.

Table 11. I²C Bus AC Characteristics [1]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Serial Clock Frequency (SCL)	F_{SCLK}	-	10	-	400	kHz
Bus Free Time between Stop and Start	t_{BUF}	-	1.3	-	-	µs
Setup Time, Start	$t_{SU:START}$	-	0.6	-	-	µs
Hold Time, Start	$t_{HD:START}$	-	0.6	-	-	µs
Setup Time, Data Input (SDA)	$t_{SU:DATA}$	-	0.1	-	-	µs
Hold Time, Data Input (SDA) [2]	$t_{HD:DATA}$	-	0	-	-	µs
Output Data Valid from Clock	t_{OVD}	-	-	-	0.9	µs
Capacitive Load for Each Bus Line	C_B	-	-	-	400	pF
Rise Time, Data and Clock (SDA, SCL)	t_R	-	20 + 0.1 × C_B	-	300	ns
Fall Time, Data and Clock (SDA, SCL)	t_F	-	20 + 0.1 × C_B	-	300	ns
High Time, Clock (SCL)	t_{HIGH}	-	0.6	-	-	µs
Low Time, Clock (SCL)	t_{LOW}	-	1.3	-	-	µs
Setup Time, Stop	$t_{SU:STOP}$	-	0.6	-	-	µs

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

4. Test Loads

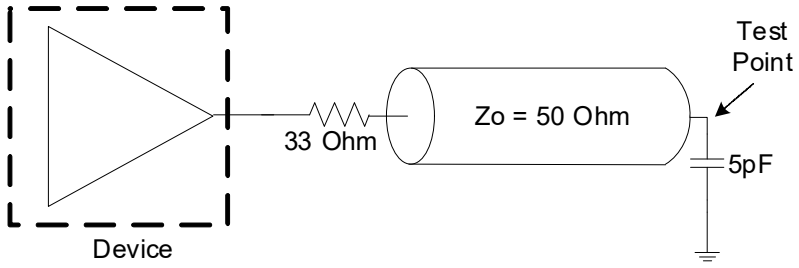


Figure 3. LVCMOS Test Load

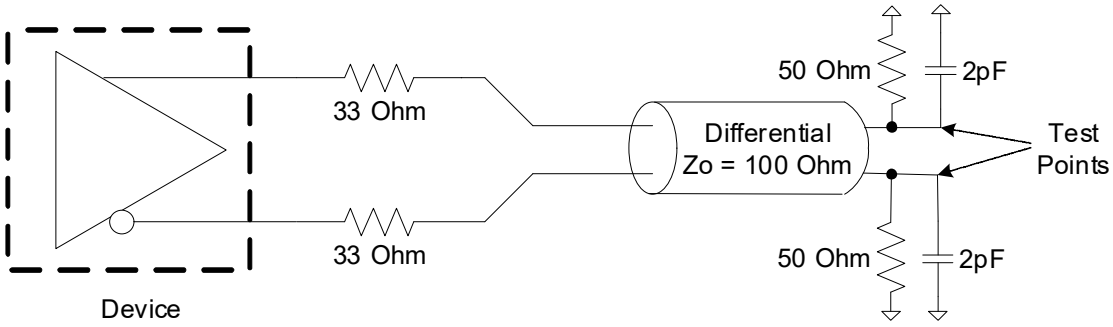


Figure 4. HCSL Test Load

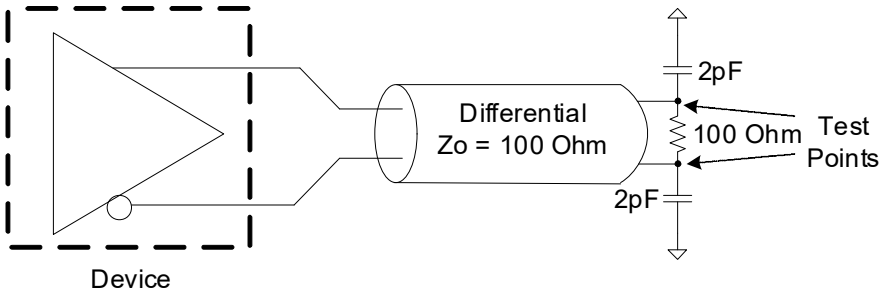


Figure 5. LVDS Test Load

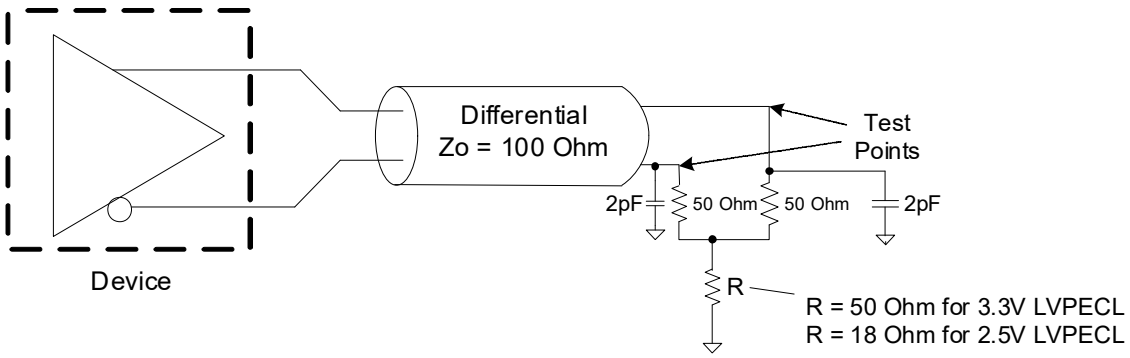
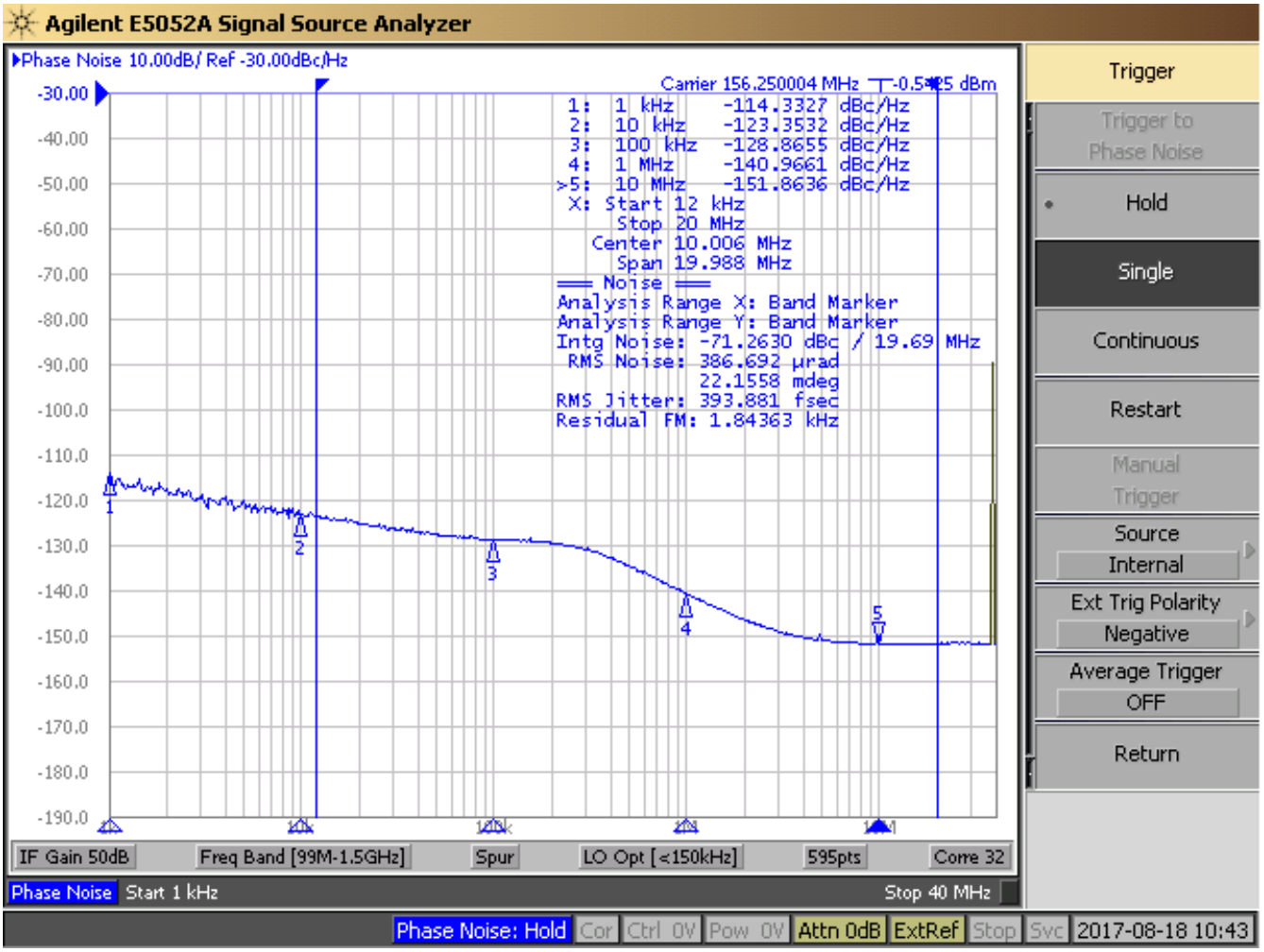


Figure 6. LVPECL Test Load

5. Jitter Performance Characteristics



Note: Measured with OUT2 = 156.25MHz on, 39.625MHz input.

Figure 7. Typical Phase Jitter Plot at 156.5MHz

Table 12. Jitter Performance [1][2][3]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Cycle to Cycle Jitter	J_{CY-CY}	LVCMOS	-	5	30	ps
		All differential outputs	-	25	35	ps
Period Jitter	J_{PK-PK}	LVCMOS	-	28	40	ps
		All differential outputs	-	4	30	ps
RMS Phase Jitter	J_{RMS}	LVCMOS (12kHz - 5MHz)[4]	-	0.3	-	ps
		All differential outputs (12kHz - 20MHz)	-	0.5	-	ps

1. V_{DDA}, V_{DDD} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%. V_{DDOx} = 3.3V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. Measured with 25MHz crystal input.
3. Configured with OUT0 = 25MHz–LVCMOS; OUT1 = 100MHz–HCSL; OUT2 = 125MHz–LVDS; OUT3 = 156.25MHz–LVPECL.
4. This is a limitation of the phase noise analyzer and Nyquist. The 25MHz signal has a Nyquist frequency of 12.5MHz and cannot be measured to 20MHz. The phase noise analyzer can measure up to 5MHz.

Table 13. PCI Express Jitter Performance [1][2][3]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Unit
PCIe Jitter (Common Clock–CC)	$t_{jphPCIeG1-CC}$	PCIe Gen1 [4]	-	28.7	-	86	ps (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz)	-	0.27	-	3	ps (rms)
		PCIe Gen High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz)	-	2.56	-	3.1	ps (rms)
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	-	0.8	-	1	ps (rms)
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	-	0.26	-	0.5	ps (rms)
PCIe Jitter (IR) [5][6]	$t_{jphPCIeG2-SRNS}$	PCIe Gen2 (SSC off) (PLL BW of 16MHz, CDR = 5MHz)	-	0.93	-	2	ps (rms)
	$t_{jphPCIeG3-SRNS}$	PCIe Gen3 (SSC off) (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)	-	0.32	-	0.7	ps (rms)

1. V_{DDA}, V_{DDD}, V_{DDOx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +105°C unless otherwise specified.
2. Confirmed by design and characterization, not 100% tested in production.
3. Based on PCIe Base Specification Rev 4.0 version 1.0. See http://www.pcisig.com for latest specifications.
4. Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.
5. According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 data rates.
6. IR (Independent Reference) is the inclusive name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

6. Features and Functional Blocks

6.1 Device Startup and Power-On-Reset

The device has an internal power-up reset (POR) circuit. All V_{DD}s must be connected to desired supply voltage to trigger POR.

User can define specific default configurations through internal One-Time-Programmable (OTP) memory. Either customer or factory can program the default configuration. For more details, refer to VersaClock 6E Family Register Descriptions and Programming Guide or contact Renesas if a specific factory-programmed default configuration is required.

Device will identity which of the 2 modes to operate in by the state of OUT0_SEL_I2CB pin at POR. Both of the modes default configurations can be programmed as stated above.

1. **Software Mode (I^2C)**: OUT0_SEL_I2CB is low at POR.

   I^2C interface will be open to users for in-system programming, overriding device default configurations at any time.

2. **Hardware Select Mode**: OUT0_SEL_I2CB is high at POR.

   Device has been programmed to load OTP at power-up (REG0[7] = 1). The device will load internal registers according to Table 14.

   Internal OTP memory can support up to 4 configurations, selectable by SEL0/SEL1 pins.

   At POR, logic levels at SEL0 and SEL1 pins must be settled, resulting the selected configuration to be loaded at power up.

   After the first 10ms of operation, the levels of the SELx pins can be changed, either to low or to the same level as V_{DDD}/V_{DDA}. The SELx pins must be driven with a digital signal of < 300ns rise/fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

Table 14. Power-up Behavior

OUT0_SEL_I2CB at POR	SEL1	SEL0	I^2C Access	REG0:7	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I^2C defaults
0	X	X	Yes	0	0

6.2 Reference Clock and Selection

The device supports up to two clock inputs.

- Crystal input, can be driven by a single-ended clock.
- Clock input (CLKIN, CLKINB), a fully differential input that only accepts a reference clock. A single-ended clock can also drive it on CLKIN.

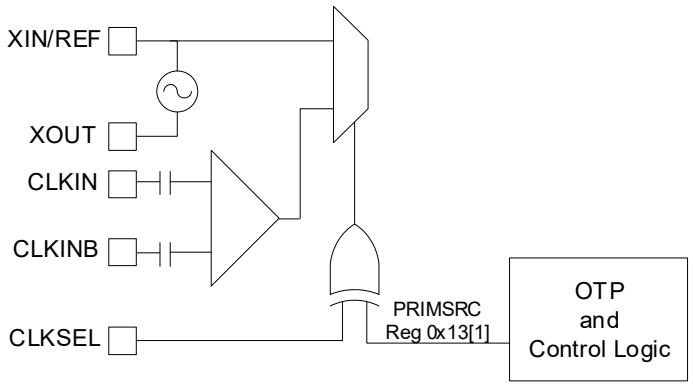


Figure 8. Clock Input Diagram, Internal Logic

6.3 Manual Switchover

The CLKSEL pin selects the input clock between either XTAL/REF or (CLKIN, CLKINB). CLKSEL polarity can be changed by I^2C programming (Byte 0x13[1]) as shown in the table below.

0 = XIN/REF, XOUT (default); 1 = CLKIN, CLKINB.

Table 15. Input Clock Select

PRIMSRC (Register 0x13[1])	CLKSEL	Source
0	0	XIN/REF
0	1	CLKIN, CLKINB
1	0	CLKIN, CLKINB
1	1	XIN/REF

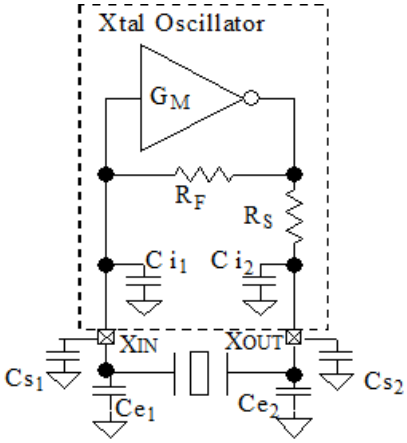
When SM[1:0] is “0x”, the redundant inputs are in manual switchover mode. In this mode, CLKSEL pin is used to switch between the primary and secondary clock sources. The PRIMSRC bit determines the primary and secondary clock source setting. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

6.4 Internal Crystal Oscillator (XIN/REF)

6.4.1 Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa. Therefore, for an accurate oscillation frequency, ensure to match the oscillator load capacitance with the crystal load capacitance.

6.4.2 Tuning the Crystal Load Capacitor



Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.

Ce1 and Ce2 are additional external capacitors, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding Ce1 and/or Ce2 to avoid crystal startup issues. Ci1 and Ci2 are integrated programmable load capacitors, one at XIN and one at XOUT. Ci1 and Ci2.

The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register.

Ci1 and Ci2 are commonly programmed to be the same value. Adjustment of the crystal tuning capacitors allows maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

Ci1/Ci2 starts at 9pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.5pF.

Table 16. XTAL[5:0] Tuning Capacitor

Parameter	Bits	Step (pF)	Minimum (pF)	Maximum (pF)
XTAL	6	0.5	9	25

The following equation can be written for this capacitance:

$Ci = 9pF + 0.5pF \times XTAL[5:0]$
$C_{XIN} = Ci1 + Cs1 + Ce1$
$C_{XOUT} = Ci2 + Cs2 + Ce2$

The final load capacitance of the crystal:

$$C_L = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

It is recommended to set the same value for capacitors the same at each crystal pin, meaning:

$$C_{XIN} = C_{XOUT}$$

Example 1: The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs = 1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:

$8pF = (9pF + 0.5pF \times XTAL[5:0] + 1.5pF) / 2$

So, XTAL[5:0] = 11 (decimal).

Example 2: The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. For now, use Cs + Ce = 5pF and the right value for Ce can be determined later to make 5pF together with Cs.

12pF = (9pF + 0.5pF × XTAL[5:0] + 5pF) / 2

So, XTAL[5:0] = 20 (decimal).

Table 17. Recommended Crystal Characteristics

Parameter	Minimum	Typical	Maximum	Unit
Mode of Oscillation		Fundamental		-
Frequency	8	25	40	MHz
Equivalent Series Resistance (ESR)	-	10	100	Ω
Shunt Capacitance	-	-	7	pF
Load Capacitance (C_L) at < = 25MHz	6	8	12	pF
Load Capacitance (C_L) > 25MHz to 40MHz	6	-	8	pF
Maximum Crystal Drive Level	-	-	100	µW

6.5 Programmable Loop Filter

Table 18. Loop Filter [1]

Input Reference Frequency (MHz)	Loop Bandwidth Minimum (kHz)	Loop Bandwidth Maximum (kHz)
1	40	126
350	300	1000

1. The device PLL loop bandwidth range depends on the input reference frequency (Fref).

6.6 Fractional Output Dividers (FOD)

The device has 4 fractional output dividers (FOD). Each of the FODs are comprised of a 12-bit integer counter, and a 24-bit fractional counter. The output divider can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate a clock frequency accurate to 50ppb.

The FOD's features are described in the following sections.

6.6.1 Individual Spread Spectrum Modulation

The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI.

Each divider has individual spread ability. Spread modulation independent of output frequency, a triangle wave modulation between 30kHz and 63kHz.

Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount from ±0.25% to ±2.5% center-spread and -0.5% to -5% down-spread.

6.6.2 Bypass Mode

Bypass mode (divide by 1) to allow the output to behave as a buffered copy from the input or another FOD.

6.6.3 Dividers Alignment

Each output divider block has a synchronizing pulse to provide startup alignment between outputs dividers. This allows alignment of outputs for low skew performance.

When the device is at hardware select mode, outputs will be automatically aligned at POR. The same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration.

When using software mode I^2C to reprogram an output divider during operation, alignment can be lost. Alignment can be restored by manually triggering the reset through I^2C.

The outputs are aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by utilizing the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

6.6.4 Programmable Skew

The device has the ability to skew outputs by quadrature values. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. So, for 100MHz output and a 2500MHz VCO, you can select how many 12.5ps units you want added to your skew (resulting in units of 0.45 degrees). For example, 0, 0.45, 0.90, 1.35, 1.80, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

6.7 Output Drivers

The device output drivers support the following features individually:

- 2.5V or 3.3V voltage level for HCSL/LVPECL operation
- 1.8V, 2.5V or 3.3V voltage levels for CMOS/LVDS operation
- CMOS supports 4 operating modes:
  - CMOSD: OUTx and OUTxB 180 degrees out of phase
  - CMOSX2: OUTx and OUTxB phase-aligned
  - CMOS1: only OUTx pin is on
  - CMOS2: only OUTxB pin is on

When a given output is configured to at CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.

- Independent output enable/disabled by register bits. When disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

1. Output turned off by I^2C.
2. Output turned off by SD/OE pin.

Output unused, which means is turned off regardless of OE pin status.

6.8 SD/OE Pin Function

SD/OE pin can be programmed as following functions:

1. OE output enable (low active).
2. OE output enable (high active).

   Note: In this mode, toggling the OE input from low level to high level is mandatory to activate outputs. This should occur after the device has started up and the PLL has reached lock status. For more details, refer to the VersaClock 6E Family Register Descriptions and Programming Guide, chapter “Shutdown Function”.
3. Global shutdown (low active).
4. Global shutdown (high active).

Output behavior when disabled is also programmable. User will have the option to choose output driver behavior when it's off:

1. OUTx pin high, OUTxB pin low. (Controlled by SD/OE pin).
2. OUTx/OUTxB Hi-Z (Controlled by SD/OE pin).
3. OUTx pin high, OUTxB pin low. (Configured through I^2C).
4. OUTx/OUTxB Hi-Z (Configured by I^2C).

The user has the option to disable the output with either I^2C or SD/OE pin. For more details, refer to the VersaClock 6E Family Register Descriptions and Programming Guide.

6.9 I^2C Operation

The device acts as a slave device on the I^2C bus using one of the two I^2C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations.

Address bytes (2 bytes) specify the register address of the byte position of the first register to write or read.

Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first).

Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I^2C compliance, use external pull-up resistors for SDATA and SCLK.

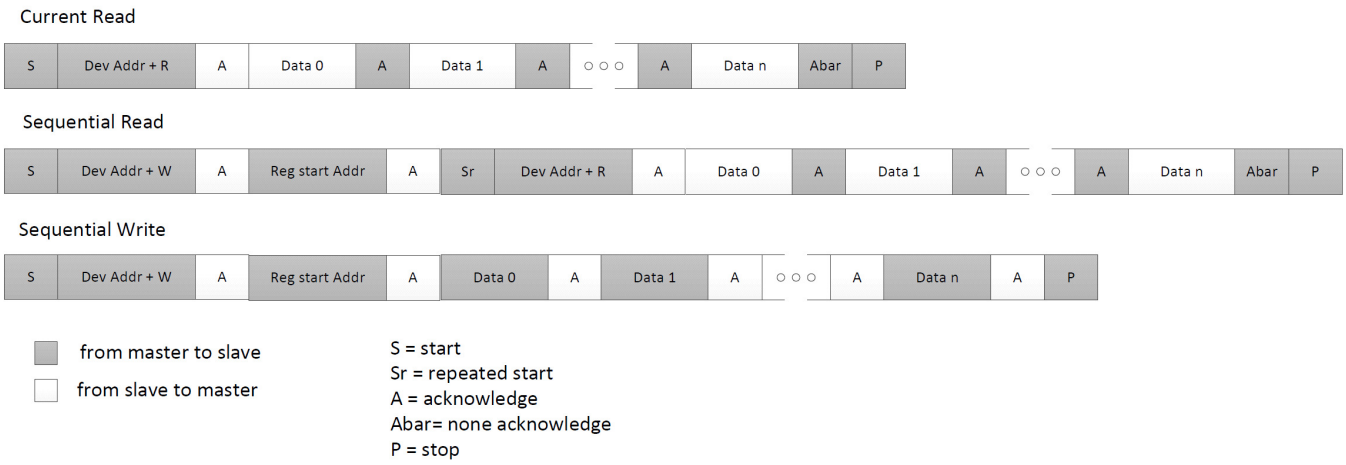


Figure 9. I^2C R/W Sequence

7. Typical Application Circuits

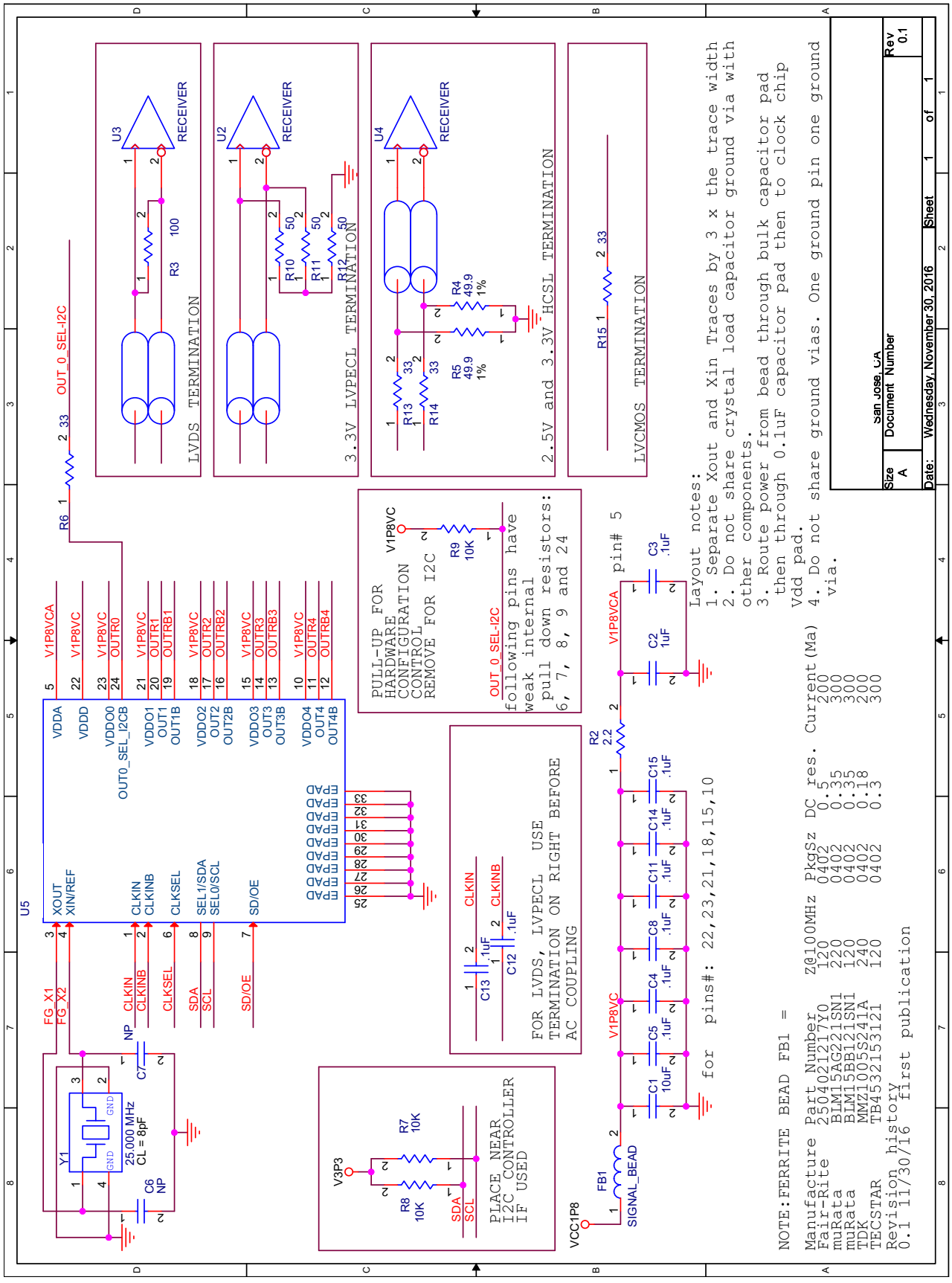


Figure 10. Application Circuit Example

7.1 Input – Driving the XIN/REF or CLKIN

7.1.1 Driving XIN/REF with a CMOS Driver

In some cases, it is encouraged to have XIN/REF driven by a clock input for reasons like better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin requires an input amplitude between 500mV and 1.2V. The clock slew rate should be at least 0.2V/ns (≥ 0.2V/ns).

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

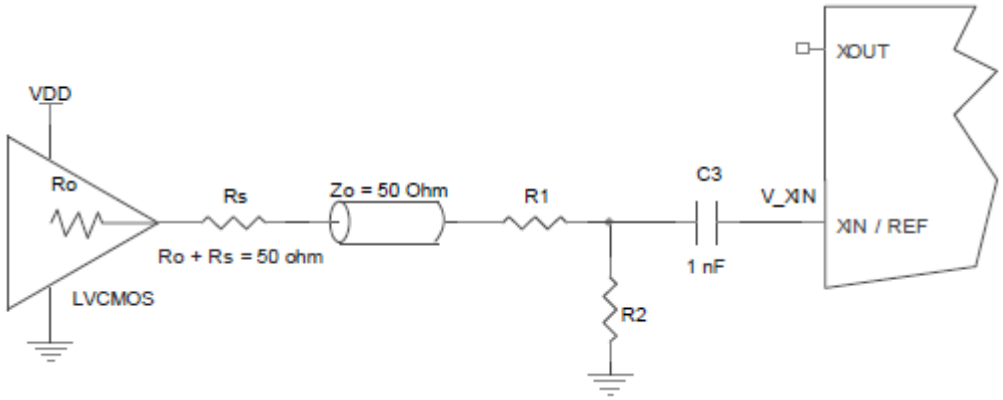


Figure 11. Overdriving XIN with a CMOS Driver

Table 19. Nominal Voltage Divider Values for Overdriving XIN with Single-ended Driver

LVCMOS Diver V_{DD}	Ro + Rs	R1	R2	V_XIN (peak)	Ro + Rs + R1 + R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

7.1.2 Driving XIN with an LVPECL Driver

Figure 12 shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

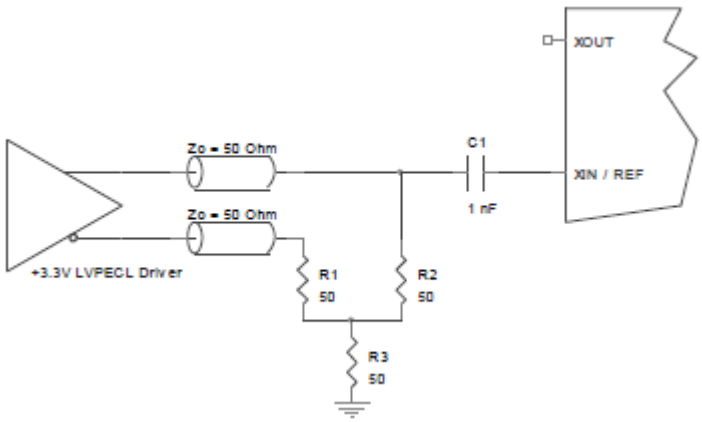


Figure 12. Overdriving XIN with an LVPECL Driver

7.1.3 Wiring the CLKIN Pin to Accept Single-ended Inputs

CLKIN cannot take a signal larger than 1.2V pk-pk due to the 1.2V regulated input inside. However, it is internally AC coupled so it is able to accept both LVDS and LVPECL input signals.

Occasionally, it is desired to have CLKIN to take CMOS levels. Below is an example showing how this can be achieved.

This configuration has three properties:

1. Total output impedance of Ro and Rs matches the 50Ω transmission line impedance.
2. Vrx voltage is generated at the CLKIN which maintains the LVCMOS driver voltage level across the transmission line for best S/N.
3. R1–R2 voltage divider values ensure that Vrx p-p at CLKIN is less than the maximum value of 1.2V.

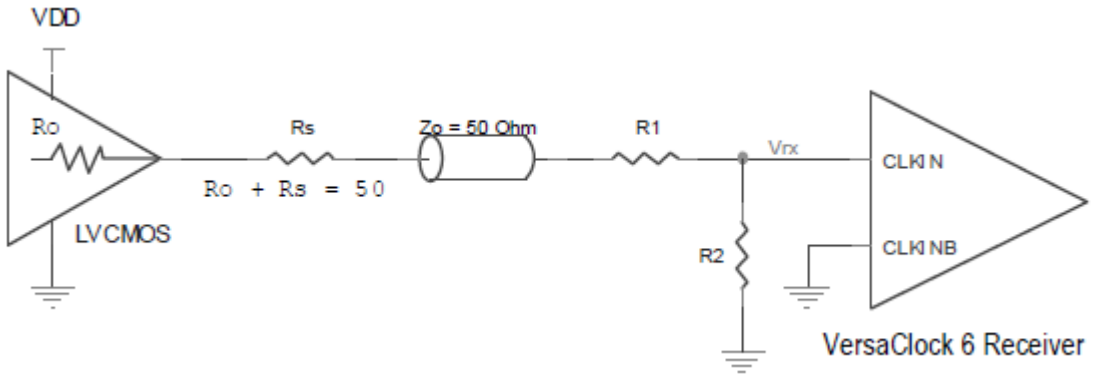


Figure 13. Recommended Schematic for Driving CLKIN with LVCMOS Driver

Table 20 shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver V_{DD}, V_{DDO0} and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the R1–R2 divider. To better assist this assessment, the total load (Ro + Rs + R1 + R2) on the driver is included in the table.

Table 20. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver

LVCMOS Diver V_{DD}	Ro + Rs	R1	R2	Vrx (peak)	Ro + Rs + R1 + R2
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

7.1.4 Driving CLKIN with Differential Clock

CLKIN/CLKINB will accept DC coupled HCSL/LVPECL/LVDS signals.

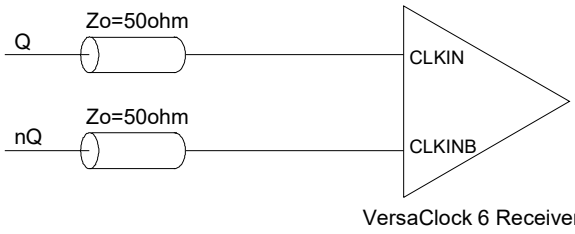


Figure 14. CLKIN, CLKINB Input Driven by an HCSL Driver

7.2 Output – Single-ended or Differential Clock Terminations

7.2.1 LVDS Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Zo) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination or optional termination schematic as shown in Figure 15 can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the Renesas LVDS output. If using a non-standard termination, it is recommended to contact Renesas and confirm that the termination will function as intended. For example, the LVDS outputs cannot be AC coupled by placing capacitors between the LVDS outputs and the 100Ω shunt load. If AC coupling is required, the coupling caps must be placed between the 100Ω shunt termination and the receiver. In this manner, the termination of the LVDS output remains DC coupled.

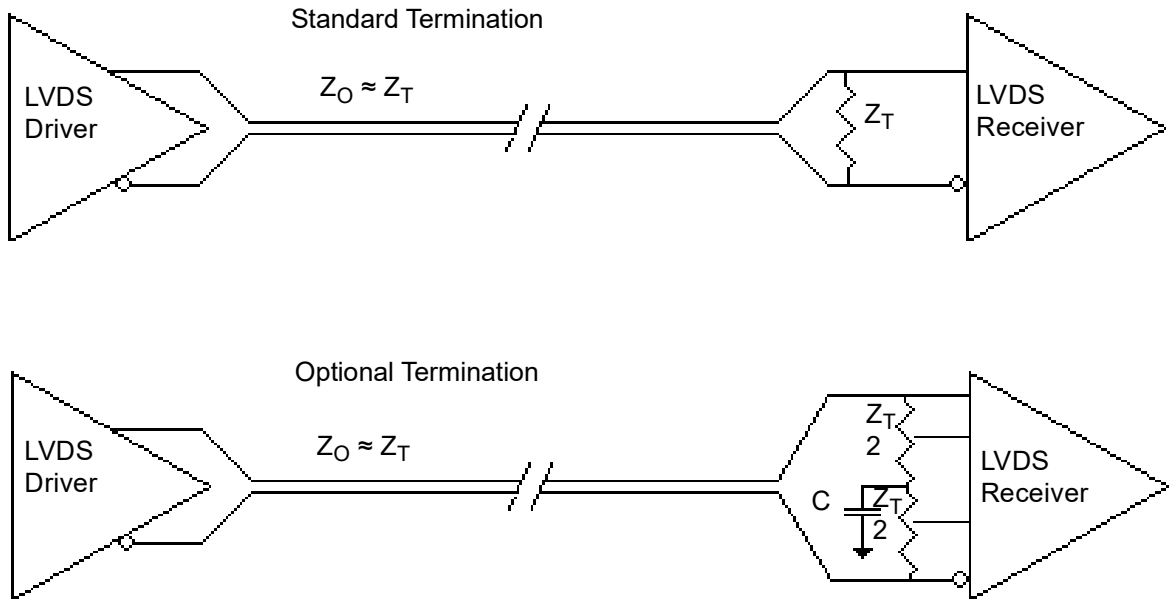


Figure 15. Standard and Optional Terminations

7.2.2 LVPECL Termination

The clock layout topology shown below is a typical termination for LVPECL outputs.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

For V_{DDO} = 2.5V, the V_{DDO} - 2V is very close to ground level. The R3 in 2.5V LVPECL output termination can be eliminated and the termination is shown in Figure 18, 2.5V LVPECL Output Termination.

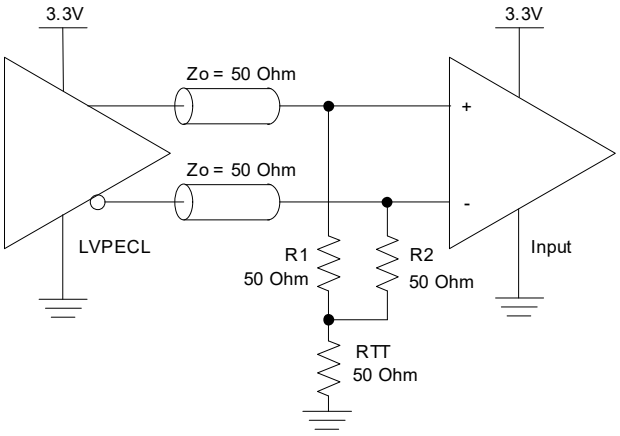


Figure 16. 3.3V LVPECL Output Termination (1)

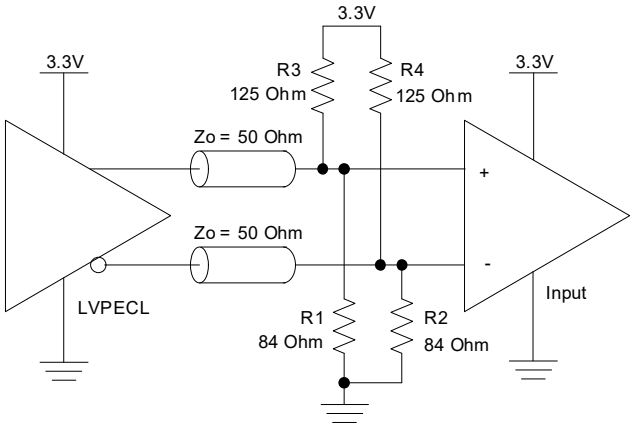


Figure 17. 3.3V LVPECL Output Termination (2)

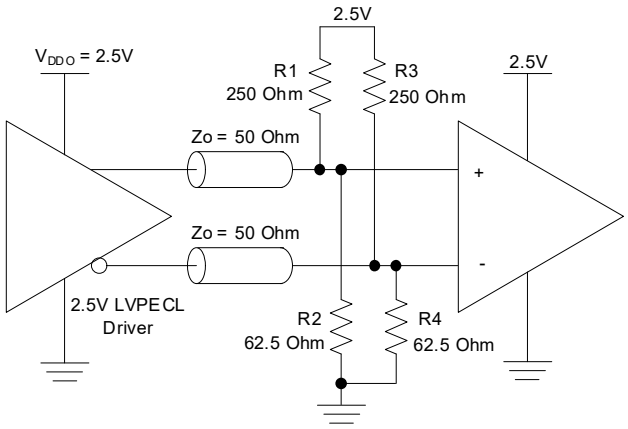


Figure 18. 2.5V LVPECL Output Termination

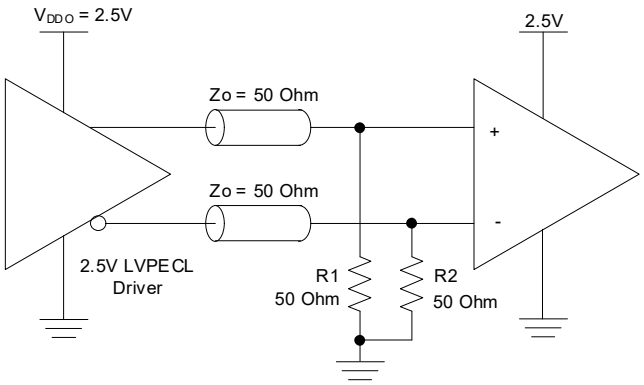


Figure 19. 2.5V LVPECL Driver Termination (1)

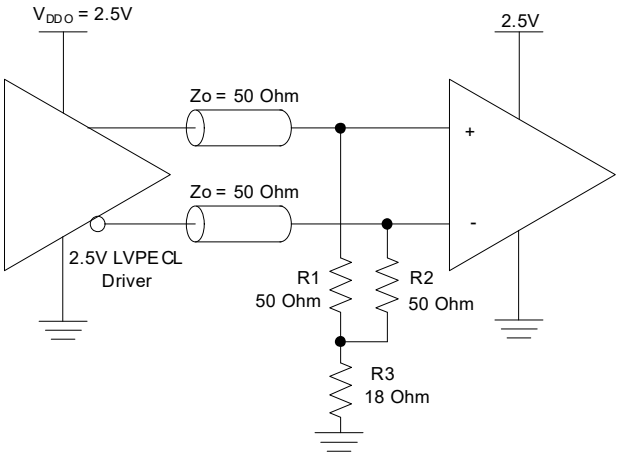


Figure 20. 2.5V LVPECL Driver Termination (2)

7.2.3 HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V V_{DDO}.

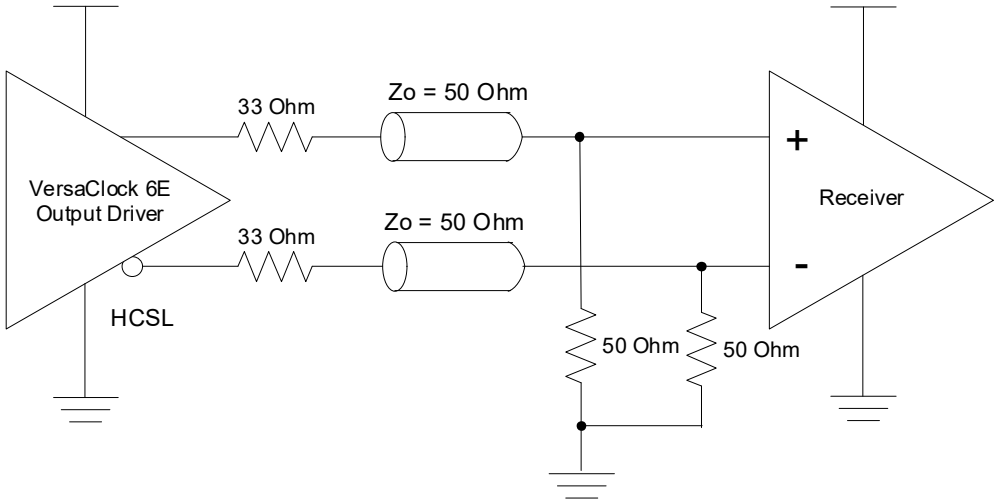


Figure 21. HCSL Receiver Terminated

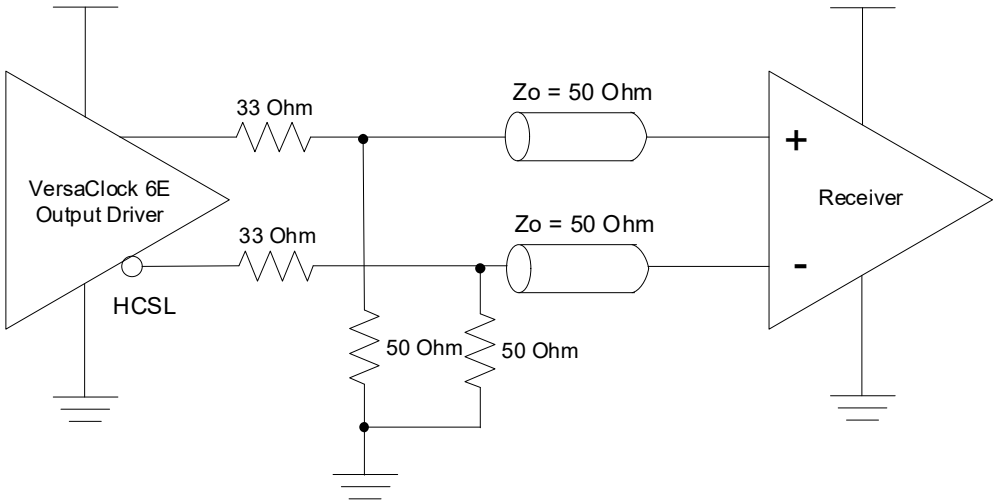


Figure 22. HCSL Source Terminated

7.2.4 LVCMOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. Example of CMOSD driver termination is shown below.

- CMOS1 – Single CMOS active on OUTx pin.
- CMOS2 – Single CMOS active on OUTxB pin.
- CMOSD – Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase.
- CMOSX2 – Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase.

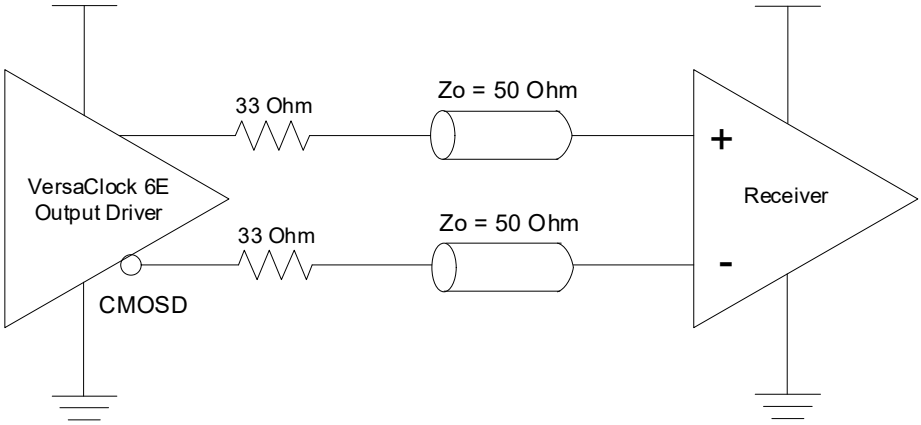
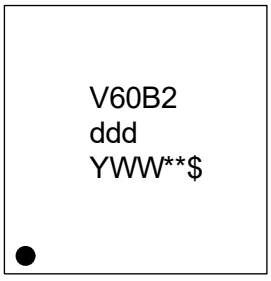


Figure 23. LVCMOS Termination

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

9. Marking Diagram



- Line 1: truncated part number.
- Line 2: “ddd” denotes dash code.
- Line 3:
  - “YWW” is the last digit of the year and week that the part was assembled.
  - “**” denotes sequential lot number.
  - “$” denotes mark code.

10. Ordering Information

Part Number [1]	Package Description	Carrier Type	Temperature Range
5P49V60BdddNLG2	4.0 × 4.0 mm, 0.5mm pitch 24-VFQFPN Wettable Flank	Tray	-40° to +105°C
5P49V60BdddNLG28	4.0 × 4.0 mm, 0.5mm pitch 24-VFQFPN Wettable Flank	Reel	-40° to +105°C

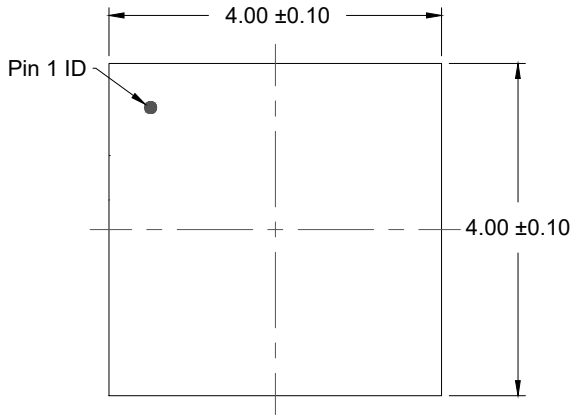
1. “ddd” denotes factory programmed configurations based on required settings. Contact factory for factory programming.

11. Revision History

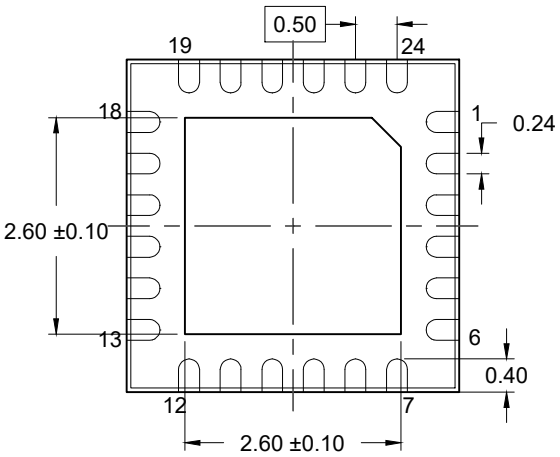
Revision	Date	Description
1.02	Jun 13, 2024	▪ Added ESD Charged Device Model and Latch Up specifications to Absolute Maximum Ratings.
1.01	Nov 3, 2023	▪ Corrected absolute maximum voltage for VDD pins in Absolute Maximum Ratings ▪ Removed footnote 1 (3.3V limitation) from I2C Bus DC Characteristics and adding V_{BUS} parameter. ▪ Corrected I2C Bus AC Characteristics footnote 2 to indicate 3.3V tolerance and moved to I2C Bus DC Characteristics where it belongs. ▪ Updated environmental conditions to a common footnote for electrical tables in Electrical Specifications and Jitter Performance Characteristics. ▪ Corrected RMS phase jitter conditions for LVCMOS outputs in Jitter Performance ▪ Removed heading 5.1 from PCI Express Jitter. Jitter is now provided in two tables in Jitter Performance Characteristics. ▪ Completed other minor changes.
1.00	Aug 9, 2023	Initial release.

Package Outline Drawing

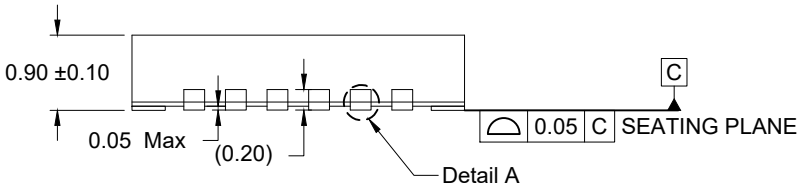
Package Code:NLG24S3
24-VFQFPN 4.0 x 4.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4192-07, Revision: 06, Date Created: Aug 1, 2022



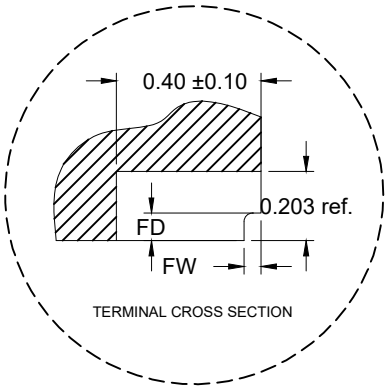
TOP VIEW



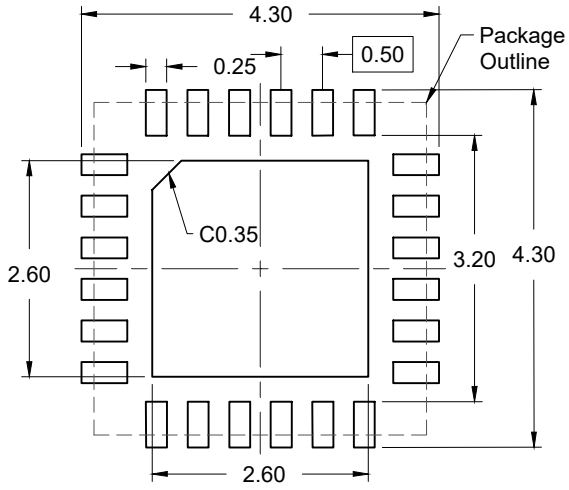
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.001	0.075

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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