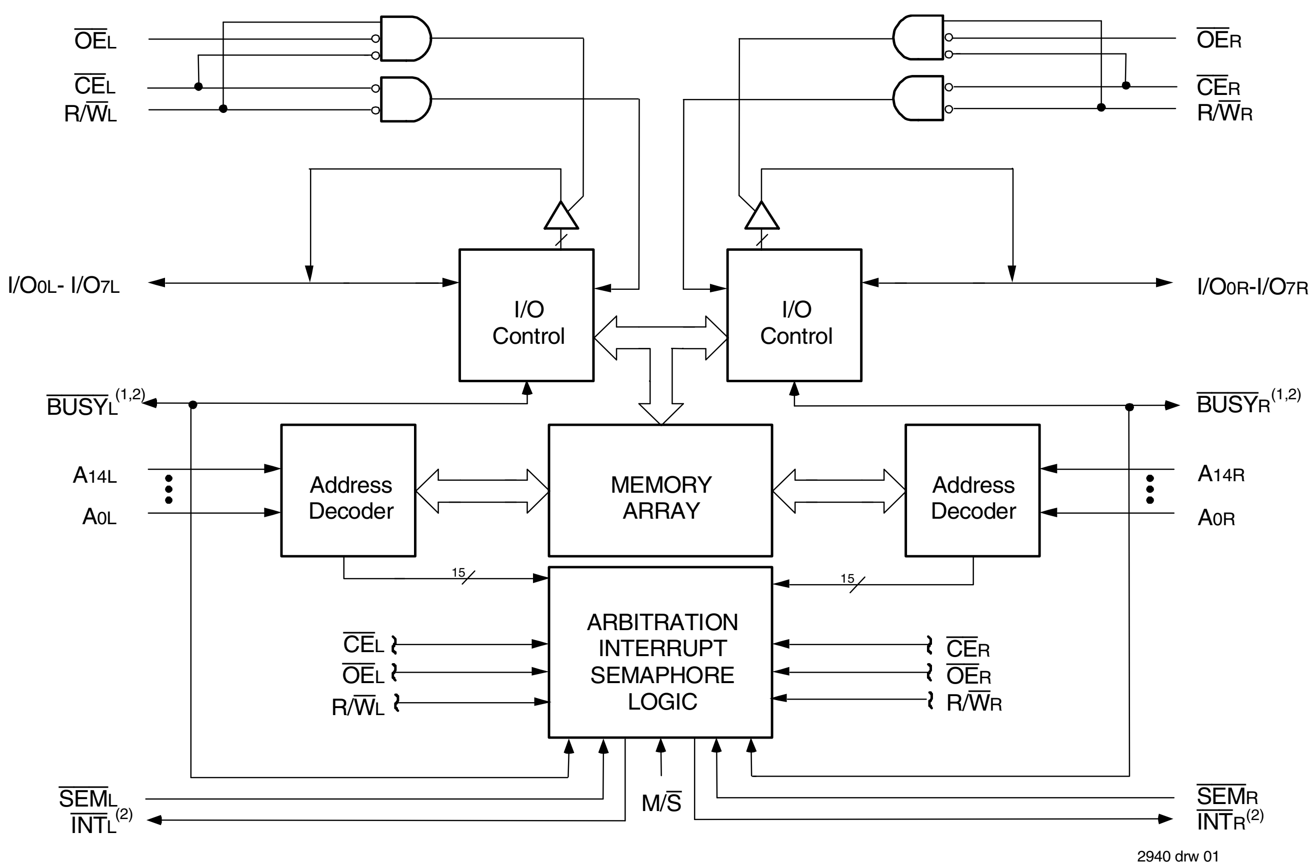
HIGH-SPEED 32K x 8 DUAL-PORT STATIC RAM

7007L

Features

- **True Dual-Ported memory cells which allow simultaneous reads of the same memory location**
- **High-speed access**
  - *Commercial: 15ns (max.)*
  - *Industrial: 20ns (max.)*
- **Low-power operation**
  - *IDT7007L*
    Active: 850mW (typ.)
    Standby: 1mW (typ.)
- **IDT7007 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device**
- **M/S = H for BUSY output flag on Master, M/S = L for BUSY input on Slave**
- **Interrupt Flag**
- **On-chip port arbitration logic**
- **Full on-chip hardware support of semaphore signaling between ports**
- **Fully asynchronous operation from either port**
- **TTL-compatible, single 5V (±10%) power supply**
- **Available in a 68-pin PLCC and a 80-pin TQFP**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



NOTES:
1. (MASTER): BUSY is output; (SLAVE): BUSY is input.
2. BUSY and INT outputs are non-tri-stated push-pull.

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DSC 2940/16

Description

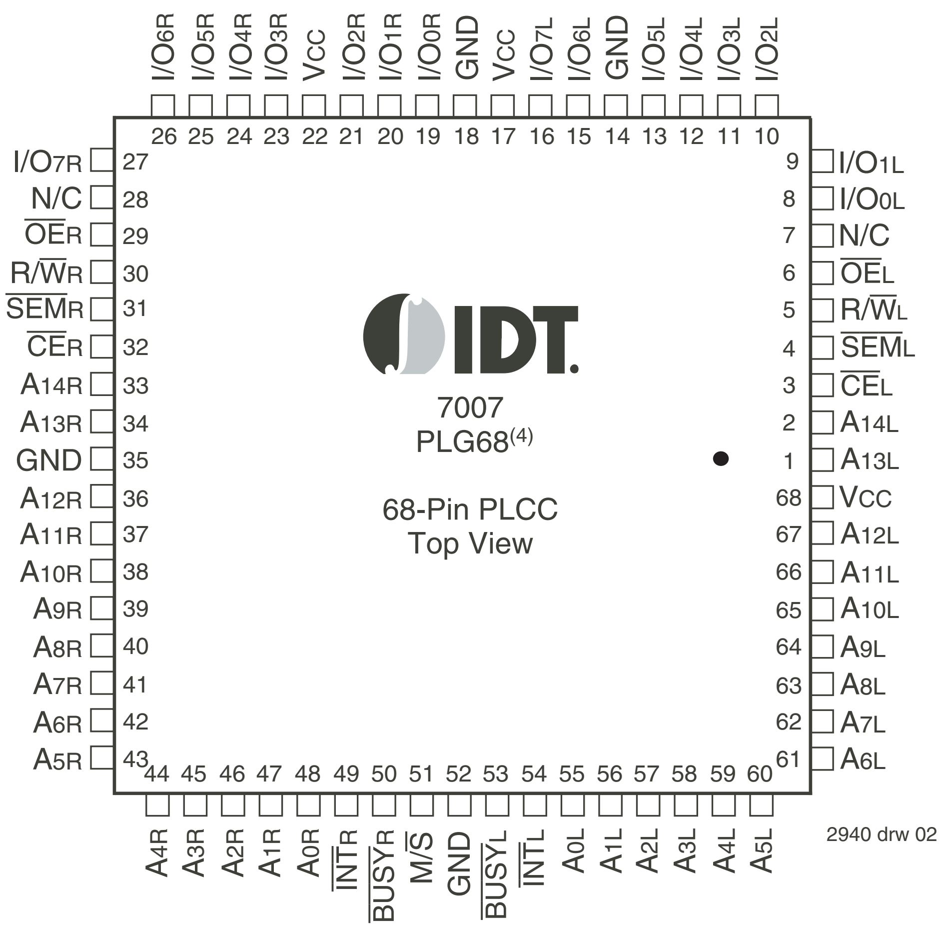
The IDT7007 is a high-speed 32K x 8 Dual-Port Static RAM. The IDT7007 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very LOW standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 850mW of power.

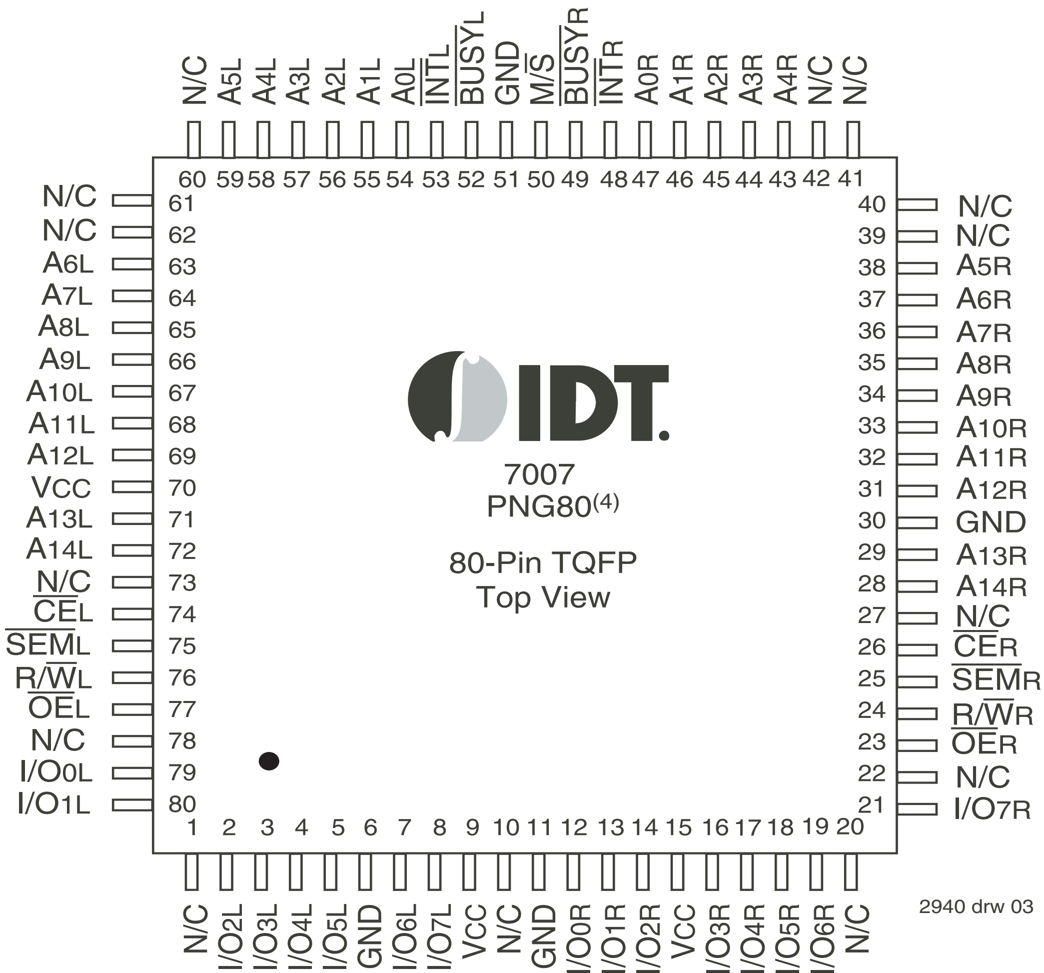
The IDT7007 is packaged in a 68-pin PLCC and an 80-pin thin quad flatpack TQFP.

Pin Configurations(1,2,3)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately .95 in x .95 in x .17 in.
4. This package code is used to reference the package diagram.

Pin Configurations(1,2,3) (con't.)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Pin Configurations[1,2,3] (con't.)

	A	B	C	D	E	F	G	H	J	K	L
11		51 A5L	50 A4L	48 A2L	46 A0L	44 $\overline{\text{BUSY}}$L	42 M/$\overline{\text{S}}$	40 $\overline{\text{INT}}$R	38 A1R	36 A3R	11/06/01
10	53 A7L	52 A6L	49 A3L	47 A1L	45 $\overline{\text{INT}}$L	43 GND	41 $\overline{\text{BUSY}}$R	39 A0R	37 A2R	35 A4R	34 A5R
09	55 A9L	54 A8L								32 A7R	33 A6R
08	57 A11L	56 A10L								30 A9R	31 A8R
07	59 VCC	58 A12L								28 A11R	29 A10R
06	61 A14L	60 A13L								26 GND	27 A12R
05	63 $\overline{\text{SEM}}$L	62 $\overline{\text{CE}}$L								24 A14R	25 A13R
04	65 $\overline{\text{OE}}$L	64 R/$\overline{\text{W}}$L								22 $\overline{\text{SEM}}$R	23 $\overline{\text{CE}}$R
03	67 I/O0L	66 N/C								20 $\overline{\text{OE}}$R	21 R/$\overline{\text{W}}$R
02	68 I/O1L	1 I/O2L	3 I/O4L	5 GND	7 I/O7L	9 GND	11 I/O1R	13 VCC	15 I/O4R	18 I/O7R	19 N/C
01	INDEX	2 I/O3L	4 I/O5L	6 I/O6L	8 VCC	10 I/O0R	12 I/O2R	14 I/O3R	16 I/O5R	17 I/O6R	

IDT7007G
GU68[4]

68-Pin PGA
Top View[5]

2940 drw 04b

NOTES:
1. All Vcc pins must be connected to power supply
2. All GND pins must be connected to ground.
3. Package body is approximately 1.8 in x 1.8 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part marking.

Pin Names

Left Port	Right Port	Names
$\overline{\text{CE}}$L	$\overline{\text{CE}}$R	Chip Enables
R/$\overline{\text{W}}$L	R/$\overline{\text{W}}$R	Read/Write Enable
$\overline{\text{OE}}$L	$\overline{\text{OE}}$R	Output Enable
A0L - A14L	A0R - A14R	Address
I/O0L - I/O7L	I/O0R - I/O7R	Data Input/Output
$\overline{\text{SEM}}$L	$\overline{\text{SEM}}$R	Semaphore Enable
$\overline{\text{INT}}$L	$\overline{\text{INT}}$R	Interrupt Flag
$\overline{\text{BUSY}}$L	$\overline{\text{BUSY}}$R	Busy Flag
M/$\overline{\text{S}}$		Master or Slave Select
VCC		Power
GND		Ground

2940 tbl 01

Truth Table I: Non-Contention Read/Write Control

Inputs[1]				Outputs	Mode
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

2940 tbl 02

NOTE:
1. $A_{0L} — A_{14L} \neq A_{0R} — A_{14R}$

Truth Table II: Semaphore Read/Write Control[1]

Inputs				Outputs	Mode
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	
H	H	L	L	DATAOUT	Read Semaphore Flag Data Out (I/O0-I/O7)
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	——	Not Allowed

2940 tbl 03

NOTE:
1. There are eight semaphore flags written to via I/O0 and read from all I/O's. These eight semaphores are addressed by A0 - A2.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2940 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of VTERM $\geq$ Vcc + 10%.

Capacitance (TA = +25°C, f = 1.0Mhz)

Symbol	Parameter[1]	Conditions[2]	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

2940 tbl 07

NOTES:
1. This parameter is determined by device characterization but is not production tested. TQFP package only.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage[1]

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to+125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2940 tbl 05

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	——	6.0[2]	V
VIL	Input Low Voltage	-0.5[1]	——	0.8	V

2940 tbl 06

NOTES:
1. VIL $\geq$ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7007S Min.	7007S Max.	7007L Min.	7007L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2940 tbl 08

NOTE:
1. At Vcc $\leq$ 2.0V, input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7007X15 Com'l Only Typ.[2]	7007X15 Com'l Only Max.	7007X20 Com'l & Ind Typ.[2]	7007X20 Com'l & Ind Max.	7007X25 Com'l, Ind & Military Typ.[2]	7007X25 Com'l, Ind & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	190 190	325 285	180 180	315 275	170 170	305 265	mA
			MIL & IND	S L	— —	— —	— 180	— 315	170 170	345 305	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH} $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	35 35	85 60	30 30	85 60	25 25	85 60	mA
			MIL & IND	S L	— —	— —	— 30	— 80	25 25	100 80	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[3] $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	COM'L	S L	125 125	220 190	115 115	210 180	105 105	200 170	mA
			MIL & IND	S L	— —	— —	— 115	— 210	105 105	230 200	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0[4] $\overline{SEM_R}$ = $\overline{SEM_L}$ $\geq$ V_{CC} - 0.2V	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 5	mA
			MIL & IND	S L	— —	— —	— 0.2	— 10	1.0 0.2	30 10	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{CC} - 0.2V[5] $\overline{SEM_R}$ = $\overline{SEM_L}$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	S L	120 120	190 160	110 110	185 160	100 100	175 160	mA
			MIL & IND	S L	— —	— —	— 110	— 185	100 100	200 175	

2940 tbl 09

NOTES:
1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using “AC Test Conditions” of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1] (con't.) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7007X35 Com'l, Ind & Military		7007X55 Com'l, Ind & Military		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Disabled $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	160 160	295 255	150 150	270 230	mA
			MIL & IND	S L	160 160	335 295	150 150	310 270	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	20 20	85 60	20 20	85 60	mA
			MIL & IND	S L	20 20	100 80	13 13	100 80	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Disabled, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S L	95 95	185 155	85 85	165 135	mA
			MIL & IND	S L	95 95	215 185	85 85	195 165	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ $\geq$ V_{CC} - 0.2V	COM'L	S L	1.0 0.2	15 5	1.0 0.2	15 5	mA
			MIL & IND	S L	1.0 0.2	30 10	1.0 0.2	30 10	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ $\leq$ 0.2V and $\overline{CE}_{"B"}$ $\geq$ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ $\geq$ V_{CC} - 0.2V V_{IN} $\geq$ V_{CC} - 0.2V or V_{IN} $\leq$ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	S L	90 90	160 135	80 80	135 110	mA
			MIL & IND	S L	90 90	190 165	80 80	165 140	

2940 tbl 10

NOTES:
1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/t_{RC}$, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2940 tbl 11

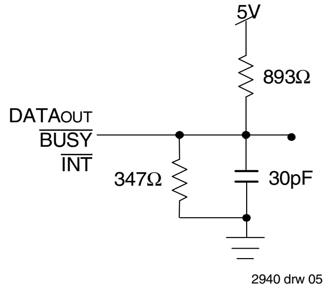


Figure 1. AC Output Test Load

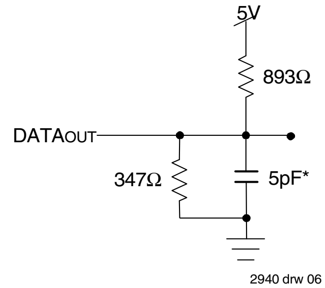


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
* Including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(4)

Symbol	Parameter	7007X15 Com'l Only Min.	7007X15 Com'l Only Max.	7007X20 Com'l & Ind Min.	7007X20 Com'l & Ind Max.	7007X25 Com'l, Ind & Military Min.	7007X25 Com'l, Ind & Military Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time(3)	—	15	—	20	—	25	ns
t_{AOE}	Output Enable Access Time	—	10	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	10	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	15	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	12	—	ns
t_{SAA}	Semaphore Address Access Time	—	15	—	20	—	25	ns

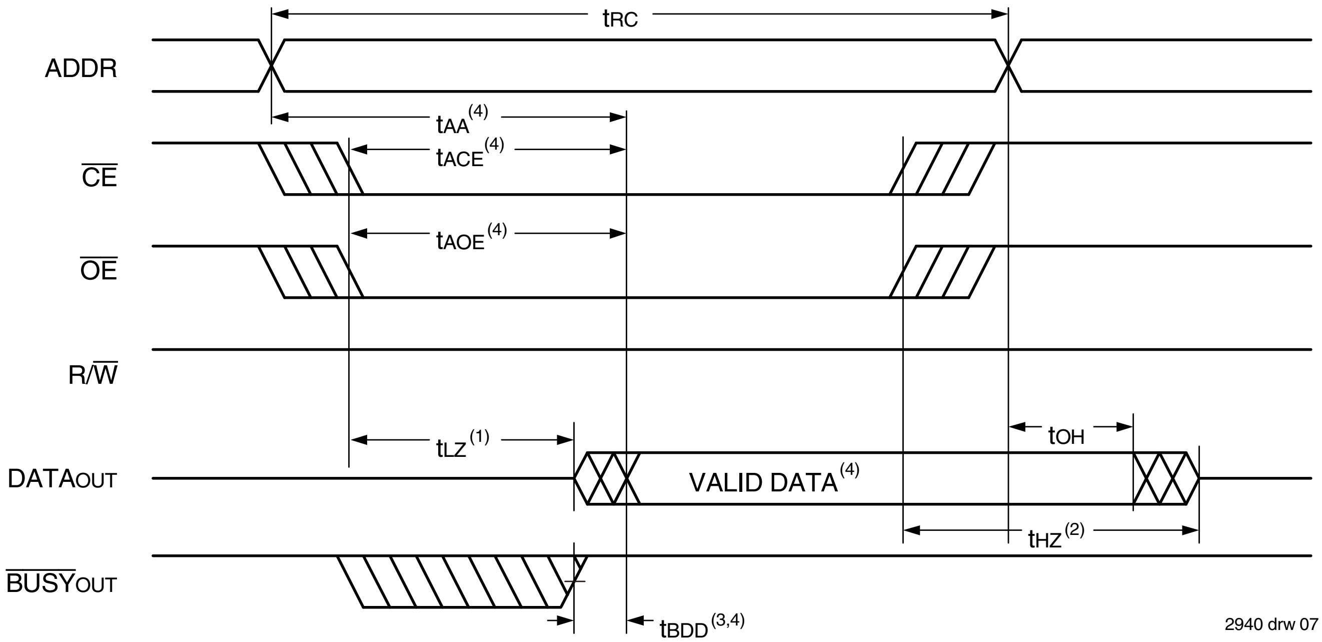
2940 tbl 12a

Symbol	Parameter	7007X35 Com'l, Ind & Military Min.	7007X35 Com'l, Ind & Military Max.	7007X55 Com'l, Ind & Military Min.	7007X55 Com'l, Ind & Military Max.	Unit
READ CYCLE						
t_{RC}	Read Cycle Time	35	—	55	—	ns
t_{AA}	Address Access Time	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time(3)	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time(1,2)	3	—	3	—	ns
t_{HZ}	Output High-Z Time(1,2)	—	15	—	25	ns
t_{PU}	Chip Enable to Power Up Time(2)	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time(2)	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	35	—	55	ns

2940 tbl 12b

NOTES:
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, CE = V_{IH} and SEM = V_{IL}.
4. 'X' in part numbers indicates power rating (S or L).

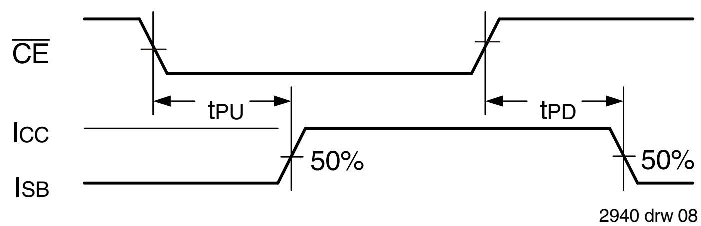
Waveform of Read Cycles(5)



NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. t_{BDD} delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.

Timing of Power-Up Power-Down



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5]

Symbol	Parameter	7007X15 Com'l Only		7007X20 Com'l & Ind		7007X25 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	12	—	15	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	10	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

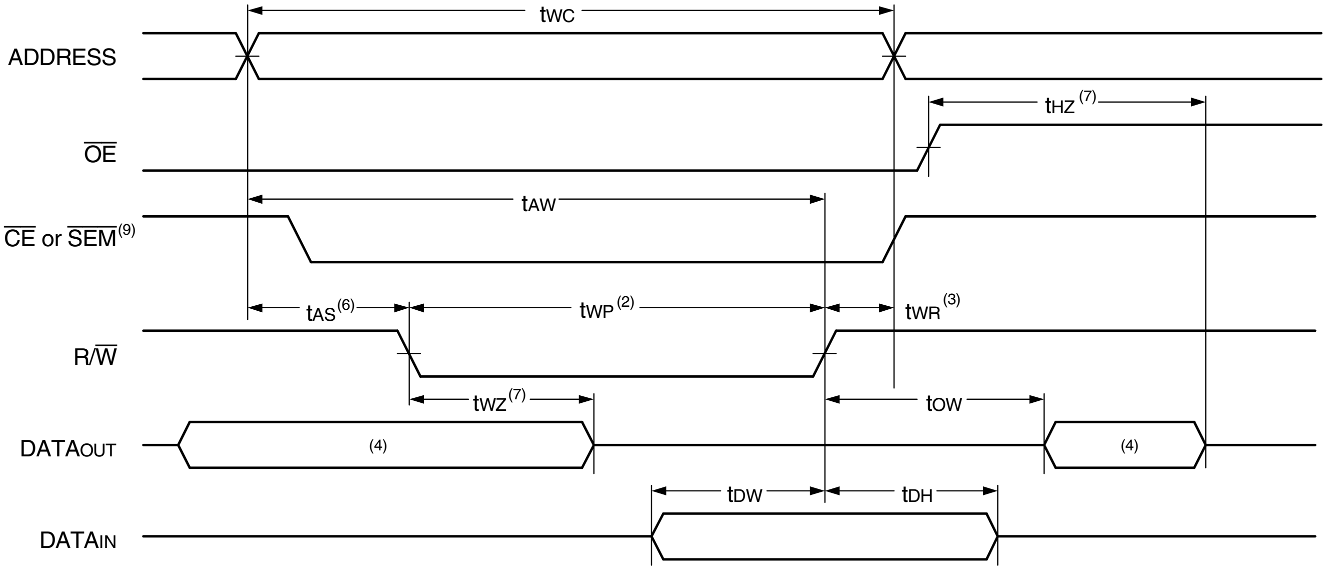
2940 tbl 13a

Symbol	Parameter	7007X35 Com'l, Ind & Military		7007X55 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	25	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	12	—	25	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

2940 tbl 13b

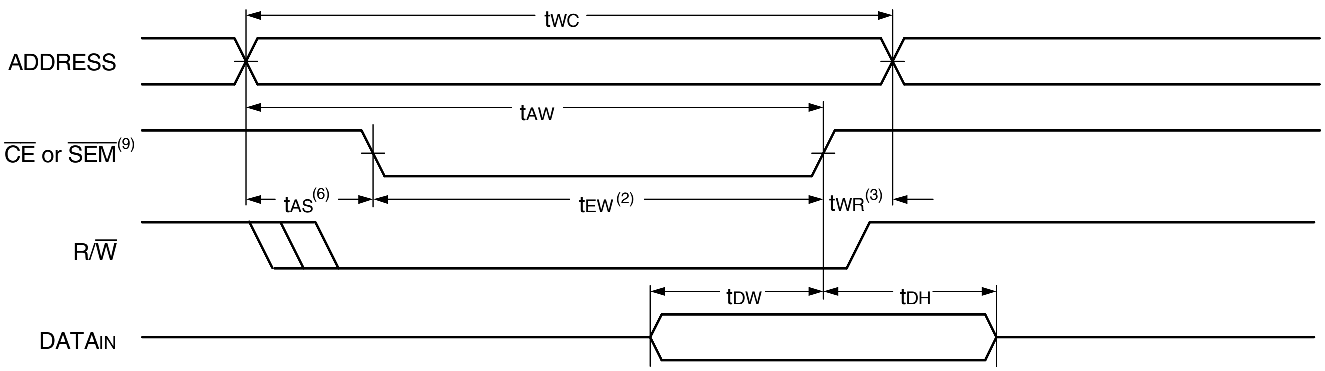
NOTES:
1. Transition is measured 0mV from Low- or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part numbers indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



2940 drw 09

Timing Waveform of Write Cycle No. 2, $\overline{CE}$ Controlled Timing(1,5)

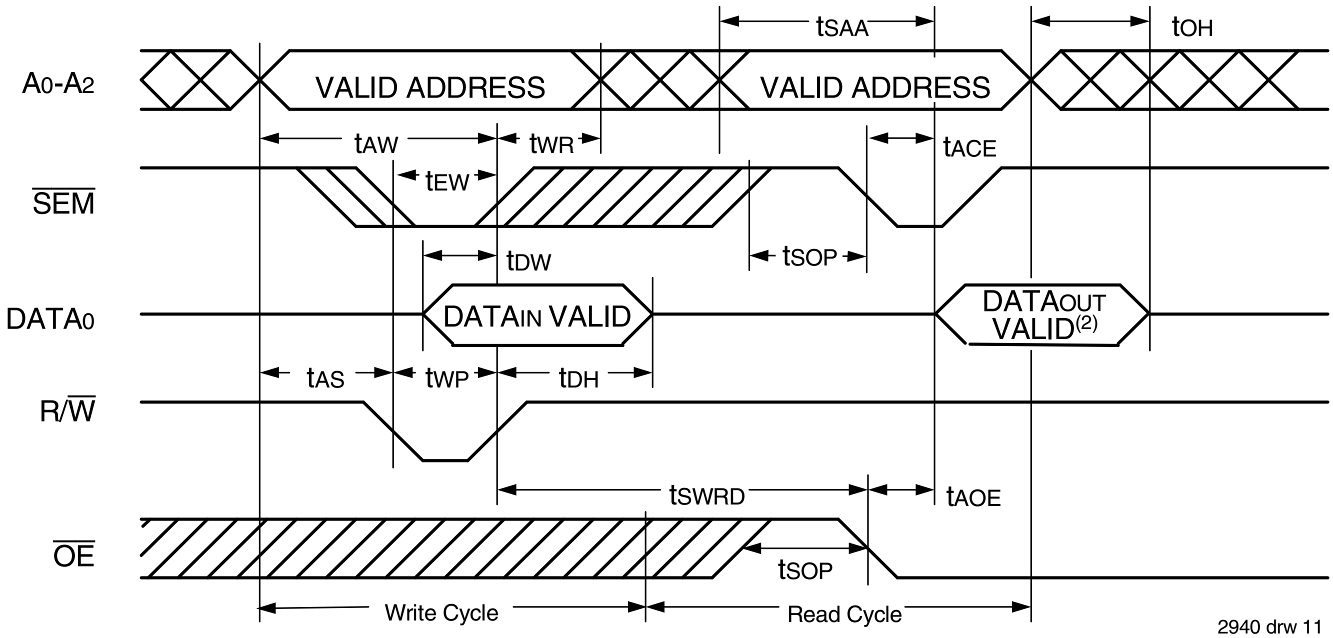


2940 drw 10

NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. t_{EW} must be met for either condition.

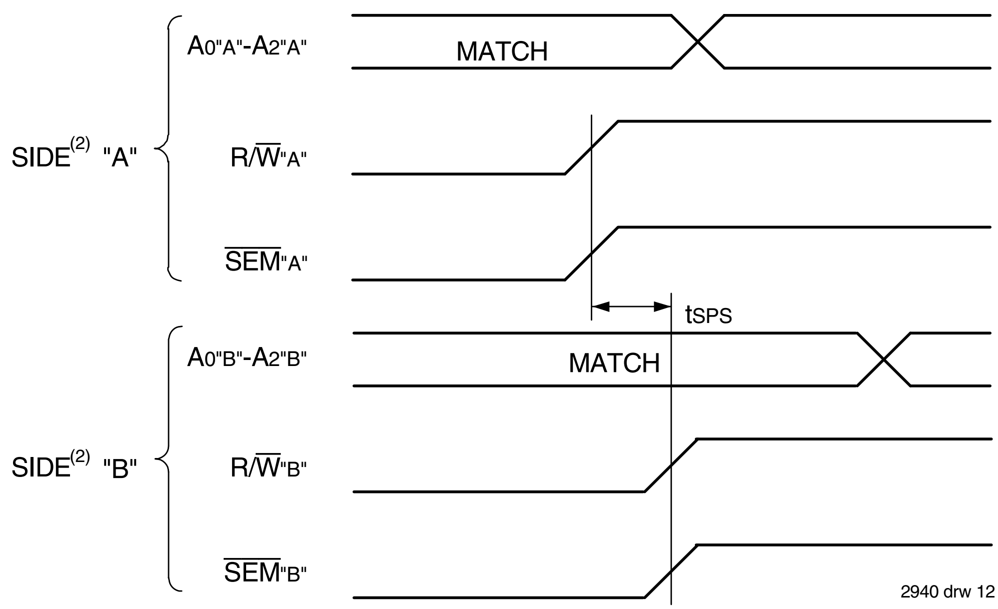
Timing Waveform of Semaphore Read after Write Timing, Either Side(1)



2940 drw 11

NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

Timing Waveform of Semaphore Write Contention(1,3,4)



2940 drw 12

NOTES:
1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$A or $\overline{SEM}$A going HIGH to R/$\overline{W}$B or $\overline{SEM}$B going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[6]

Symbol	Parameter	7007X15 Com'l Only		7007X20 Com'l & Ind		7007X25 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/S=VIH)								
tBAA	BUSY Access Time from Address Match	—	15	—	20	—	20	ns
tBDA	BUSY Disable Time from Address Not Matched	—	15	—	20	—	20	ns
tBAC	BUSY Access Time from Chip Enable Low	—	15	—	20	—	20	ns
tBDC	BUSY Access Time from Chip Enable High	—	15	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[3]	—	18	—	30	—	30	ns
tWH	Write Hold After BUSY[5]	12	—	15	—	17	—	ns
BUSY TIMING (M/S=VIL)								
tWB	BUSY Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After BUSY[5]	12	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	30	—	35	ns

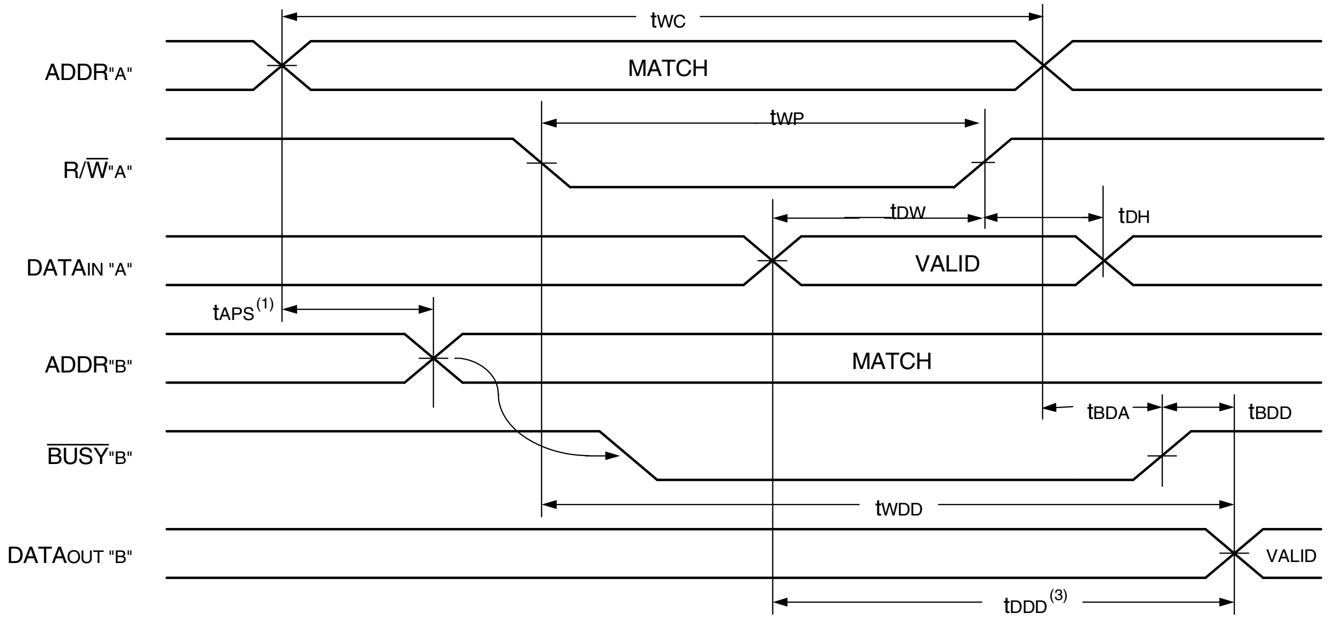
2940 tbl 14a

Symbol	Parameter	7007X35 Com'l, Ind & Military		7007X55 Com'l, Ind & Military		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/S=VIH)						
tBAA	BUSY Access Time from Address Match	—	20	—	45	ns
tBDA	BUSY Disable Time from Address Not Matched	—	20	—	40	ns
tBAC	BUSY Access Time from Chip Enable Low	—	20	—	40	ns
tBDC	BUSY Access Time from Chip Enable High	—	20	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	BUSY Disable to Valid Data[3]	—	35	—	40	ns
tWH	Write Hold After BUSY[5]	25	—	25	—	ns
BUSY TIMING (M/S=VIL)						
tWB	BUSY Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After BUSY[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	ns

2940 tbl 14b

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY (M/S = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (S or L).

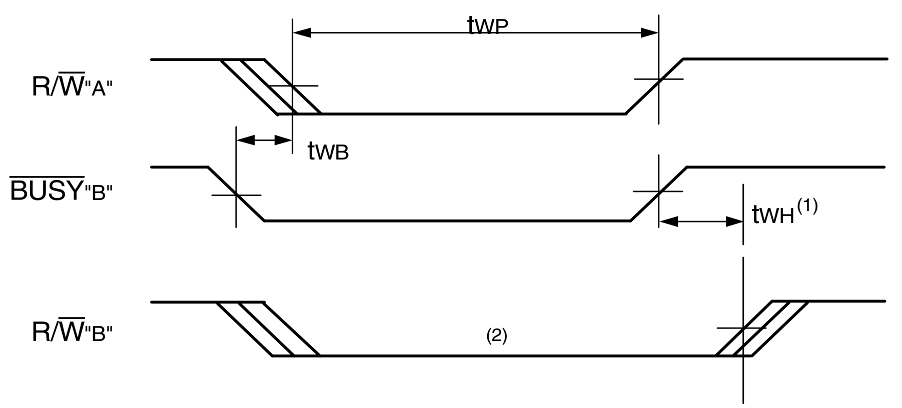
Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$[2,5] (M/$\overline{S}$ = VIH)[4]



2940 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}$L = $\overline{CE}$R = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

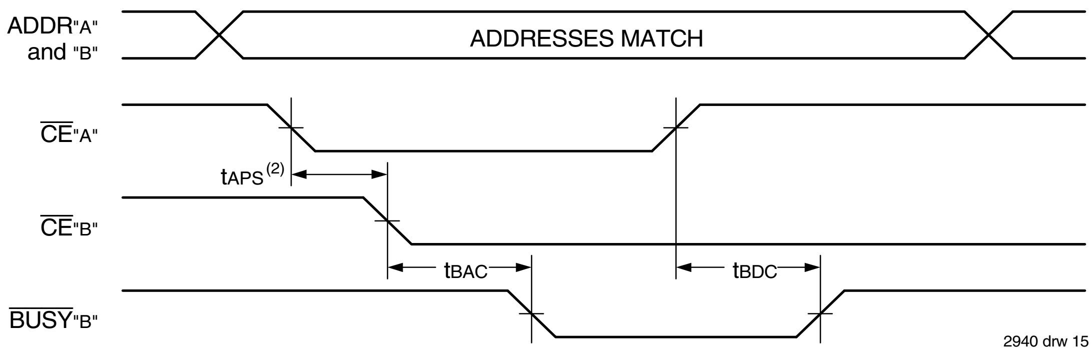
Timing Waveform of Write with $\overline{BUSY}$ (M/$\overline{S}$ = VIL)



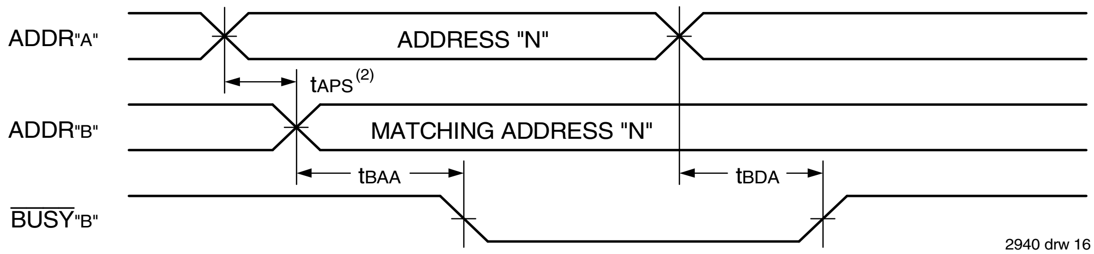
2940 drw 14

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.

Waveform of BUSY Arbitration Controlled by CE Timing[1] (M/S = VIH)



Waveform of BUSY Arbitration Cycle Controlled by Address Match Timing[1] (M/S = VIH)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,2]

		7007X15 Com'l Only		7007X20 Com'l & Ind		7007X25 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	ns

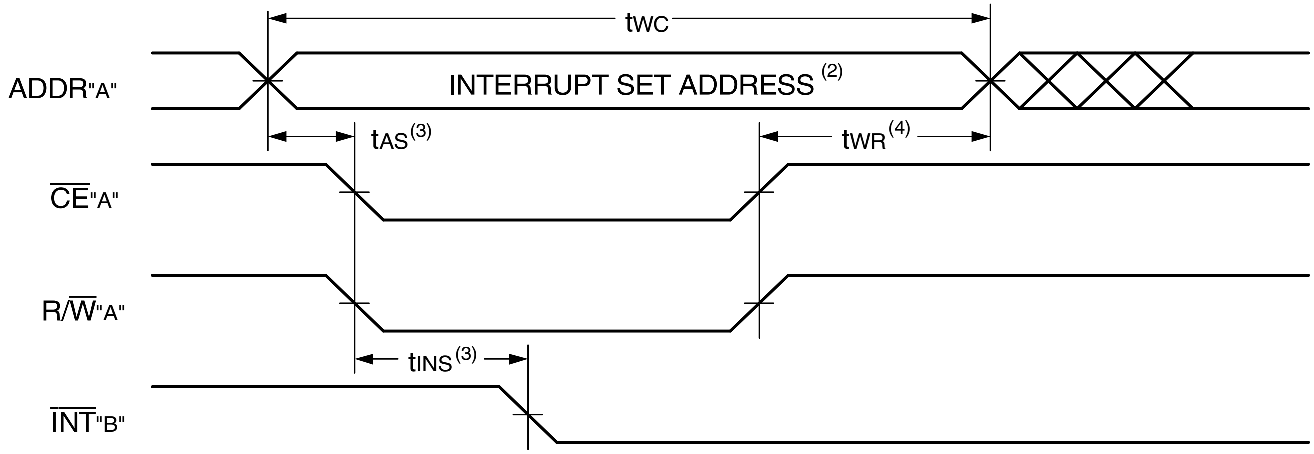
2940 tbl 15a

		7007X35 Com'l, Ind & Military		7007X55 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	ns
tINR	Interrupt Reset Time	—	25	—	40	ns

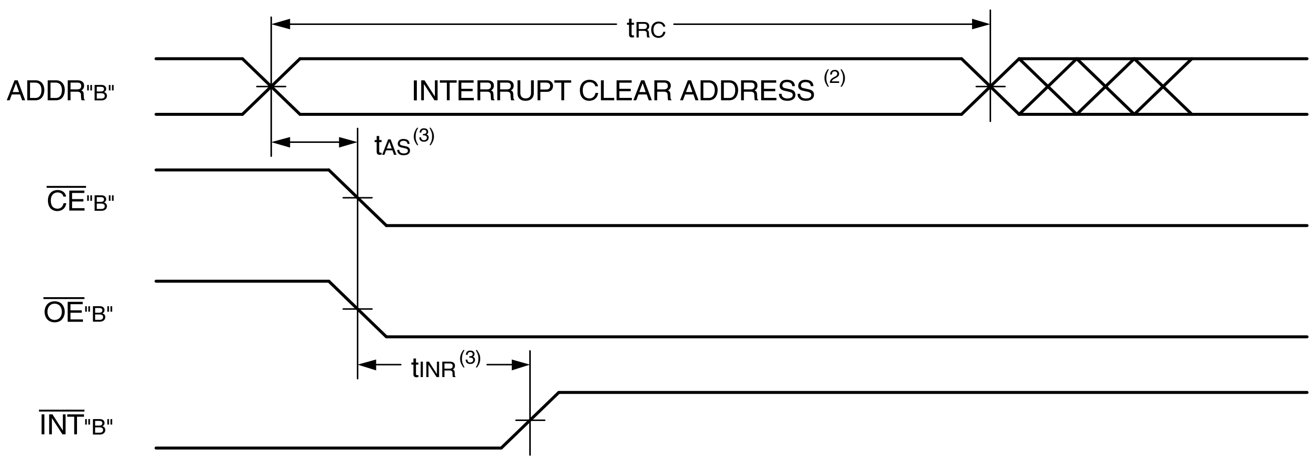
2940 tbl 15b

NOTES:
1. 'X' in part numbers indicates power rating (S or L).

Waveform of Interrupt Timing[1]



2940 drw 17



2940 drw 18

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from port “A”.
2. See Interrupt Truth Table III.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

Truth Table III — Interrupt Flag[1]

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{14L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{14R}-A_{0R}	$\overline{INT}_R$	
L	L	X	7FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2940 tbl 16

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.

Truth Table IV — Address $\overline{\text{BUSY}}$ Arbitration

Inputs			Outputs		Function
$\overline{\text{CE}}_L$	$\overline{\text{CE}}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{\text{BUSY}}_L$(1)	$\overline{\text{BUSY}}_R$(1)	
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2940 tbl 17

NOTES:
1. Pins $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{\text{BUSY}}$ outputs on the IDT7007 are push-pull, not open drain outputs. On slaves the $\overline{\text{BUSY}}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{\text{BUSY}}_L$ or $\overline{\text{BUSY}}_R$ = LOW will result. $\overline{\text{BUSY}}_L$ and $\overline{\text{BUSY}}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{\text{BUSY}}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{\text{BUSY}}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Truth Table V — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2940 tbl 18

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7007.
2. There are eight semaphore flags written to via I/O_5(I/O_0 - I/O_7) and read from all I/O_0. These eight semaphores are addressed by A_0 - A_2.
3. $\overline{\text{CE}}$ = V_{IH}, $\overline{\text{SEM}}$ = V_{IL} to access the semaphores. Refer to the Semaphore Read/Write Control Truth Table.

Functional Description

The IDT7007 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7007 has an automatic power down feature controlled by $\overline{\text{CE}}$. The $\overline{\text{CE}}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{\text{CE}}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{\text{INT}}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{\text{CE}}$ = R/$\overline{\text{W}}$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFE when $\overline{\text{CE}}_R$ = $\overline{\text{OE}}_R$ = V_{IL}, R/$\overline{\text{W}}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{\text{INT}}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{\text{INT}}_R$), the right port must read the memory location 7FFF. The message (8 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Table III for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT 7007 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic

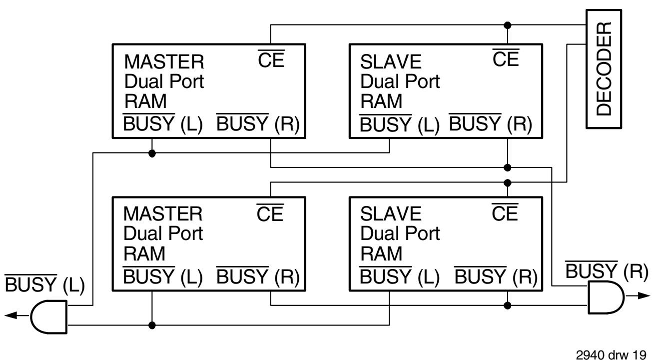


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7007 RAMs.

Master/Slave Arrays

When expanding an IDT7007 RAM array in width while using BUSY logic, one master part is used to decide which side of the RAMs array will receive a BUSY indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the BUSY signal as a write inhibit signal. Thus on the IDT7007 RAM the BUSY pin is an output if the part is used as a master (M/S pin = H), and the BUSY pin is an input if the part used as a slave (M/S pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a BUSY flag to be output from the master before the actual write pulse can be initiated with the R/W signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT7007 is an extremely fast Dual-Port 16K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by CE, the Dual-Port RAM enable, and SEM, the semaphore enable. The CE and SEM pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where CE and SEM are both HIGH.

Systems which can best use the IDT7007 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7007 hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7007 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7007 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A_0–A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table V). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table V). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

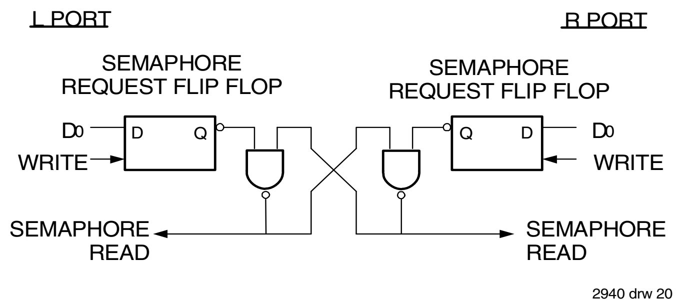


Figure 4. IDT7007 Semaphore Logic

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7007's Dual-Port RAM. Say the 32K x 8 RAM was to be divided into two 16K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 16K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 16K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 16K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 16K blocks of Dual-Port RAM with each other.

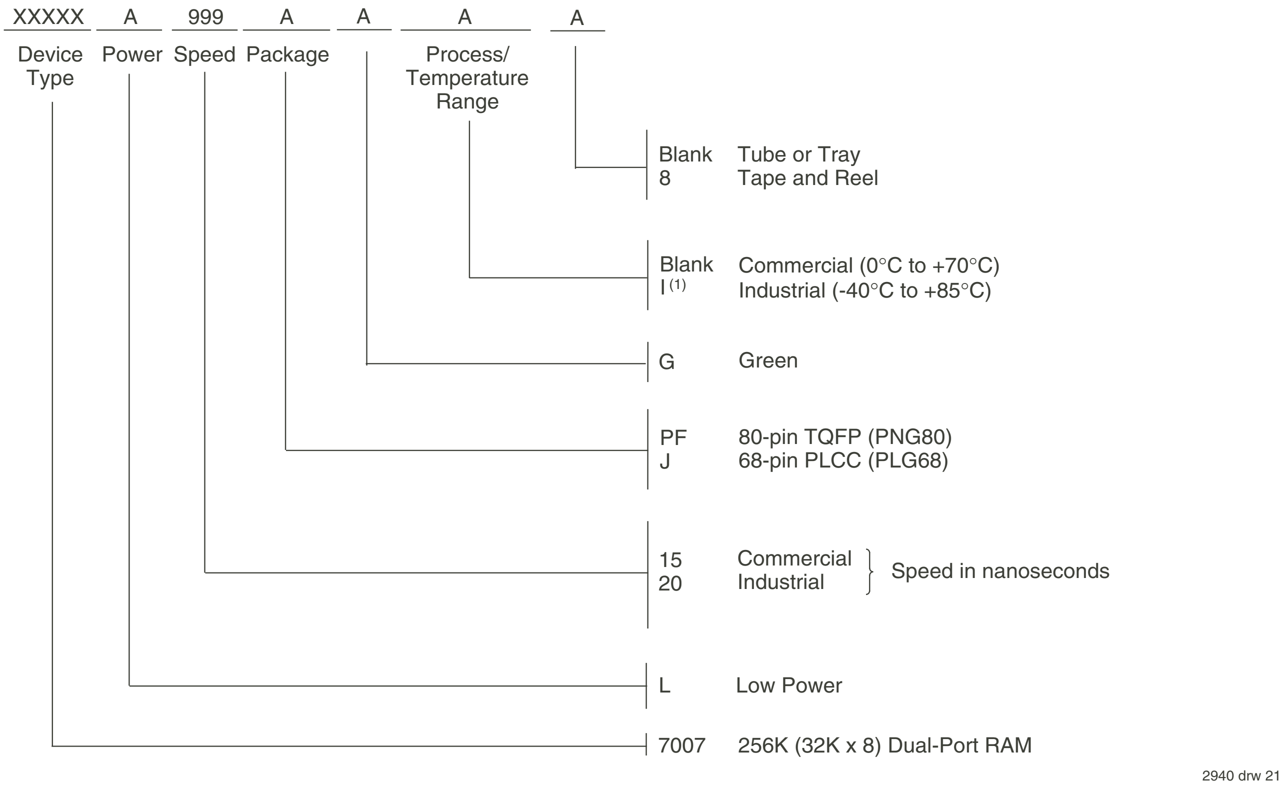
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

Ordering Information



NOTES:
1. Contact your local sales office for industrial temp. range for other speeds, packages and powers.
   LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02
   Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
15	7007L15JG	PLG68	PLCC	C
	7007L15JG8	PLG68	PLCC	C
	7007L15PFG	PNG80	TQFP	C
20	7007L20JGI	PLG68	PLCC	I
	7007L20JGI8	PLG68	PLCC	I
	7007L20PFGI	PNG80	TQFP	I

Datasheet Document History

01/05/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Pages 2, 3, 4	Added additional notes to pin configurations
06/03/99:		Changed drawing format
03/24/00:		Added Industrial Temperature Ranges and removed related notes
		Replaced IDT logo
		Changed ±200mV to 0mV in notes
05/08/00:	Page 1	Added copyright info
	Page 5	Fixed Absolute Maximum Ratings chart, corrected typos
	Page 9	Updated drawings
	Page 12	Corrected waveform drawing
	Page 5	Increased storage temperature parameter
		Clarified T_A parameter
	Pages 6, 7	DC Electrical parameters–changed working from open to disabled
09/11/01:	Page 2 - 4	Added date revision for pin configurations
	Page 6	Removed standard power offering for Industrial temp for 20ns from DC Electrical Characteristics
01/31/06:	Page 1	Added green availability to features
	Page 21	Added green indicator to ordering information
10/21/08:	Page 21	Removed "IDT" from orderable part number
08/12/14:	Page 21	Added Tape and Reel to Ordering Information
	Page 2, 3, 4 & 21	The package codes PN80-1, G68-1 & J68-1 changed to PN80, G68 & J68 respectively to match standard package codes
04/01/19:	Page 1	Updated Features by removing all speed grade offerings except the Commercial 15ns and Industrial 20ns and by removing all of the Military speed and temp range offerings
	Page 2	Removed "IDT's" from the fabrication reference in the Description text
		Additionally, updated the Description text by removing the ceramic 68-pin PGA package offering
	Page 2, 3 & 21	The package codes J68 & PN80 changed to PLG68 & PNG80 respectively to match standard package codes
	Page 17 & 18	Format updates to "Interrupts" heading and third paragraph in "How the Semaphore Flags Work"
	Page 21	Updated Ordering Information by removing all of the Military temp range offerings and removing the Industrial temp range except for the 20ns
		Additionally, removed the GU68 package offering from the ordering information
		Product Discontinuation Notice - PDN# SP-17-02
		Last time buy expires June 15, 2018
09/04/19:	Page 2 & 3	Rotated PLG68 PLCC and PNG80 TQFP pin configurations to accurately reflect pin 1 orientation
	Page 21	Added Orderable Part Information table