Crystal-to-HCSL 156.25MHz or 155.52MHz Clock Synthesizer

841S104I-02

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES AUGUST 14, 2016

DATA SHEET

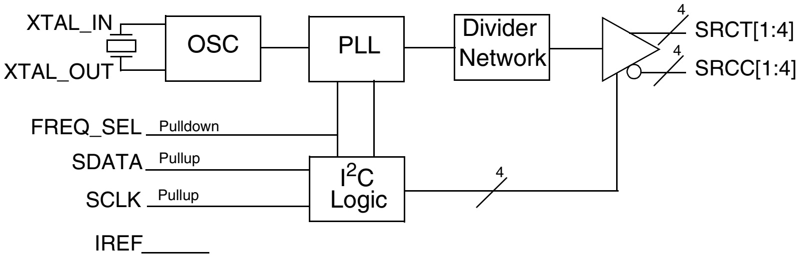
General Description

The 841S104I-02 is a PLL-based clock synthesizer specifically designed for Ethernet and SONET™ Clock applications. This device generates either a 156.25MHz or 155.52MHz differential HCSL clock from an input reference of either 25MHz or 19.44MHz. The input reference may be derived from an external source or by the addition of a 25MHz or a 19.44MHz crystal to the on-chip crystal oscillator. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating. An I^2C bus interface is used to enable or disable each individual clock output. The 841S104I-02 is available in a lead-free 24-Lead package.

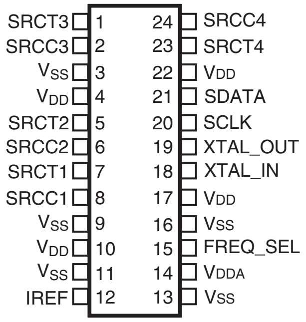
Features

- Four 0.7V current mode differential HCSL output pairs
- Crystal oscillator interface: 25MHz or 19.44MHz
- Output frequency: 156.25MHz or 155.52MHz
- RMS phase jitter @ 156.25MHz (12kHz – 20MHz): 0.691ps (typical)
- Cycle-to-cycle jitter: 25ps (maximum)
- I^2C support with readback capabilities up to 400kHz
- 3.3V operating supply mode
- -40°C to 85°C ambient operating temperature
- Available lead-free (RoHS 6) package
- **Use replacement part 8T49N241-dddNLGI**

Block Diagram



Pin Assignment



841S104I-02
24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	SRCT3, SRCC3	Output		Differential output pair. HCSL interface levels.
3, 9, 11, 13, 16	V_{SS}	Power		Power supply ground.
4, 10, 17, 22	V_{DD}	Power		Positive supply pins.
5, 6	SRCT2, SRCC2	Output		Differential output pair. HCSL interface levels.
7, 8	SRCT1, SRCC1	Output		Differential output pair. HCSL interface levels.
12	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode SRCCx, SRCTx clock outputs.
14	V_{DDA}	Power		Analog supply for PLL.
15	FREQ_SEL	Input	Pulldown	Selects output frequency and I^{2}C address (See Table 3).
18, 19	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
20	SCLK	Input	Pullup	I^{2}C compatible SCLK. This pin has an internal pullup resistor. LVCMOS/LVTTL interface levels.
21	SDATA	I/O	Pullup	I^{2}C compatible SDATA. This pin has an internal pullup resistor. Open drain. LVCMOS/LVTTL interface levels.
23, 24	SRCT4, SRCC4	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. FREQ_SEL

FREQ_SEL	Required Crystal (MHz)	Output Frequency Configuration	I^{2}C Address
0	25	156.25MHz	11010100 (D4h)
1	19.44	155.52MHz	11010110 (D6h)

NOTE: The slave receiver address is 11010100 (D4h) or 11010110 (D6h) based on the setting of the FREQ_SEL pin.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal I^2C serial interface is provided. Through the Serial Data Interface, various device functions, such as clock output buffers, can be individually enabled or disabled. The registers associated with the serial interface initialize to their default settings upon power-up, and therefore, use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 4A.

The block write and block read protocol is outlined in Table 4B, while Table 4C outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010100 (D4h) or 11010110 (D6h) based on the setting of the FREQ_SEL pin.

Table 4A.Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
6:5	Chip select address, set to “00” to access device
4:0	Byte offset for byte read or byte write operation. For block read or block write operations, these bits must be “00000”.

Table 4B. Block Read and Block Write Protocol

Bit	Description = Block Write	Bit	Description = Block Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 1 - 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 2 - 8 bits	30:37	Byte Count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
	Data Byte/Slave Acknowledges	39:46	Data Byte 1 from slave - 8 bits
	Data Byte N - 8 bits	47	Acknowledge
	Acknowledge from slave	48:55	Data Byte 2 from slave - 8 bits
	Stop	56	Acknowledge
			Data Bytes from Slave/Acknowledge
			Data Byte N from slave - 8 bits
			Not Acknowledge

Table 4C. Byte Read and Byte Write Protocol

Bit	Description = Byte Write	Bit	Description = Byte Read
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits	11:18	Command Code - 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data Byte- 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Registers

Table 4D. Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z) 1 = Enable
5	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z) 1 = Enable
4	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z) 1 = Enable
3	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z) 1 = Enable
2	1	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

NOTE: Pup denotes power-up.

Table 4E. Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 4F. Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	0	Reserved	Reserved

Table 4G. Byte 3:Control Register 3

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

NOTE: Pup denotes power-up.

Table 4H. Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	1	Reserved	Reserved

Table 4I. Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Table 4J. Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Hi-Z Select 0 = Hi-Z, 1 = REF/N
6	0	TEST_MODE	TEST Clock Mode Entry Control 0 = Normal Operation, 1 = REF/N or Hi-Z Mode
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	1	Reserved	Reserved

Table 4K. Byte 7: Control Register 7

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	1		Vendor ID Bit 0

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	77.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 5A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.21	3.3	V_{DD}	V
I_{DD}	Power Supply Current				71	mA
I_{DDA}	Analog Supply Current				21	mA

NOTE: The device has a power sequence requirement, refer to the *Applications Section.*

Table 5B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SDATA, SCLK	V_{DD} = V_{IN} = 3.465V			10	µA
		FREQ_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	SDATA, SCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		FREQ_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

Table 6. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			19.44 or 25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

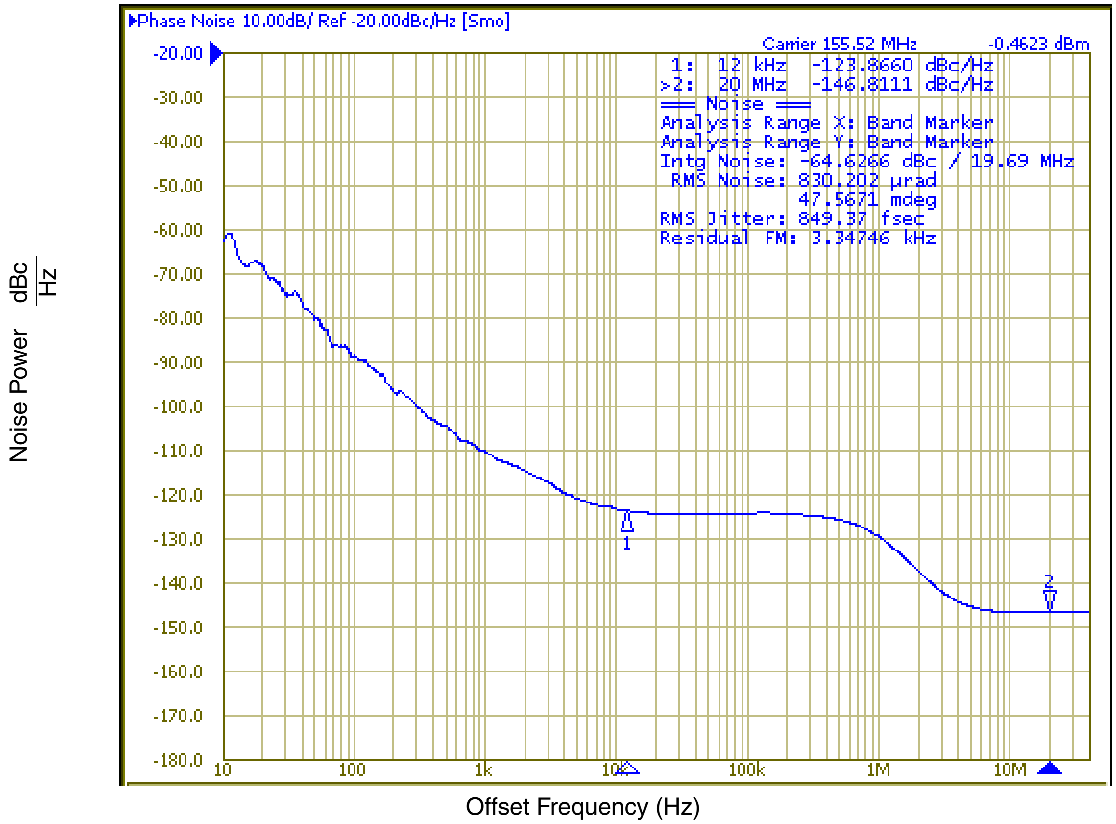
AC Electrical Characteristics

Table 7. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

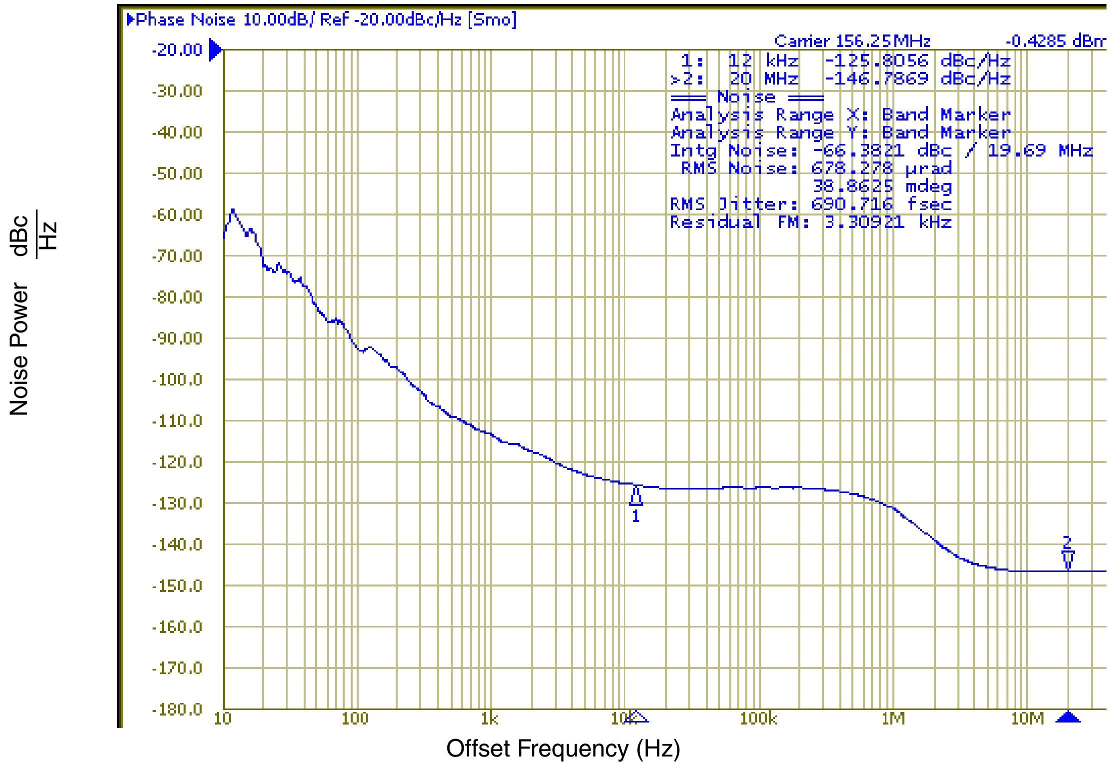
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using 25MHz Crystal		156.25		MHz
		Using 19.44MHz Crystal		155.52		MHz
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 1	19.44MHz crystal, *ƒ* = 155.52MHz, Integration Range: 12kHz – 20MHz		0.849		ps
		25MHz crystal, *ƒ* = 156.25MHz, Integration Range: 12kHz – 20MHz		0.691		ps
*t*sk(o)	Output Skew; NOTE 2, 3				30	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2	PLL Mode			25	ps
t_L	PLL Lock Time				100	ms
V_{RB}	Ring-back Voltage Margin; NOTE 4, 5		-100		100	mV
V_{MAX}	Voltage High; NOTE 6, 7				1150	mV
V_{MIN}	Voltage Low; NOTE 6, 8		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 6, 9, 10		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 6, 9, 11				150	mV
	Rise/Fall Edge Rate; NOTE 6, 12	Measured between 150mV to +150mV	0.6		4.0	V/ns
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using 19.44MHz and 25MHz crystals.
NOTE 1: Refer to phase jitter plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points.
NOTE 4: Measurement taken from differential waveform.
NOTE 5: T_{STABLE} is the time the differential clock must maintain a minimum ± 150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.
NOTE 6: Measurement taken from single-ended waveform.
NOTE 7: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 8: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of SRCT equals the falling edge of SRCC.
NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 11: Defined as the total variation of all crossing voltages of rising SRCT and falling SRCC, This is the maximum allowed variance in Vcross for any particular system.
NOTE 12: Measured from -150mV to +150mV on the differential waveform (SRCT minus SRCC). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

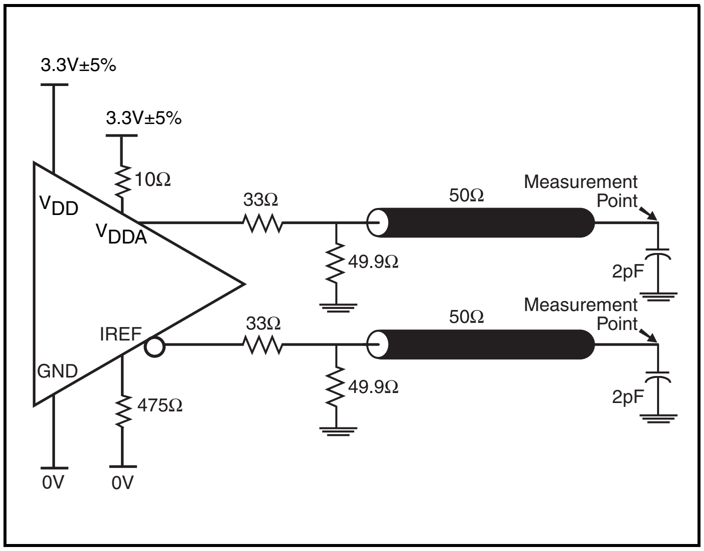
Typical Phase Noise at 155.52MHz



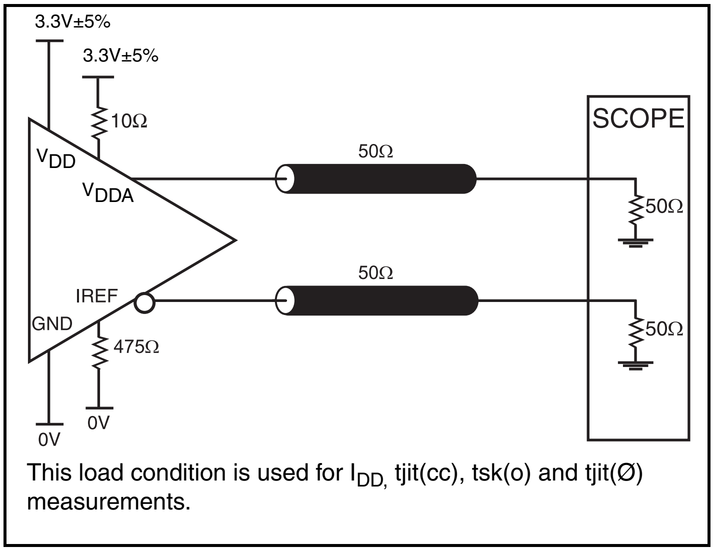
Typical Phase Noise at 156.25MHz



Parameter Measurement Information

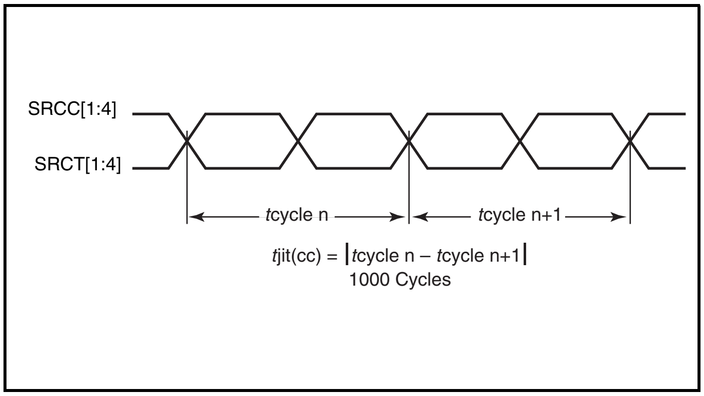


3.3V HCSL Output Load AC Test Circuit



This load condition is used for I_{DD}, tjit(cc), tsk(o) and tjit(Ø) measurements.

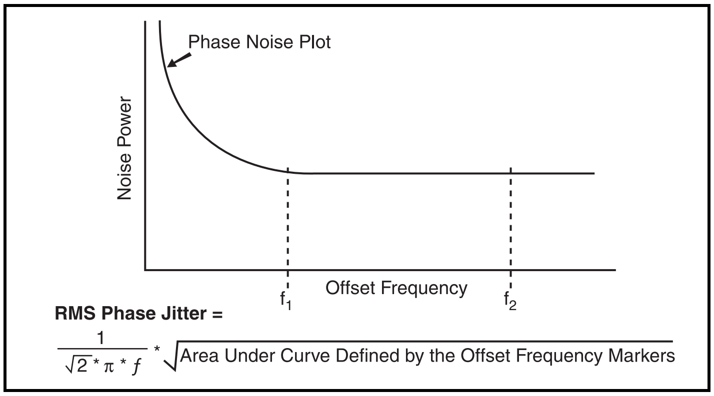
3.3V HCSL Output Load AC Test Circuit



$$t_{jit}(cc) = \left| t_{cycle\,n} - t_{cycle\,n+1} \right|$$

1000 Cycles

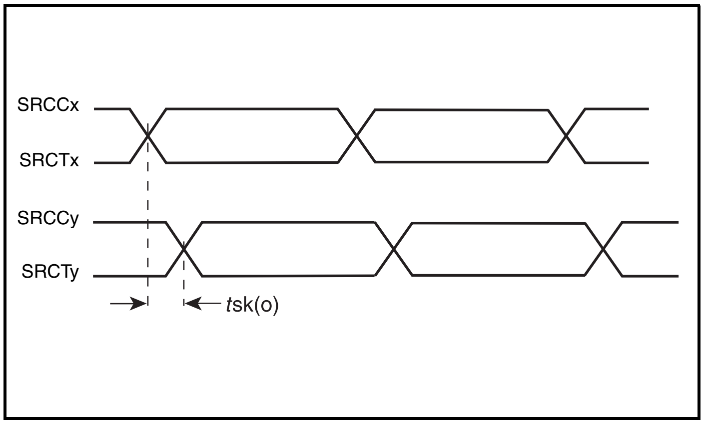
Cycle-to-Cycle Jitter



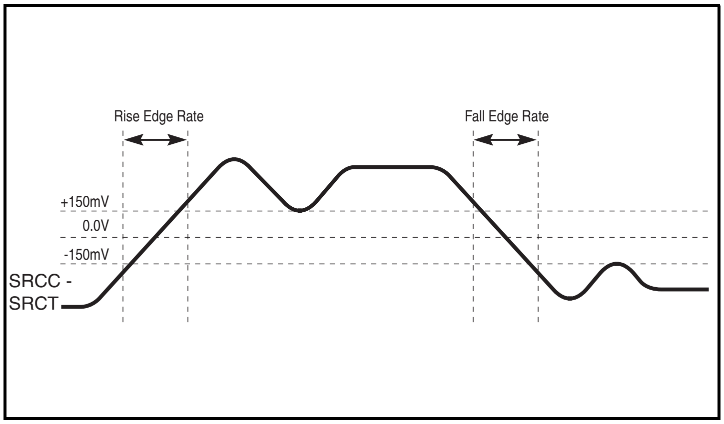
RMS Phase Jitter =

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

RMS Phase Jitter

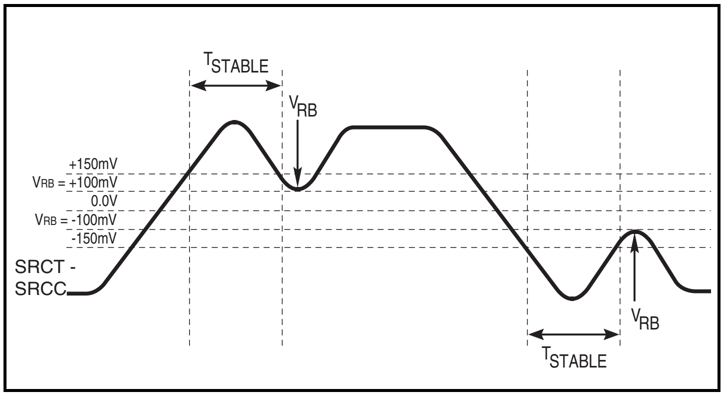


Output Skew

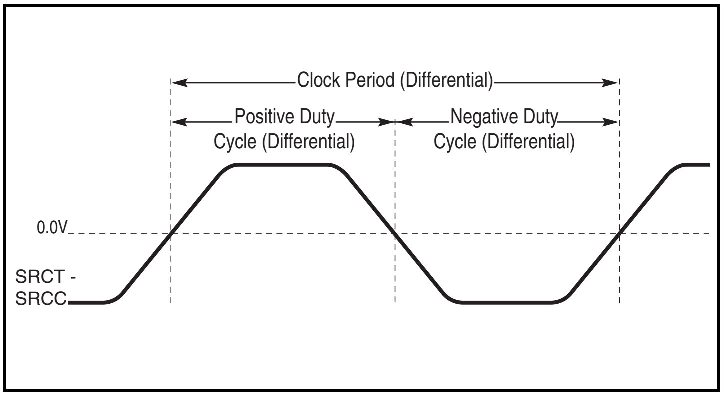


Differential Measurement Points for Rise/Fall Edge Rate

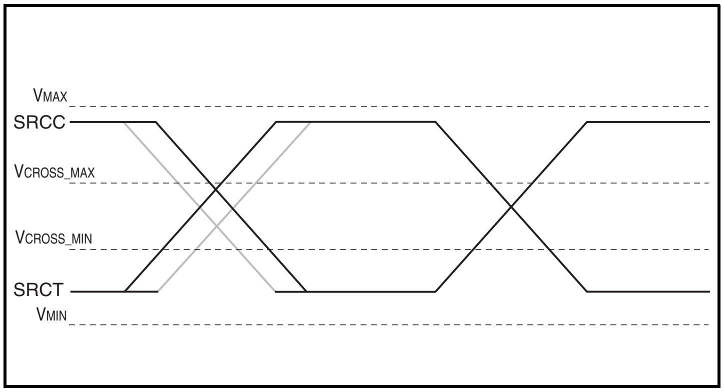
Parameter Measurement Information, continued



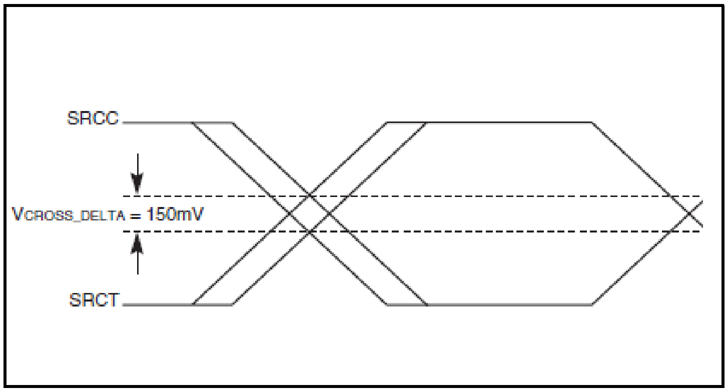
Differential Measurement Points for Ringback



Differential Measurement Points for Duty Cycle/Period



Single-ended Measurement Points for Absolute Cross Point and Swing



Single-ended Measurement Points for Delta Cross Point

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841S104I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

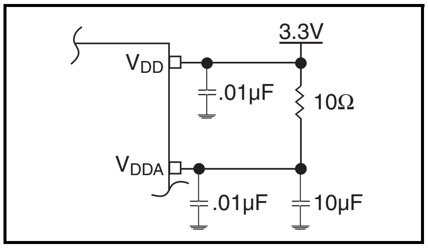


Figure 1. Power Supply Filtering

Power Supply Sequence Requirement

The 841S104I-02 has a power supply sequence requirement. This device requires that V_{DD} and V_{DDA} are powered simultaneously. This device has been characterized using the recommended power supply filtering techniques in *Figure 1.*

Power Sequence:

1. V_{DD} and V_{DDA}

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Crystal Input Interface

The 841S104I-02 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

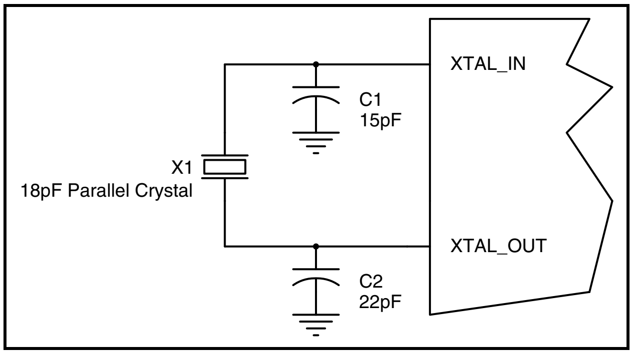


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

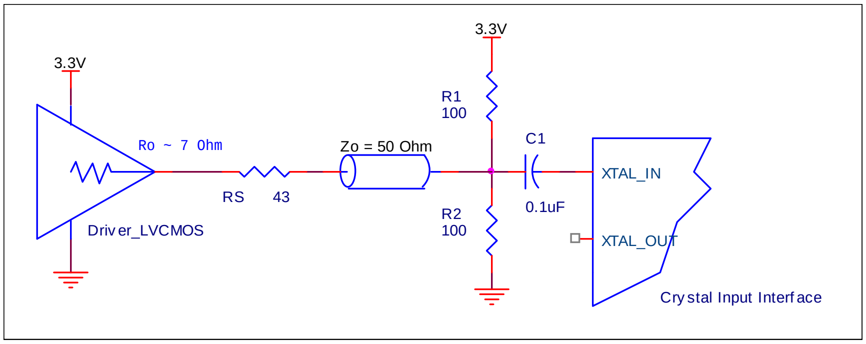


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

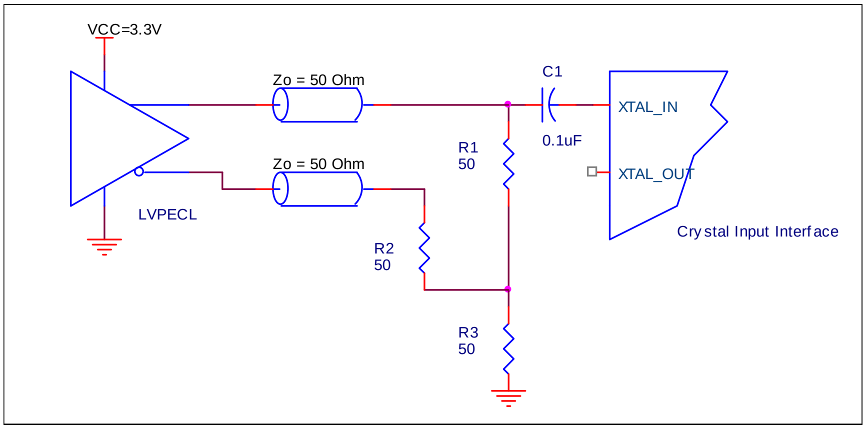


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommended Termination

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

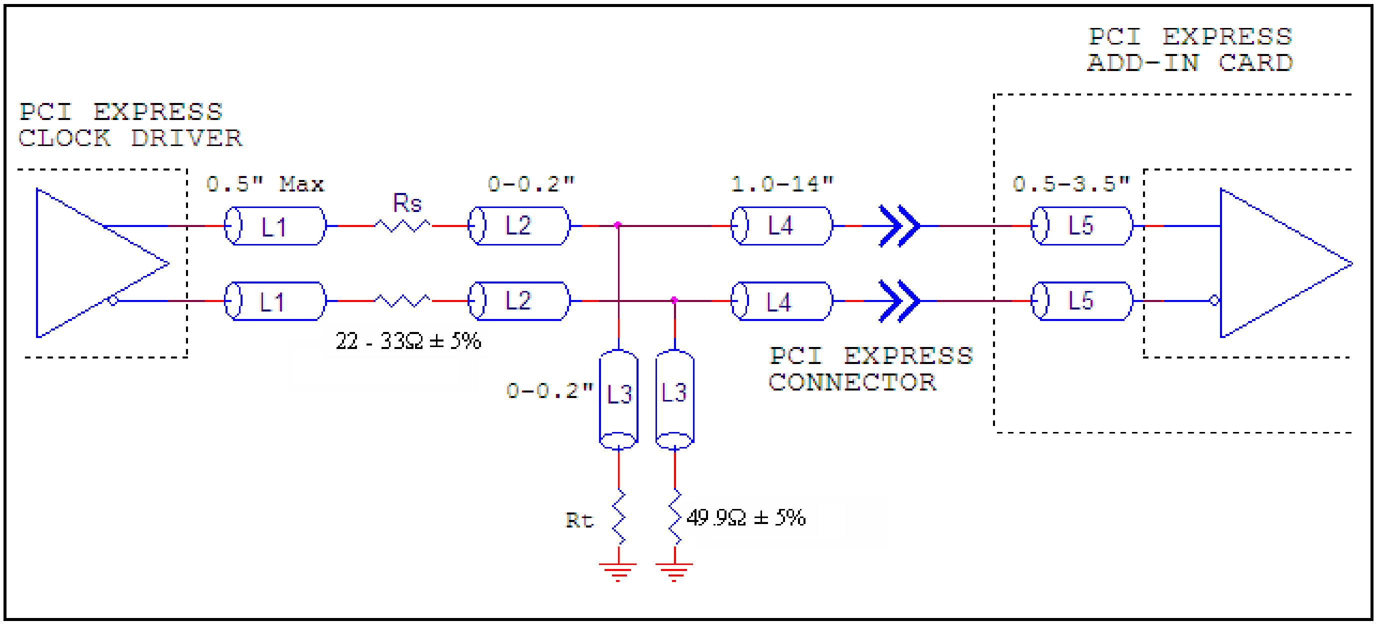


Figure 4A. Recommended Termination

Figure 4B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

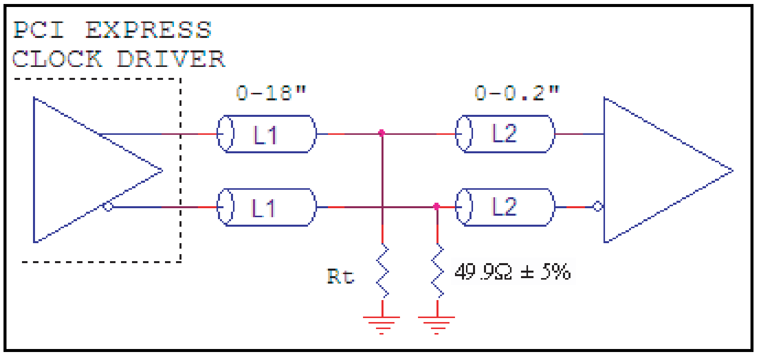


Figure 4B. Recommended Termination

Schematic Layout

Figure 5 shows an example of 841S104I-02 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 =18pF and C2 = 33pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of HCSL termination are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

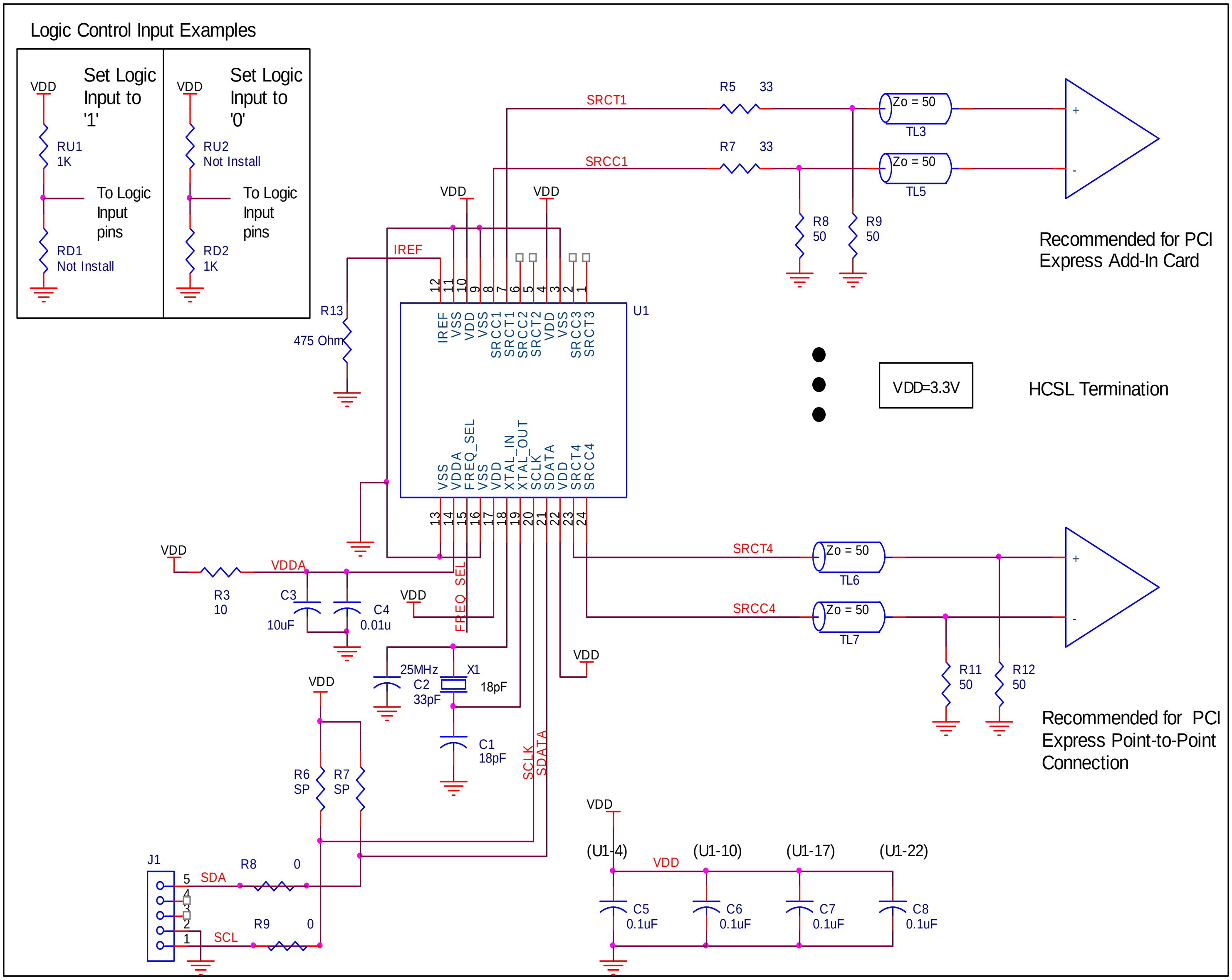


Figure 5. 841S104I-02 Application Schematic.

Power Considerations

This section provides information on power dissipation and junction temperature for the 841S104I-02.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 841S104I-02 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

The maximum current at 85°C is as follows:
I_{DD_MAX} = 65mA
I_{DDA_MAX} = 20mA

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V *(65mA + 20mA) = **294.525mW**
- Power $(outputs)_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 44.5mW = **178mW**

Total Power$_{\_MAX}$ = 294.525mW + 178mW = **472.525mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 77.5°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.473W * 77.5°C/W = 121.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.5°C/W	73.2°C/W	71.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

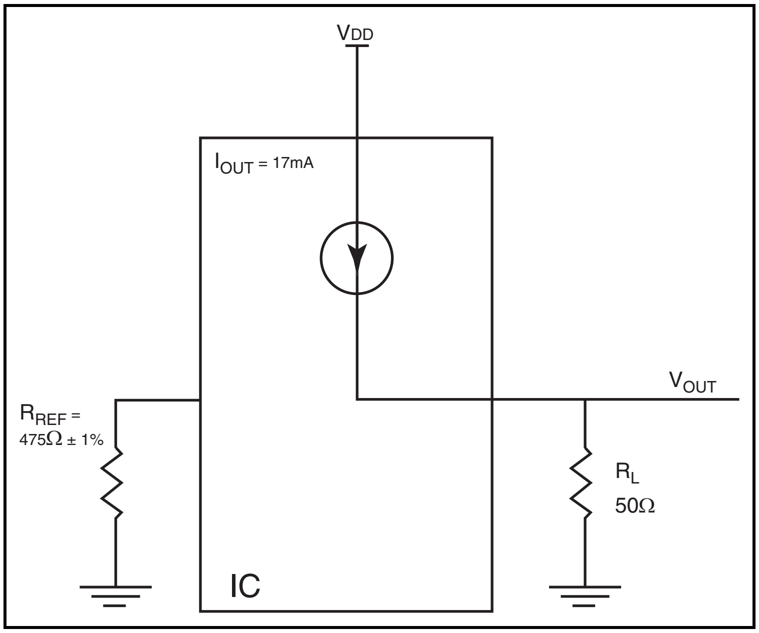


Figure 6. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD-MAX}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT},$

since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	77.5°C/W	73.2°C/W	71.0°C/W

Transistor Count

The transistor count for 841S104I-02 is: 11,360

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

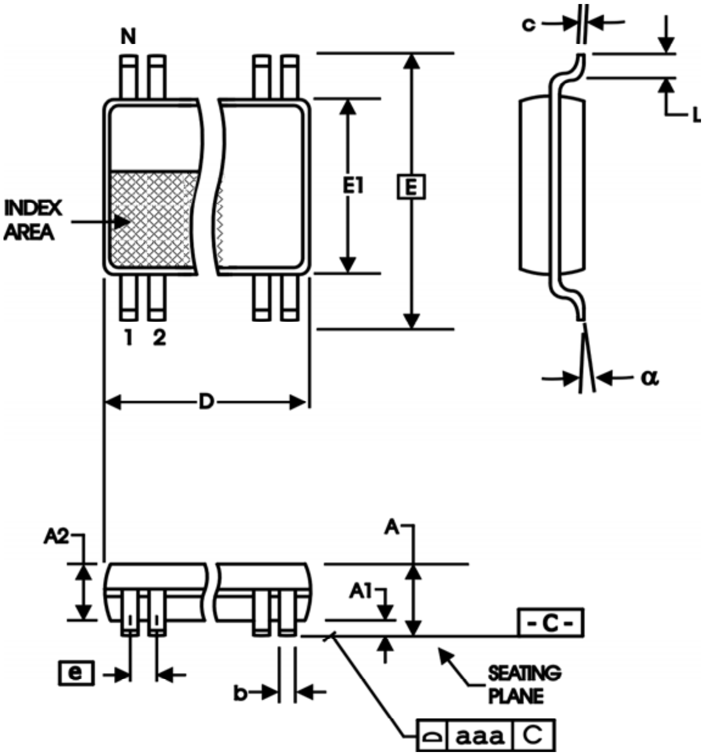


Table 10. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 11. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841S104BGI-02LF	ICS1S104BI02L	“Lead-Free” 24 Lead TSSOP	Tube	-40°C to 85°C
841S104BGI-02LFT	ICS1S104BI02L	“Lead-Free” 24 Lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			Product Discontinuation Notice - Last time buy expires August 14, 2016 PDN CQ-15-4	8/14/15

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