

## Description

The 8T49N282 has two independent, fractional-feedback PLLs that can be used as jitter attenuators and frequency translators. It is equipped with six integer and two fractional output dividers, allowing the generation of up to eight different output frequencies, ranging from 8kHz to 1GHz. Four of these frequencies are completely independent of each other and the inputs. The other four are related frequencies. The eight outputs may select among LVPECL, LVDS or LVCMOS output levels.

This functionality makes it ideal to be used in any frequency translation application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates. The device may also behave as a frequency synthesizer.

The 8T49N282 accepts up to four differential or single-ended input clocks and a crystal input. Each of the two internal PLLs can lock to different input clocks which may be of independent frequencies. The other two input clocks are intended for redundant backup of the primary clocks and must be related in frequency to their primary.

The device supports hitless reference switching between input clocks. The device monitors all input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The 8T49N282 supports holdover for each PLL. The holdover has an initial accuracy of  $\pm 50$ ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for each PLL that may be returned to in holdover at a limited phase slope.

The device places no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error.

Each PLL has a register-selectable loop bandwidth from 0.5Hz to 512Hz.

Each output supports individual phase delay settings to allow output-output alignment.

The device supports Output Enable inputs and Lock, Holdover and LOS status outputs.

The device is programmable through an I<sup>2</sup>C interface. It also supports I<sup>2</sup>C master capability to allow the register configuration to be read from an external EEPROM. The user may select whether the programming interface uses I<sup>2</sup>C protocols or SPI protocols, however in SPI mode, read from the external EEPROM is not supported.

## Typical Applications

- OTN or SONET / SDH equipment Line cards (up to OC-192, and supporting FEC ratios)
- OTN de-mapping (Gapped Clock and DCO mode)
- Gigabit and Terabit IP switches / routers including support of Synchronous Ethernet
- Wireless base station baseband
- Data communications

## Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- Two differential outputs meet jitter limits for 100G Ethernet and STM-256/OC-768
  - <0.3ps RMS (including spurs): 12kHz to 20MHz
- All outputs <0.5ps RMS (including spurs) 12kHz to 20MHz
- Operating modes: locked to input signal, holdover and free-run
- Initial holdover accuracy of  $\pm 50$ ppb
- Accepts up to four LVPECL, LVDS, LVHSTL, HCSL or LVCMOS input clocks
  - Accepts frequencies ranging from 8kHz up to 875MHz
  - Auto and manual input clock selection with hitless switching
  - Clock input monitoring, including support for gapped clocks
- Phase-Slope Limiting and Fully Hitless Switching options to control output phase transients
- Operates from a 10MHz to 40MHz fundamental-mode crystal
- Generates eight LVPECL / LVDS or 16 LVCMOS output clocks
  - Output frequencies ranging from 8kHz up to 1.0GHz (diff)
  - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
- Eight General Purpose I/O pins with optional support for status and control
  - Eight Output Enable control inputs
  - Lock, Holdover and Loss-of-Signal status outputs
- Open-drain Interrupt pin
- Write-protect pin to prevent configuration registers being altered
- Programmable PLL bandwidth settings for each PLL:
  - 0.5Hz, 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, 64Hz, 128Hz, 256Hz or 512Hz
  - Optional Fast Lock function
- Programmable output phase delays in steps as small as 16ps
- Register programmable through I<sup>2</sup>C / SPI or via external I<sup>2</sup>C EEPROM
- Bypass clock paths for system tests
- Power supply modes:
  - $V_{CC} / V_{CCA} / V_{CCO}$
  - 3.3V / 3.3V / 3.3V
  - 3.3V / 3.3V / 2.5V
  - 3.3V / 3.3V / 1.8V (LVCMOS)
  - 2.5V / 2.5V / 3.3V
  - 2.5V / 2.5V / 2.5V
  - 2.5V / 2.5V / 1.8V (LVCMOS)
- Power down modes support consumption as low as 1.7W (see [Power Dissipation and Thermal Considerations](#) section for details)
- -40°C to 85°C ambient operating temperature
- Package: 72QFN, lead-free RoHs (6)

### 8T49N282 Block Diagram

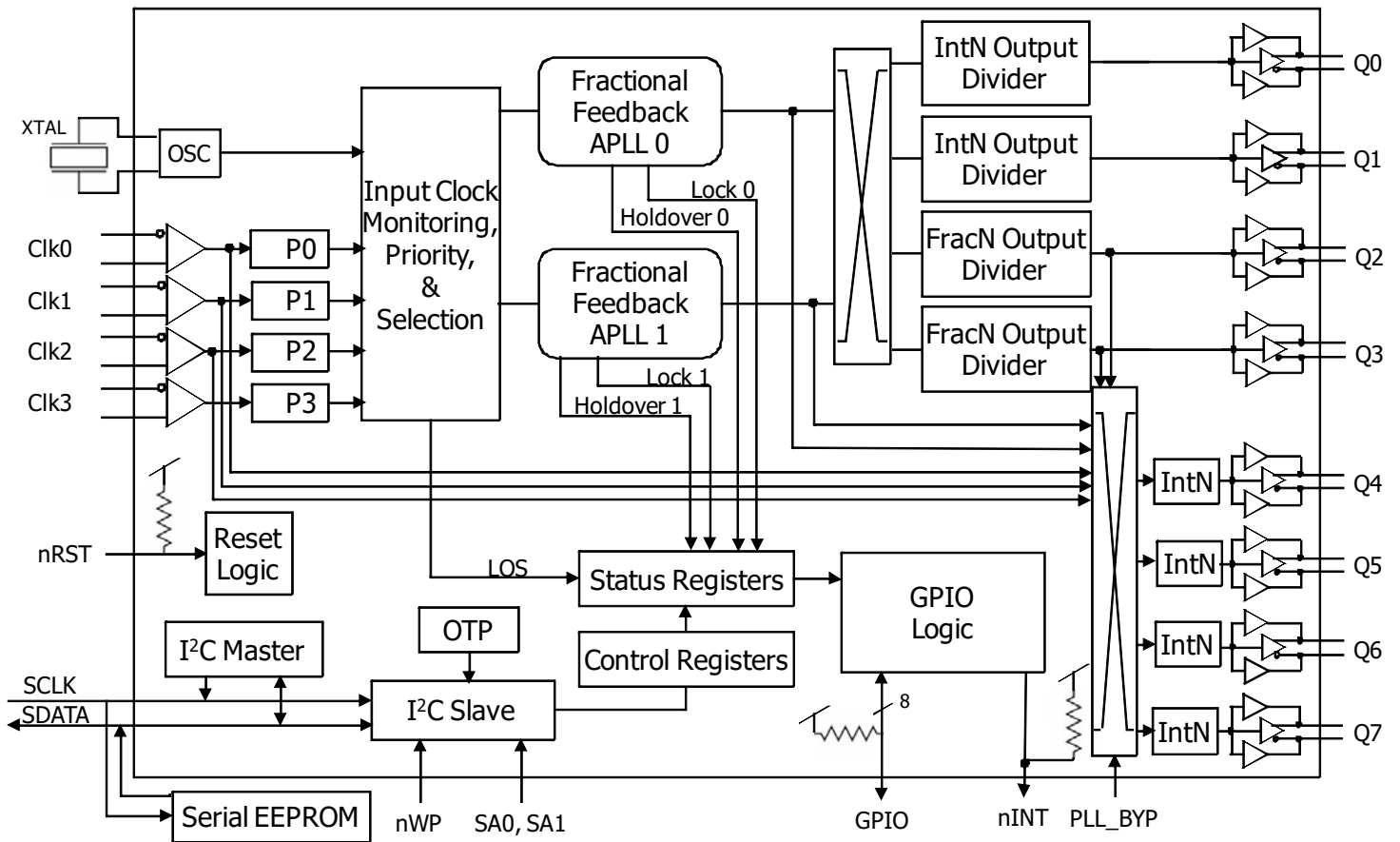


Figure 1. 8T49N282 Functional Block Diagram

## Pin Assignment

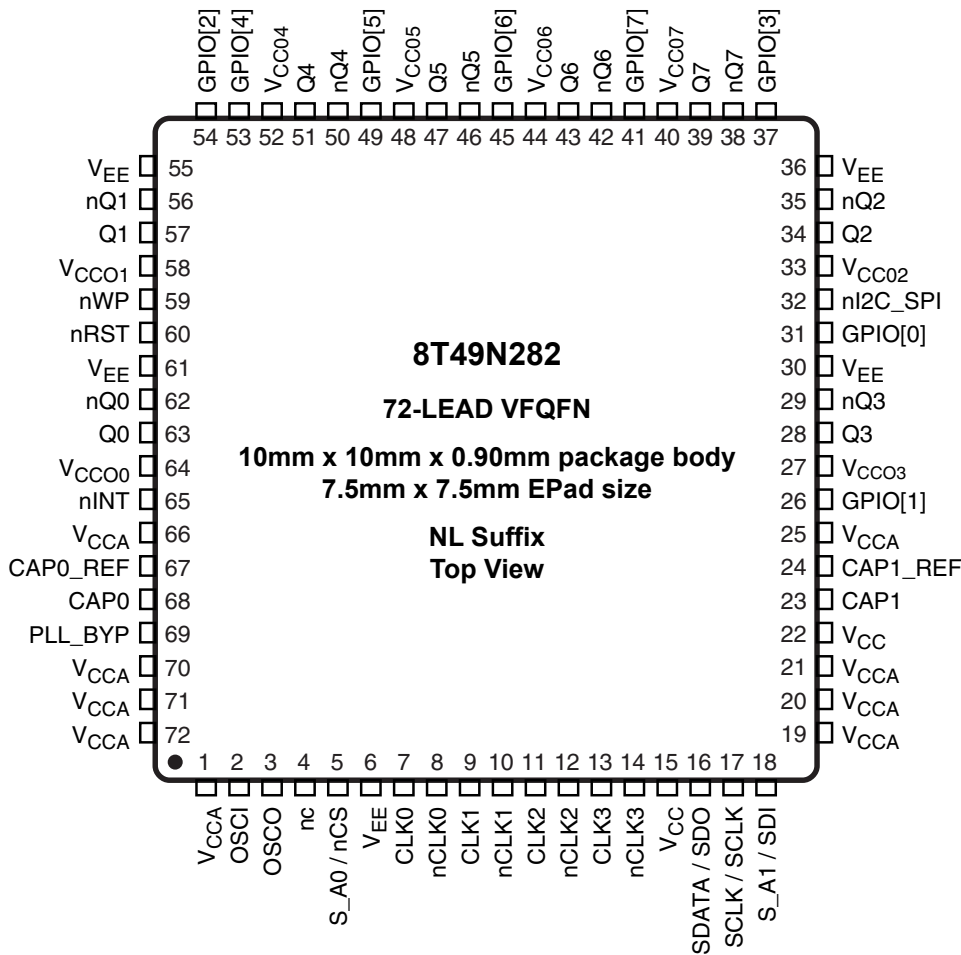


Figure 2. Pinout Drawing

## Pin Description and Pin Characteristic Tables

**Table 1. Pin Descriptions**

| Number                                  | Name        | Type |                           | Description  |
|---|-------------|------|---------------------------|--|
| 2                                       | OSCI        | I    |                           | Crystal Input. Accepts a 10MHz-40MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal. For proper device functionality, a crystal or external oscillator must be connected to this pin.     |
| 3                                       | OSCO        | O    |                           | Crystal Output. This pin must be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected.  |
| 5                                       | S_A0 / nCS  | I    | Pulldown                  | I <sup>2</sup> C lower address bit A0 / SPI interface chip select signal.  |
| 16                                      | SDATA / SDO | I/O  | Pullup                    | I <sup>2</sup> C interface bi-directional Data / SPI interface serial data output signal.  |
| 17                                      | SCLK / SCLK | I/O  | Pullup                    | I <sup>2</sup> C interface bi-directional Clock / SPI interface clock input signal.  |
| 18                                      | S_A1 / SDI  | I    | Pulldown                  | I <sup>2</sup> C lower address bit A1 / SPI interface serial data input signal.  |
| 32                                      | nI2C_SPI    | I    | Pulldown                  | Serial Interface Mode Selection. LVCMOS Input Levels:<br>0 = I <sup>2</sup> C Mode<br>1 = SPI Mode   |
| 7                                       | CLK0        | I    | Pulldown                  | Non-inverting differential clock input.  |
| 8                                       | nCLK0       | I    | Pullup/<br>Pulldown       | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)   |
| 9                                       | CLK1        | I    | Pulldown                  | Non-inverting differential clock input.  |
| 10                                      | nCLK1       | I    | Pullup/<br>Pulldown       | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)   |
| 11                                      | CLK2        | I    | Pulldown                  | Non-inverting differential clock input.  |
| 12                                      | nCLK2       | I    | Pullup/<br>Pulldown       | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)   |
| 13                                      | CLK3        | I    | Pulldown                  | Non-inverting differential clock input.  |
| 14                                      | nCLK3       | I    | Pullup/<br>Pulldown       | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.)   |
| 63, 62                                  | Q0, nQ0     | O    | Universal                 | Output Clock 0. Please refer to the Output Drivers section for more details.   |
| 57, 56                                  | Q1, nQ1     | O    | Universal                 | Output Clock 1. Please refer to the Output Drivers section for more details.   |
| 34, 35                                  | Q2, nQ2     | O    | Universal                 | Output Clock 2. Please refer to the Output Drivers section for more details.   |
| 28, 29                                  | Q3, nQ3     | O    | Universal                 | Output Clock 3. Please refer to the Output Drivers section for more details.   |
| 51, 50                                  | Q4, nQ4     | O    | Universal                 | Output Clock 4. Please refer to the Output Drivers section for more details.   |
| 47, 46                                  | Q5, nQ5     | O    | Universal                 | Output Clock 5. Please refer to the Output Drivers section for more details.   |
| 43, 42                                  | Q6, nQ6     | O    | Universal                 | Output Clock 6. Please refer to the Output Drivers section for more details.   |
| 39, 38                                  | Q7, nQ7     | O    | Universal                 | Output Clock 7. Please refer to the Output Drivers section for more details.   |
| 60                                      | nRST        | I    | Pullup                    | Master Reset input. LVTTTL / LVCMOS interface levels.<br>0 = All registers and state machines are reset to their default values<br>1 = Device runs normally  |
| 65                                      | nINT        | O    | Open-drain<br>with pullup | Interrupt output.  |
| 59                                      | nWP         | I    | Pullup                    | Write protect input. LVTTTL / LVCMOS interface levels:<br>0 = Write operations on the serial port will complete normally, but will have no effect except on interrupt registers<br>1 = Serial port writes may change any register. |
| 41, 45,<br>49, 53,<br>37, 54,<br>26, 31 | GPIO[7:0]   | I/O  | Pullup                    | General-purpose input-outputs. LVTTTL / LVCMOS Input levels Open-drain output. Pulled-up with 5.1k $\Omega$ resistor to $V_{CC}$ .   |

| Number                        | Name              | Type   |          | Description   |
|-------------------------------|-------------------|--------|----------|---|
| 69                            | PLL_BYP           | I      | Pulldown | Bypass Selection. Allow input references to bypass both PLLs. LVTTTL / LVCMOS interface levels.                             |
| 6, 30, 36,<br>55, 61,<br>ePAD | V <sub>EE</sub>   | Power  |          | Negative supply voltage. All V <sub>EE</sub> pins and EPAD must be connected before any positive supply voltage is applied. |
| 15                            | V <sub>CC</sub>   | Power  |          | Core and digital function supply voltage.   |
| 22                            | V <sub>CC</sub>   | Power  |          | Core and digital functions supply voltage.  |
| 1                             | V <sub>CCA</sub>  | Power  |          | Analog function supply voltage for core analog functions.   |
| 19, 20,<br>21, 25             | V <sub>CCA</sub>  | Power  |          | Analog function supply voltage for analog functions associated with PLL1.   |
| 66, 70,<br>71, 72             | V <sub>CCA</sub>  | Power  |          | Analog function supply voltage for analog functions associated with PLL0.   |
| 64                            | V <sub>CCO0</sub> | Power  |          | High-speed output supply voltage for output pair Q0, nQ0.   |
| 58                            | V <sub>CCO1</sub> | Power  |          | High-speed output supply voltage for output pair Q1, nQ1.   |
| 33                            | V <sub>CCO2</sub> | Power  |          | High-speed output supply voltage for output pair Q2, nQ2.   |
| 27                            | V <sub>CCO3</sub> | Power  |          | High-speed output supply voltage for output pair Q3, nQ3.   |
| 52                            | V <sub>CCO4</sub> | Power  |          | High-speed output supply voltage for output pair Q4, nQ4.   |
| 48                            | V <sub>CCO5</sub> | Power  |          | High-speed output supply voltage for output pair Q5, nQ5.   |
| 44                            | V <sub>CCO6</sub> | Power  |          | High-speed output supply voltage for output pair Q6, nQ6.   |
| 40                            | V <sub>CCO7</sub> | Power  |          | High-speed output supply voltage for output pair Q7, nQ7.   |
| 68,<br>67                     | CAP0,<br>CAP0_REF | Analog |          | PLL0 External Capacitance. A 0.1μF capacitance value across these pins is recommended.                                      |
| 23,<br>24                     | CAP1,<br>CAP1_REF | Analog |          | PLL1 External Capacitance. A 0.1μF capacitance value across these pins is recommended.                                      |
| 4                             | nc                | Unused |          | No connect.   |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

**Table 2. Pin Characteristics,  $V_{CC} = V_{CCOX} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$** 

| Symbol         | Parameter                                       | Test Conditions                     | Minimum                         | Typical | Maximum | Units      |
|----------------|---|-------------------------------------|---------------------------------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance; <b>NOTE 1</b>                |                                     |                                 | 3.5     |         | pF         |
| $R_{PULLUP}$   | Internal Pullup Resistor                        | nRST, nWP, SDATA / SDO, SCLK / SCLK |                                 | 51      |         | k $\Omega$ |
|                |   | nINT                                |                                 | 50      |         | k $\Omega$ |
|                |   | GPIO[7:0]                           |                                 | 5.1     |         | k $\Omega$ |
| $R_{PULLDOWN}$ | Internal Pulldown Resistor                      |                                     |                                 | 51      |         | k $\Omega$ |
| $C_{PD}$       | Power Dissipation Capacitance (per output pair) | LVC MOS Q[0:1], Q[4:7]              | $V_{CCOX} = 3.465V$             | 14.5    |         | pF         |
|                |   | LVC MOS Q[2:3]                      | $V_{CCOX} = 3.465V$             | 18.5    |         | pF         |
|                |   | LVC MOS Q[0:1], Q[4:7]              | $V_{CCOX} = 2.625V$             | 13      |         | pF         |
|                |   | LVC MOS Q[2:3]                      | $V_{CCOX} = 2.625V$             | 17.5    |         | pF         |
|                |   | LVC MOS Q[0:1], Q[4:7]              | $V_{CCOX} = 1.89V$              | 12.5    |         | pF         |
|                |   | LVC MOS Q[2:3]                      | $V_{CCOX} = 1.89V$              | 17      |         | pF         |
|                |   | LVDS or LVPECL Q[0:1], Q[4:7]       | $V_{CCOX} = 3.465V$ or $2.625V$ | 2       |         | pF         |
|                |   | LVDS or LVPECL Q[2:3]               | $V_{CCOX} = 3.465V$ or $2.625V$ | 4.5     |         | pF         |
| $R_{OUT}$      | Output Impedance                                | GPIO[7:0]                           | Output HIGH                     |         | 5.1     | k $\Omega$ |
|                |   |                                     | Output LOW                      |         | 25      | $\Omega$   |
|                |   | LVC MOS Q[7:0], nQ[7:0]             |                                 | 20      |         | $\Omega$   |

NOTE:  $V_{CCOX}$  denotes:  $V_{CCO0}$  through  $V_{CCO7}$ .

NOTE 1: This specification does not apply to OSC1 and OSC0 pins.

## Principles of Operation

The 8T49N282 has two PLLs that can each independently be locked to any of the input clocks and generate a wide range of synchronized output clocks.

It incorporates two completely independent PLLs. These could be used for example in the transmit and receive path of Synchronous Ethernet equipment. Any of the input clocks can be selected as the reference for either PLL. From the output of the two PLLs a wide range of output frequencies can be simultaneously generated.

The 8T49N282 accepts up to four differential input clocks ranging from 8kHz up to 875MHz. It generates up to eight output clocks ranging from 8kHz up to 1.0GHz.

Each PLL path within the 8T49N282 supports three states: Lock, Holdover and Free-run. Lock & holdover status may be monitored on register bits and pins. Each PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. Each of the PLL paths within the 8T49N282 has an initial holdover frequency offset of  $\pm 50$ ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, each PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N282 continuously monitors each input for activity (signal transitions).

In automatic reference switching, when an input clock has been validated the PLL will transition to the locked state. If the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the 8T49N282 will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive.

The device supports conversion of any input frequency to four different, independent output frequencies on the Q[0:3] outputs. Additionally, a further four output frequencies may be generated that are integer-related to the four independent frequencies. These additional four frequencies are on the Q[4:7] outputs.

The 8T49N282 has a programmable loop bandwidth from 0.5Hz to 512Hz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device supports programmable individual output phase adjustments in order to allow control of input to output phase adjustments and output to output phase alignment.

The device is programmable through an I<sup>2</sup>C or SPI interface and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I<sup>2</sup>C EEPROM.

## Bypass Path

For system test purposes, each of PLL0 and PLL1 may be bypassed. When PLL\_BYP is asserted the CLK0 input reference will be presented to the Q4 dividers. The CLK1 input reference will be presented to the Q5 dividers.

Additionally, CLK0, CLK1 or CLK2 may be used as a clock source for the output dividers of Q[4:7]. This may only be done for input frequencies of 250MHz or less.

## Input Clock Selection

The 8T49N282 accepts up to four input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels. To use LVCMOS inputs, please refer to the Application Note, *Wiring the Differential Input to Accept Single-ended Levels* for biasing instructions.

The device has independent input clock selection control for each PLL. In Manual mode, only one of these inputs may be chosen per PLL and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIOs must be used as Clock Select inputs (CSELn[1:0]) for PLLn.

| <u>CSELn[1]</u> | <u>CSELn[0]</u> | <u>Selected Input Reference</u> |
|-----------------|-----------------|---------------------------------|
| 0               | 0               | CLK0                            |
| 0               | 1               | CLK1                            |
| 1               | 0               | CLK2                            |
| 1               | 1               | CLK3                            |

In addition, the crystal frequency may be passed directly to the output dividers for Q[4:7] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of  $\pm 100$ ppm or better.

If the PLL is working in automatic mode, then each of the input reference sources is assigned a priority of 1-4. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see [Input Clock Monitor](#) section for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control registers. It is recommended that all input references for a PLL be given different priority settings in the Clock Input Priority control registers for that PLL.



## Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of PLL0's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL(s) tracking this input will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL(s) will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and will be validated by the receipt of 8 rising clock edges on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation time starts over.

Each LOS flag may also be reflected on one of the GPIO[7:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

## Holdover

8T49N282 supports a small initial holdover frequency offset for each PLL path in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for at least 2 LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The 8T49N282 can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When a PLL loses all valid input references, it will enter the holdover state. In fast average mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings. This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the  $V_{CO}$  band
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in the AC Table.
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3dB attenuation point corresponding to a nominal period of 20 minutes. The accuracy is shown in the AC Table.

When entering holdover, each PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While a PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks derived from that PLL will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) derived from that PLL will have drifted outside of the limits of the holdover state and the system will be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the 8T49N282 cannot know or influence when that transition occurs. As a result, the 8T49N282 will remain in the holdover state internally.



## Input to Output Clock Frequency

The 8T49N282 is designed to accept any frequency within its input range and generate eight different output frequencies that are independent from the input frequencies. The internal architecture of the device ensures that most translations will result in the exact output frequency specified. Where exact frequency translation is not possible, the frequency translation error will be minimized. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

### Synthesizer Mode Operation

The device may also act as a frequency synthesizer with either or both PLL's generating their operating frequency from just the crystal input. By setting the SYN\_MODEn register bit and setting the STATEn[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

### Loop Filter and Bandwidth

When operating in Synthesizer Mode as described above, the 8T49N282 has a fixed loop bandwidth of approximately 200kHz. When operating in all other modes, the following information applies:

The 8T49N282 uses no external components to support a range of loop bandwidths: 0.5Hz, 1Hz, 2Hz, 4Hz, 8Hz, 16Hz, 32Hz, 64Hz, 128Hz, 256Hz or 512Hz. Each PLL shall support separate loop filter settings.

The device supports three different loop bandwidth settings for each PLL: acquisition, locked and tight-locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to 'fast-lock'. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times. The tight-locked setting may be used to lower phase noise in situations where the input reference only varies within a very narrow, register-programmed range.

### Output Dividers and Mapping to PLLs

Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in Table 3.

In addition, the first divider stage for the Q[4:7] outputs supports a bypass (i.e. divide-by-1) operation for some clock sources.

**Table 3. Q0, Q1, Q[4:7] Output Divide Ratios**

| 1st-Stage Divide | 2nd-Stage Divide | Total Divide | Minimum F <sub>OUT</sub> MHz | Maximum F <sub>OUT</sub> MHz |
|------------------|------------------|--------------|------------------------------|------------------------------|
| 4                | 1                | 4            | 750                          | 1000                         |
| 5                | 1                | 5            | 600                          | 800                          |
| 6                | 1                | 6            | 500                          | 666.7                        |
| 4                | 2                | 8            | 375                          | 500                          |
| 5                | 2                | 10           | 300                          | 400                          |
| 6                | 2                | 12           | 250                          | 333.3                        |
| 4                | 4                | 16           | 187.5                        | 250                          |
| 5                | 4                | 20           | 150                          | 200                          |
| 6                | 4                | 24           | 125                          | 166.7                        |
| ...              |                  |              |                              |                              |
| 4                | 131,070          | 524,280      | 0.0057                       | 0.0076                       |
| 5                | 131,070          | 655,350      | 0.0046                       | 0.0061                       |
| 6                | 131,070          | 786,420      | 0.0038                       | 0.0051                       |

NOTE: Above frequency ranges for Q[4:7] apply when driven directly from PLL0 or PLL1.

### Fractional Output Divider Programming (Q2, Q3 only)

For the FracN output dividers Q2-Q3, the output divide ratio is given by:

$$\text{Output Divide Ratio} = (N.F) \times 2$$

$$N = \text{Integer Part: } 4, 5, \dots, (2^{18}-1)$$

$$F = \text{Fractional Part: } [0, 1, 2, \dots, (2^{28}-1)] / (2^{28})$$

For integer operation of these outputs dividers, N = 3 is also supported.

### Output Divider Frequency Sources

Output dividers associated with the Q[0:3] outputs can take their input frequencies from either PLL0 or PLL1.

Output dividers associated with the Q[4:7] outputs can take their input frequencies from PLL0, PLL1, Q2 or Q3 output dividers, the CLK0, CLK1 or CLK2 input reference frequencies or the crystal frequency.

### Output Banks

Outputs of the 8T49N282 are divided into three banks for purposes of output skew measurement.

- Q0, nQ0, Q1, nQ1
- Q4, nQ4, Q5, nQ5
- Q6, nQ6, Q7, nQ7

## Output Phase Control on Switchover

There are two options on how the output phase can be controlled when the 8T49N282 enters or leaves the holdover state, or either PLL switches between input references. Phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODEn bit selects which behavior is to be followed for PLLn.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used. Fully hitless switching should not be used unless all input references are in the same clock domain. Note that use of this mode may prevent an output frequency and phase from being able to trace its alignment back to a primary reference source.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEWn[1:0] bits. Phase-slope limiting should be used if all input references are not in the same clock domain or users wish to retain traceability to a primary reference source.

## Output Phase Alignment

The device has a programmable output to output phase alignment for each of the eight output dividers. After power-up and the PLLs have achieved lock, the device will be in a state where the outputs are synchronized with a deterministic offset relative to each other. After synchronization, the output alignment will depend on the particular configuration of each output according to the following rules. The step size is defined as the period of the clock to that divider:

- 1) Only outputs derived from the same source will be aligned with each other. 'Source' means the reference selected to drive the output divider as controlled by the CLK\_SELn bit for each output.
- 2) For integer dividers (Q0, Q1, Q[4:-7]) when both divider stages are active, edges are aligned. This case is used as a baseline to compare the other cases here.
- 3) For integer dividers where the 1st-stage divider is bypassed (only Q[4:-7] support this), coarse delay adjustments can't be performed. The output phase will be one step earlier than in Case 2.
- 4) Fractional output dividers (Q2 or Q3) do not guarantee any specific phase on power-up or after a synchronization event
- 5) Integer dividers using Q2 or Q3 as a source (Q[4:-7] support this option) will be aligned to their source divider's output (Q2 or Q3).
- 6) Phase alignments listed above may differ by the output-output skews in the AC Table.

Once the device is in operation, the outputs associated with each PLL may have their phase adjustments re-synced in one of two ways:

- 1) If the PLL becomes unlocked, the coarse phase adjustments will be reset and the fine phase adjustments will be re-loaded once it becomes locked again.
- 2) Toggling of PLLn\_SYN bit may also be used to force a re-sync / re-load for outputs associated with that PLL.

The user may apply adjustments that are proportional to the period of the clock source driving each output divider. For example, if the divider associated with Output Q3 is running off PLL0, which has a VCO frequency of 4GHz, then the appropriate period would be 250ps. The output phase may be adjusted in these steps across the full period of the output.

- Coarse Adjustment: all Output Dividers may have their phase adjusted in steps of the source clock period. For example a 4GHz VCO gives a step size of 250ps. The user may request an adjustment of phase of up to 31 steps using a single register write. The phase will be adjusted by lengthening the period of the output by 250ps at a time. This process will be repeated every 4 output clock periods until the full requested adjustment has been achieved. A busy signal will remain asserted in the phase delay register until the requested adjustment is complete. Then a further adjustment may be setup and triggered by toggling the trigger bit.
- Fine Adjustment: For the Fractional Output Dividers associated with the Q2 and Q3 outputs, the phase of those outputs may be further adjusted with a granularity of 1/16th of the VCO period. For example a 4GHz VCO frequency gives a granularity of 16ps. This is performed by directly writing the required offset (from the nominal rising edge position) in units of 1/16<sup>th</sup> of the output period into a register. Then the appropriate PLLn\_SYN bit must be toggled to load the new value. Note that toggling this bit will clear all Coarse Delays for all outputs associated with that PLL, so Fine Delays should be set first, before Coarse Delays. The output will then jump directly to that new offset value. For this reason, this adjustment should be made as the output is initially programmed or in high-impedance.

Each output has the capability of being inverted (180 degree phase shift).

## Jitter and Wander Tolerance

The 8T49N282 can be used as a line card device and therefore is expected to tolerate the jitter and wander output of a timing card PLL (e.g 82V3390).

## Output Drivers

The Q0 to Q7 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin ( $V_{CCO}$ ) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V  $V_{CCO}$ .

Each output may be enabled or disabled by register bits and/or GPIO pins configured as Output Enables. The outputs will be enabled if the register bit and the associated OE pin are both asserted (high). When disabled an output will be in a high impedance state.

## LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q and nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Phase-aligned outputs will have increased simultaneous switching currents which can negatively affect phase noise performance and power consumption. It is recommended that use of this selection be kept to a minimum.

## Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions are included under register control:

- PLL1 may be shut down.
- Any unused output, including all output divider and phase adjustment logic, can be individually powered-off.
- Clock gating on logic that is not being used.

## Status / Control Signals and Interrupts

### General-Purpose I/Os & Interrupts

The 8T49N282 provides eight General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in [Table 4](#). Note that the default state prior to configuration being loaded from internal OTP or external EEPROM will be to set each GPIO to function as an Output Enable. If used in the Fixed Function mode of operation, the GPIO bits will reflect the

real-time status of their respective status bits as shown in [Table 4](#). Note that the LOL signal represents the lock status of the PLL. It does not account for the process of synchronization of the output dividers associated with that PLL. The output dividers programmed to operate from that PLL will automatically go through a re-synchronization process when the PLL locks or re-locks or if the user triggers a re-sync manually via register bit PLLn\_SYN. This synchronization process may result in a period of instability on the affected outputs for a duration of up to 350ns after the re-lock (LOL de-asserts) or the PLLn\_SYN bit is de-asserted.

### Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock Status (LOL[1:0]), PLL Holdover Status (HOLD[1:0]) and Input Reference Status (LOS[3:0]) that is set whenever there is an alarm on any of those signals. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status flag and nINT output pin are asserted if any of the enabled Interrupt Status flags are set.

**Table 4. GPIO Configuration<sup>1</sup>**

| GPIO Pin | Configured as Input     |              |                 | Configured as Output |                 |
|----------|-------------------------|--------------|-----------------|----------------------|-----------------|
|          | Fixed Function          |              | General Purpose | Fixed Function       | General Purpose |
|          | Output Enable (default) | Clock Select |                 |                      |                 |
| 7        | OE[7]                   | CSEL1[1]     | GPI[7]          | LOS[3]               | GPO[7]          |
| 6        | OE[6]                   | CSEL0[1]     | GPI[6]          | LOS[2]               | GPO[6]          |
| 5        | OE[5]                   | -            | GPI[5]          | LOS[1]               | GPO[5]          |
| 4        | OE[4]                   | -            | GPI[4]          | HOLD[1]              | GPO[4]          |
| 3        | OE[3]                   | CSEL1[0]     | GPI[3]          | LOL[1]               | GPO[3]          |
| 2        | OE[2]                   | CSEL0[0]     | GPI[2]          | LOS[0]               | GPO[2]          |
| 1        | OE[1]                   | -            | GPI[1]          | HOLD[0]              | GPO[1]          |
| 0        | OE[0]                   | -            | GPI[0]          | LOL[0]               | GPO[0]          |

NOTE 1. **OE[x]**: Output Enable Control for output Qx, nQx. Logic-high enables the output pair.

**GPI[x]**: General Purpose Input. Logic state on GPIO[x] pin is directly reflected in GPI[x] register.

**LOS[x]**: Loss-of-Signal Status Flag for Input Reference x. Logic-high indicates input reference failure.

**GPO[x]**: General Purpose Output. Logic state is determined by value written in register GPO[x].

**CSELn[1:0]**: Manual Clock Select Input for PLLn. Refer to [Input Clock Selection](#).

**HOLD[n]**: Holdover Status Flag for Digital PLLn. Logic-high indicates digital PLLn in holdover status.

**LOL[n]**: Loss-of-Lock Status Flag for Digital PLLn. Logic-high indicates digital PLL not locked.

Refer to [Register Descriptions](#) for additional details.

## Device Hardware Configuration

The 8T49N282 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with one complete device configuration. If the device is set to read a configuration from an external, serial EEPROM, then the values read will overwrite the OTP-defined values.

This configuration can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

## Device Start-up & Reset Behavior

The 8T49N282 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it's common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input pin.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as OE[7:0] inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the latter of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N282 will check the register settings to see if it should load the remainder of its configuration from an external I<sup>2</sup>C EEPROM at a defined address or continue loading from OTP. See [I<sup>2</sup>C Boot-up Initialization Mode](#) for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock both PLLs to the selected sources and begin operation. Once the PLLs are locked, all the outputs derived from a given PLL will be synchronized and output phase adjustments can then be applied if desired.

## Serial Control Port Description

### Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I<sup>2</sup>C or SPI compatible configuration, to allow access to any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details. Selection of I<sup>2</sup>C versus SPI protocol will be done via an input pin.

The device has the additional capability of becoming a master on the I<sup>2</sup>C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I<sup>2</sup>C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I<sup>2</sup>C bus or pre-programmed into the device prior to assembly. This capability is unavailable if SPI protocols are selected for the programming interface.

### SPI Mode Operation

In a read operation (R/W bit is '1') data on SDO will be clocked out on the falling edge of SCLK.

In a write operation (R/W bit is '0'), data on SDI will be clocked in on the rising edge of SCLK.

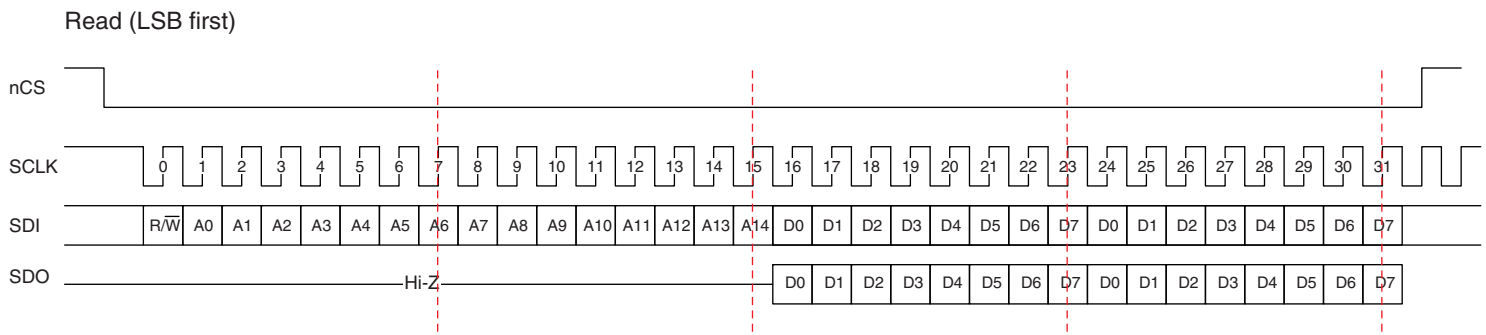
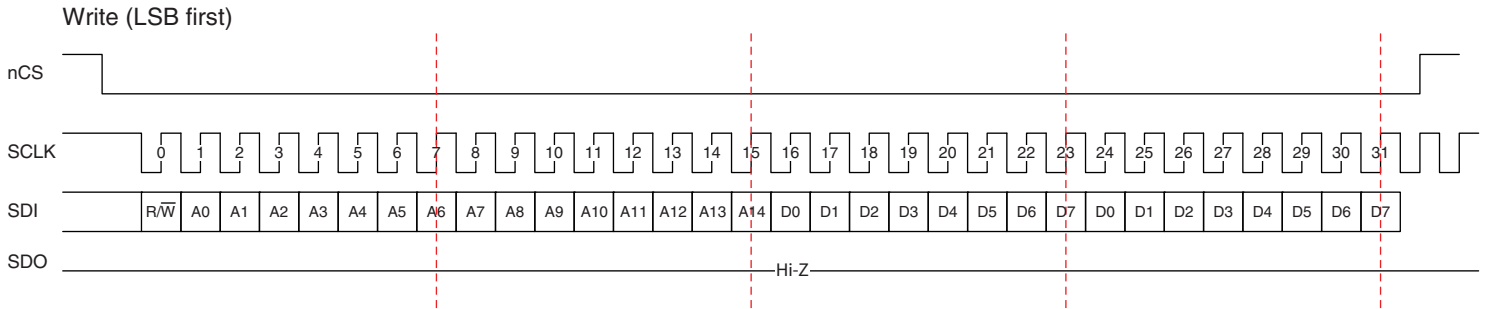


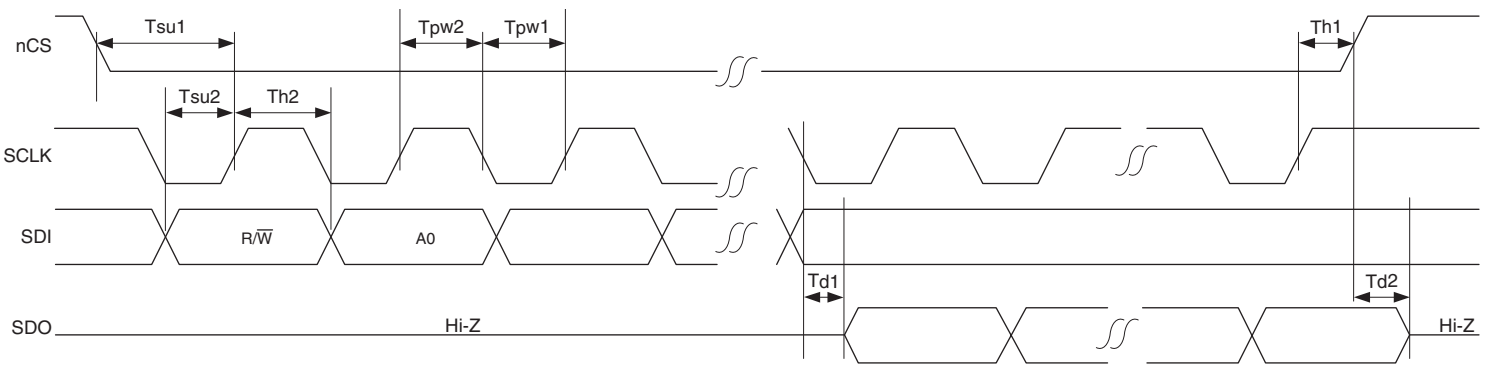
Figure 3. SPI Read Sequencing Diagram

During SPI Write operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 32,767 bytes in a

single block write. Once nCS is driven high, then all data will be written into sequential registers starting at the address given.



**Figure 4. SPI Write Sequencing Diagram**



**Figure 5. SPI Read/Write Timing Diagram**

**Table 5. Timing Characteristics in SPI Mode**

| Symbol    | Parameter   | Min                  | Typ | Max    | Unit |
|-----------|---|----------------------|-----|--------|------|
| T         | Internal timing parameter used to calculate SPI timing specs                                    | T = PLL0 period * 64 |     |        | ns   |
| $t_{su1}$ | Valid nCS to SCLK rising setup time   | 2T                   |     |        | ns   |
| $t_{su2}$ | Valid SDI to SCLK rising setup time   | 5                    |     |        | ns   |
| $t_{d1}$  | SCLK falling to valid data delay time   |                      |     | 4T + 5 | ns   |
| $t_{d2}$  | nCS rising edge to SDO high impedance delay time  |                      |     | 15     | ns   |
| $t_{pw1}$ | SCLK pulse width low  | 5T                   |     |        | ns   |
| $t_{pw2}$ | SCLK pulse width high   | 5T                   |     |        | ns   |
| $t_{h1}$  | Valid nCS after valid SCLK hold time  | 2T                   |     |        | ns   |
| $t_{h2}$  | Valid SDI after valid SCLK hold time  | 3T                   |     |        | ns   |
| $t_{csh}$ | Time between consecutive Read-Read or Read-Write accesses (nCS rising edge to nCS falling edge) | 3T                   |     |        | ns   |

NOTE: Specifications guaranteed by design and characterization.

### I<sup>2</sup>C Mode Operation

The I<sup>2</sup>C interface is designed to fully support v1.2 of the I<sup>2</sup>C Specification for Normal and Fast mode operation. The device acts as a slave device on the I<sup>2</sup>C bus at 100kHz or 400kHz using the address defined in the Serial Interface Control register (0006h), as modified by the S\_A0 & S\_A1 input pin settings. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant

bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I<sup>2</sup>C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

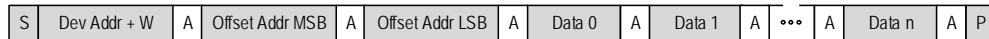
Current Read



Sequential Read



Sequential Write



- From master to slave
- From slave to master
- S = Start
- Sr = Repeated start
- A = Acknowledge
- A-bar = Non-acknowledge
- P = Stop

**Figure 6. I<sup>2</sup>C Slave Read and Write Cycle Sequencing**

### I<sup>2</sup>C Master Mode

When operating in I<sup>2</sup>C mode, the 8T49N282 has the capability to become a bus master on the I<sup>2</sup>C bus for the purposes of reading its configuration from an external I<sup>2</sup>C EEPROM. Only a block read cycle will be supported.

As an I<sup>2</sup>C bus master, the 8T49N282 will support the following functions:

- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (E0h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1- or 2-byte addressing mode

- Master arbitration with programmable number of retries
  - Fixed-period cycle response timer to prevent permanently hanging the I<sup>2</sup>C bus.
  - Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out
- The 8T49N282 will not support the following functions:

- I<sup>2</sup>C General Call
- Slave clock stretching
- I<sup>2</sup>C Start Byte protocol
- EEPROM Chaining
- CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I<sup>2</sup>C devices including the external EEPROM used for booting

Sequential Read (1-Byte Offset Address)



Sequential Read (2-Byte Offset Address)



- From master to slave
- From slave to master
- S = Start
- Sr = Repeated start
- A = Acknowledge
- A-bar = Non-acknowledge
- P = Stop

**Figure 7. I<sup>2</sup>C Master Read Cycle Sequencing**



### I<sup>2</sup>C Boot-up Initialization Mode

If enabled (via the BOOT\_EEP bit in the Startup register), once the nRST input has been deasserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I<sup>2</sup>C bus to read its initial register settings from a memory location on the I<sup>2</sup>C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address E0h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit (021Eh) in the Global Interrupt Status register will also be set in this event.

If the BOOTFAIL bit is set, then both LOL[n] indicators will be set.

Contents of the EEPROM should be as shown in [Table 6](#).

**Table 6. External Serial EEPROM Contents**

| EEPROM Offset<br>(Hex) | Contents                                       |  |    |    |    |    |    |   |   |
|------------------------|--|--|----|----|----|----|----|---|---|
|                        | D7   | D6   | D5 | D4 | D3 | D2 | D1 | D0  |   |
| 00                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   |   |
| 01                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   |   |
| 02                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   |   |
| 03                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   |   |
| 04                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1   |   |
| 05                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | Serial EEPROM<br>Speed Select<br>0 = 100kHz<br>1 = 400kHz |   |
| 06                     | 1  | 8T49N282 Device I <sup>2</sup> C Address [6:2] |    |    |    |    |    | 1   | 1 |
| 07                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0   |   |
| 08 - DF                | Desired contents of Device Registers 08h - DFh |  |    |    |    |    |    |   |   |
| E0                     | Serial EEPROM CRC                              |  |    |    |    |    |    |   |   |
| E1 - FF                | Unused   |  |    |    |    |    |    |   |   |



## Register Descriptions

**Table 7A. Register Blocks**

| Register Ranges Offset (Hex) | Register Block Description                |
|------------------------------|---|
| 0000 - 0001                  | Startup Control Registers                 |
| 0002 - 0005                  | Device ID Control Registers               |
| 0006 - 0007                  | Serial Interface Control Registers        |
| 0008 - 003A                  | Digital PLL0 Control Registers            |
| 003B - 006D                  | Digital PLL1 Control Registers            |
| 006E - 0076                  | GPIO Control Registers                    |
| 0077 - 00AB                  | Output Clock Control Registers            |
| 00AC - 00AF                  | Analog PLL0 Control Registers             |
| 00B0 - 00B3                  | Analog PLL1 Control Registers             |
| 00B4 - 00B8                  | Power-Down Control Registers              |
| 00B9 - 00C6                  | Input Monitor Control Registers           |
| 00C7 - 00C8                  | Interrupt Enable Registers                |
| 00C9 - 01FF                  | Reserved                                  |
| 0200 - 0203                  | Interrupt Status Registers                |
| 0204                         | Output Phase Adjustment Status Register   |
| 0205 - 020E                  | Digital PLL0 Status Registers             |
| 020F - 0218                  | Digital PLL1 Status Registers             |
| 0219                         | General-Purpose Input Status Register     |
| 021A - 021F                  | Global Interrupt and Boot Status Register |
| 0220 - 03FF                  | Reserved                                  |

**Table 7B. Startup Control Register Bit Field Locations and Descriptions**

| Startup Control Register Block Field Locations |              |               |    |    |    |      |           |           |  |
|--|--------------|---------------|----|----|----|------|-----------|-----------|--|
| Address (Hex)                                  | D7           | D6            | D5 | D4 | D3 | D2   | D1        | D0        |  |
| 0000   | EEP_RTY[4:0] |               |    |    |    | Rsvd | nBOOT_OTP | nBOOT_EEP |  |
| 0001   | EEP_A15      | EEP_ADDR[6:0] |    |    |    |      |           |           |  |

| Startup Control Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name                                    | Field Type | Default Value | Description  |
| EEP_RTY[4:0]                                      | R/W        | 00001b        | Select number of times arbitration for the I <sup>2</sup> C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try. |
| nBOOT_OTP   | R/W        | NOTE 1        | Internal One-Time Programmable (OTP) memory usage on power-up:<br>0 = Load power-up configuration from OTP<br>1 = Only load 1st eight bytes from OTP                                     |
| nBOOT_EEP   | R/W        | NOTE 1        | External EEPROM usage on power-up:<br>0 = Load power-up configuration from external serial EEPROM (overwrites OTP values)<br>1 = Don't use external EEPROM                               |
| EEP_A15   | R/W        | NOTE 1        | Serial EEPROM supports 15-bit addressing mode (multiple pages).  |
| EEP_ADDR[6:0]                                     | R/W        | NOTE 1        | I <sup>2</sup> C base address for serial EEPROM.   |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.  |

NOTE 1: These values are specific to the device configuration 'dash-code'. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for exact default values.

**Table 7C. Device ID Control Register Bit Field Locations and Descriptions**

| Device ID Register Control Block Field Locations |                |    |    |                 |    |    |    |    |  |
|--|----------------|----|----|-----------------|----|----|----|----|--|
| Address (Hex)                                    | D7             | D6 | D5 | D4              | D3 | D2 | D1 | D0 |  |
| 0002   | REV_ID[3:0]    |    |    | DEV_ID[15:12]   |    |    |    |    |  |
| 0003   | DEV_ID[11:4]   |    |    |                 |    |    |    |    |  |
| 0004   | DEV_ID[3:0]    |    |    | DASH_CODE[10:7] |    |    |    |    |  |
| 0005   | DASH_CODE[6:0] |    |    |                 |    |    |    | 1  |  |

| Device ID Control Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name                                      | Field Type | Default Value | Description  |
| REV_ID[3:0]   | R/W        | 0010b         | Device revision.   |
| DEV_ID[15:0]  | R/W        | 0600h         | Device ID code.  |
| DASH_CODE [10:0]                                    | R/W        | <b>NOTE 1</b> | Device Dash Code:<br>Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time. Refer to <i>FemtoClock NG Universal Frequency Translator Ordering Product Information</i> to identify major configuration parameters associated with this Dash Code value. |

NOTE 1: These values are specific to the device configuration 'dash-code'. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for exact default values.

**Table 7D. Serial Interface Control Register Bit Field Locations and Descriptions**

| Serial Interface Control Block Field Locations |         |             |    |    |    |    |           |           |  |
|--|---------|-------------|----|----|----|----|-----------|-----------|--|
| Address (Hex)                                  | D7      | D6          | D5 | D4 | D3 | D2 | D1        | D0        |  |
| 0006   | SPI_SEL | UFTADD[6:2] |    |    |    |    | UFTADD[1] | UFTADD[0] |  |
| 0007   | Rsvd    |             |    |    |    |    |           | 1         |  |

| Device ID Control Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name                                      | Field Type | Default Value | Description   |
| SPI_SEL   | R/O        | 0b            | Select Mode for serial interface as read from the nI2C_SPI pin:<br>0 = I <sup>2</sup> C<br>1 = SPI  |
| UFTADD[6:2]   | R/W        | <b>NOTE 1</b> | Configurable portion of I <sup>2</sup> C Base Address (bits 6:2) for this device.   |
| UFTADD[1]   | R/O        | 0b            | I <sup>2</sup> C Base Address bit 1. This address bit reflects the status of the S_A1 / SDI external input pin. See <a href="#">Table 1</a> , Pin Descriptions. |
| UFTADD[0]   | R/O        | 0b            | I <sup>2</sup> C Base Address bit 0. This address bit reflects the status of the S_A0 / nCS external input pin. See <a href="#">Table 1</a> , Pin Descriptions. |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

NOTE 1: These values are specific to the device configuration 'dash-code'. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for exact default values.

**Table 7E. Digital PLL0 Input Control Register Bit Field Locations and Descriptions**

| Digital PLL0 Input Control Register Block Field Locations |              |           |             |               |             |      |             |         |
|---|--------------|-----------|-------------|---------------|-------------|------|-------------|---------|
| Address (Hex)   | D7           | D6        | D5          | D4            | D3          | D2   | D1          | D0      |
| 0008  | REFSEL0[2:0] |           |             | FBSEL0[2:0]   |             |      | RVRT0       | SWMODE0 |
| 0009  | PRI0_3[1:0]  |           | PRI0_2[1:0] |               | PRI0_1[1:0] |      | PRI0_0[1:0] |         |
| 000A  | REFDIS0_3    | REFDIS0_2 | REFDIS0_1   | REFDIS0_0     | Rsvd        | Rsvd | STATE0[1:0] |         |
| 000B  | Rsvd         |           |             | PRE0_0[20:16] |             |      |             |         |
| 000C  | PRE0_0[15:8] |           |             |               |             |      |             |         |
| 000D  | PRE0_0[7:0]  |           |             |               |             |      |             |         |
| 000E  | Rsvd         |           |             | PRE0_1[20:16] |             |      |             |         |
| 000F  | PRE0_1[15:8] |           |             |               |             |      |             |         |
| 0010  | PRE0_1[7:0]  |           |             |               |             |      |             |         |
| 0011  | Rsvd         |           |             | PRE0_2[20:16] |             |      |             |         |
| 0012  | PRE0_2[15:8] |           |             |               |             |      |             |         |
| 0013  | PRE0_2[7:0]  |           |             |               |             |      |             |         |
| 0014  | Rsvd         |           |             | PRE0_3[20:16] |             |      |             |         |
| 0015  | PRE0_3[15:8] |           |             |               |             |      |             |         |
| 0016  | PRE0_3[7:0]  |           |             |               |             |      |             |         |

| Digital PLL0 Input Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| REFSEL0[2:0]   | R/W        | 000b          | Input reference selection for Digital PLL0:<br>000 = Automatic selection<br>001 = Manual selection by GPIO inputs<br>010 through 011 = Reserved<br>100 = Force selection of Input Reference 0<br>101 = Force selection of Input Reference 1<br>110 = Force selection of Input Reference 2<br>111 = Force selection of Input Reference 3 |
| FBSEL0[2:0]  | R/W        | 000b          | Feedback mode selection for Digital PLL0:<br>000 - 011 = internal feedback divider<br>100 = external feedback from Input Reference 0<br>101 = external feedback from Input Reference 1<br>110 = external feedback from Input Reference 2<br>111 = external feedback from Input Reference 3  |
| RVRT0  | R/W        | 1b            | Automatic switching mode for Digital PLL0:<br>0 = non-revertive switching<br>1 = revertive switching  |
| SWMODE0  | R/W        | 1b            | Controls how Digital PLL0 adjusts output phase when switching between input references:<br>0 = Absorb any phase differences between old & new input references<br>1 = Track to follow new input reference's phase using phase-slope limiting  |
| PRI0_0[1:0]  | R/W        | 00b           | Switchover priority for Input Reference 0 when used by Digital PLL0:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |

| Digital PLL0 Input Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| PRI0_1[1:0]  | R/W        | 01b           | Switchover priority for Input Reference 1 when used by Digital PLL0:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| PRI0_2[1:0]  | R/W        | 10b           | Switchover priority for Input Reference 2 when used by Digital PLL0:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| PRI0_3[1:0]  | R/W        | 11b           | Switchover priority for Input Reference 3 when used by Digital PLL0:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| REFDIS0_0  | R/W        | 0b            | Input Reference 0 Switching Selection Disable for Digital PLL0:<br>0 = Input Reference 0 is included in the switchover sequence for Digital PLL0<br>1 = Input Reference 0 is not included in the switchover sequence for Digital PLL0 |
| REFDIS0_1  | R/W        | 0b            | Input Reference 1 Switching Selection Disable for Digital PLL0:<br>0 = Input Reference 1 is included in the switchover sequence for Digital PLL0<br>1 = Input Reference 1 is not included in the switchover sequence for Digital PLL0 |
| REFDIS0_2  | R/W        | 0b            | Input Reference 2 Switching Selection Disable for Digital PLL0:<br>0 = Input Reference 2 is included in the switchover sequence for Digital PLL0<br>1 = Input Reference 2 is not included in the switchover sequence for Digital PLL0 |
| REFDIS0_3  | R/W        | 0b            | Input Reference 3 Switching Selection Disable for Digital PLL0:<br>0 = Input Reference 3 is included in the switchover sequence for Digital PLL0<br>1 = Input Reference 3 is not included in the switchover sequence for Digital PLL0 |
| STATE0[1:0]  | R/W        | 00b           | Digital PLL0 State Machine Control:<br>00 = Run automatically<br>01 = Force FREERUN state - set this if in Synthesizer Mode for PLL0.<br>10 = Force NORMAL state<br>11 = Force HOLDOVER state   |
| PRE0_0[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 0 when used by Digital PLL0.  |
| PRE0_1[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 1 when used by Digital PLL0.  |
| PRE0_2[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 2 when used by Digital PLL0.  |
| PRE0_3[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 3 when used by Digital PLL0.  |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7F. Digital PLL0 Feedback Control Register Bit Field Locations and Descriptions**

| Digital PLL0 Feedback Control Register Block Field Locations |                |      |                |                 |      |                |             |    |
|--|----------------|------|----------------|-----------------|------|----------------|-------------|----|
| Address (Hex)  | D7             | D6   | D5             | D4              | D3   | D2             | D1          | D0 |
| 0017   | M1_0_0[23:16]  |      |                |                 |      |                |             |    |
| 0018   | M1_0_0[15:8]   |      |                |                 |      |                |             |    |
| 0019   | M1_0_0[7:0]    |      |                |                 |      |                |             |    |
| 001A   | M1_0_1[23:16]  |      |                |                 |      |                |             |    |
| 001B   | M1_0_1[15:8]   |      |                |                 |      |                |             |    |
| 001C   | M1_0_1[7:0]    |      |                |                 |      |                |             |    |
| 001D   | M1_0_2[23:16]  |      |                |                 |      |                |             |    |
| 001E   | M1_0_2[15:8]   |      |                |                 |      |                |             |    |
| 001F   | M1_0_2[7:0]    |      |                |                 |      |                |             |    |
| 0020   | M1_0_3[23:16]  |      |                |                 |      |                |             |    |
| 0021   | M1_0_3[15:8]   |      |                |                 |      |                |             |    |
| 0022   | M1_0_3[7:0]    |      |                |                 |      |                |             |    |
| 0023   | LCKBW0[3:0]    |      |                | ACQBW0[3:0]     |      |                |             |    |
| 0024   | LCKDAMP0[2:0]  |      | ACQDAMP0[2:0]  |                 |      | PLLGAIN0[1:0]  |             |    |
| 0025   | TGLCKDMP0[2:0] |      | TGLCKHYS<br>0  | TGLCKBW0[2:0]   |      |                | Rsvd        |    |
| 0026   | Rsvd           |      |                |                 |      |                |             |    |
| 0027   | Rsvd           |      |                |                 |      |                |             |    |
| 0028   | TGLCKTHR0[6:0] |      |                |                 |      |                | Rsvd        |    |
| 0029   | Rsvd           |      |                |                 |      |                |             |    |
| 002A   | Rsvd           |      |                |                 |      |                |             |    |
| 002B   | FFh            |      |                |                 |      |                |             |    |
| 002C   | FFh            |      |                |                 |      |                |             |    |
| 002D   | FFh            |      |                |                 |      |                |             |    |
| 002E   | FFh            |      |                |                 |      |                |             |    |
| 002F   | SLEW0[1:0]     | Rsvd | HOLD0[1:0]     |                 | Rsvd | HOLDAVG0       | FASTLCK0    |    |
| 0030   | LOCK0[7:0]     |      |                |                 |      |                |             |    |
| 0031   | Rsvd           |      |                |                 |      |                | DSM_INT0[8] |    |
| 0032   | DSM_INT0[7:0]  |      |                |                 |      |                |             |    |
| 0033   | Rsvd           |      |                | DSMFRAC0[20:16] |      |                |             |    |
| 0034   | DSMFRAC0[15:8] |      |                |                 |      |                |             |    |
| 0035   | DSMFRAC0[7:0]  |      |                |                 |      |                |             |    |
| 0036   | Rsvd           |      |                |                 |      |                |             |    |
| 0037   | Rsvd           |      |                |                 |      |                |             |    |
| 0038   | Rsvd           |      |                |                 |      |                |             |    |
| 0039   | Rsvd           |      |                |                 |      |                |             |    |
| 003A   | DSM_ORD0[1:0]  |      | DCXOGAIN0[1:0] |                 | Rsvd | DITHGAIN0[2:0] |             |    |

| Digital PLL0 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| M1_0_0[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL0.  |
| M1_0_1[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL0.  |
| M1_0_2[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 2 when used by Digital PLL0.  |
| M1_0_3[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 3 when used by Digital PLL0.  |
| LCKBW0[3:0]   | R/W        | 0111b         | Digital PLL0 Loop Bandwidth while locked:<br>0000 = 512mHz<br>0001 = 1Hz<br>0010 = 2Hz<br>0011 = 4Hz<br>0100 = 8Hz<br>0101 = 16Hz<br>0110 = 32Hz<br>0111 = 64Hz<br>1000 = 128Hz<br>1001 = 256Hz<br>1010 = 512Hz<br>1011 = Reserved<br>1100 through 1111 = Reserved                      |
| ACQBW0[3:0]   | R/W        | 0111b         | Digital PLL0 Loop Bandwidth while in acquisition (not-locked):<br>0000 = 512mHz<br>0001 = 1Hz<br>0010 = 2Hz<br>0011 = 4Hz<br>0100 = 8Hz<br>0101 = 16Hz<br>0110 = 32Hz<br>0111 = 64Hz<br>1000 = 128Hz<br>1001 = 256Hz<br>1010 = 512Hz<br>1011 = Reserved<br>1100 through 1111 = Reserved |
| LCKDAMP0[2:0]   | R/W        | 011b          | Damping factor for Digital PLL0 while locked:<br>000 = Reserved<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved  |
| ACQDAMP0[2:0]   | R/W        | 011b          | Damping factor for Digital PLL0 while in acquisition (not locked):<br>000 = Reserved<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved   |

| Digital PLL0 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| PLLGAIN0[1:0]   | R/W        | 01b           | Digital Loop Filter Gain Settings for Digital PLL0:<br>00 = 0.5<br>01 = 1<br>10 = 1.5<br>11 = 2   |
| TGLCKBW0[2:0]   | R/W        | 011b          | Loop Bandwidth Setting used when PLL0 is in tight lock and phase error is very close to 0:<br>000 = Off (use Loop Bandwidth LCKBW0[3:0])<br>001 = 1Hz<br>010 = 2Hz<br>011 = 4Hz<br>100 = 8Hz<br>101 = 16Hz<br>110 = 32Hz<br>111 = 64Hz  |
| TGLCKDMP0[2:0]  | R/W        | 000b          | Tight Lock Operation Damping Factor for PLL0:<br>000 = Off (Use Locked Damping Factor LCKDAMP0[2:0])<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved   |
| TGLCKHYS0   | R/W        | 0b            | Tight Lock Hysteresis Enable for PLL0. Indicates when Tight Lock Operation is entered / exited.<br>0 = Non-hysteresis - enter & exit when phase error crosses threshold in TGLCKTHR0[6:0]<br>1 = Hysteresis - enter when phase error less than 5nsec and exit when larger than TGLCKTHR0[6:0] |
| TGLCKTHR0[6:0]  | R/W        | 00h           | Tight Lock Threshold for PLL0, used to decide when to enter / exit Tight Lock operation.<br>Effective value = (entered value + 2) * (PLL0 period * 8 = 2.0-2.67nsec). Range is 4-345nsec.   |
| SLEW0[1:0]  | R/W        | 00b           | Phase-slope control for Digital PLL0:<br>00 = no limit - controlled by loop bandwidth of Digital PLL0, <a href="#">NOTE1</a> .<br>01 = 193 $\mu$ sec/sec<br>10 = 24 $\mu$ sec/sec<br>11 = Reserved  |
| HOLD0[1:0]  | R/W        | 00b           | Holdover Averaging mode selection for Digital PLL0:<br>00 = Instantaneous mode - uses historical value 100ms prior to entering holdover<br>01 = Fast Average Mode<br>10 = Reserved<br>11 = Set VCO control voltage to $V_{CC}/2$  |
| HOLDAVG0  | R/W        | 0b            | Holdover Averaging Enable for Digital PLL0:<br>0 = Holdover averaging disabled<br>1 = Holdover averaging enabled as defined in HOLD0[1:0]   |
| FASTLCK0  | R/W        | 0b            | Enables Fast Lock operation for Digital PLL0:<br>0 = Normal locking using LCKBW0 & LCKDAMP0 fields in all cases<br>1 = Fast Lock mode using ACQBW0 & ACQDAMP0 when not phase locked and LCKBW0 & LCKDAMP0 once phase locked   |
| LOCK0[7:0]  | R/W        | 3Fh           | Lock window size for Digital PLL0. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.   |



| Digital PLL0 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| DSM_INT0[8:0]   | R/W        | 02Dh          | Integer portion of the Delta-Sigma Modulator value.   |
| DSMFRAC0[20:0]  | R/W        | 000000h       | Fractional portion of Delta-Sigma Modulator value. Divide this number by $2^{21}$ to determine the actual fraction.   |
| DSM_ORD0[1:0]   | R/W        | 11b           | Delta-Sigma Modulator Order for Digital PLL0:<br>00 = Delta-Sigma Modulator disabled<br>01 = 1st order modulation<br>10 = 2nd order modulation<br>11 = 3rd order modulation                           |
| DCXOGAIN0[1:0]  | R/W        | 01b           | Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL0:<br>00 = 0.5<br>01 = 1<br>10 = 2<br>11 = 4                            |
| DITHGAIN0[2:0]  | R/W        | 000b          | Dither Gain setting for Digital PLL0:<br>000 = no dither<br>001 = Least Significant Bit (LSB) only<br>010 = 2 LSBs<br>011 = 4 LSBs<br>100 = 8 LSBs<br>101 = 16 LSBs<br>110 = 32 LSBs<br>111 = 64 LSBs |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

NOTE 1: Settings other than "00" may result in a significant increase in initial lock time.

**Table 7G. Digital PLL1 Input Control Register Bit Field Locations and Descriptions**

| Digital PLL1 Input Control Register Block Field Locations |              |           |             |               |             |      |             |         |
|---|--------------|-----------|-------------|---------------|-------------|------|-------------|---------|
| Address (Hex)   | D7           | D6        | D5          | D4            | D3          | D2   | D1          | D0      |
| 003B  | REFSEL1[2:0] |           |             | FBSEL1[2:0]   |             |      | RVRT1       | SWMODE1 |
| 003C  | PRI1_3[1:0]  |           | PRI1_2[1:0] |               | PRI1_1[1:0] |      | PRI1_0[1:0] |         |
| 003D  | REFDIS1_3    | REFDIS1_2 | REFDIS1_1   | REFDIS1_0     | Rsvd        | Rsvd | STATE1[1:0] |         |
| 003E  | Rsvd         |           |             | PRE1_0[20:16] |             |      |             |         |
| 003F  | PRE1_0[15:8] |           |             |               |             |      |             |         |
| 0040  | PRE1_0[7:0]  |           |             |               |             |      |             |         |
| 0041  | Rsvd         |           |             | PRE1_1[20:16] |             |      |             |         |
| 0042  | PRE1_1[15:8] |           |             |               |             |      |             |         |
| 0043  | PRE1_1[7:0]  |           |             |               |             |      |             |         |
| 0044  | Rsvd         |           |             | PRE1_2[20:16] |             |      |             |         |
| 0045  | PRE1_2[15:8] |           |             |               |             |      |             |         |
| 0046  | PRE1_2[7:0]  |           |             |               |             |      |             |         |
| 0047  | Rsvd         |           |             | PRE1_3[20:16] |             |      |             |         |
| 0048  | PRE1_3[15:8] |           |             |               |             |      |             |         |
| 0049  | PRE1_3[7:0]  |           |             |               |             |      |             |         |

| Digital PLL1 Input Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| REFSEL1[2:0]   | R/W        | 000b          | Input reference selection for Digital PLL1:<br>000 = Automatic selection<br>001 = Manual selection by GPIO inputs<br>010 through 011 = Reserved<br>100 = Force selection of Input Reference 0<br>101 = Force selection of Input Reference 1<br>110 = Force selection of Input Reference 2<br>111 = Force selection of Input Reference 3 |
| FBSEL1[2:0]  | R/W        | 000b          | Feedback mode selection for Digital PLL1:<br>000 through 011 = internal feedback divider<br>100 = external feedback from Input Reference 0<br>101 = external feedback from Input Reference 1<br>110 = external feedback from Input Reference 2<br>111 = external feedback from Input Reference 3  |
| RVRT1  | R/W        | 1b            | Automatic switching mode for Digital PLL1:<br>0 = non-revertive switching<br>1 = revertive switching  |
| SWMODE1  | R/W        | 1b            | Controls how Digital PLL1 adjusts output phase when switching between input references:<br>0 = Absorb any phase differences between old & new input references<br>1 = Track to follow new input reference's phase using phase-slope limiting  |
| PRI1_0[1:0]  | R/W        | 00b           | Switchover priority for Input Reference 0 when used by Digital PLL1:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |

| Digital PLL1 Input Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| PRI1_1[1:0]  | R/W        | 01b           | Switchover priority for Input Reference 1 when used by Digital PLL1:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| PRI1_2[1:0]  | R/W        | 10b           | Switchover priority for Input Reference 2 when used by Digital PLL1:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| PRI1_3[1:0]  | R/W        | 11b           | Switchover priority for Input Reference 3 when used by Digital PLL1:<br>00 = 1st priority<br>01 = 2nd priority<br>10 = 3rd priority<br>11 = 4th priority  |
| REFDIS1_0  | R/W        | 0b            | Input Reference 0 Switching Selection Disable for Digital PLL1:<br>0 = Input Reference 0 is included in the switchover sequence for Digital PLL1<br>1 = Input Reference 0 is not included in the switchover sequence for Digital PLL1 |
| REFDIS1_1  | R/W        | 0b            | Input Reference 1 Switching Selection Disable for Digital PLL1:<br>0 = Input Reference 1 is included in the switchover sequence for Digital PLL1<br>1 = Input Reference 1 is not included in the switchover sequence for Digital PLL1 |
| REFDIS1_2  | R/W        | 0b            | Input Reference 2 Switching Selection Disable for Digital PLL1:<br>0 = Input Reference 2 is included in the switchover sequence for Digital PLL1<br>1 = Input Reference 2 is not included in the switchover sequence for Digital PLL1 |
| REFDIS1_3  | R/W        | 0b            | Input Reference 3 Switching Selection Disable for Digital PLL1:<br>0 = Input Reference 3 is included in the switchover sequence for Digital PLL1<br>1 = Input Reference 3 is not included in the switchover sequence for Digital PLL1 |
| STATE1[1:0]  | R/W        | 00b           | Digital PLL1 State Machine Control:<br>00 = Run automatically<br>01 = Force FREERUN state - set this if in Synthesizer Mode for PLL1<br>10 = Force NORMAL state<br>11 = Force HOLDOVER state  |
| PRE1_0[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 0 when used by Digital PLL1.  |
| PRE1_1[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 1 when used by Digital PLL1.  |
| PRE1_2[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 2 when used by Digital PLL1.  |
| PRE1_3[20:0]   | R/W        | 000000h       | Pre-divider ratio for Input Reference 3 when used by Digital PLL1.  |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7H. Digital PLL1 Feedback Control Register Bit Field Locations and Descriptions**

| Digital PLL1 Feedback Control Register Block Field Locations |                |      |                |                 |      |                |             |    |
|--|----------------|------|----------------|-----------------|------|----------------|-------------|----|
| Address (Hex)  | D7             | D6   | D5             | D4              | D3   | D2             | D1          | D0 |
| 004A   | M1_1_0[23:16]  |      |                |                 |      |                |             |    |
| 004B   | M1_1_0[15:8]   |      |                |                 |      |                |             |    |
| 004C   | M1_1_0[7:0]    |      |                |                 |      |                |             |    |
| 004D   | M1_1_1[23:16]  |      |                |                 |      |                |             |    |
| 004E   | M1_1_1[15:8]   |      |                |                 |      |                |             |    |
| 004F   | M1_1_1[7:0]    |      |                |                 |      |                |             |    |
| 0050   | M1_1_2[23:16]  |      |                |                 |      |                |             |    |
| 0051   | M1_1_2[15:8]   |      |                |                 |      |                |             |    |
| 0052   | M1_1_2[7:0]    |      |                |                 |      |                |             |    |
| 0053   | M1_1_3[23:16]  |      |                |                 |      |                |             |    |
| 0054   | M1_1_3[15:8]   |      |                |                 |      |                |             |    |
| 0055   | M1_1_3[7:0]    |      |                |                 |      |                |             |    |
| 0056   | LCKBW1[3:0]    |      |                | ACQBW1[3:0]     |      |                |             |    |
| 0057   | LCKDAMP1[2:0]  |      | ACQDAMP1[2:0]  |                 |      | PLLGAIN1[1:0]  |             |    |
| 0058   | TGLCKDMP1[2:0] |      | TGLCKHYS<br>1  | TGLCKBW1[2:0]   |      |                | Rsvd        |    |
| 0059   | Rsvd           |      |                |                 |      |                |             |    |
| 005A   | Rsvd           |      |                |                 |      |                |             |    |
| 005B   | TGLCKTHR1[6:0] |      |                |                 |      |                | Rsvd        |    |
| 005C   | Rsvd           |      |                |                 |      |                |             |    |
| 005D   | Rsvd           |      |                |                 |      |                |             |    |
| 005E   | FFh            |      |                |                 |      |                |             |    |
| 005F   | FFh            |      |                |                 |      |                |             |    |
| 0060   | FFh            |      |                |                 |      |                |             |    |
| 0061   | FFh            |      |                |                 |      |                |             |    |
| 0062   | SLEW1[1:0]     | Rsvd | HOLD1[1:0]     |                 | Rsvd | HOLDAVG1       | FASTLCK1    |    |
| 0063   | LOCK1[7:0]     |      |                |                 |      |                |             |    |
| 0064   | Rsvd           |      |                |                 |      |                | DSM_INT1[8] |    |
| 0065   | DSM_INT1[7:0]  |      |                |                 |      |                |             |    |
| 0066   | Rsvd           |      |                | DSMFRAC1[20:16] |      |                |             |    |
| 0067   | DSMFRAC1[15:8] |      |                |                 |      |                |             |    |
| 0068   | DSMFRAC1[7:0]  |      |                |                 |      |                |             |    |
| 0069   | Rsvd           |      |                |                 |      |                |             |    |
| 006A   | Rsvd           |      |                |                 |      |                |             |    |
| 006B   | Rsvd           |      |                |                 |      |                |             |    |
| 006C   | Rsvd           |      |                |                 |      |                |             |    |
| 006D   | DSM_ORD1[1:0]  |      | DCXOGAIN1[1:0] |                 | Rsvd | DITHGAIN1[2:0] |             |    |

| Digital PLL1 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| M1_1_0[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL1.  |
| M1_1_1[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL1.  |
| M1_1_2[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 2 when used by Digital PLL1.  |
| M1_1_3[23:0]  | R/W        | 070000h       | M1 Feedback divider ratio for Input Reference 3 when used by Digital PLL1.  |
| LCKBW1[3:0]   | R/W        | 0111b         | Digital PLL1 Loop Bandwidth while locked:<br>0000 = 512mHz<br>0001 = 1Hz<br>0010 = 2Hz<br>0011 = 4Hz<br>0100 = 8Hz<br>0101 = 16Hz<br>0110 = 32Hz<br>0111 = 64Hz<br>1000 = 128Hz<br>1001 = 256Hz<br>1010 = 512Hz<br>1011 = Reserved<br>1100 through 1111 = Reserved                      |
| ACQBW1[3:0]   | R/W        | 0111b         | Digital PLL1 Loop Bandwidth while in acquisition (not-locked):<br>0000 = 512mHz<br>0001 = 1Hz<br>0010 = 2Hz<br>0011 = 4Hz<br>0100 = 8Hz<br>0101 = 16Hz<br>0110 = 32Hz<br>0111 = 64Hz<br>1000 = 128Hz<br>1001 = 256Hz<br>1010 = 512Hz<br>1011 = Reserved<br>1100 through 1111 = Reserved |
| LCKDAMP1[2:0]   | R/W        | 011b          | Damping factor for Digital PLL1 while locked:<br>000 = Reserved<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved  |
| ACQDAMP1[2:0]   | R/W        | 011b          | Damping factor for Digital PLL1 while in acquisition (not locked):<br>000 = Reserved<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved   |

| Digital PLL1 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| PLLGAIN1[1:0]   | R/W        | 01b           | Digital Loop Filter Gain Settings for Digital PLL1:<br>00 = 0.5<br>01 = 1.0<br>10 = 1.5<br>11 = 2.0   |
| TGLCKBW1[2:0]   | R/W        | 011b          | Loop Bandwidth Setting used when PLL1 is in tight lock and phase error is very close to 0:<br>000 = Off (Use Locked loop bandwidth LCKBW1[3:0])<br>001 = 1Hz<br>010 = 2Hz<br>011 = 4Hz<br>100 = 8Hz<br>101 = 16Hz<br>110 = 32Hz<br>111 = 64Hz   |
| TGLCKDMP1[2:0]  | R/W        | 000b          | Tight Lock Operation Damping Factor for PLL1:<br>000 = Off (Use Locked Damping Factor LCKDAMP1[2:0])<br>001 = 1<br>010 = 2<br>011 = 5<br>100 = 10<br>101 = 20<br>110 = Reserved<br>111 = Reserved   |
| TGLCKHYS1   | R/W        | 0b            | Tight Lock Hysteresis Enable for PLL1. Indicates when Tight Lock Operation is entered / exited.<br>0 = Non-hysteresis - enter & exit when phase error crosses threshold in TGLCKTHR1[6:0]<br>1 = Hysteresis - enter when phase error less than 5nsec and exit when larger than TGLCKTHR1[6:0] |
| TGLCKTHR1[6:0]  | R/W        | 00h           | Tight Lock Threshold for PLL1, used to decide when to enter / exit Tight Lock operation.<br>Effective value = (entered value + 2) * (PLL0 period * 8 = 2.0-2.67nsec). Range is 4-345nsec.   |
| SLEW1[1:0]  | R/W        | 00b           | Phase-slope control for Digital PLL1:<br>00 = no limit - controlled by loop bandwidth of Digital PLL1, <a href="#">NOTE 1</a> .<br>01 = 193µsec/sec<br>10 = 24µsec/sec<br>11 = Reserved   |
| HOLD1[1:0]  | R/W        | 00b           | Holdover Averaging mode selection for Digital PLL1:<br>00 = Instantaneous mode - uses historical value 100ms prior to entering holdover<br>01 = Fast Average Mode<br>10 = Reserved<br>11 = Set VCO control voltage to $V_{CC}/2$  |
| HOLDAVG1  | R/W        | 0b            | Holdover Averaging Enable for Digital PLL1:<br>0 = Holdover averaging disabled<br>1 = Holdover averaging enabled as defined in HOLD1[1:0]   |
| FASTLCK1  | R/W        | 0b            | Enables Fast Lock operation for Digital PLL1:<br>0 = Normal locking using LCKBW1 & LCKDAMP1 fields in all cases<br>1 = Fast Lock mode using ACQBW1 & ACQDAMP1 when not phase locked and LCKBW1 & LCKDAMP1 once phase locked   |
| LOCK1[7:0]  | R/W        | 3Fh           | Lock window size for Digital PLL1. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0.   |

| Digital PLL1 Feedback Configuration Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| DSM_INT1[8:0]   | R/W        | 02Dh          | Integer portion of the Delta-Sigma Modulator value.   |
| DSMFRAC1[20:0]  | R/W        | 000000h       | Fractional portion of Delta-Sigma Modulator value. Divide this number by $2^{21}$ to determine the actual fraction.   |
| DSM_ORD1[1:0]   | R/W        | 11b           | Delta-Sigma Modulator Order for Digital PLL1.<br>00 = Delta-Sigma Modulator disabled<br>01 = 1st order modulation<br>10 = 2nd order modulation<br>11 = 3rd order modulation                           |
| DCXOGAIN1[1:0]  | R/W        | 01b           | Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL1.<br>00 = 0.5<br>01 = 1.0<br>10 = 2.0<br>11 = 4.0                      |
| DITHGAIN1[2:0]  | R/W        | 000b          | Dither Gain setting for Digital PLL1.<br>000 = no dither<br>001 = Least Significant Bit (LSB) only<br>010 = 2 LSBs<br>011 = 4 LSBs<br>100 = 8 LSBs<br>101 = 16 LSBs<br>110 = 32 LSBs<br>111 = 64 LSBs |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

NOTE 1: Settings other than "00" may result in a significant increase in initial lock time.



**Table 71. GPIO Control Register Bit Field Locations and Descriptions**

The values observed on any GPIO pins that are used as general purpose inputs are visible in the GPI[7:0] register that is located at location 0219h near a number of other read-only registers.

| GPIO Control Register Block Field Locations |               |            |            |            |            |            |            |            |
|---|---------------|------------|------------|------------|------------|------------|------------|------------|
| Address (Hex)                               | D7            | D6         | D5         | D4         | D3         | D2         | D1         | D0         |
| 006E  | GPIO_DIR[7:0] |            |            |            |            |            |            |            |
| 006F  | GPI7SEL[2]    | GPI6SEL[2] | GPI5SEL[2] | GPI4SEL[2] | GPI3SEL[2] | GPI2SEL[2] | GPI1SEL[2] | GPI0SEL[2] |
| 0070  | GPI7SEL[1]    | GPI6SEL[1] | GPI5SEL[1] | GPI4SEL[1] | GPI3SEL[1] | GPI2SEL[1] | GPI1SEL[1] | GPI0SEL[1] |
| 0071  | GPI7SEL[0]    | GPI6SEL[0] | GPI5SEL[0] | GPI4SEL[0] | GPI3SEL[0] | GPI2SEL[0] | GPI1SEL[0] | GPI0SEL[0] |
| 0072  | GPO7SEL[2]    | GPO6SEL[2] | GPO5SEL[2] | GPO4SEL[2] | GPO3SEL[2] | GPO2SEL[2] | GPO1SEL[2] | GPO0SEL[2] |
| 0073  | GPO7SEL[1]    | GPO6SEL[1] | GPO5SEL[1] | GPO4SEL[1] | GPO3SEL[1] | GPO2SEL[1] | GPO1SEL[1] | GPO0SEL[1] |
| 0074  | GPO7SEL[0]    | GPO6SEL[0] | GPO5SEL[0] | GPO4SEL[0] | GPO3SEL[0] | GPO2SEL[0] | GPO1SEL[0] | GPO0SEL[0] |
| 0075  | Rsvd          |            |            |            |            |            |            |            |
| 0076  | GPO[7:0]      |            |            |            |            |            |            |            |

| GPIO Control Register Block Field Descriptions |            |               |  |
|--|------------|---------------|--|
| Bit Field Name                                 | Field Type | Default Value | Description  |
| GPIO_DIR[7:0]                                  | R/W        | 00h           | Direction control for General-Purpose I/O Pins GPIO[7:0]:<br>0 = input mode<br>1 = output mode   |
| GPI0SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[0] pin when set to input mode by GPIO_DIR[0] register bit:<br>000 = General Purpose Input (value on GPIO[0] pin directly reflected in GPI[0] register bit)<br>001 = Output Enable control for output Q0<br>010 = reserved<br>011 = reserved<br>100 through 111 = reserved   |
| GPI1SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[1] pin when set to input mode by GPIO_DIR[1] register bit:<br>000 = General Purpose Input (value on GPIO[1] pin directly reflected in GPI[1] register bit)<br>001 = Output Enable control for output Q1<br>010 = reserved<br>011 through 111 = reserved   |
| GPI2SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[2] pin when set to input mode by GPIO_DIR[2] register bit:<br>000 = General Purpose Input (value on GPIO[2] pin directly reflected in GPI[2] register bit)<br>001 = Output Enable control for output Q2<br>010 = reserved<br>011 = reserved<br>100 = reserved<br>101 = CSEL0[0]: Manual Clock Select Input 0 for PLL0<br>110 through 111 = reserved |
| GPI3SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[3] pin when set to input mode by GPIO_DIR[3] register bit:<br>000 = General Purpose Input (value on GPIO[3] pin directly reflected in GPI[3] register bit)<br>001 = Output Enable control for output Q3<br>010 = reserved<br>011 = reserved<br>101 = CSEL1[0]: Manual Clock Select Input 0 for PLL1<br>100, 110, 111 = reserved                     |
| GPI4SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[4] pin when set to input mode by GPIO_DIR[4] register bit:<br>000 = General Purpose Input (value on GPIO[4] pin directly reflected in GPI[4] register bit)<br>001 = Output Enable control for output Q4<br>010 through 111 = reserved   |

**GPIO Control Register Block Field Descriptions**

| Bit Field Name | Field Type | Default Value | Description   |
|----------------|------------|---------------|---|
| GPI5SEL[2:0]   | R/W        | 000b          | Function of GPIO[5] pin when set to input mode by GPIO_DIR[5] register bit:<br>000 = General Purpose Input (value on GPIO[5] pin directly reflected in GPI[5] register bit)<br>001 = Output Enable control for output Q5<br>010 through 111 = reserved  |
| GPI6SEL[2:0]   | R/W        | 000b          | Function of GPIO[6] pin when set to input mode by GPIO_DIR[6] register bit:<br>000 = General Purpose Input (value on GPIO[6] pin directly reflected in GPI[6] register bit)<br>001 = Output Enable control for output Q6<br>101 = CSEL0[1]: Manual Clock Select Input 1 for PLL0<br>010, 011, 100, 110, 111 = reserved  |
| GPI7SEL[2:0]   | R/W        | 000b          | Function of GPIO[7] pin when set to input mode by GPIO_DIR[7] register bit:<br>000 = General Purpose Input (value on GPIO[7] pin directly reflected in GPI[7] register bit)<br>001 = Output Enable control for output Q7<br>101 = CSEL1[1]: Manual Clock Select Input 1 for PLL1<br>010, 011, 100, 110, 111 = reserved  |
| GPO0SEL[2:0]   | R/W        | 000b          | Function of GPIO[0] pin when set to output mode by GPIO_DIR[0] register bit:<br>000 = General Purpose Output (value in GPO[0] register bit driven on GPIO[0] pin)<br>001 = Loss-of-Lock Status Flag for Digital PLL0 reflected on GPIO[0] pin<br>010 = Loss-of-Lock Status Flag for Digital PLL1 reflected on GPIO[0] pin<br>011 = reserved<br>100 = reserved<br>101 = reserved<br>110 through 111 = reserved |
| GPO1SEL[2:0]   | R/W        | 000b          | Function of GPIO[1] pin when set to output mode by GPIO_DIR[1] register bit:<br>000 = General Purpose Output (value in GPO[1] register bit driven on GPIO[1] pin)<br>001 = Holdover Status Flag for Digital PLL0 reflected on GPIO[1] pin<br>010 = Holdover Status Flag for Digital PLL1 reflected on GPIO[1] pin<br>011 = reserved<br>100 = reserved<br>101 = reserved<br>110 = reserved<br>111 = reserved   |
| GPO2SEL[2:0]   | R/W        | 000b          | Function of GPIO[2] pin when set to output mode by GPIO_DIR[2] register bit:<br>000 = General Purpose Output (value in GPO[2] register bit driven on GPIO[2] pin)<br>001 = Loss-of-Signal Flag for Input Reference 0 reflected on GPIO[2] pin<br>010 = reserved<br>011 = reserved<br>100 = reserved<br>101 through 111 = reserved   |
| GPO3SEL[2:0]   | R/W        | 000b          | Function of GPIO[3] pin when set to output mode by GPIO_DIR[3] register bit:<br>000 = General Purpose Output (value in GPO[3] register bit driven on GPIO[3] pin)<br>001 = Loss-of-Lock Status Flag for Digital PLL1 reflected on GPIO[3] pin<br>010 = Loss-of-Signal Status Flag for Input Reference 1 reflected on GPIO[3] pin<br>011 = reserved<br>100 = reserved<br>101 through 111 = reserved            |
| GPO4SEL[2:0]   | R/W        | 000b          | Function of GPIO[4] pin when set to output mode by GPIO_DIR[4] register bit:<br>000 = General Purpose Output (value in GPO[4] register bit driven on GPIO[4] pin)<br>001 = Holdover Status Flag for Digital PLL1 reflected on GPIO[4] pin<br>010 through 111 = reserved   |
| GPO5SEL[2:0]   | R/W        | 000b          | Function of GPIO[5] pin when set to output mode by GPIO_DIR[5] register bit:<br>000 = General Purpose Output (value in GPO[5] register bit driven on GPIO[5] pin)<br>001 = Loss-of-Signal Status Flag for Input Reference 1 reflected on GPIO[5] pin<br>010 through 111 = reserved  |

| GPIO Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name                                 | Field Type | Default Value | Description   |
| GPO6SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[6] pin when set to output mode by GPIO_DIR[6] register bit:<br>000 = General Purpose Output (value in GPO[6] register bit driven on GPIO[6] pin<br>001 = Loss-of-Signal Status Flag for Input Reference 2 reflected on GPIO[6] pin<br>010 through 111 = reserved |
| GPO7SEL[2:0]                                   | R/W        | 000b          | Function of GPIO[7] pin when set to output mode by GPIO_DIR[7] register bit:<br>000 = General Purpose Output (value in GPO[7] register bit driven on GPIO[7] pin<br>001 = Loss-of-Signal Status Flag for Input Reference 3 reflected on GPIO[7] pin<br>010 through 111 = reserved |
| GPO[7:0]                                       | R/W        | 00h           | Output Values reflect on pin GPIO[7:0] when General-Purpose Output Mode selected.   |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7J. Output Driver Control Register Bit Field Locations and Descriptions**

| Output Driver Control Register Block Field Locations |               |    |    |          |               |    |    |          |
|--|---------------|----|----|----------|---------------|----|----|----------|
| Address (Hex)  | D7            | D6 | D5 | D4       | D3            | D2 | D1 | D0       |
| 0077   | OUTEN[7:0]    |    |    |          |               |    |    |          |
| 0078   | POL_Q[7:0]    |    |    |          |               |    |    |          |
| 0079   | OUTMODE7[2:0] |    |    | SE_MODE7 | OUTMODE6[2:0] |    |    | SE_MODE6 |
| 007A   | OUTMODE5[2:0] |    |    | SE_MODE5 | OUTMODE4[2:0] |    |    | SE_MODE4 |
| 007B   | OUTMODE3[2:0] |    |    | SE_MODE3 | OUTMODE2[2:0] |    |    | SE_MODE2 |
| 007C   | OUTMODE1[2:0] |    |    | SE_MODE1 | OUTMODE0[2:0] |    |    | SE_MODE0 |

| Output Driver Control Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name  | Field Type | Default Value | Description  |
| OUTEN[7:0]  | R/W        | 00h           | Output Enable control for Clock Outputs Q[7:0], nQ[7:0]:<br>0 = Qn is in a high-impedance state<br>1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field  |
| POL_Q[7:0]  | R/W        | 00h           | Polarity of Clock Outputs Q[7:0], nQ[7:0]:<br>0 = normal polarity<br>1 = inverted polarity   |
| OUTMODEm<br>[2:0]                                       | R/W        | 001b          | Output Driver Mode of Operation for Clock Output Pair Qm, nQm:<br>000 = High-impedance<br>001 = LVPECL<br>010 = LVDS<br>011 = LVCMOS<br>100 = reserved<br>101 - 111 = reserved   |
| SE_MODEm  | R/W        | 0b            | Behavior of Output Pair Qm, nQm when LVCMOS operation is selected<br>(Must be 0 if LVDS or LVPECL output style is selected):<br>0 = Qm and nQm are both the same frequency but inverted in phase<br>1 = Qm and nQm are both the same frequency and phase |

**Table 7K. Output Divider Control Register Bit Field Locations and Descriptions**

| Output Divider Control Register Block Field Locations |                 |    |    |    |                 |    |             |    |
|---|-----------------|----|----|----|-----------------|----|-------------|----|
| Address (Hex)   | D7              | D6 | D5 | D4 | D3              | D2 | D1          | D0 |
| 007D  | Rsvd            |    |    |    |                 |    | NS1_Q0[1:0] |    |
| 007E  | NS2_Q0[15:8]    |    |    |    |                 |    |             |    |
| 007F  | NS2_Q0[7:0]     |    |    |    |                 |    |             |    |
| 0080  | Rsvd            |    |    |    |                 |    | NS1_Q1[1:0] |    |
| 0081  | NS2_Q1[15:8]    |    |    |    |                 |    |             |    |
| 0082  | NS2_Q1[7:0]     |    |    |    |                 |    |             |    |
| 0083  | Rsvd            |    |    |    |                 |    | N_Q2[17:16] |    |
| 0084  | N_Q2[15:8]      |    |    |    |                 |    |             |    |
| 0085  | N_Q2[7:0]       |    |    |    |                 |    |             |    |
| 0086  | Rsvd            |    |    |    |                 |    | N_Q3[17:16] |    |
| 0087  | N_Q3[15:8]      |    |    |    |                 |    |             |    |
| 0088  | N_Q3[7:0]       |    |    |    |                 |    |             |    |
| 0089  | Rsvd            |    |    |    |                 |    | NS1_Q4[1:0] |    |
| 008A  | NS2_Q4[15:8]    |    |    |    |                 |    |             |    |
| 008B  | NS2_Q4[7:0]     |    |    |    |                 |    |             |    |
| 008C  | Rsvd            |    |    |    |                 |    | NS1_Q5[1:0] |    |
| 008D  | NS2_Q5[15:8]    |    |    |    |                 |    |             |    |
| 008E  | NS2_Q5[7:0]     |    |    |    |                 |    |             |    |
| 008F  | Rsvd            |    |    |    |                 |    | NS1_Q6[1:0] |    |
| 0090  | NS2_Q6[15:8]    |    |    |    |                 |    |             |    |
| 0091  | NS2_Q6[7:0]     |    |    |    |                 |    |             |    |
| 0092  | Rsvd            |    |    |    |                 |    | NS1_Q7[1:0] |    |
| 0093  | NS2_Q7[15:8]    |    |    |    |                 |    |             |    |
| 0094  | NS2_Q7[7:0]     |    |    |    |                 |    |             |    |
| 0095  | Rsvd            |    |    |    | NFRAC_Q2[27:24] |    |             |    |
| 0096  | NFRAC_Q2[23:16] |    |    |    |                 |    |             |    |
| 0097  | NFRAC_Q2[15:8]  |    |    |    |                 |    |             |    |
| 0098  | NFRAC_Q2[7:0]   |    |    |    |                 |    |             |    |
| 0099  | Rsvd            |    |    |    | NFRAC_Q3[27:24] |    |             |    |
| 009A  | NFRAC_Q3[23:16] |    |    |    |                 |    |             |    |
| 009B  | NFRAC_Q3[15:8]  |    |    |    |                 |    |             |    |
| 009C  | NFRAC_Q3[7:0]   |    |    |    |                 |    |             |    |

| Output Divider Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| NS1_Qm[1:0]<br>(m = 0,1)                                 | R/W        | 10b           | 1st Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1):<br>00 = /5<br>01 = /6<br>10 = /4<br>11 = Output Qm, nQm not switching   |
| NS1_Qm[1:0]<br>(m = 4, 5, 6, 7)                          | R/W        | 10b           | 1st Stage Output Divider Ratio for Output Clock Qm, nQm (m = 4, 5, 6, 7):<br>00 = /5<br>01 = /6<br>10 = /4<br>11 = /1 (Do not use this selection if PLL0 or PLL1 are the source since the 2nd-stage divider has a limit of 1GHz). |
| NS2_Qm[15:0]   | R/W        | 0002h         | 2nd Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 4, 5, 6, 7):<br>Actual divider ratio is 2x the value written here.<br>A value of 0 in this register will bypass the second stage of the divider.               |
| N_Qm[17:0]   | R/W        | 00008h        | Integer Portion of Output Divider Ratio for Output Clock Qm, nQm (m = 2, 3):<br>Values of 0, 1 or 2 cannot be written to this register. Actual integer portion is 2x the value written here.                                      |
| NFRAC_Qm[27:0]   | R/W        | 0000000h      | Fractional Portion of Output Divider Ratio for Output Clock Qm, nQm (m = 2, 3):<br>Actual fractional portion is 2x the value written here.<br>Fraction = (NFRAC_Qm * 2) * 2 <sup>-28</sup>  |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7L. Output Clock Phase Adjustment Control Register Bit Field Locations and Descriptions**

| Output Clock Phase Adjustment Control Control Register Block Field Locations |               |      |    |    |    |              |    |    |
|--|---------------|------|----|----|----|--------------|----|----|
| Address (Hex)  | D7            | D6   | D5 | D4 | D3 | D2           | D1 | D0 |
| 009D   | CRSE_TRG[7:0] |      |    |    |    |              |    |    |
| 009E   |               | Rsvd |    |    |    | COARSE0[4:0] |    |    |
| 009F   |               | Rsvd |    |    |    | COARSE1[4:0] |    |    |
| 00A0   |               | Rsvd |    |    |    | COARSE2[4:0] |    |    |
| 00A1   |               | Rsvd |    |    |    | COARSE3[4:0] |    |    |
| 00A2   |               | Rsvd |    |    |    | COARSE4[4:0] |    |    |
| 00A3   |               | Rsvd |    |    |    | COARSE5[4:0] |    |    |
| 00A4   |               | Rsvd |    |    |    | COARSE6[4:0] |    |    |
| 00A5   |               | Rsvd |    |    |    | COARSE7[4:0] |    |    |
| 00A6   |               | Rsvd |    |    |    | FINE2[3:0]   |    |    |
| 00A7   |               | Rsvd |    |    |    | FINE3[3:0]   |    |    |

| Output Clock Phase Adjustment Control Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| CRSE_TRG[7:0]   | R/W        | 00h           | Trigger Coarse Phase Adjustment for output Qm, nQm by amount specified in COARSEm[4:0] register upon 0→1 transition of this Trigger register bit. Please ensure the PA_BUSYm status bit is 0 before triggering another adjustment cycle on that particular output. Trigger bit must be returned to 0 before another delay cycle can be triggered.   |
| COARSEm[4:0]  | R/W        | 00000b        | Number of periods to be inserted when Trigger happens. Relevant clock period is determined by the clock source selected for output Qm, nQm in its CLK_SELm register field.  |
| FINEm[3:0]  | R/W        | 0000b         | Number of 1/16ths of the relevant clock period to add to the phase of output Qm, nQm (m = 2, 3). Relevant clock period is determined by the clock source selected for output Qm, nQm in its CLK_SELm register field. The PLLn_SYN bit for the PLL driving the output divider for the output in question must be toggled to make this value take effect. Note that toggling the PLLn_SYN bit will clear all Coarse delay values and so Fine delay should be set first. |
| Rsvd  | R/W        | -             | Always write a 0 to this bit location. Read values are not defined.   |

**Table 7M. Output Clock Source Control Register Bit Field Locations and Descriptions**

| Output Clock Source Control Register Block Field Locations |      |               |          |          |          |               |          |          |
|--|------|---------------|----------|----------|----------|---------------|----------|----------|
| Address (Hex)  | D7   | D6            | D5       | D4       | D3       | D2            | D1       | D0       |
| 00A8   | Rsvd |               | PLL1_SYN | PLL0_SYN | CLK_SEL3 | CLK_SEL2      | CLK_SEL1 | CLK_SEL0 |
| 00A9   | Rsvd | CLK_SEL5[2:0] |          |          | Rsvd     | CLK_SEL4[2:0] |          |          |
| 00AA   | Rsvd | CLK_SEL7[2:0] |          |          | Rsvd     | CLK_SEL6[2:0] |          |          |
| 00AB   | 10   |               | 10       |          | Rsvd     |               | Rsvd     |          |

| Output Clock Source Control Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| PLL1_SYN  | R/W        | 0b            | Output Synchronization Control for Outputs Derived from PLL1.<br>Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset.<br>Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0. |
| PLL0_SYN  | R/W        | 0b            | Output Synchronization Control for Outputs Derived from PLL0.<br>Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset.<br>Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0. |
| CLK_SEL0  | R/W        | 0b            | Clock Source Selection for output Q0, nQ0:<br>0 = PLL0<br>1 = PLL1  |
| CLK_SEL1  | R/W        | 1b            | Clock Source Selection for output Q1, nQ1:<br>0 = PLL0<br>1 = PLL1  |
| CLK_SEL2  | R/W        | 0b            | Clock Source Selection for output Q2, nQ2:<br>0 = PLL0<br>1 = PLL1  |
| CLK_SEL3  | R/W        | 1b            | Clock Source Selection for output Q3, nQ3:<br>0 = PLL0<br>1 = PLL1  |
| CLK_SEL4[2:0]   | R/W        | 000b          | Clock Source Selection for output Q4, nQ4. Do not select Input Reference 0, 1 or 2 if that input is faster than 250MHz:<br>000 = PLL0<br>001 = PLL1<br>010 = Output Q2, nQ2<br>011 = Output Q3, nQ3<br>100 = Input Reference 0 (CLK0)<br>101 = Input Reference 1 (CLK1)<br>110 = Input Reference 2 (CLK2)<br>111 = Crystal Input                              |
| CLK_SEL5[2:0]   | R/W        | 010b          | Clock Source Selection for output Q5, nQ5. Do not select Input Reference 0, 1 or 2 if that input is faster than 250MHz:<br>000 = PLL0<br>001 = PLL1<br>010 = Output Q2, nQ2<br>011 = Output Q3, nQ3<br>100 = Input Reference 0 (CLK0)<br>101 = Input Reference 1 (CLK1)<br>110 = Input Reference 2 (CLK2)<br>111 = Crystal Input                              |



**Output Clock Source Control Register Block Field Descriptions**

| Bit Field Name | Field Type | Default Value | Description  |
|----------------|------------|---------------|--|
| CLK_SEL6[2:0]  | R/W        | 110b          | Clock Source Selection for output Q6, nQ6. Do not select Input Reference 0, 1 or 2 if that input is faster than 250MHz:<br>000 = PLL0<br>001 = PLL1<br>010 = Output Q2, nQ2<br>011 = Output Q3, nQ3<br>100 = Input Reference 0 (CLK0)<br>101 = Input Reference 1 (CLK1)<br>110 = Input Reference 2 (CLK2)<br>111 = Crystal Input |
| CLK_SEL7[2:0]  | R/W        | 101b          | Clock Source Selection for output Q7, nQ7. Do not select Input Reference 0, 1 or 2 if that input is faster than 250MHz:<br>000 = PLL0<br>001 = PLL1<br>010 = Output Q2, nQ2<br>011 = Output Q3, nQ3<br>100 = Input Reference 0 (CLK0)<br>101 = Input Reference 1 (CLK1)<br>110 = Input Reference 2 (CLK2)<br>111 = Crystal Input |
| Rsvd           | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.  |

**Table 7N. Analog PLL0 Control Register Bit Field Locations and Descriptions**

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

| Analog PLL0 Control Register Block Field Locations |              |    |          |              |               |           |         |         |
|--|--------------|----|----------|--------------|---------------|-----------|---------|---------|
| Address (Hex)                                      | D7           | D6 | D5       | D4           | D3            | D2        | D1      | D0      |
| 00AC   | CPSET_0[2:0] |    |          | RS_0[1:0]    |               | CP_0[1:0] |         | WPOST_0 |
| 00AD   | Rsvd         |    |          |              | SYN_MODE<br>0 | Rsvd      | DLCNT_0 | DBITM_0 |
| 00AE   | Rsvd         |    | VCOMAN_0 | DBIT1_0[4:0] |               |           |         |         |
| 00AF   | Rsvd         |    |          | DBIT2_0[4:0] |               |           |         |         |

| Analog PLL0 Control Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| CPSET_0[2:0]  | R/W        | 100b          | Charge Pump Current Setting for Analog PLL0:<br>000 = 110µA<br>001 = 220µA<br>010 = 330µA<br>011 = 440µA<br>100 = 550µA<br>101 = 660µA<br>110 = 770µA<br>111 = 880µA  |
| RS_0[1:0]   | R/W        | 01b           | Internal Loop Filter Series Resistor Setting for Analog PLL0:<br>00 = 330Ω<br>01 = 640Ω<br>10 = 1.2kΩ<br>11 = 1.79kΩ  |
| CP_0[1:0]   | R/W        | 01b           | Internal Loop Filter Parallel Capacitor Setting for Analog PLL0:<br>00 = 40pF<br>01 = 80pF<br>10 = 140pF<br>11 = 200pF  |
| WPOST_0   | R/W        | 1b            | Internal Loop Filter 2nd Pole Setting for Analog PLL0:<br>0 = Rpost = 497Ω, Cpost = 40pF<br>1 = Rpost = 1.58kΩ, Cpost = 40pF  |
| DLCNT_0   | R/W        | 1b            | Digital Lock Count Setting for Analog PLL0. Set to 0 if external capacitor (CAP0) for PLL0 is >95nF, otherwise set to 1:<br>0 = 1 ppm accuracy<br>1 = 16 ppm accuracy   |
| DBITM_0   | R/W        | 0b            | Digital Lock Manual Override Setting for Analog PLL0:<br>0 = Automatic Mode<br>1 = Manual Mode  |
| VCOMAN_0  | R/W        | 1b            | Manual Lock Mode VCO Selection Setting for Analog PLL0:<br>0 = VCO2<br>1 = VCO1   |
| DBIT1_0[4:0]  | R/W        | 01011b        | Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL0.   |
| DBIT2_0[4:0]  | R/W        | 00000b        | Manual Mode Digital Lock Control Setting for VCO2 in Analog PLL0.   |
| SYN_MODE0   | R/W        | 0b            | Frequency Synthesizer Mode Control for PLL0:<br>0 = PLL0 jitter attenuates and translates one or more input references<br>1 = PLL0 synthesizes output frequencies using only the crystal as a reference<br>Note that the STATE0[1:0] field in the Digital PLL0 Control Register must be set to Force Freerun state. |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 70. Analog PLL1 Control Register Bit Field Locations and Descriptions**

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

| Analog PLL1 Control Register Block Field Locations |              |    |          |              |               |           |         |         |
|--|--------------|----|----------|--------------|---------------|-----------|---------|---------|
| Address (Hex)                                      | D7           | D6 | D5       | D4           | D3            | D2        | D1      | D0      |
| 00B0   | CPSET_1[2:0] |    |          | RS_1[1:0]    |               | CP_1[1:0] |         | WPOST_1 |
| 00B1   | Rsvd         |    |          |              | SYN_MODE<br>1 | Rsvd      | DLCNT_1 | DBITM_1 |
| 00B2   | Rsvd         |    | VCOMAN_1 | DBIT1_1[4:0] |               |           |         |         |
| 00B3   | Rsvd         |    |          | DBIT2_1[4:0] |               |           |         |         |

| Analog PLL1 Control Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| CPSET_1[2:0]  | R/W        | 100b          | Charge Pump Current Setting for Analog PLL1:<br>000 = 110 $\mu$ A<br>001 = 220 $\mu$ A<br>010 = 330 $\mu$ A<br>011 = 440 $\mu$ A<br>100 = 550 $\mu$ A<br>101 = 660 $\mu$ A<br>110 = 770 $\mu$ A<br>111 = 880 $\mu$ A  |
| RS_1[1:0]   | R/W        | 01b           | Internal Loop Filter Series Resistor Setting for Analog PLL1:<br>00 = 330 $\Omega$<br>01 = 640 $\Omega$<br>10 = 1.2 k $\Omega$<br>11 = 1.79 k $\Omega$  |
| CP_1[1:0]   | R/W        | 01b           | Internal Loop Filter Parallel Capacitor Setting for Analog PLL1:<br>00 - 40 pF<br>01 = 80 pF<br>10 = 140 pF<br>11 = 200 pF  |
| WPOST_1   | R/W        | 1b            | Internal Loop Filter 2nd Pole Setting for Analog PLL1:<br>0 = Rpost = 497 $\Omega$ , Cpost = 40pF<br>1 = Rpost = 1.58 k $\Omega$ , Cpost = 40pF   |
| DLCNT_1   | R/W        | 1b            | Digital Lock Count Setting for Analog PLL1: Set to 0 if external capacitor (CAP1) for PLL1 is >95nF, otherwise set to 1:<br>0 = 1 ppm accuracy<br>1 = 16 ppm accuracy   |
| DBITM_1   | R/W        | 0b            | Digital Lock Manual Override Setting for Analog PLL1:<br>0 = Automatic Mode<br>1 = Manual Mode  |
| VCOMAN_1  | R/W        | 1b            | Manual Lock Mode VCO Selection Setting for Analog PLL1:<br>0 = VCO2<br>1 = VCO1   |
| DBIT1_1[4:0]  | R/W        | 01011b        | Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL1:   |
| DBIT2_1[4:0]  | R/W        | 00000b        | Manual Mode Digital Lock Control Setting for VCO2 in Analog PLL1.   |
| SYN_MODE1   | R/W        | 0b            | Frequency Synthesizer Mode Control for PLL1:<br>0 = PLL1 jitter attenuates and translates one or more input references.<br>1 = PLL1 synthesizes output frequencies using only the crystal as a reference.<br>Note that the STATE1[1:0] field in the Digital PLL1 Control Register must be set to Force Freerun state. |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7P. Power Down Control Register Bit Field Locations and Descriptions**

| Power Down Control Register Block Field Locations |        |        |        |          |           |           |          |          |
|---|--------|--------|--------|----------|-----------|-----------|----------|----------|
| Address (Hex)                                     | D7     | D6     | D5     | D4       | D3        | D2        | D1       | D0       |
| 00B4  | Rsvd   |        |        |          |           |           |          | DBL_DIS  |
| 00B5  | Rsvd   |        |        |          | CLK3_DIS  | CLK2_DIS  | CLK1_DIS | CLK0_DIS |
| 00B6  | Rsvd   |        |        | PLL1_DIS | Rsvd      |           |          |          |
| 00B7  | Q7_DIS | Q6_DIS | Q5_DIS | Q4_DIS   | Q3_DIS    | Q2_DIS    | Q1_DIS   | Q0_DIS   |
| 00B8  | Rsvd   |        |        |          | DPLL1_DIS | DPLL0_DIS | CALRST1  | CALRST0  |

| Power Down Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name                                       | Field Type | Default Value | Description   |
| DBL_DIS  | R/W        | 0b            | Controls whether Crystal Input Frequency is doubled before being used in PLL0 or PLL1:<br>0 = 2x Actual Crystal Frequency Used<br>1 = Actual Crystal Frequency Used       |
| CLKm_DIS   | R/W        | 0b            | Disable Control for Input Reference m:<br>0 = Input Reference m is Enabled<br>1 = Input Reference m is Disabled   |
| PLL1_DIS   | R/W        | 0b            | Disable Control for Analog PLL1:<br>0 = PLL1 Enabled<br>1 = Analog PLL1 Disabled  |
| Qm_DIS   | R/W        | 0b            | Disable Control for Output Qm, nQm:<br>0 = Output Qm, nQm functions normally<br>1 = All logic associated with Output Qm, nQm is Disabled & Driver in High-Impedance state |
| DPLLm_DIS  | R/W        | 0b            | Disable Control for Digital PLLm:<br>0 = Digital PLLm Enabled<br>1 = Digital PLLm Disabled  |
| CALRSTm  | R/W        | 0b            | Reset Calibration Logic for Analog PLLm:<br>0 = Calibration Logic for Analog PLLm Enabled<br>1 = Calibration Logic for Analog PLLm Disabled                               |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7Q. Input Monitor Control Register Bit Field Locations and Descriptions**

| Input Monitor Control Register Block Field Locations |             |    |    |    |    |    |    |           |
|--|-------------|----|----|----|----|----|----|-----------|
| Address (Hex)  | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0        |
| 00B9   | Rsvd        |    |    |    |    |    |    | LOS_0[16] |
| 00BA   | LOS_0[15:8] |    |    |    |    |    |    |           |
| 00BB   | LOS_0[7:0]  |    |    |    |    |    |    |           |
| 00BC   | Rsvd        |    |    |    |    |    |    | LOS_1[16] |
| 00BD   | LOS_1[15:8] |    |    |    |    |    |    |           |
| 00BE   | LOS_1[7:0]  |    |    |    |    |    |    |           |
| 00BF   | Rsvd        |    |    |    |    |    |    | LOS_2[16] |
| 00C0   | LOS_2[15:8] |    |    |    |    |    |    |           |
| 00C1   | LOS_2[7:0]  |    |    |    |    |    |    |           |
| 00C2   | Rsvd        |    |    |    |    |    |    | LOS_3[16] |
| 00C3   | LOS_3[15:8] |    |    |    |    |    |    |           |
| 00C4   | LOS_3[7:0]  |    |    |    |    |    |    |           |
| 00C5   | Rsvd        |    |    |    |    |    |    |           |
| 00C6   | Rsvd        |    |    |    |    |    |    |           |

| Input Monitor Control Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name  | Field Type | Default Value | Description  |
| LOS_m[16:0]   | R/W        | 1FFFFh        | Number of Input Monitoring clock periods before Input Reference m is considered to be missed (soft alarm). Minimum setting is 3. |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.  |

**Table 7R. Interrupt Enable Control Register Bit Field Locations and Descriptions**

| Interrupt Enable Control Register Block Field Locations |         |         |          |          |         |         |         |         |
|---|---------|---------|----------|----------|---------|---------|---------|---------|
| Address (Hex)   | D7      | D6      | D5       | D4       | D3      | D2      | D1      | D0      |
| 00C7  | LOL1_EN | LOLO_EN | HOLD1_EN | HOLD0_EN | LOS3_EN | LOS2_EN | LOS1_EN | LOS0_EN |
| 00C8  | Rsvd    |         |          |          |         |         |         |         |

| Interrupt Enable Control Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| LOLm_EN  | R/W        | 0b            | Interrupt Enable Control for Loss-of-Lock Interrupt Status Bit for PLLm:<br>0 = LOLm_INT register bit will not affect status of nINT output signal<br>1 = LOLm_INT register bit will affect status of nINT output signal                |
| HOLDm_EN   | R/W        | 0b            | Interrupt Enable Control for Holdover Interrupt Status Bit for PLLm:<br>0 = HOLDm_INT register bit will not affect status of nINT output signal<br>1 = HOLDm_INT register bit will affect status of nINT output signal                  |
| LOSm_EN  | R/W        | 0b            | Interrupt Enable Control for Loss-of-Signal Interrupt Status Bit for Input Reference m:<br>0 = LOSm_INT register bit will not affect status of nINT output signal<br>1 = LOSm_INT register bit will affect status of nINT output signal |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7S. Interrupt Status Register Bit Field Locations and Descriptions**

This register contains 'sticky' bits for tracking the status of the various alarms. Whenever an alarm occurs, the appropriate Interrupt Status bit will be set. The Interrupt Status bit will remain asserted even after the original alarm goes away. The Interrupt Status bits remain

asserted until explicitly cleared by a write of a '1' to the bit over the serial port. This type of functionality is referred to as Read / Write-1-to-Clear (R/W1C).

| Interrupt Status Register Block Field Locations |          |          |           |           |          |          |          |          |
|---|----------|----------|-----------|-----------|----------|----------|----------|----------|
| Address (Hex)                                   | D7       | D6       | D5        | D4        | D3       | D2       | D1       | D0       |
| 0200  | LOL1_INT | LOL0_INT | HOLD1_INT | HOLD0_INT | LOS3_INT | LOS2_INT | LOS1_INT | LOS0_INT |
| 0201  | Rsvd     |          |           |           |          |          |          |          |
| 0202  | Rsvd     |          |           |           |          |          |          |          |
| 0203  | Rsvd     |          |           |           |          |          |          |          |

| Interrupt Status Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name                                     | Field Type | Default Value | Description   |
| LOLm_INT   | R/W1C      | 0b            | Interrupt Status Bit for Loss-of-Lock on PLLm:<br>0 = No Loss-of-Lock alarm flag on PLLm has occurred since the last time this register bit was cleared.<br>1 = At least one Loss-of-Lock alarm flag on PLLm has occurred since the last time this register bit was cleared.  |
| HOLDm_INT  | R/W1C      | 0b            | Interrupt Status Bit for Holdover on PLLm:<br>0 = No Holdover alarm flag on PLLm has occurred since the last time this register bit was cleared.<br>1 = At least one Holdover alarm flag on PLLm has occurred since the last time this register bit was cleared.  |
| LOSm_INT   | R/W1C      | 0b            | Interrupt Status Bit for Loss-of-Signal on Input Reference m:<br>0 = No Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared.<br>1 = At least one Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared. |
| Rsvd   | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

**Table 7T. Output Phase Adjustment Status Register Bit Field Locations and Descriptions**

| Output Phase Adjustment Status Register Block Field Locations |          |          |          |          |          |          |          |          |
|---|----------|----------|----------|----------|----------|----------|----------|----------|
| Address (Hex)   | D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0       |
| 0204  | PA_BUSY7 | PA_BUSY6 | PA_BUSY5 | PA_BUSY4 | PA_BUSY3 | PA_BUSY2 | PA_BUSY1 | PA_BUSY0 |

| Output Phase Adjustment Status Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| PA_BUSYm   | R/O        | -             | Phase Adjustment Event Status for output Qm, nQm:<br>0 = No phase adjustment is currently in progress on output Qm, nQm<br>1 = Phase adjustment still in progress on output Qm, nQm. Do not initiate any new phase adjustment at this time. |

**Table 7U. Digital PLL0 Status Register Bit Field Locations and Descriptions**

| Digital PLL0 Status Register Block Field Locations |    |      |    |         |      |      |                |      |
|--|----|------|----|---------|------|------|----------------|------|
| Address (Hex)                                      | D7 | D6   | D5 | D4      | D3   | D2   | D1             | D0   |
| 0205   |    | Rsvd |    | EXTLOS0 | Rsvd |      | CURR_REF0[2:0] |      |
| 0206   |    | Rsvd |    | Rsvd    | Rsvd | Rsvd |                | Rsvd |
| 0207   |    |      |    | Rsvd    |      |      |                | Rsvd |
| 0208   |    |      |    |         | Rsvd |      |                |      |
| 0209   |    |      |    |         | Rsvd |      |                |      |
| 020A   |    |      |    | Rsvd    |      |      |                | Rsvd |
| 020B   |    |      |    |         | Rsvd |      |                |      |
| 020C   |    |      |    |         | Rsvd |      |                |      |
| 020D   |    |      |    |         | Rsvd |      |                |      |
| 020E   |    |      |    |         | Rsvd |      |                |      |

| Digital PLL0 Status Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name  | Field Type | Default Value | Description  |
| CURR_REF0[2:0]  | R/O        | -             | Currently Selected Reference Status for Digital PLL0:<br>000 - 011 = No reference currently selected<br>100 = Input Reference 0 (CLK0, nCLK0) selected<br>101 = Input Reference 1 (CLK1, nCLK1) selected<br>110 = Input Reference 2 (CLK2, nCLK2) selected<br>111 = Input Reference 3 (CLK3, nCLK3) selected |
| EXTLOS0   | R/O        | -             | External Loopback signal lost for PLL0:<br>0 = PLL0 has a valid feedback reference signal<br>1 = PLL0 has lost the external feedback reference signal and is no longer locked  |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.  |

**Table 7V. Digital PLL1 Status Register Bit Field Locations and Descriptions**

| Digital PLL1 Status Register Block Field Locations |    |      |    |         |      |      |                |      |
|--|----|------|----|---------|------|------|----------------|------|
| Address (Hex)                                      | D7 | D6   | D5 | D4      | D3   | D2   | D1             | D0   |
| 020F   |    | Rsvd |    | EXTLOS1 | Rsvd |      | CURR_REF1[2:0] |      |
| 0210   |    | Rsvd |    | Rsvd    | Rsvd | Rsvd | Rsvd           |      |
| 0211   |    | Rsvd |    |         |      |      |                | Rsvd |
| 0212   |    | Rsvd |    |         |      |      |                |      |
| 0213   |    | Rsvd |    |         |      |      |                |      |
| 0214   |    | Rsvd |    |         |      |      |                | Rsvd |
| 0215   |    | Rsvd |    |         |      |      |                |      |
| 0216   |    | Rsvd |    |         |      |      |                |      |
| 0217   |    | Rsvd |    |         |      |      |                |      |
| 0218   |    | Rsvd |    |         |      |      |                |      |

| Digital PLL1 Status Register Block Field Descriptions |            |               |  |
|---|------------|---------------|--|
| Bit Field Name  | Field Type | Default Value | Description  |
| CURR_REF1[2:0]  | R/O        | -             | Currently Selected Reference Status for Digital PLL1:<br>000 - 011 = No reference currently selected<br>100 = Input Reference 0 (CLK0, nCLK0) selected<br>101 = Input Reference 1 (CLK1, nCLK1) selected<br>110 = Input Reference 2 (CLK2, nCLK2) selected<br>111 = Input Reference 3 (CLK3, nCLK3) selected |
| EXTLOS1   | R/O        | -             | External Loopback signal lost for PLL1<br>0 = PLL1 has a valid feedback reference signal<br>1 = PLL1 has lost the external feedback reference signal and is no longer locked   |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.  |

**Table 7W. General Purpose Input Status Register Bit Field Locations and Descriptions**

| Global Interrupt Status Register Block Field Locations |        |        |        |        |        |        |        |        |
|--|--------|--------|--------|--------|--------|--------|--------|--------|
| Address (Hex)  | D7     | D6     | D5     | D4     | D3     | D2     | D1     | D0     |
| 0219   | GPI[7] | GPI[6] | GPI[5] | GPI[4] | GPI[3] | GPI[2] | GPI[1] | GPI[0] |

| General Purpose Input Status Register Block Field Descriptions |            |               |   |
|--|------------|---------------|---|
| Bit Field Name   | Field Type | Default Value | Description   |
| GPI[7:0]   | R/O        | -             | Shows current values on GPIO[7:0] pins that are configured as General-Purpose Inputs. |



**Table 7X. Global Interrupt Status Register Bit Field Locations and Descriptions**

| Global Interrupt Status Register Block Field Locations |      |      |      |      |          |      |      |          |
|--|------|------|------|------|----------|------|------|----------|
| Address (Hex)  | D7   | D6   | D5   | D4   | D3       | D2   | D1   | D0       |
| 021A   | Rsvd |      |      | Rsvd |          |      | INT  |          |
| 021B   | Rsvd |      |      |      |          |      |      |          |
| 021C   | Rsvd |      | Rsvd |      |          |      |      |          |
| 021D   | Rsvd |      | Rsvd |      |          |      |      |          |
| 021E   | Rsvd |      |      |      | Rsvd     |      | Rsvd | BOOTFAIL |
| 021F   | Rsvd | Rsvd | Rsvd | Rsvd | nEEP_CRC | Rsvd | Rsvd | EEPDONE  |

| Global Interrupt Status Register Block Field Descriptions |            |               |   |
|---|------------|---------------|---|
| Bit Field Name  | Field Type | Default Value | Description   |
| INT   | R/O        | -             | Device Interrupt Status:<br>0 = No Interrupt Status bits that are enabled are asserted (nINT pin released)<br>1 = At least one Interrupt Status bit that is enabled is asserted (nINT pin asserted low) |
| BOOTFAIL  | R/O        | -             | Reading of Serial EEPROM failed. Once set this bit is only cleared by reset.  |
| nEEP_CRC  | R/O        | -             | EEPROM CRC Error (Active Low):<br>0 = EEPROM was detected and read, but CRC check failed - please reset the device via the nRST pin to retry (serial port is locked)<br>1 = No EEPROM CRC Error         |
| EEPDONE   | R/O        | -             | Serial EEPROM Read cycle has completed. Once set this bit is only cleared by reset.   |
| Rsvd  | R/W        | -             | Reserved. Always write 0 to this bit location. Read values are not defined.   |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                               |
|--|--------------------------------------|
| Supply Voltage, $V_{CC}$   | 3.63V                                |
| Inputs, $V_I$<br>OSCI<br>Other Input   | 0V to 2V<br>-0.5V to $V_{CC} + 0.5V$ |
| Outputs, $V_O$ (Q[0:7], nQ[0:7])   | -0.5V to $V_{CCOX} + 0.5V$           |
| Outputs, $V_O$ (GPIO[0:7], SDATA, SCLK, nINT)  | -0.5V to $V_{CC} + 0.5V$             |
| Outputs, $I_O$ (Q[0:7], nQ[0:7])<br>Continuous Current<br>Surge Current              | 40mA<br>65mA                         |
| Outputs, $I_O$ (GPIO[0:7], SDATA, SCLK, nINT)<br>Continuous Current<br>Surge Current | 8mA<br>13mA                          |
| Junction Temperature, $T_J$  | 125°C                                |
| Storage Temperature, $T_{STG}$   | -65°C to 150°C                       |

NOTE:  $V_{CCOX}$  denotes  $V_{CC0}$ ,  $V_{CC1}$ ,  $V_{CC2}$ ,  $V_{CC3}$ ,  $V_{CC4}$ ,  $V_{CC5}$ ,  $V_{CC6}$ ,  $V_{CC7}$ .

## Supply Voltage Characteristics

**Table 8A. Power Supply Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol    | Parameter  | Test Conditions   | Minimum         | Typical | Maximum  | Units |
|-----------|--|---|-----------------|---------|----------|-------|
| $V_{CC}$  | Core Supply Voltage                              |   | 3.135           | 3.3     | 3.465    | V     |
| $V_{CCA}$ | Analog Supply Voltage                            |   | $V_{CC} - 0.13$ | 3.3     | $V_{CC}$ | V     |
| $I_{CC}$  | Core Supply Current;<br><a href="#">NOTE 1</a>   |   |                 | 82      | 100      | mA    |
| $I_{CCA}$ | Analog Supply Current;<br><a href="#">NOTE 1</a> | PLL0 and PLL1 Enabled   |                 | 207     | 265      | mA    |
|           |  | Analog PLL1, Digital PLL1, and Calibration Logic for Analog PLL1 Disabled |                 | 121     | 187      | mA    |
| $I_{EE}$  | Power Supply Current;<br><a href="#">NOTE 2</a>  | Q[0:7] Configured for LVPECL Logic Levels;<br>Outputs Unloaded            |                 | 575     | 735      | mA    |

NOTE 1:  $I_{CC}$  and  $I_{CCA}$  are included in  $I_{EE}$  when Q[0:7] configured for LVPECL logic levels.

NOTE 2: Internal dynamic switching current at maximum  $f_{OUT}$  is included.

**Table 8B. Power Supply Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol    | Parameter  | Test Conditions   | Minimum         | Typical | Maximum  | Units |
|-----------|--|---|-----------------|---------|----------|-------|
| $V_{CC}$  | Core Supply Voltage                              |   | 2.375           | 2.5     | 2.625    | V     |
| $V_{CCA}$ | Analog Supply Voltage                            |   | $V_{CC} - 0.13$ | 2.5     | $V_{CC}$ | V     |
| $I_{CC}$  | Core Supply Current;<br><a href="#">NOTE 1</a>   |   |                 | 79      | 95       | mA    |
| $I_{CCA}$ | Analog Supply Current;<br><a href="#">NOTE 1</a> | PLL0 and PLL1 enabled   |                 | 201     | 260      | mA    |
|           |  | Analog PLL1, Digital PLL1, and Calibration Logic for Analog PLL1 Disabled |                 | 116     | 182      | mA    |
| $I_{EE}$  | Power Supply Current;<br><a href="#">NOTE 2</a>  | Q[0:7] Configured for LVPECL Logic Levels; Outputs Unloaded               |                 | 544     | 695      | mA    |

NOTE 1:  $I_{CC}$  and  $I_{CCA}$  are included in  $I_{EE}$  when Q[0:7] configured for LVPECL logic levels.

NOTE 2: Internal dynamic switching current at maximum  $f_{OUT}$  is included.

**Table 8C. Maximum Output Supply Current,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol     | Parameter                     | Test Conditions  | $V_{CCox} = 3.3V \pm 5\%$ |      |         | $V_{CCox} = 2.5V \pm 5\%$ |      |         | $V_{CCox} = 1.8V \pm 5\%$ | Units |
|------------|-------------------------------|------------------|---------------------------|------|---------|---------------------------|------|---------|---------------------------|-------|
|            |                               |                  | LVPECL                    | LVDS | LVC MOS | LVPECL                    | LVDS | LVC MOS | LVC MOS                   |       |
| $I_{CC00}$ | Q0, nQ0 Output Supply Current | Outputs Unloaded | 50                        | 60   | 55      | 40                        | 50   | 45      | 35                        | mA    |
| $I_{CC01}$ | Q1, nQ1 Output Supply Current | Outputs Unloaded | 50                        | 60   | 55      | 40                        | 50   | 45      | 35                        | mA    |
| $I_{CC02}$ | Q2, nQ2 Output Supply Current | Outputs Unloaded | 80                        | 90   | 80      | 70                        | 80   | 70      | 60                        | mA    |
| $I_{CC03}$ | Q3, nQ3 Output Supply Current | Outputs Unloaded | 80                        | 90   | 80      | 70                        | 80   | 70      | 60                        | mA    |
| $I_{CC04}$ | Q4, nQ4 Output Supply Current | Outputs Unloaded | 55                        | 65   | 55      | 45                        | 55   | 45      | 40                        | mA    |
| $I_{CC05}$ | Q5, nQ5 Output Supply Current | Outputs Unloaded | 55                        | 65   | 55      | 45                        | 55   | 45      | 40                        | mA    |
| $I_{CC06}$ | Q6, nQ6 Output Supply Current | Outputs Unloaded | 55                        | 65   | 55      | 45                        | 55   | 45      | 40                        | mA    |
| $I_{CC07}$ | Q7, nQ7 Output Supply Current | Outputs Unloaded | 55                        | 65   | 55      | 45                        | 55   | 45      | 40                        | mA    |

NOTE:  $V_{CCox}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Internal dynamic switching current at maximum  $f_{OUT}$  is included.

## DC Electrical Characteristics

**Table 9A. LVCMOS/LVTTL DC Characteristics,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol   | Parameter           |   | Test Conditions  | Minimum | Typical | Maximum        | Units   |
|----------|---------------------|---|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage  |   | $V_{CC} = 3.3V$  | 2       |         | $V_{CC} + 0.3$ | V       |
|          |                     |   | $V_{CC} = 2.5V$  | 1.7     |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage   |   | $V_{CC} = 3.3V$  | -0.3    |         | 0.8            | V       |
|          |                     |   | $V_{CC} = 2.5V$  | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current  | nI2C_SPI, PLL_BYP, S_A0/nCS, S_A1/SDI     | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$                     |         |         | 150            | $\mu A$ |
|          |                     | nRST, SDATA/SDO, nWP, SCLK/SCLK           | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$                     |         |         | 5              | $\mu A$ |
|          |                     | GPIO[7:0]                                 | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$                     |         |         | 1              | mA      |
| $I_{IL}$ | Input Low Current   | nI2C_SPI, PLL_BYP, S_A0/nCS, S_A1/SDI     | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$              | -5      |         |                | $\mu A$ |
|          |                     | nRST, SDATA/SDO, nWP, SCLK/SCLK           | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$              | -150    |         |                | $\mu A$ |
|          |                     | GPIO[7:0]                                 | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$              | -1      |         |                | mA      |
| $V_{OH}$ | Output High Voltage | nINT, SDATA/SDO, SCLK/SCLK; <b>NOTE 1</b> | $V_{CC} = 3.3V \pm 5\%$ , $I_{OH} = -5\mu A$               | 2.6     |         |                | V       |
|          |                     | GPIO[7:0]                                 | $V_{CC} = 3.3V \pm 5\%$ , $I_{OH} = -50\mu A$              | 2.6     |         |                | V       |
|          |                     | nINT, SDATA/SDO, SCLK/SCLK; <b>NOTE 1</b> | $V_{CC} = 2.5V \pm 5\%$ , $I_{OH} = -5\mu A$               | 1.8     |         |                | V       |
|          |                     | GPIO[7:0]                                 | $V_{CC} = 2.5V \pm 5\%$ , $I_{OH} = -50\mu A$              | 1.8     |         |                | V       |
| $V_{OL}$ | Output Low Voltage  | nINT, SDATA/SDO, SCLK/SCLK; <b>NOTE 1</b> | $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ , $I_{OL} = 5mA$ |         |         | 0.5            | V       |
|          |                     | GPIO[7:0]                                 | $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$ , $I_{OL} = 5mA$ |         |         | 0.5            | V       |

NOTE 1: Use of external pull-up resistors is recommended.

**Table 9B. Differential Input DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol    | Parameter                                   |             | Test Conditions                               | Minimum  | Typical | Maximum        | Units   |
|-----------|---|-------------|---|----------|---------|----------------|---------|
| $I_{IH}$  | Input High Current                          | CLKx, nCLKx | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$        |          |         | 150            | $\mu A$ |
| $I_{IL}$  | Input Low Current                           | CLKx        | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -5       |         |                | $\mu A$ |
|           |   | nCLKx       | $V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$ | -150     |         |                | $\mu A$ |
| $V_{PP}$  | Peak-to-Peak Voltage; <b>NOTE 1</b>         |             |   | 0.15     |         | 1.3            | V       |
| $V_{CMR}$ | Common Mode Input Voltage; <b>NOTE 1, 2</b> |             |   | $V_{EE}$ |         | $V_{CC} - 1.2$ | V       |

NOTE: CLKx denotes CLK0, CLK1, CLK2, CLK3. nCLKx denotes nCLK0, nCLK1, nCLK2, nCLK3.

NOTE 1:  $V_{IL}$  should not be less than -0.3V.  $V_{IH}$  should not be higher than  $V_{CC}$ .

NOTE 2: Common mode voltage is defined as the cross-point.

**Table 9C. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol   | Parameter                      | Test Conditions | $V_{CC0x} = 3.3V \pm 5\%$ |         |                   | $V_{CC0x} = 2.5V \pm 5\%$ |         |                   | Units |
|----------|--------------------------------|-----------------|---------------------------|---------|-------------------|---------------------------|---------|-------------------|-------|
|          |                                |                 | Minimum                   | Typical | Maximum           | Minimum                   | Typical | Maximum           |       |
| $V_{OH}$ | Output High Voltage;<br>NOTE 1 | Qx, nQx         | $V_{CC0x} - 1.3$          |         | $V_{CC0x} - 0.8$  | $V_{CC0x} - 1.35$         |         | $V_{CC0x} - 0.9$  | V     |
| $V_{OL}$ | Output Low Voltage;<br>NOTE 1  | Qx, nQx         | $V_{CC0x} - 1.95$         |         | $V_{CC0x} - 1.75$ | $V_{CC0x} - 1.95$         |         | $V_{CC0x} - 1.75$ | V     |

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC0x} - 2V$ .

**Table 9D. LVDS DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CC0x} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage | Qx, nQx         | 195     |         | 454     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   | Qx, nQx         |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              | Qx, nQx         | 1.1     |         | 1.375   | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   | Qx, nQx         |         |         | 50      | mV    |

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

NOTE: Terminated  $100\Omega$  across Qx and nQx.

**Table 9E. LVCMOS DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol   | Parameter           | Test Conditions            | $V_{CC0x} = 3.3V \pm 5\%$ |         |         | $V_{CC0x} = 2.5V \pm 5\%$ |         |         | $V_{CC0x} = 1.8V \pm 5\%$ |         |         | Units |
|----------|---------------------|----------------------------|---------------------------|---------|---------|---------------------------|---------|---------|---------------------------|---------|---------|-------|
|          |                     |                            | Minimum                   | Typical | Maximum | Minimum                   | Typical | Maximum | Minimum                   | Typical | Maximum |       |
| $V_{OH}$ | Output High Voltage | Qx, nQx<br>$I_{OH} = -8mA$ | 2.6                       |         |         | 1.8                       |         |         | 1.1                       |         |         | V     |
| $V_{OL}$ | Output Low Voltage  | Qx, nQx<br>$I_{OL} = 8mA$  |                           |         | 0.5     |                           |         | 0.5     |                           |         | 0.5     | V     |

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

**Table 10. Input Frequency Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol     | Parameter                           | Test Conditions            | Minimum | Typical | Maximum | Units |
|------------|-------------------------------------|----------------------------|---------|---------|---------|-------|
| $f_{IN}$   | Input Frequency;<br>NOTE 1          | OSCI, OSCO                 | 10      |         | 40      | MHz   |
|            |                                     | CLKx, nCLKx                | 0.008   |         | 875     | MHz   |
| $f_{SCLK}$ | Serial Port Clock SCLK (slave mode) | I <sup>2</sup> C Operation | 100     |         | 400     | kHz   |
|            |                                     | SPI Operation              |         |         | 4.25    | MHz   |

NOTE: CLKx denotes CLK0, CLK1, CLK2, CLK3. nCLKx denotes nCLK0, nCLK1, nCLK2, nCLK3.

NOTE 1: For the input reference frequency, the divider values must be set for the VCO to operate within its supported range.

**Table 11. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 10          |         | 40      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             | 15      |         | $\Omega$ |
| Load Capacitance ( $C_L$ )         |                 |             | 12      |         | pF       |
| Frequency Stability (total)        |                 | -100        |         | 100     | ppm      |

## AC Electrical Characteristics

**Table 12. AC Characteristics**,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CCOx} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$  (1.8V only supported for LVCMOS outputs),  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol      | Parameter                  | Test Conditions  | Minimum  | Typical            | Maximum | Units |      |
|-------------|----------------------------|--|--|--------------------|---------|-------|------|
| $f_{VCO}$   | VCO Operating Frequency    |  | 3000   |                    | 4000    | MHz   |      |
| $f_{OUT}$   | Output Frequency           | Q0, Q1, Q4, Q5, Q6, Q7 outputs                             | 0.008  |                    | 1000    | MHz   |      |
|             |                            | Q2, Q3 outputs Integer Divide Ratio & No Added Phase Delay | 0.008  |                    | 666.67  | MHz   |      |
|             |                            | Q2, Q3 outputs Non-integer divide and/or added phase delay | 0.008  |                    | 400     | MHz   |      |
|             |                            | LVCMOS   | 0.008  |                    | 250     | MHz   |      |
| $t_R / t_F$ | Output Rise and Fall Times | LVPECL   | 20% to 80%   | 145                | 340     | 600   | ps   |
|             |                            | LVDS   | 20% to 80%   | 100                | 250     | 500   | ps   |
|             |                            | LVCMOS   | 20% to 80%, $V_{CCOx} = 3.3V$                              | 180                | 350     | 600   | ps   |
|             |                            |  | 20% to 80%, $V_{CCOx} = 2.5V$                              | 200                | 350     | 550   | ps   |
| SR          | Output Slew Rate           | LVPECL   | measured on differential waveform, $\pm 150mV$ from center | 1                  |         | 5     | V/ns |
|             |                            | LVDS   | measured on differential waveform, $\pm 150mV$ from center | 0.5                |         | 4     | V/ns |
| $t_{sk(b)}$ | Bank Skew                  | LVPECL   | Q0, nQ0, Q1, nQ1   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            |  | Q4, nQ4, Q5, nQ5   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            |  | Q6, nQ6, Q7, nQ7   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            | LVDS   | Q0, nQ0, Q1, nQ1   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            |  | Q4, nQ4, Q5, nQ5   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            |  | Q6/nQ6, Q7,nQ7   | NOTE 1, 2, 3, 5    |         | 75    | ps   |
|             |                            | LVCMOS   | Q0, nQ0, Q1, nQ1   | NOTE 1, 2, 4, 5, 6 |         | 80    | ps   |
|             |                            |  | Q4, nQ4, Q5, nQ5   | NOTE 1, 2, 4, 5, 6 |         | 115   | ps   |
|             |                            |  | Q6, nQ6, Q7, nQ7   | NOTE 1, 2, 4, 5, 6 |         | 115   | ps   |

| Symbol             | Parameter                                      |                                      | Test Conditions   | Minimum | Typical | Maximum | Units  |
|--------------------|--|--------------------------------------|---|---------|---------|---------|--------|
| odc                | Output Duty Cycle; NOTE 7                      | LVPECL                               | $f_{OUT} \leq 666.667\text{MHz}$  | 45      | 50      | 55      | %      |
|                    |  |                                      | $f_{OUT} > 666.667\text{MHz}$   | 40      | 50      | 60      | %      |
|                    |  | LVDS                                 | $f_{OUT} \leq 666.667\text{MHz}$  | 45      | 50      | 55      | %      |
|                    |  |                                      | $f_{OUT} > 666.667\text{MHz}$   | 40      | 50      | 60      | %      |
|                    |  | LVC MOS                              |   | 40      | 50      | 60      | %      |
|                    | Initial Frequency Offset                       |                                      | Switchover or entering / leaving Holdover state; NOTE 8, 13                                       | -50     |         | 50      | ppb    |
|                    | Output Phase Change in Fully Hitless Switching |                                      | Switchover or entering / leaving Holdover state; NOTE 10, 13                                      |         | 5       |         | ns     |
| $\Phi_{SSB}(1k)$   | Single Sideband Phase Noise; NOTE 9            | 1kHz                                 | 122.88MHz output  |         | -115    |         | dBc/Hz |
| $\Phi_{SSB}(10k)$  |  | 10kHz                                | 122.88MHz output  |         | -129    |         | dBc/Hz |
| $\Phi_{SSB}(100k)$ |  | 100kHz                               | 122.88MHz output  |         | -134    |         | dBc/Hz |
| $\Phi_{SSB}(1M)$   |  | 1MHz                                 | 122.88MHz output  |         | -147    |         | dBc/Hz |
| $\Phi_{SSB}(10M)$  |  | 10MHz                                | 122.88MHz output  |         | -153    |         | dBc/Hz |
| $\Phi_{SSB}(30M)$  |  | $\geq 30\text{MHz}$                  | 122.88MHz output  |         | -154    |         | dBc/Hz |
|                    | Spurious Limit at offset                       | $\geq 800\text{kHz}$                 | 122.88MHz output; NOTE 11   |         | -85     |         | dBc    |
| tstartup           | Startup time                                   | Internal OTP Startup; NOTE 13        | from $V_{CC} > 80\%$ to first output clock edge   |         | 110     | 150     | ms     |
|                    |  | External EEPROM Startup; NOTE 12, 13 | from $V_{CC} > 80\%$ to first output clock edge (0 retries). I <sup>2</sup> C frequency = 100kHz  |         | 150     | 200     | ms     |
|                    |  |                                      | from $V_{CC} > 80\%$ to first output clock edge (0 retries). I <sup>2</sup> C frequency = 400kHz  |         | 130     | 150     | ms     |
|                    |  |                                      | from $V_{CC} > 80\%$ to first output clock edge (31 retries). I <sup>2</sup> C frequency = 100kHz |         | 925     | 1200    | ms     |
|                    |  |                                      | from $V_{CC} > 80\%$ to first output clock edge (31 retries). I <sup>2</sup> C frequency = 400kHz |         | 360     | 500     | ms     |

NOTE:  $V_{CCOx}$  denotes  $V_{CCO0}$ ,  $V_{CCO1}$ ,  $V_{CCO2}$ ,  $V_{CCO3}$ ,  $V_{CCO4}$ ,  $V_{CCO5}$ ,  $V_{CCO6}$ ,  $V_{CCO7}$ .

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is guaranteed by characterization. Not tested in production.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Measured at the output differential crosspoints.

NOTE 4: Measured at  $V_{CCOx}/2$  of the rising edge. All Qx and nQx outputs phase-aligned.

NOTE 5: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions running off the same clock source.

NOTE 6: Appropriate SE\_MODE bit must be set to enable phase-aligned operation.

NOTE 7: Characterized in synthesizer mode. Duty cycle of bypassed signals (input reference clocks or crystal input) is not adjusted by the device.

NOTE 8: Tested in fast-lock operation after >20 minutes of locked operation to ensure holdover averaging logic is stable.

NOTE 9: Characterized with 8T49N282B-901units (synthesizer mode).

NOTE 10: Device programmed with SWMODEn = 0 (absorbs phase differences).

NOTE 11: Tested with all outputs operating at 122.88MHz.

NOTE 12: Assuming a clear I<sup>2</sup>C bus.

NOTE 13: This parameter is guaranteed by design.

**Table 13A. Typical RMS Phase Jitter (Synthesizer Mode),**  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CC0x} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$  (1.8V only supported for LVCMOS outputs),  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol                         | Parameter                 | Test Conditions   | LVPECL | LVDS | LVCMOS <sup>NOTE 6</sup>          | Units |
|--------------------------------|---------------------------|---|--------|------|-----------------------------------|-------|
| t <sub>jitter</sub> ( $\phi$ ) | RMS Phase Jitter (Random) | Q0, Q1<br>$f_{OUT} = 122.88MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 1</a> | 281    | 286  | 273                               | fs    |
|                                |                           | Q0, Q1<br>$f_{OUT} = 156.25MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 2</a> | 261    | 250  | 259                               | fs    |
|                                |                           | Q0, Q1<br>$f_{OUT} = 622.08MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 3</a> | 220    | 209  | N/A<br>( <a href="#">NOTE 5</a> ) | fs    |
|                                |                           | Q2, Q3 Integer;<br><a href="#">NOTE 1</a>   | 297    | 319  | 306                               | fs    |
|                                |                           | Q2, Q3 Fractional;<br><a href="#">NOTE 4</a>  | 288    | 263  | 254                               | fs    |
|                                |                           | Q4, Q5, Q6, Q7;<br><a href="#">NOTE 1</a>   | 293    | 332  | 296                               | fs    |

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Fox part numbers: 277LF-40-18 and 277LF-38.88-2 used for 40MHz and 38.88MHz crystals, respectively.

NOTE: All outputs configured for the specific output type, as shown in the table.

NOTE 1: Characterized with 8T49N282B-901.

NOTE 2: Characterized with 8T49N282B-902.

NOTE 3: Characterized with 8T49N282B-903.

NOTE 4: Characterized with 8T49N282B-900.

NOTE 5: This frequency is not supported for LVCMOS operation.

NOTE 6: Qx and nQx are  $180^\circ$  out of phase.

**Table 13B. Typical RMS Phase Jitter (Jitter Attenuator Mode),**  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CC0x} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  or  $1.8V \pm 5\%$  (1.8V only supported for LVCMOS outputs),  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol                         | Parameter                 | Test Conditions   | LVPECL | LVDS | LVCMOS <sup>NOTE 6</sup>          | Units |
|--------------------------------|---------------------------|---|--------|------|-----------------------------------|-------|
| t <sub>jitter</sub> ( $\phi$ ) | RMS Phase Jitter (Random) | Q0, Q1<br>$f_{OUT} = 122.88MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 1</a> | 283    | 287  | 282                               | fs    |
|                                |                           | Q0, Q1<br>$f_{OUT} = 156.25MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 2</a> | 260    | 261  | 272                               | fs    |
|                                |                           | Q0, Q1<br>$f_{OUT} = 622.08MHz$ ,<br>Integration Range: 12kHz - 20MHz; <a href="#">NOTE 3</a> | 256    | 255  | N/A<br>( <a href="#">NOTE 5</a> ) | fs    |
|                                |                           | Q2, Q3 Integer;<br><a href="#">NOTE 1</a>   | 311    | 315  | 317                               | fs    |
|                                |                           | Q2, Q3 Fractional;<br><a href="#">NOTE 4</a>  | 259    | 266  | 262                               | fs    |
|                                |                           | Q4, Q5, Q6, Q7;<br><a href="#">NOTE 1</a>   | 298    | 308  | 302                               | fs    |

NOTE:  $V_{CC0x}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Measured using a Rohde & Schwarz SMA100A as the input source.

NOTE: Fox part numbers: 277LF-40-18 and 277LF-38.88-2 used for 40MHz and 38.88MHz crystals, respectively.

NOTE: All outputs configured for the specific output type, as shown in the table.

NOTE 1: Characterized with 8T49N282B-905.

NOTE 2: Characterized with 8T49N282B-906.

NOTE 3: Characterized with 8T49N282B-907.

NOTE 4: Characterized with 8T49N282B-904.

NOTE 5: This frequency is not supported for LVCMOS operation.

NOTE 6: Qx and nQx are  $180^\circ$  out of phase.



**Table 14A. PCI Express Jitter Specifications,  $V_{CC} = V_{CCOx} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol                                | Parameter   | Test Conditions  | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---------------------------------------|---|--|---------|---------|---------|-----------------------------|-------|
| $t_{j}$<br>(PCIe Gen 1)               | Phase Jitter<br>Peak-to-Peak;<br><a href="#">NOTE 1, 4, 5</a> | $f = 100MHz$ , 40MHz Crystal Input,<br>Evaluation Band: 0Hz - Nyquist (clock<br>frequency/2) |         | 8       | 30      | 86                          | ps    |
| $t_{REFCLK\_HF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter<br>RMS;<br><a href="#">NOTE 2, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>High Band: 1.5MHz - Nyquist (clock<br>frequency/2)    |         | 0.5     | 2       | 3.10                        | ps    |
| $t_{REFCLK\_LF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter<br>RMS;<br><a href="#">NOTE 2, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>Low Band: 10kHz - 1.5MHz                              |         | 0.04    | 0.2     | 3.0                         | ps    |
| $t_{REFCLK\_RMS}$<br>(PCIe Gen 3)     | Phase Jitter<br>RMS;<br><a href="#">NOTE 3, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>Evaluation Band: 0Hz - Nyquist (clock<br>frequency/2) |         | 0.1     | 0.4     | 0.8                         | ps    |

NOTE:  $V_{CCOx}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

NOTE 5: Outputs configured for LVPECL mode. Fox 277LF-40-18 crystal used with doubler logic enabled.

**Table 14B. PCI Express Jitter Specifications,  $V_{CC} = V_{CCOx} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol                                | Parameter   | Test Conditions  | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---------------------------------------|---|--|---------|---------|---------|-----------------------------|-------|
| $t_{j}$<br>(PCIe Gen 1)               | Phase Jitter<br>Peak-to-Peak;<br><a href="#">NOTE 1, 4, 5</a> | $f = 100MHz$ , 40MHz Crystal Input,<br>Evaluation Band: 0Hz - Nyquist (clock<br>frequency/2) |         | 12      | 65      | 86                          | ps    |
| $t_{REFCLK\_HF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter<br>RMS;<br><a href="#">NOTE 2, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>High Band: 1.5MHz - Nyquist (clock<br>frequency/2)    |         | 0.8     | 3.10    | 3.10                        | ps    |
| $t_{REFCLK\_LF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter<br>RMS;<br><a href="#">NOTE 2, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>Low Band: 10kHz - 1.5MHz                              |         | 0.05    | 0.4     | 3.0                         | ps    |
| $t_{REFCLK\_RMS}$<br>(PCIe Gen 3)     | Phase Jitter<br>RMS;<br><a href="#">NOTE 3, 4, 5</a>          | $f = 100MHz$ , 40MHz Crystal Input,<br>Evaluation Band: 0Hz - Nyquist (clock<br>frequency/2) |         | 0.2     | 0.8     | 0.8                         | ps    |

NOTE:  $V_{CCOx}$  denotes  $V_{CC00}$ ,  $V_{CC01}$ ,  $V_{CC02}$ ,  $V_{CC03}$ ,  $V_{CC04}$ ,  $V_{CC05}$ ,  $V_{CC06}$ ,  $V_{CC07}$ .

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1

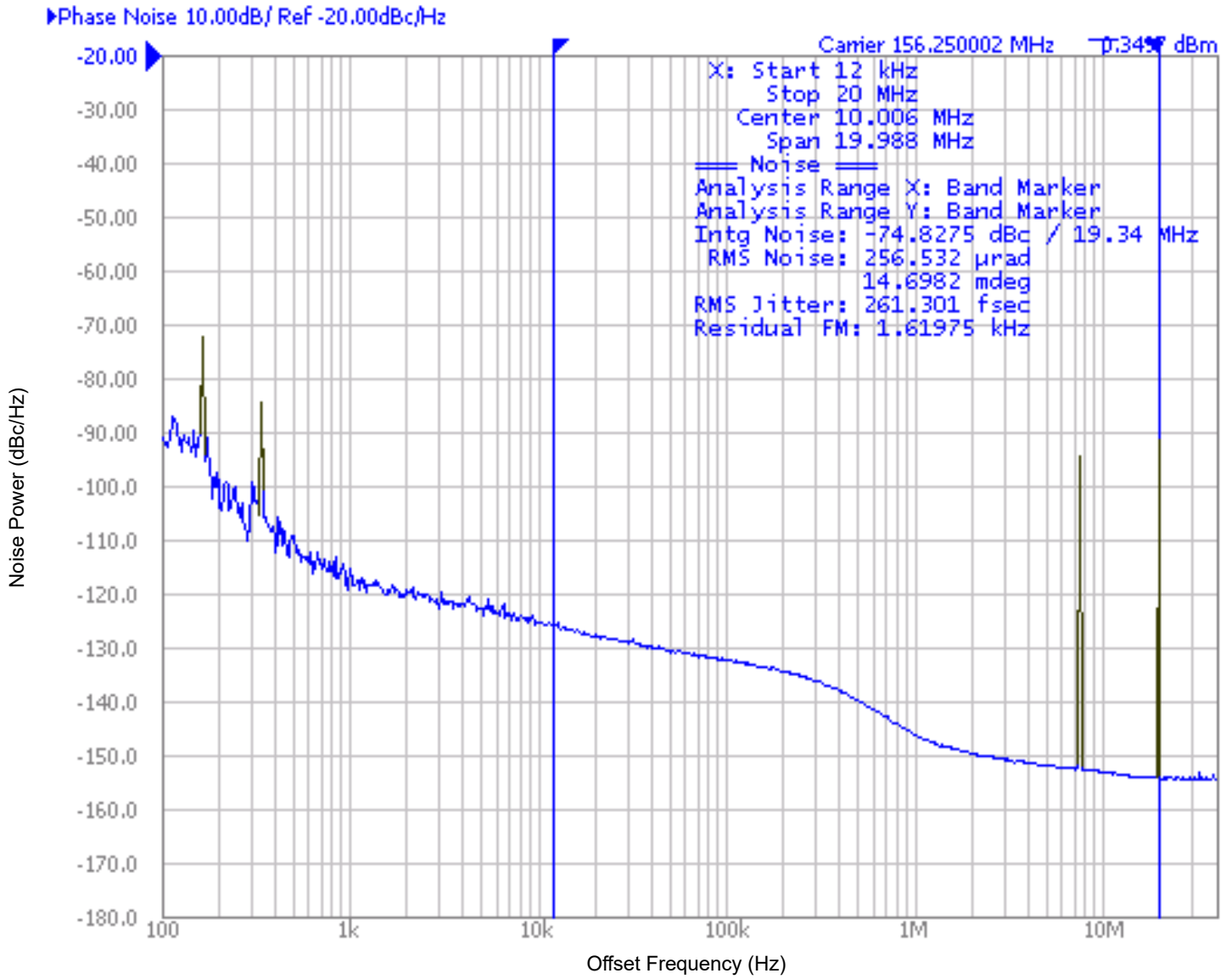
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

NOTE 5: Outputs configured for LVPECL mode. Fox 277LF-40-18 crystal used with doubler logic enabled.

### Typical Phase Noise at 156.25MHz



## Applications Information

### Overdriving the XTAL Interface

The OSC1 input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSC0 pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise.

Figure 8A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 8B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSC1 input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

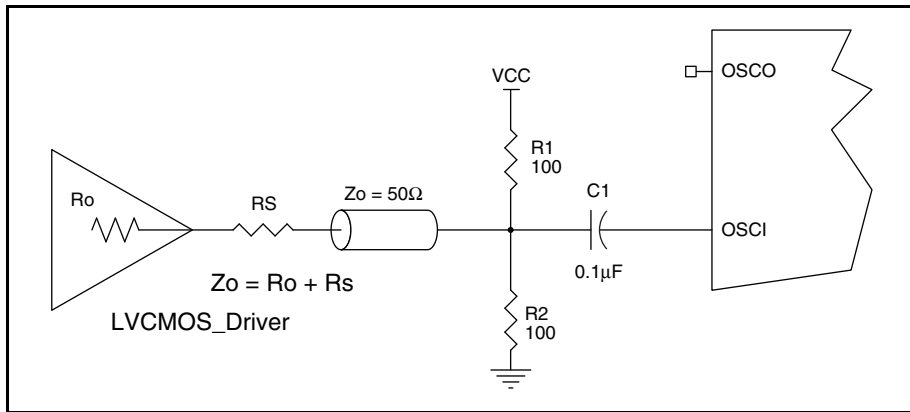


Figure 8A. General Diagram for LVCMOS Driver to XTAL Input Interface

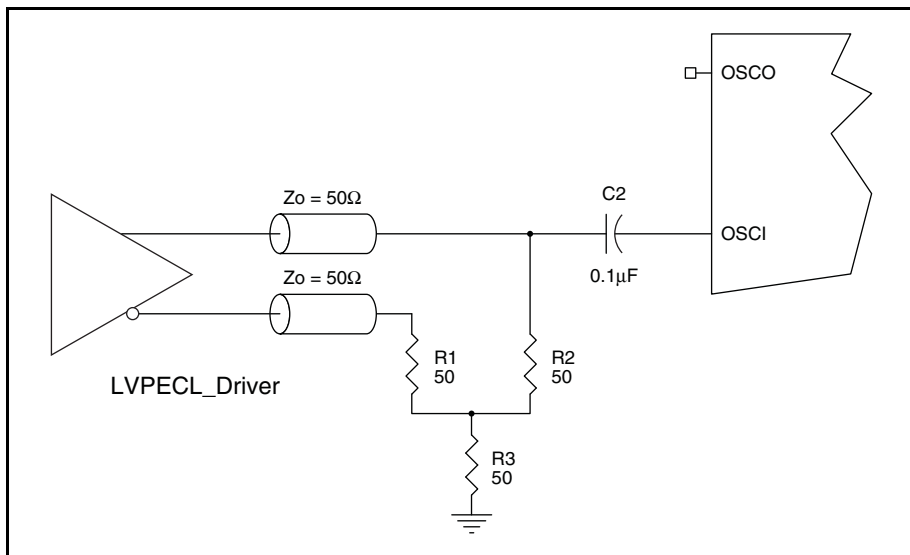


Figure 8B. General Diagram for LVPECL Driver to XTAL Input Interface

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 9 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{CC}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_1$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. Similarly, if the input clock swing is 1.8V and  $V_{CC} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 0.9V. It is recommended to always use R1 and R2 to provide a known  $V_1$  voltage. The values below are for when both the single ended swing and  $V_{CC}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways.

First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{CC} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

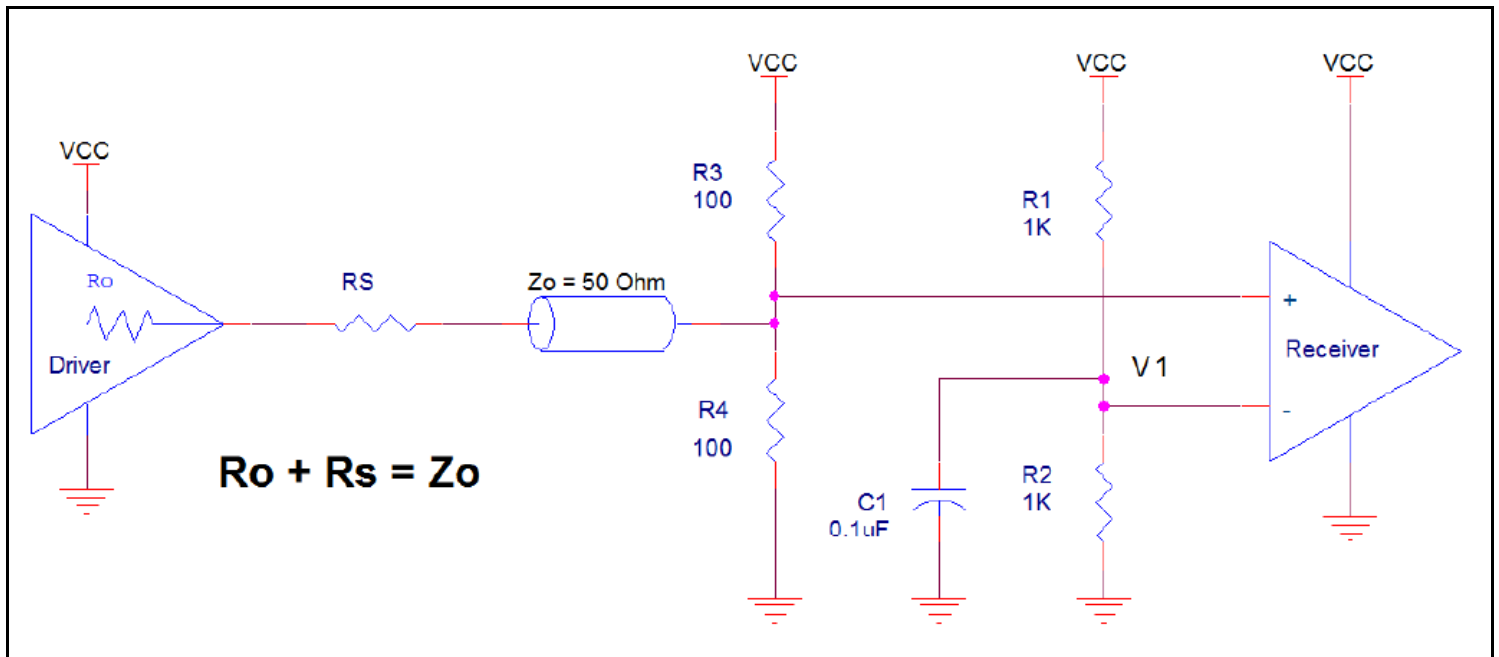
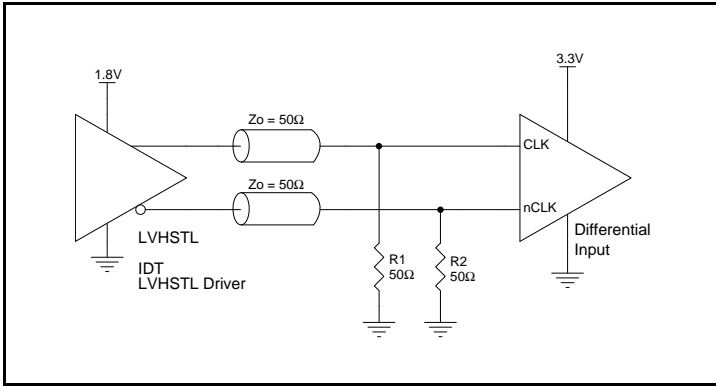


Figure 9. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

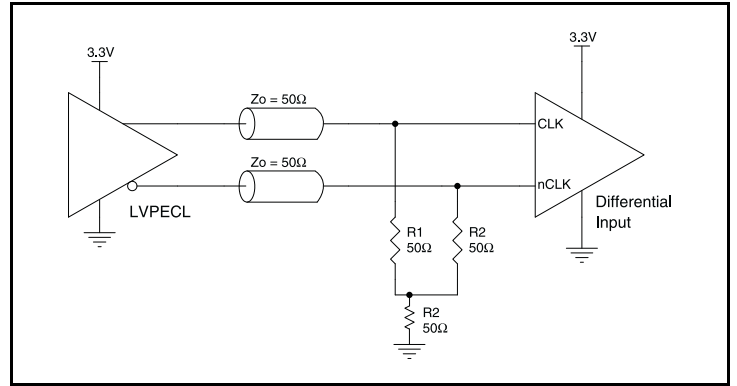
### 3.3V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. *Figure 10A* to *Figure 10E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

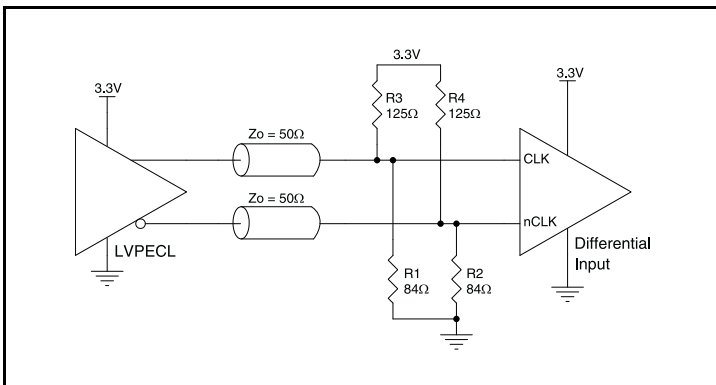
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 10A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



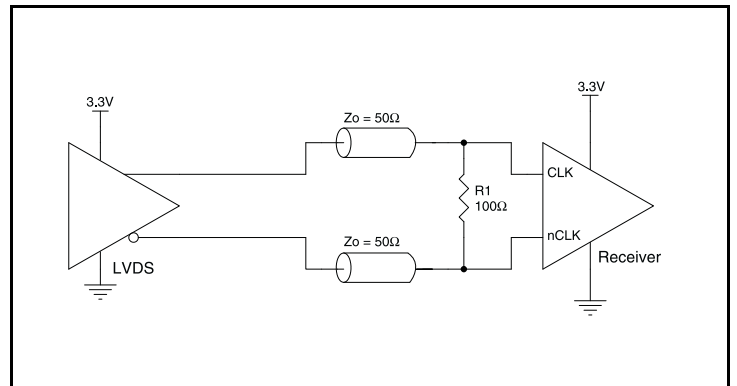
**Figure 10A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver**



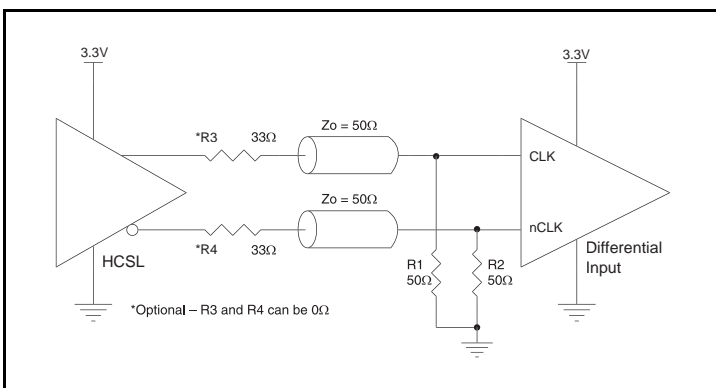
**Figure 10D. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver**



**Figure 10B. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver**



**Figure 10E. CLKx/nCLKx Input Driven by a 3.3V LVDS Driver**

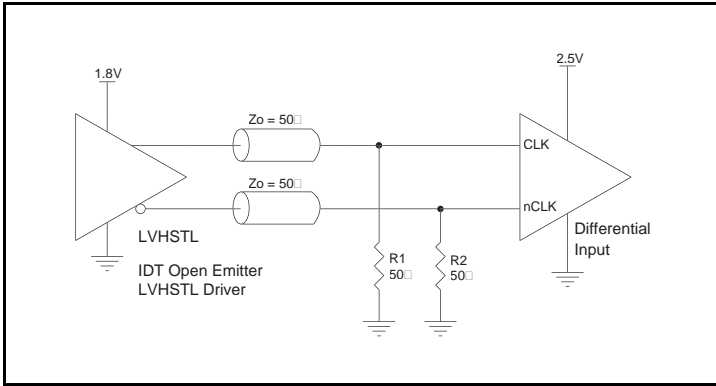


**Figure 10C. CLKx/nCLKx Input Driven by a 3.3V HCSL Driver**

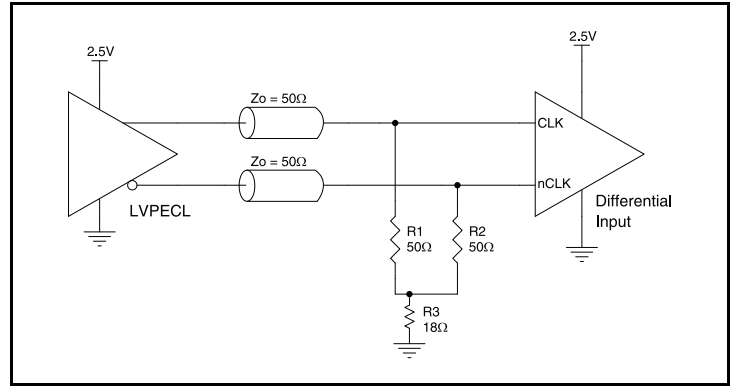
## 2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. [Figure 11A](#) to [Figure 11D](#) show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

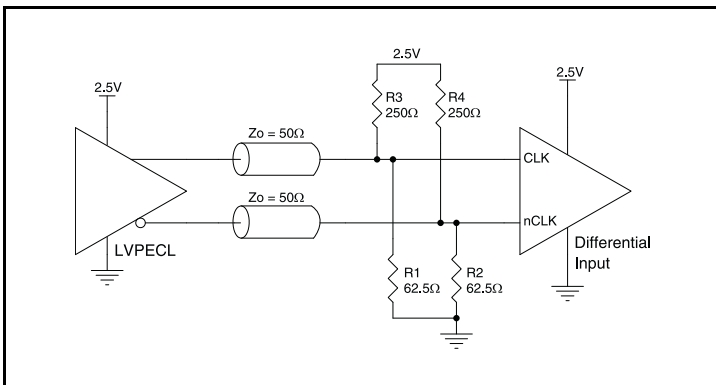
with the vendor of the driver component to confirm the driver termination requirements. For example, in [Figure 11A](#), the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



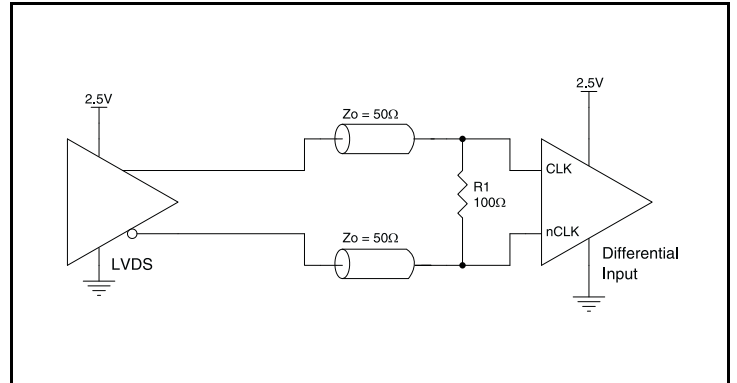
**Figure 11A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver**



**Figure 11C. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver**



**Figure 11B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver**



**Figure 11D. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### CLKx/nCLKx Input

For applications not requiring the use of one or more reference clock inputs, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx not be driven with active signals when not enabled for use by either PLL.

#### LVC MOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

### Outputs:

#### LVPECL Outputs

Any unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

#### LVDS Outputs

Any unused LVDS output pair can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

#### LVC MOS Outputs

Any LVC MOS output can be left floating if unused. There should be no trace attached.

standard termination schematic as shown in [Figure 12A](#) can be used with either type of output structure. [Figure 12B](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

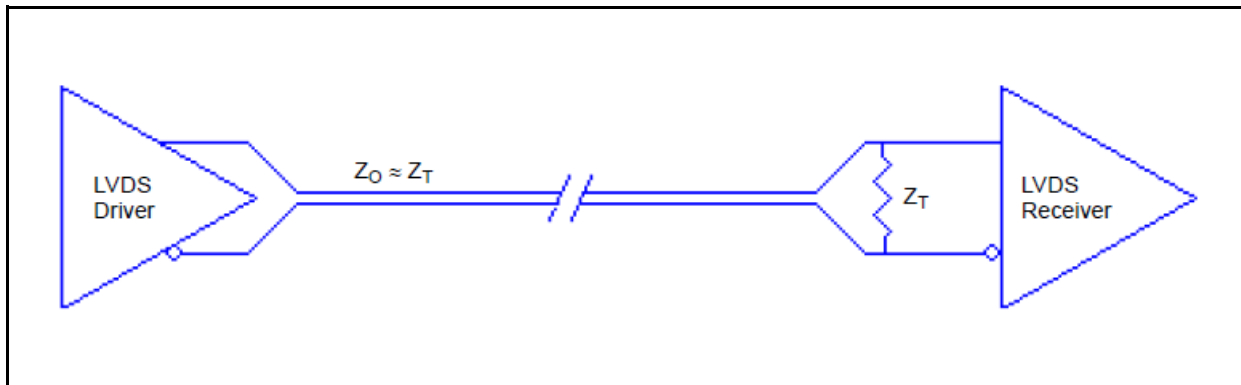


Figure 12A. Standard LVDS Termination

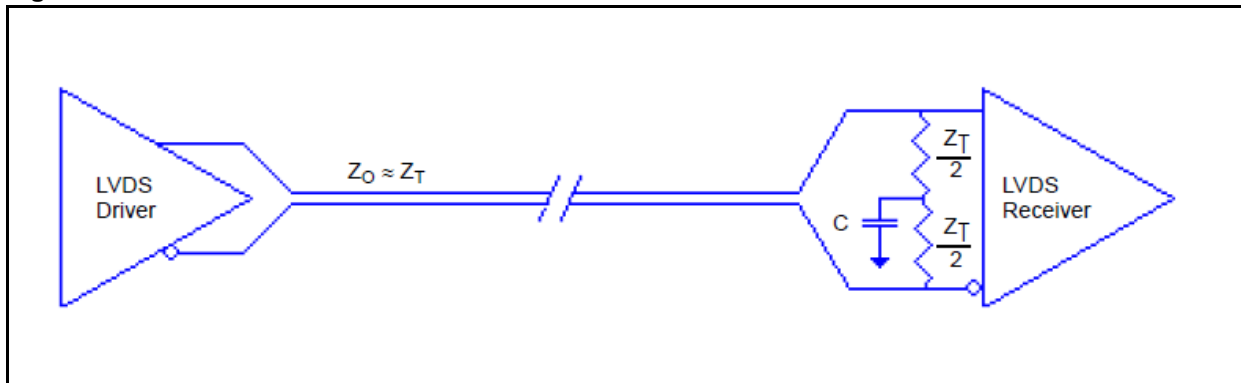


Figure 12B. Optional LVDS Termination

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. [Figure 13A](#) and [Figure 13B](#) show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

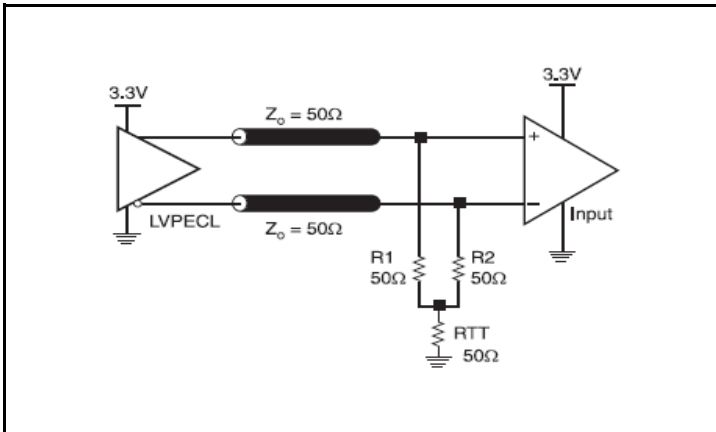


Figure 13A. 3.3V LVPECL Output Termination

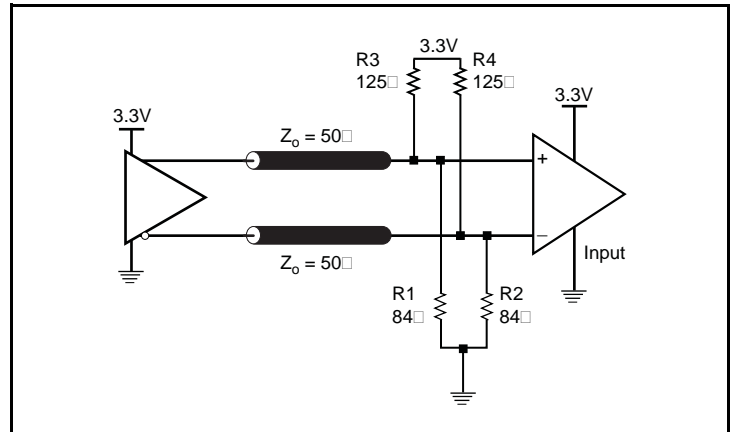


Figure 13B. 3.3V LVPECL Output Termination



### Termination for 2.5V LVPECL Outputs

Figure 14A and Figure 14C show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to  $V_{CC0} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to ground

level. The R3 in Figure 14C can be eliminated and the termination is shown in Figure 14B.

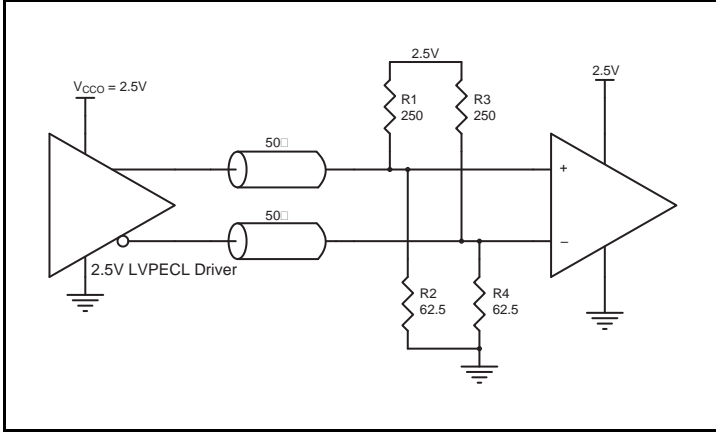


Figure 14A. 2.5V LVPECL Driver Termination Example

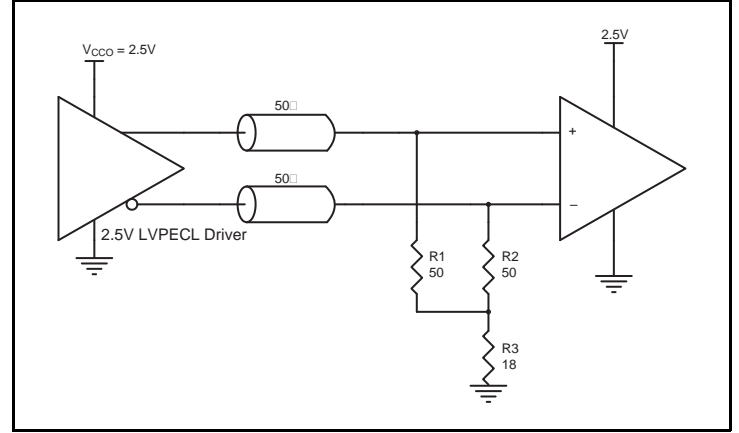


Figure 14C. 2.5V LVPECL Driver Termination Example

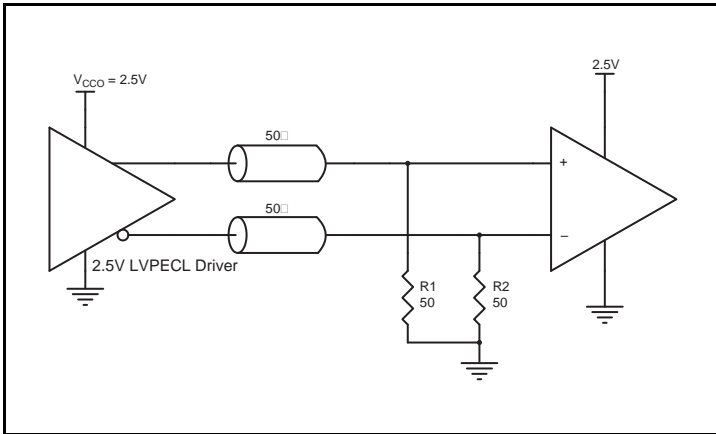


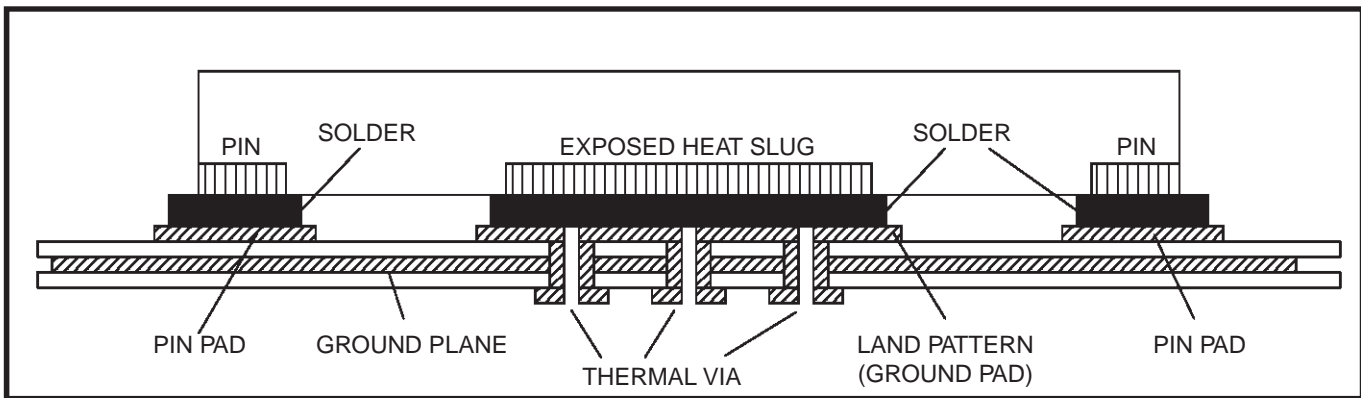
Figure 14B. 2.5V LVPECL Driver Termination Example

### VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 15*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.



**Figure 15. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

### Schematic and Layout Information

Schematics for 8T49N282 can be found on IDT.com. Please search for the 8T49N282 device and click on the link for evaluation board schematics.

### Crystal Recommendation

This device was validated using FOX 277LF series through-hole crystals including part #277LF-40-18 (40MHz) and 277LF-38.88-2 (38.88MHz). If a surface mount crystal is desired, we recommend FOX Part #603-40-48 (40MHz) or 603-38.88-7 (38.88MHz).

### I<sup>2</sup>C Serial EEPROM Recommendation

The 8T49N282 was designed to operate with most standard I<sup>2</sup>C serial EEPROMs of 256 bytes or larger. Atmel AT24C04C was used during device characterization and is recommended for use. Please contact IDT for review of any other I<sup>2</sup>C EEPROM's compatibility with the 8T49N282.

### PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

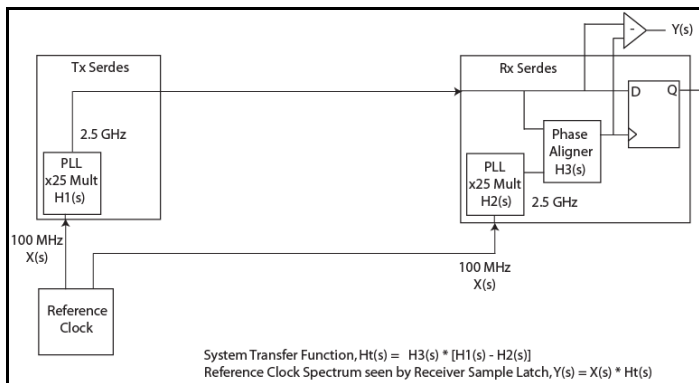
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

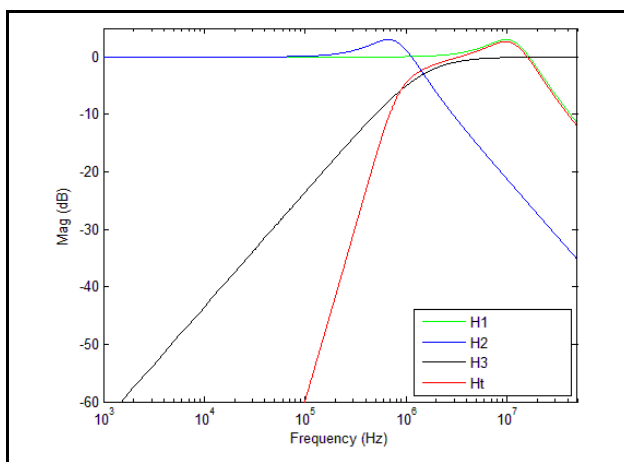
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)\*H3(s) \* [H1(s) - H2(s)].



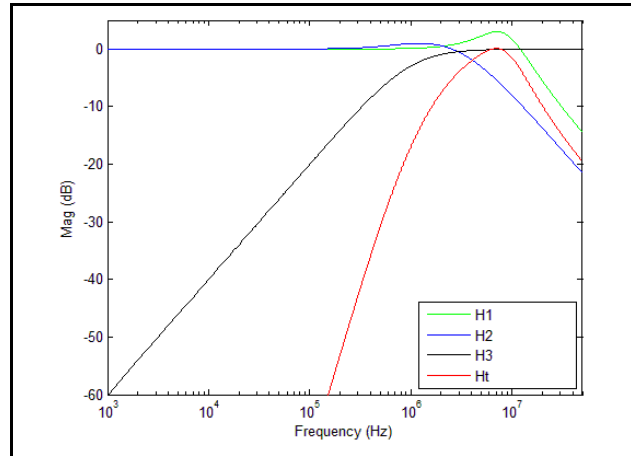
**PCI Express Common Clock Architecture**

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

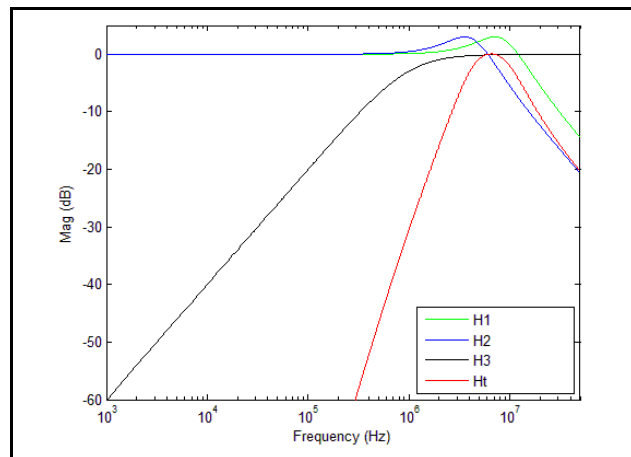


**PCI Express Gen 1 Magnitude of Transfer Function**

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

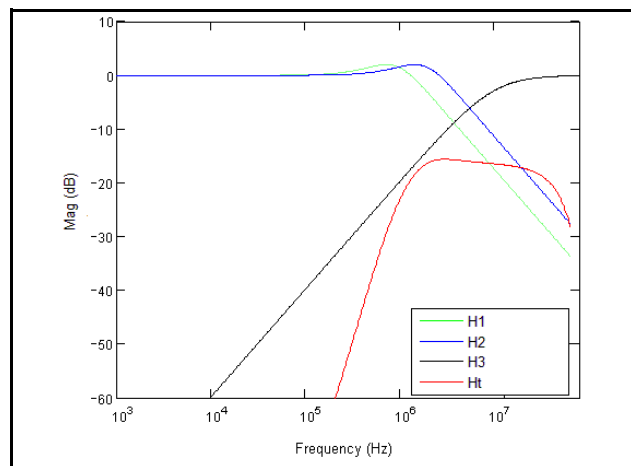


**PCIe Gen 2A Magnitude of Transfer Function**



**PCIe Gen 2B Magnitude of Transfer Function**

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



**PCIe Gen 3 Magnitude of Transfer Function**

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

## Power Dissipation and Thermal Considerations

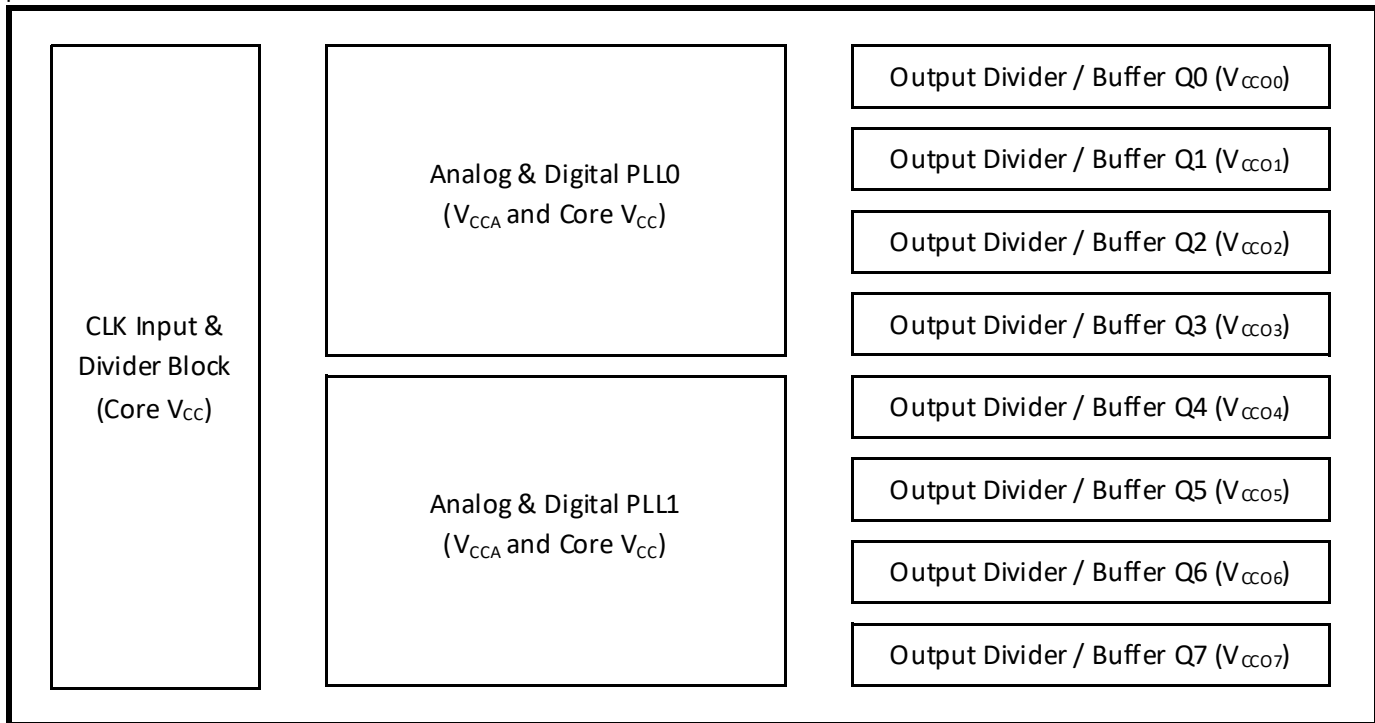
The 8T49N282 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8T49N282 device was designed and characterized to operate within the ambient industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding  $125^{\circ}\text{C}$  junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

## Power Domains

The 8T49N282 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). [Figure 16](#) below indicates the individual domains and the associated power pins.



**Figure 16. 8T49N282 Power Domains**

For the output paths shown above, there are three different structures that are used. Q0 and Q1 use one output path structure, Q2 and Q3 use a second structure and Q4 – Q7 use a 3<sup>rd</sup> structure. Power consumption data will vary slightly depending on the structure used as shown in the appropriate tables below.

## Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core and analog voltage supplies from Tables 8A and 8B.
2. Determine the nominal power consumption of each enabled output path.
  - a. This consists of a base amount of power that is independent of operating frequency, as shown in Tables 17A through 17G (depending on the chosen output protocol).
  - b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ\_Factor shown in Tables 17A through 17G.
3. All of the above totals are then summed.

## Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heatsink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in [Table 15](#) below. Please contact IDT for assistance in calculating results under other scenarios.

**Table 15. Thermal Resistance  $\theta_{JA}$  for 72-Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 16.1°C/W | 12.4°C/W | 11.1°C/W |

## Current Consumption Data and Equations

**Table 16A. 3.3V LVPECL Output Calculation Table**

| LVPECL | FQ_Factor (mA/MHz) | Base_Current (mA) |
|--------|--------------------|-------------------|
| Q0     | 0.00624            | 40.3              |
| Q1     |                    |                   |
| Q2     | 0.01445            | 63.6              |
| Q3     |                    |                   |
| Q4     | 0.00609            | 42.2              |
| Q5     |                    |                   |
| Q6     |                    |                   |
| Q7     |                    |                   |

**Table 16D. 2.5V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|------|--------------------|-------------------|
| Q0   | 0.00412            | 41.9              |
| Q1   |                    |                   |
| Q2   | 0.01217            | 65.3              |
| Q3   |                    |                   |
| Q4   | 0.00425            | 43.6              |
| Q5   |                    |                   |
| Q6   |                    |                   |
| Q7   |                    |                   |

**Table 16B. 2.5V LVPECL Output Calculation Table**

| LVPECL | FQ_Factor (mA/MHz) | Base_Current (mA) |
|--------|--------------------|-------------------|
| Q0     | 0.00409            | 33.0              |
| Q1     |                    |                   |
| Q2     | 0.01179            | 56.4              |
| Q3     |                    |                   |
| Q4     | 0.00369            | 35.4              |
| Q5     |                    |                   |
| Q6     |                    |                   |
| Q7     |                    |                   |

**Table 16E. 3.3V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|--------|-------------------|
| Q0     | 37.5              |
| Q1     |                   |
| Q2     | 61.1              |
| Q3     |                   |
| Q4     | 40.1              |
| Q5     |                   |
| Q6     |                   |
| Q7     |                   |

**Table 16C. 3.3V LVDS Output Calculation Table**

| LVDS | FQ_Factor (mA/MHz) | Base_Current (mA) |
|------|--------------------|-------------------|
| Q0   | 0.00664            | 49.6              |
| Q1   |                    |                   |
| Q2   | 0.01479            | 73.0              |
| Q3   |                    |                   |
| Q4   | 0.00646            | 51.5              |
| Q5   |                    |                   |
| Q6   |                    |                   |
| Q7   |                    |                   |

**Table 16F. 2.5V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|--------|-------------------|
| Q0     | 31.0              |
| Q1     |                   |
| Q2     | 54.6              |
| Q3     |                   |
| Q4     | 33.2              |
| Q5     |                   |
| Q6     |                   |
| Q7     |                   |

**Table 16G. 1.8V LVCMOS Output Calculation Table**

| LVCMOS | Base_Current (mA) |
|--------|-------------------|
| Q0     | 26.8              |
| Q1     |                   |
| Q2     | 50.4              |
| Q3     |                   |
| Q4     | 29.0              |
| Q5     |                   |
| Q6     |                   |
| Q7     |                   |

Applying the values to the following equation will yield output current by frequency:

$$Qx \text{ Current (mA)} = FQ\_Factor * \text{Frequency (MHz)} + \text{Base\_Current}$$

**where:**

*Qx Current* is the specific output current according to output type and frequency

*FQ\_Factor* is used for calculating current increase due to output frequency

*Base\_Current* is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$$T_J = T_A + (\theta_{JA} * P_{d_{total}})$$

**where:**

$T_J$  is the junction temperature (°C)

$T_A$  is the ambient temperature (°C)

$\theta_{JA}$  is the thermal resistance value from Table 15, dependent on ambient airflow (°C/W)

$P_{d_{total}}$  is the total power dissipation of the 8T49N282 under usage conditions, including power dissipated due to loading (W)

Note that for LVPECL outputs the power dissipation through the load is assumed to be 27.95mW. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using  $C_{PD}$  (found in *Table 2*) and output frequency:

$$P_{d_{OUT}} = C_{PD} * F_{OUT} * V_{CCO}^2$$

**where:**

$P_{d_{OUT}}$  is the power dissipation of the output (W)

$C_{PD}$  is the power dissipation capacitance (pF)

$F_{OUT}$  is the output frequency of the selected output (MHz)

$V_{CCO}$  is the voltage supplied to the appropriate output (V)

## Example Calculations

### Example 1. Common Customer Configuration (3.3V Core Voltage)

| Output | Output Type | Frequency (MHz) | V <sub>CCO</sub> |
|--------|-------------|-----------------|------------------|
| Q0     | LVPECL      | 245.76          | 3.3              |
| Q1     | LVPECL      | 245.76          | 3.3              |
| Q2     | LVPECL      | 33.333          | 3.3              |
| Q3     | LVPECL      | 33.333          | 3.3              |
| Q4     | LVDS        | 125             | 3.3              |
| Q5     | LVDS        | 125             | 3.3              |
| Q6     | LVC MOS     | 25              | 3.3              |
| Q7     | LVC MOS     | 25              | 3.3              |
| PLL0   | Enabled     |                 |                  |
| PLL1   | Enabled     |                 |                  |

- Core Supply Current, I<sub>CC</sub> = **100mA (max)**
- Analog Supply Current, I<sub>CCA</sub> = **265mA (max)**
  - Q0 Current =  $0.00624 \times 245.76 + 40.3 = 41.83\text{mA}$
  - Q1 Current =  $0.00624 \times 245.76 + 40.3 = 41.83\text{mA}$
  - Q2 Current =  $0.01445 \times 33.333 + 63.6 = 64.08\text{mA}$
  - Q3 Current =  $0.01445 \times 33.333 + 63.6 = 64.08\text{mA}$
  - Q4 Current =  $0.00646 \times 125 + 51.5 = 52.3\text{mA}$
  - Q5 Current =  $0.00646 \times 125 + 51.5 = 52.3\text{mA}$
  - Q6 Current = 40.1mA
  - Q7 Current = 40.1mA
- Total Output Current = **396.62mA (max)**
  - Total Device Current = 100mA + 265mA + 396.6mA = **761.6mA**
  - Total Device Power =  $3.465\text{V} \times 761.6\text{mA} = \mathbf{2639\text{mW}}$
- Power dissipated through output loading:
  - LVPECL =  $27.95\text{mW} \times 4 = \mathbf{111.8\text{mW}}$
  - LVDS = already accounted for in device power
  - LVC MOS =  $14.5\text{pF} \times 25\text{MHz} \times 3.465\text{V}^2 \times 2 \text{ output pairs} = \mathbf{8.7\text{mW}}$
- Total Power =  $2639\text{mW} + 111.8\text{mW} + 8.7\text{mW} = \mathbf{2759.5\text{mW or } 2.76\text{W}}$

With an ambient temperature of 85°C and no airflow, the junction temperature is:

$$T_J = 85^\circ\text{C} + 16.1^\circ\text{C/W} \times 2.76\text{W} = \mathbf{129.4^\circ\text{C}}$$

This junction temperature is above the maximum allowable. In instances where maximum junction temperature is exceeded adjustments need to be made to either airflow or ambient temperature. In this case, adjusting airflow to 1m/s ( $\theta_{JA} = 12.4^\circ\text{C/W}$ ) will reduce junction temperature to 119.2°C. If no airflow adjustments can be made, the maximum ambient operating temperature must be reduced by a minimum of 4.4°C.

**Example 2. High-Frequency Customer Configuration (3.3V Core Voltage)**

| Output | Output Type | Frequency (MHz) | V <sub>CCO</sub> |
|--------|-------------|-----------------|------------------|
| Q0     | LVDS        | 625.00          | 2.5              |
| Q1     | LVDS        | 625.00          | 2.5              |
| Q2     | LVPECL      | 161.133         | 2.5              |
| Q3     | LVPECL      | 161.133         | 2.5              |
| Q4     | LVDS        | 25              | 3.3              |
| Q5     | LVDS        | 25              | 3.3              |
| Q6     | LVPECL      | 125             | 2.5              |
| Q7     | LVDS        | 156.25          | 2.5              |
| PLL0   | Enabled     |                 |                  |
| PLL1   | Disabled    |                 |                  |

- Core Supply Current, I<sub>CC</sub> = **100mA (max)**
- Analog Supply Current, I<sub>CCA</sub> = **187mA (max, PLL0 path only)**
  - Q0 Current =  $0.00412 \times 625 + 41.9 = 44.48\text{mA}$
  - Q1 Current =  $0.00412 \times 625 + 41.9 = 44.48\text{mA}$
  - Q2 Current =  $0.01179 \times 161.133 + 56.4 = 58.3\text{mA}$
  - Q3 Current =  $0.01179 \times 161.133 + 56.4 = 58.3\text{mA}$
  - Q4 Current =  $0.00646 \times 25 + 51.5 = 51.66\text{mA}$
  - Q5 Current =  $0.00646 \times 25 + 51.5 = 51.66\text{mA}$
  - Q6 Current =  $0.00369 \times 125 + 35.4 = 35.86\text{mA}$
  - Q7 Current =  $0.00425 \times 156.25 + 43.6 = 44.26\text{mA}$
- Total Output Current = **285.68mA** (V<sub>CCO</sub> = 2.5V), **103.3mA** (V<sub>CCO</sub> = 3.3V)  
 Total Device Power =  $3.465\text{V} \times (100\text{mA} + 187\text{mA} + 103.3\text{mA}) + 2.625\text{V} \times 285.68\text{mA} = \mathbf{2102.3\text{mW}}$
- Power dissipated through output loading:
  - LVPECL =  $27.95\text{mW} \times 3 = \mathbf{83.9\text{mW}}$
  - LVDS = already accounted for in device power
  - LVC MOS = n/a
- Total Power =  $2102.3\text{mW} + 83.9\text{mW} = \mathbf{2186.2\text{mW}}$  or **2.19W**

With an ambient temperature of 85°C, the junction temperature is:

$$T_J = 85^\circ\text{C} + 16.1^\circ\text{C/W} \times 2.19\text{W} = \mathbf{120.3^\circ\text{C}}$$

This junction temperature is below the maximum allowable.



**Example 3. Low Power Customer Configuration (2.5V Core Voltage)**

| Output | Output Type | Frequency (MHz) | V <sub>CCO</sub> |
|--------|-------------|-----------------|------------------|
| Q0     | LVDS        | 156.25          | 2.5              |
| Q1     | LVDS        | 156.25          | 2.5              |
| Q2     | LVDS        | 161.133         | 2.5              |
| Q3     | LVC MOS     | 33.333          | 1.8              |
| Q4     | LVC MOS     | 25              | 1.8              |
| Q5     | LVC MOS     | 25              | 1.8              |
| Q6     | LVC MOS     | 25              | 1.8              |
| Q7     | LVDS        | 156.25          | 2.5              |
| PLL0   | Enabled     |                 |                  |
| PLL1   | Enabled     |                 |                  |

- Core Supply Current, I<sub>CC</sub> = **95mA (max)**
- Analog Supply Current, I<sub>CCA</sub> = **260mA (max)**
  - Q0 Current =  $0.00412 \times 156.25 + 41.9 = 42.54\text{mA}$
  - Q1 Current =  $0.00412 \times 156.25 + 41.9 = 42.54\text{mA}$
  - Q2 Current =  $0.01217 \times 161.133 + 65.3 = 67.26\text{mA}$
  - Q3 Current = 50.4mA
  - Q4 Current = 29mA
  - Q5 Current = 29mA
  - Q6 Current = 29mA
  - Q7 Current =  $0.00425 \times 156.25 + 43.6 = 44.26\text{mA}$
- Total Output Current = **196.6mA** (V<sub>CCO</sub> = 2.5V), **137.4mA** (V<sub>CCO</sub> = 1.8V)  
 Total Device Power =  $2.625\text{V} \times (95\text{mA} + 260\text{mA} + 196.6\text{mA}) + 1.89\text{V} \times 137.4\text{mA} = \mathbf{1707.6\text{mW}}$
- Power dissipated through output loading:
  - LVPECL = n/a
  - LVDS = already accounted for in device power
  - LVC MOS\_33.3MHz =  $17\text{pF} \times 33.3\text{MHz} \times 1.89\text{V}^2 \times 1 \text{ output pair} = \mathbf{2.02\text{mW}}$
  - LVC MOS\_25MHz =  $12.5\text{pF} \times 25\text{MHz} \times 1.89\text{V}^2 \times 3 \text{ output pairs} = \mathbf{3.35\text{mW}}$
  - Total Power =  $1707.6\text{mW} + 2.02\text{mW} + 3.35\text{mW} = \mathbf{1713\text{mW or } 1.7\text{W}}$

With an ambient temperature of 85°C, the junction temperature is:

$$T_J = 85^\circ\text{C} + 16.1^\circ\text{C/W} \times 1.7\text{W} = \mathbf{112.4^\circ\text{C}}$$

This junction temperature is below the maximum allowable.

## Reliability Information

**Table 17.  $\theta_{JA}$  vs. Air Flow Table for a 72-Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 16.1°C/W | 12.4°C/W | 11.1°C/W |

NOTE: Theta JA ( $\theta_{JA}$ ) values calculated using a 4-layer JEDEC PCB (114.3mm x 101.6mm), with 2oz. (70um) copper plating on all 4 layers.

## Transistor Count

The transistor count for 8T49N282 is: 959,346

## Marking Diagram



1. Lines 1 and 2 are the part number.
2. "002" is indicative of a configuration-specific number (dash code).
3. "#" denotes stepping.
4. "YYWW" denotes: "YY" is the last two digits of the year, and "WW" is the work week number that the part was assembled.
5. "\$" denotes the mark code.

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.idt.com/document/psc/nlnlg72-package-outline-100-x-100-mm-body-epad-75-mm-sq-050-mm-pitch-qfn-sawn](http://www.idt.com/document/psc/nlnlg72-package-outline-100-x-100-mm-body-epad-75-mm-sq-050-mm-pitch-qfn-sawn)

## Ordering Information

**Table 18. Ordering Information**

| Part/Order Number  | Marking              | Package                   | Shipping Packaging                        | Temperature    |
|--------------------|----------------------|---------------------------|---|----------------|
| 8T49N282C-dddNLGI  | IDT8T49N282C-dddNLGI | "Lead-Free" 72-Lead VFQFN | Tray                                      | -40°C to +85°C |
| 8T49N282C-dddNLGI8 | IDT8T49N282C-dddNLGI | "Lead-Free" 72-Lead VFQFN | Tape & Reel, Pin 1 Orientation: EIA-481-C | -40°C to +85°C |
| 8T49N282C-dddNLGI# | IDT8T49N282C-dddNLGI | "Lead-Free" 72-Lead VFQFN | Tape & Reel, Pin 1 Orientation: EIA-481-D | -40°C to +85°C |

NOTE: For the specific -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document.

**Table 19. Pin 1 Orientation in Tape and Reel Packaging**

| Part Number Suffix | Pin 1 Orientation      | Illustration  |
|--------------------|------------------------|---|
| NLGI8              | Quadrant 1 (EIA-481-C) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |
| NLGI#              | Quadrant 2 (EIA-481-D) | <p>Correct Pin 1 ORIENTATION</p> <p>CARRIER TAPE TOPSIDE (Round Sprocket Holes)</p> <p>USER DIRECTION OF FEED</p> |

## ERRATA

### Errata # 1: EEPROM CRC Check Failure

Errata: if the UFT++ attempts to load its initial configuration from an external EEPROM and the CRC check fails, the serial port will not complete write operations and will only respond to reads with values of 0 until device is reset via nRST pin.

- if no EEPROM access is attempted, no EEPROM is found or the EEPROM read succeeds there are no issues
- The CRC failure condition can be detected by reading the Global Interrupt Status Register at address 21Fh. If the nEEP\_CRC bit is low, then the device's serial port is now in the failed state
- if the device is also programmed to load its registers from the internal One-Time Programmable memory, those register settings will be correctly loaded and used.

Work-Around: by reading the nEEP\_CRC bit, this condition can be detected. Once detected, the user may attempt to retry the EEPROM load operation by asserting then releasing the nRST input pin. If the retry attempt continues to fail, then no further recovery is possible. Note that a persistent EEPROM CRC failure indicates a corrupted configuration is present and the device could not be correctly configured anyway.

Fix Plan: None

### Errata # 2: GPIOs Can't Use Input Mode if $V_{CC0} = 1.8V$

Errata: When the  $V_{CC0}$  pin adjacent to a GPIO pin is set to 1.8V and the core  $V_{CC}$  of the chip is at 3.3V, the GPIO pin will not behave as an input, either a General-Purpose Input or an Output Enable. Mappings are according to the following relationships

GPIO0 /  $V_{CC03}$

GPIO1 /  $V_{CC03}$

GPIO2 /  $V_{CC04}$

GPIO3 /  $V_{CC07}$

GPIO4 /  $V_{CC04}$

GPIO5 /  $V_{CC05}$

GPIO6 /  $V_{CC06}$

GPIO7 /  $V_{CC07}$

Work-Around: Ensure that voltage used on  $V_{CC0}$  pins is no less than  $V_{CC} - 1.6V$ .

Fix Plan: None

## Revision History

| Revision Date    | Description of Change   |
|------------------|---|
| January 28, 2019 | <ul style="list-style-type: none"> <li>Corrected the I<sup>2</sup>C read sequence diagrams in <a href="#">Figure 6</a> and <a href="#">Figure 7</a> to match I<sup>2</sup>C specification and device actual performance. Note: Only the drawings were incorrect – the part’s behavior did not change and continues to meet the I<sup>2</sup>C specification.</li> <li>Added a <a href="#">Marking Diagram</a></li> <li>Updated the <a href="#">Package Outline Drawings</a>; however, no mechanical changes</li> </ul>  |
| February 2, 2016 | Per PCN# W1512-01, Effective Date 03/18/2016 - changed Part/Order Number from 8T49N282B-dddNLGI to 8T49N282C-dddNLGI, and Marking from IDT8T49N282B-dddNLGI to IDT8T49N282C-dddNLGI.<br>Updated Datasheet header/footer.  |
| October 2, 2015  | Updated pin descriptions for pins 2, 3, 67/68, and 23/24.<br><a href="#">Output Phase Control on Switchover</a> - added sentence to second and third paragraphs.<br>Added notes to <a href="#">Table 4</a> .<br>AC Characteristics Table - updated Note 5.<br>Updated <a href="#">Figure 16, 8T49N282 Power Domains</a> .   |
| July 8, 2015     | <a href="#">Device Start-up &amp; Reset Behavior</a> - added second paragraph.  |
| May 4, 2015      | Thermal Considerations - corrected Table number in paragraph.   |
| April 27, 2015   | AC Characteristics Table - added missing minimum Output Frequency spec for Q2, Q3 (LVPECL, LVDS) and LVCMOS.<br>Termination for 3.3V LVPECL Outputs - updated <a href="#">Figure 14A</a> .<br>Crystal Recommendation - included additional crystal recommendation.  |
| May 29, 2014     | Second column, last paragraph; replaced last sentence.<br>Output Phase Alignment; replaced fourth paragraph.<br>Second column, first bullet; changed “VCO period (TVCO)” to “source clock period”. Changed “1 x TVCO” to “250ps”.<br>LVCMOS operation; replaced last sentence.<br>Corrected typo “Femto NG” to FemtoClock NG” (4 places).<br>REV_ID[3:0], fixed typo in default value “00010b” to “0010b”.<br>UFTADD[6:2]; replaced description.<br>UFTADD[1], changed Default Value from “-” to “0b”. Replaced description.<br>UFTADD[0], changed Default Value from “-” to “0b”. Replaced description.<br>00AB row, replaced “Rsvd” with “10” for D7:D6 and D5:D4.<br>Replaced “tjit(θ)” with “tjit(φ)”.<br>Replaced XTAL_IN and XTAL_OUT with OSC1 and OSC0 respectively.<br>Changed Q6 Frequency to 125MHz. Changed Q4, Q5 V <sub>CC0</sub> to 3.3V. Updated calculations.<br>Updated Package Outline drawings.<br>Ordering Information; added pin orientation info.<br>Added Pin 1 Orientation table.<br>Updated Contact Information |

| Revision Date  | Description of Change   |
|----------------|---|
| April 17, 2014 | <p>Renumbered figures with the Block Diagram as Figure 1.<br/>           Added NOTE 1 to C<sub>IN</sub>.<br/>           General-Purpose I/Os &amp; Interrupts section: replaced '0x006E' and '0x0076' with '006Eh' and '0076h'.<br/>           General-Purpose I/Os &amp; Interrupts section: added last paragraph.<br/>           SPI Mode Operation: replaced text (3 paragraphs).<br/>           Figure 1: replaced figure.<br/>           Figure 1 Title: replaced text 'SPI Read Timing Diagram' with 'SPI Read Sequencing Diagram'.<br/>           Figure 2: replaced figure.<br/>           Figure 3: replaced figure.<br/>           Figure 4: replaced figure.<br/>           I<sup>2</sup>C Master Mode, 3<sup>rd</sup> bullet: replaced '0xE0' with 'E0h'.<br/>           I<sup>2</sup>C Master Mode, 4th bullet: replaced '0x05' with '05h'.<br/>           Text section; replaced '0xE0' with 'E0h'. and '0x006' with '006h'.<br/>           I<sup>2</sup>C Boot-up Initialization Mode, second paragraph; replaced "The BOOTFAIL bit in the Status Control register will also be set in this event." with "The BOOTFAIL bit (021Eh) in the Global Interrupt Status register will also be set in this event".<br/>           EEPROM Offset (Hex) column; deleted '0x' of 0x## (15 instances).<br/>           Table Header: deleted '(Binary)' from "Default Value".<br/>           Replaced values formatting for Default Value column.<br/>           Outputs, V<sub>O</sub> (Q[0:7], nQ[0:7]): Changed V<sub>CCO</sub> to V<sub>CCOX</sub>.<br/>           Outputs, V<sub>O</sub> (GPIO, SDATA, SCLK, nINT): changed GPIO to GPIO[0:7].<br/>           Added Note: NOTE: V<sub>CCOX</sub> denotes V<sub>CCO0</sub>, V<sub>CCO1</sub>, V<sub>CCO2</sub>, V<sub>CCO3</sub>, V<sub>CCO4</sub>, V<sub>CCO5</sub>, V<sub>CCO6</sub>, V<sub>CCO7</sub>.<br/>           Table Header: Changed V<sub>CCOX</sub> to V<sub>CC</sub>.<br/>           ERRATA; 1st paragraph; replaced '0x21F' with '21Fh'.</p> |
| March 7, 2014  | <p>Move Pin Assignment from page 9 to page 5.<br/>           Fixed package drawings on page.</p>  |
| March 5, 2014  | <p>Applications - updated bullets.<br/>           Features - added <i>Power Down Mode</i> bullet.<br/>           Deleted <i>Compliance</i> section.<br/>           3.3V Power Supply Table - added test condition to original I<sub>CCA</sub> spec. Added second spec to I<sub>CCA</sub>. Updated Note 2.<br/>           2.5V Power Supply Table - added test condition to original I<sub>CCA</sub> spec. Added second spec to I<sub>CCA</sub>. Updated Note 2.<br/>           Renumbered Tables starting with Table 9D, and changed to Table 10A.<br/>           Applications Information, Crystal Recommendation Note - updated Fox part numbers.<br/>           Revised <i>Power Dissipation and Thermal Considerations</i> section.</p>   |



Corporate Headquarters  
 6024 Silver Creek Valley Road  
 San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

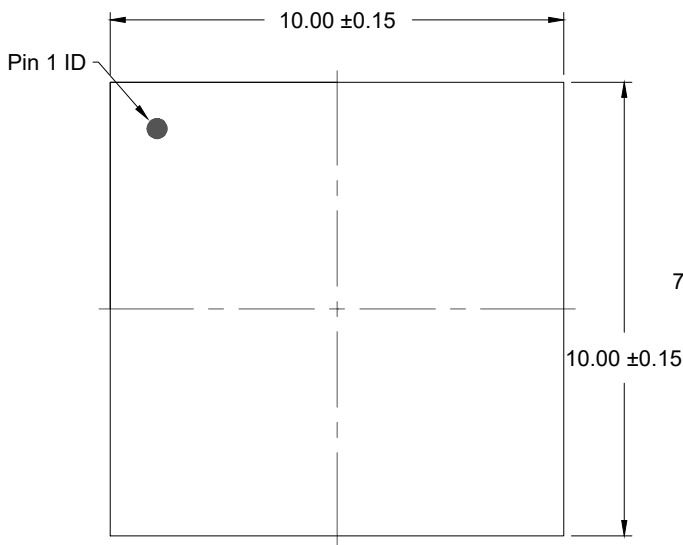
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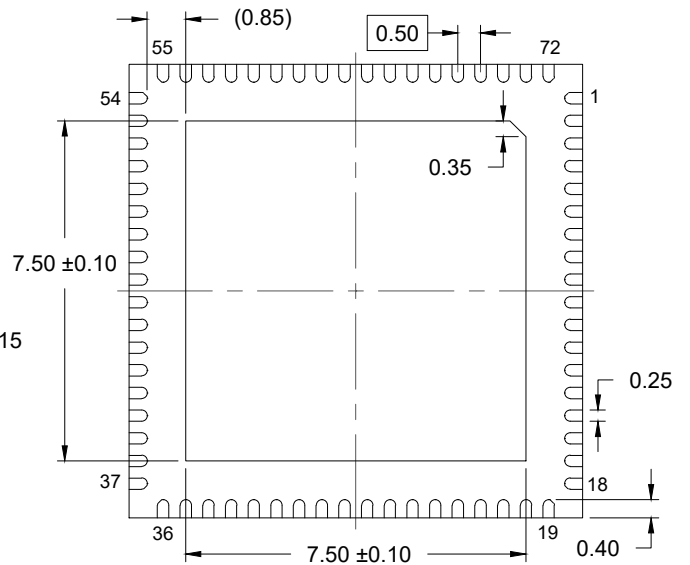
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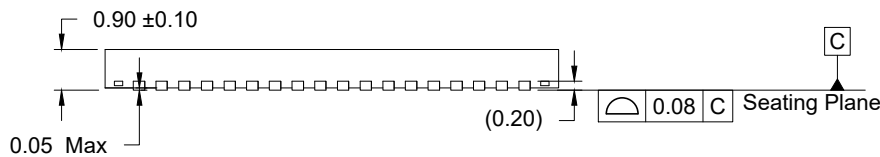
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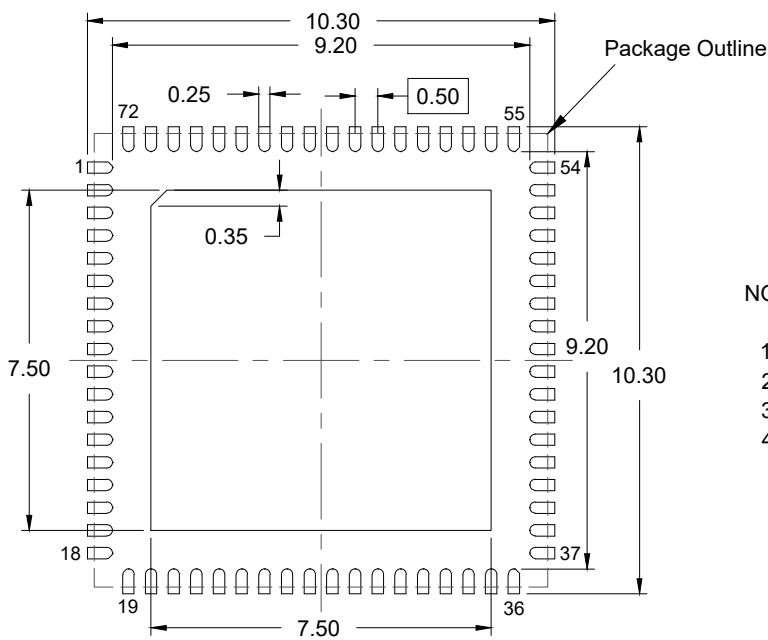
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.