

## General Description

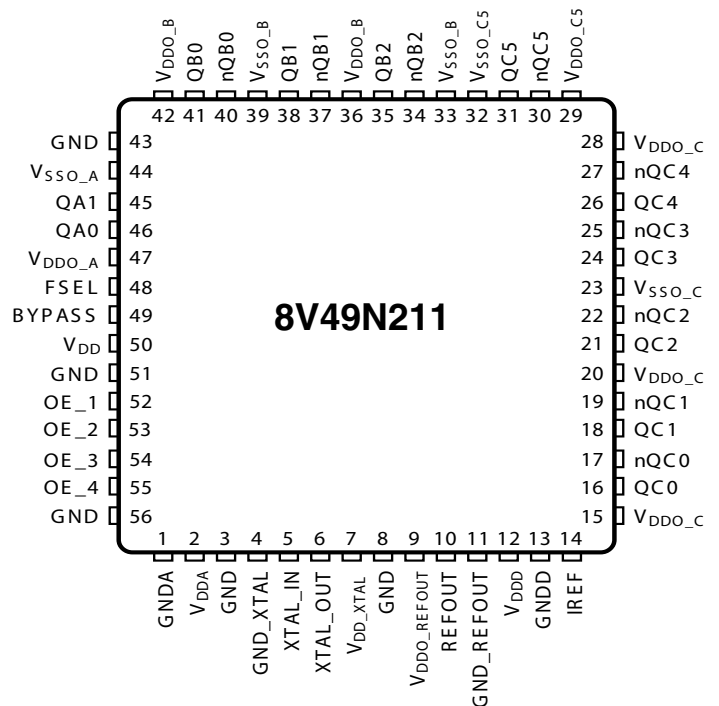
The 8V49N211 is a high-performance PLL-based clock generator designed to interface with Broadcom XLP2xxx processors. The 8V49N211 has one 25MHz crystal input to generate output frequencies to support XLP Core/DDR3, USB, SGMII/XAUI and PCIe reference clocks in a single chip. The 8V49N211 low jitter VCO easily meets PCI Express Gen 1, 2 and 3 requirements.

IDT's Fourth Generation FemtoClock® NG technology has best in class phase noise performance.

## Features

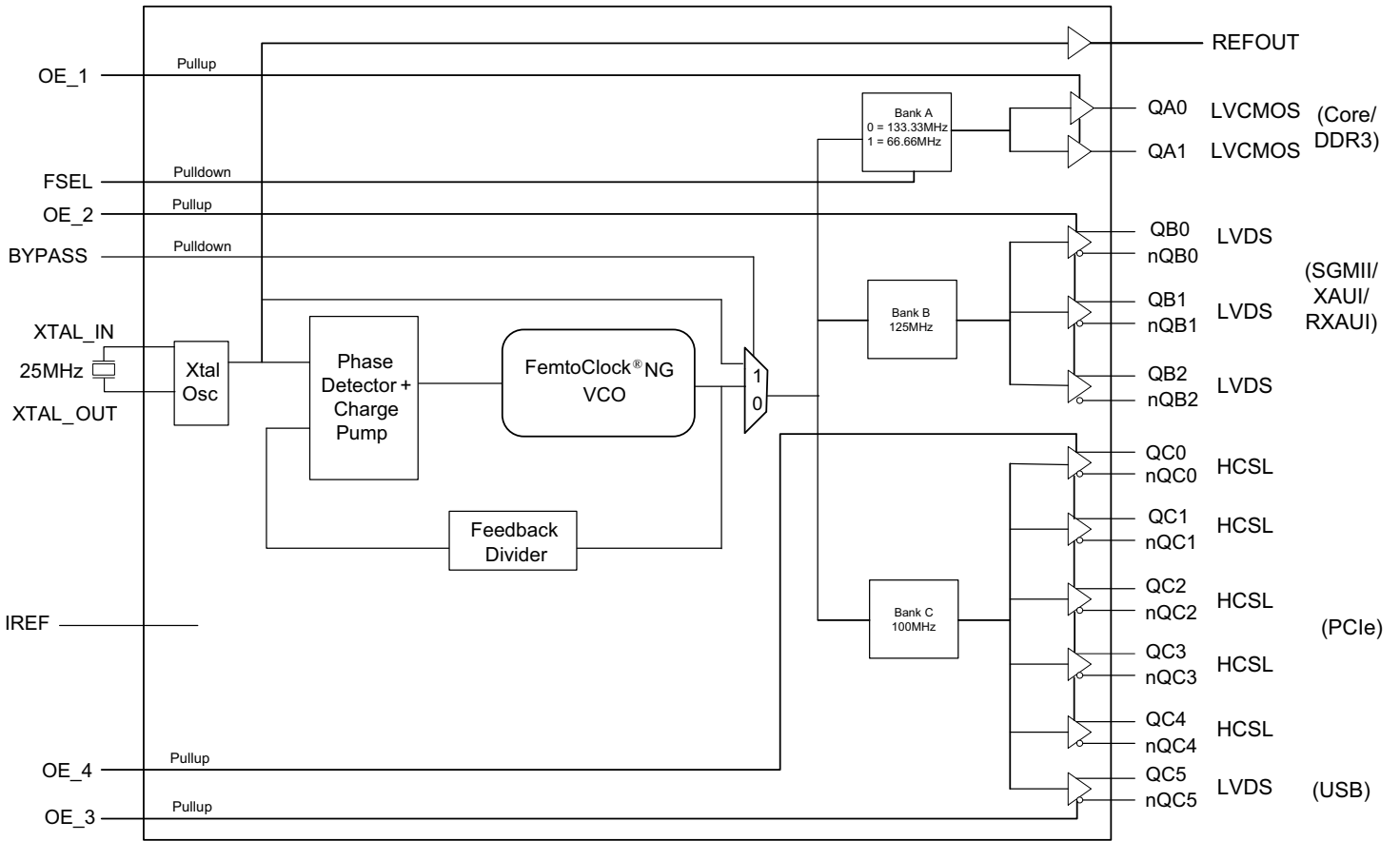
- Fourth Generation FemtoClock® NG PLL technology
- Two LVCMOS clock outputs for core/DDR3 at 133.33MHz or 66.66MHz
- One LVDS clock output for USB at 100MHz
- Three LVDS clock outputs for SGMII/XAUI at 125MHz
- Five HCSL clock outputs for PCIe at 100MHz
- Crystal oscillator interface designed for 25MHz ( $C_L = 12\text{pF}$ ) frequency, IDT Part #603-25-173
- PCI Express Gen 1 (2.5Gb/s), Gen 2 (5Gb/s) and Gen 3 (8Gb/s) jitter compliant
- Full 3.3V operating supply voltage
- Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

## Pin Assignment



56 Lead 8mm x 8mm VFQFN

# Block Diagram



## Pin Descriptions and Characteristics

Table 1. Pin Descriptions

| Number   | Name  | Type   |          | Description   |
|--|---|--------|----------|---|
| 1  | GND A   | Power  |          | Analog ground pin.  |
| 2  | V <sub>DDA</sub>  | Power  |          | Analog power supply pin.  |
| 3, 8, 43, 51, 56                               | GND   | Power  |          | Power supply ground pins.   |
| 4  | GND_XTAL  | Power  |          | XTAL ground pin.  |
| 5<br>6   | XTAL_IN,<br>XTAL_OUT  | Input  |          | Parallel resonant crystal interface. XTAL_IN is the input, XTAL_OUT is the output.  |
| 7  | V <sub>DD_XTAL</sub>  | Power  |          | XTAL power supply pin.  |
| 9  | V <sub>DDO_REFOUT</sub>                                       | Power  |          | REFOUT LVCMOS output supply pin.  |
| 10   | REFOUT  | Output |          | Reference clock output from crystal. LVCMOS/LVTTL interface levels.   |
| 11   | GND_REFOUT  | Power  |          | REFOUT LVCMOS output ground pin.  |
| 12   | V <sub>DDD</sub>  | Power  |          | Digital power supply pin.   |
| 13   | GNDD  |        |          | Digital ground pin.   |
| 14   | IREF  | Input  |          | HCSL current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for HCSL outputs. |
| 15, 20, 28                                     | V <sub>DDO_C</sub>  | Power  |          | Bank C HCSL output supply pins.   |
| 16, 17<br>18, 19<br>21, 22<br>24, 25<br>26, 27 | QC0, nQC0<br>QC1, nQC1<br>QC2, nQC2<br>QC3, nQC3<br>QC4, nQC4 | Output |          | Differential output pairs. HCSL interface levels.   |
| 23   | V <sub>SSO_C</sub>  | Power  |          | Bank C HCSL output ground pin.  |
| 29   | V <sub>DDO_C5</sub>   | Power  |          | Bank C LVDS QC5, nQC5 output power supply pin.  |
| 30, 31   | nQC5, QC5   | Output |          | Differential output pair. HCSL interface levels.  |
| 32   | V <sub>SSO_C5</sub>   | Power  |          | Bank C LVDS QC5, nQC5 output ground pin.  |
| 33, 39   | V <sub>SSO_B</sub>  | Power  |          | Bank B LVDS output ground pin.  |
| 34, 35<br>37, 38<br>40, 41                     | nQB2, QB2<br>nQB1, QB1<br>nQB0, QB0                           | Output |          | Differential output pairs. LVDS interface levels.   |
| 36, 42   | V <sub>DDO_B</sub>  | Power  |          | Bank B LVDS output supply pins.   |
| 44   | V <sub>SSO_A</sub>  | Power  |          | Bank A LVCMOS output ground pin.  |
| 45<br>46                                       | QA1<br>QA0  | Output |          | Single-ended LVCMOS/LVTTL outputs.  |
| 47   | V <sub>DDO_A</sub>  | Power  |          | Bank A LVCMOS output supply pin.  |
| 48   | FSEL  | Input  | Pulldown | Selects QAx output frequency. See “Table 3A. Frequency Select Table”.   |

| Number            | Name                     | Type  |          | Description   |
|-------------------|--------------------------|-------|----------|---|
| 49                | BYPASS                   | Input | Pulldown | PLL Bypass mode select pin. See Table 3C for function. LVCMOS/LVTTL interface levels.             |
| 50                | V <sub>DD</sub>          | Power |          | Power supply pin.   |
| 52, 53,<br>54, 55 | OE_1, OE_2<br>OE_3, OE_4 | Input | Pullup   | Output enable. LVCMOS/LVTTL interface levels. See <a href="#">"Table 3B. OE Function Table"</a> . |

NOTE: *Pulldown and Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions                | Minimum                          | Typical | Maximum | Units |
|-----------------------|-------------------------|--------------------------------|----------------------------------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       | XTAL_IN, XTAL_OUT not included |                                  | 3.5     |         | pF    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                                |                                  | 51      |         | kΩ    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                                |                                  | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance        | QA[0:1]                        | V <sub>DDO_A</sub> = 3.465V      |         | 14      | Ω     |
|                       |                         | REFOUT                         | V <sub>DDO_REFOUT</sub> = 3.465V |         | 30      | Ω     |

## Function Tables

**Table 3A. Frequency Select Table**

| FSEL        | QAx outputs |
|-------------|-------------|
| 0 (default) | 133.33MHz   |
| 1           | 66.66MHz    |

**Table 3B. OE Function Table**

| OEx         | Output State   |
|-------------|----------------|
| 0           | High Impedance |
| 1 (default) | Enabled        |

**Table 3C. PLL BYPASS Function Table**

| BYPASS      | Operation   |
|-------------|---|
| 1           | PLL is bypassed. The reference frequency is divided by the selected output dividers in Bank A, Bank B, Bank C. AC specifications do not apply in PLL BYPASS mode. |
| 0 (default) | PLL is enabled. The reference frequency is multiplied by the PLL feedback divider and then divided by the selected output dividers in Bank A, Bank B, Bank C.     |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item  | Rating                               |
|---|--------------------------------------|
| Supply Voltage, $V_{DD}$                    | 3.63V                                |
| Inputs, $V_I$<br>XTAL_IN<br>Other Inputs    | 0V to 2V<br>-0.5V to $V_{DD} + 0.5V$ |
| Outputs, $V_O$ (LVCMOS)                     | -0.5V to $V_{DDO\_A} + 0.5V$         |
| Outputs, $I_O$ (LVDS)<br>Continuous Current | 10mA<br>15mA                         |
| Outputs, $V_O$ (HCSL)                       | -0.5V to $V_{DDO\_C} + 0.5V$         |
| Junction Temperature, $T_J$                 | 125°C                                |
| Storage Temperature, $T_{STG}$              | -65°C to 150°C                       |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD\_X} = V_{DDO\_X} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol       | Parameter                                    | Test Conditions | Minimum        | Typical | Maximum  | Units |
|--------------|--|-----------------|----------------|---------|----------|-------|
| $V_{DD\_X}$  | Power Supply Voltage                         |                 | 3.135          | 3.3     | 3.465    | V     |
| $V_{DDA}$    | Analog Supply Voltage                        |                 | $V_{DD} - 0.1$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDO\_X}$ | Power Supply Voltage                         |                 | 3.135          | 3.3     | 3.465    | V     |
| $I_{DD\_X}$  | Power Supply Current                         |                 |                | 118     | 132      | mA    |
| $I_{DDA}$    | Analog Supply Current                        |                 |                | 52      | 58       | mA    |
| $I_{DDO\_X}$ | Power Supply Current; <a href="#">NOTE 1</a> |                 |                | 103     | 115      | mA    |

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

NOTE:  $V_{DDO\_X}$  denotes,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ ,  $V_{DDO\_C5}$ ,  $V_{DDO\_REFOUT}$ .

NOTE:  $I_{DD\_X}$  denotes,  $I_{DD}$ ,  $I_{DDD}$ ,  $I_{DD\_XTAL}$ .

NOTE:  $I_{DDO\_X}$  denotes,  $I_{DDO\_A} + I_{DDO\_B} + I_{DDO\_C} + I_{DDO\_C5} + I_{DDO\_REFOUT}$ .

NOTE: The device has a power sequence requirement, refer to the Application Section.

NOTE 1: HCSL outputs are disabled, LVDS outputs are terminated with 100Ω and LVCMOS, outputs enabled but without load.

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD\_X} = V_{DDO\_A} = V_{DDO\_REFOUT} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol   | Parameter           | Test Conditions | Minimum                        | Typical | Maximum        | Units |
|----------|---------------------|-----------------|--------------------------------|---------|----------------|-------|
| $V_{IH}$ | Input High Voltage  |                 | 2                              |         | $V_{DD} + 0.3$ | V     |
| $V_{IL}$ | Input Low Voltage   |                 | -0.3                           |         | 0.8            | V     |
| $I_{IH}$ | Input High Current  | FSEL, BYPASS    | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | μA    |
|          |                     | OE_[4:1]        | $V_{DD} = V_{IN} = 3.465V$     |         | 5              | μA    |
| $I_{IL}$ | Input Low Current   | FSEL, BYPASS    | $V_{DD} = 3.465V, V_{IN} = 0V$ | -5      |                | μA    |
|          |                     | OE_[4:1]        | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                | μA    |
| $V_{OH}$ | Output High Voltage | QA[0:1], REFOUT | $I_{OH} = -12mA$               | 2.6     |                | V     |
| $V_{OL}$ | Output High Voltage | QA[0:1], REFOUT | $I_{OL} = 12mA$                |         | 0.5            | V     |

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

**Table 4C. LVDS Output DC Characteristics,  $V_{DDO\_B} = V_{DDO\_C5} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage |                 | 247     |         | 454     | mV    |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   |                 |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              |                 | 1.25    |         | 1.375   | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   |                 |         |         | 50      | mV    |

**Table 5. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 25      |         | MHz      |
| Capacitance Loading ( $C_L$ )      |                 |             | 12      | 18      | pF       |
| Equivalent Series Resistance (ESR) |                 |             |         | 80      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE: IDT Part #603-25-173 recommended.

## AC Electrical Characteristics

**Table 6A. LVCMOS AC Electrical Characteristics,  $V_{DD\_X} = V_{DDO\_A} = V_{DDO\_REFOUT} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol         | Parameter   |         | Test Conditions  | Minimum | Typical | Maximum | Units  |
|----------------|---|---------|--|---------|---------|---------|--------|
| $f_{OUT}$      | Output Frequency  | REF_OUT |  |         | 25      |         | MHz    |
|                |   | QA[0:1] | FSEL = 1   |         | 66.66   |         | MHz    |
|                |   | QA[0:1] | FSEL = 0   |         | 133.33  |         | MHz    |
| $t_{JIT}$      | RMS Phase Jitter (Random); NOTE 1                             |         | $f_{OUT} = 133.33\text{MHz}$ ,<br>Integration Range (12kHz to 20MHz) |         | 0.27    | 0.40    | ps     |
|                |   |         | $f_{OUT} = 66.66\text{MHz}$ ,<br>Integration Range (12kHz to 20MHz)  |         | 0.29    | 0.45    | ps     |
| $\Phi_n(100)$  | Single-side Band Phase Noise for $f_{OUT} = 133.33\text{MHz}$ |         | 100Hz from Carrier   |         | -98     |         | dBc/Hz |
| $\Phi_n(1k)$   |   |         | 1kHz from Carrier  |         | -122    |         | dBc/Hz |
| $\Phi_n(10k)$  |   |         | 10kHz from Carrier   |         | -134    |         | dBc/Hz |
| $\Phi_n(100k)$ |   |         | 100kHz from Carrier  |         | -138    |         | dBc/Hz |
| $\Phi_n(1M)$   |   |         | 1MHz from Carrier  |         | -145    |         | dBc/Hz |
| $\Phi_n(10M)$  |   |         | 10MHz from Carrier   |         | -153    |         | dBc/Hz |
| $t_{JIT(cc)}$  | Cycle-to-Cycle Jitter; NOTE 2                                 |         | $f_{OUT} = 133.33\text{MHz}$   |         |         | 35      | ps     |
|                |   |         | $f_{OUT} = 66.66\text{MHz}$  |         |         | 40      | ps     |
| $t_{sk(o)}$    | Output Skew; NOTE 2, 3  | QA[0:1] |  |         |         | 30      | ps     |
| odc            | Output Duty Cycle   | REF_OUT |  | 47      |         | 53      | %      |
|                |   | QA[0:1] |  | 40      |         | 60      | %      |
| $t_R / t_F$    | Output Rise/ Fall Time  |         | 20% to 80%   | 275     |         | 800     | ps     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

NOTE: Characterized using IDT/ Fox Part #603-25-173 crystal.

NOTE 1: Refer to the phase noise plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

**Table 6B. LVDS AC Electrical Characteristics,  $V_{DD\_X} = V_{DDO\_B} = V_{DDO\_C5} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol         | Parameter  |                              | Test Conditions  | Minimum | Typical | Maximum | Units  |
|----------------|--|------------------------------|--|---------|---------|---------|--------|
| $f_{OUT}$      | Output Frequency                                     | QC5, nQC5                    |  |         | 100     |         | MHz    |
|                |  | QB[0:2], nQB[0:2]            |  |         | 125     |         | MHz    |
| $t_{JIT}$      | RMS Phase Jitter (Random);<br><a href="#">NOTE 1</a> |                              | $f_{OUT} = 100MHz$ ,<br>Integration Range (12kHz to 20MHz) |         | 0.27    | 0.45    | ps     |
|                |  |                              | $f_{OUT} = 125MHz$ ,<br>Integration Range (12kHz to 20MHz) |         | 0.21    | 0.35    | ps     |
| $\Phi_n(100)$  | Single-side Band Phase Noise for $f_{OUT} = 125MHz$  |                              | 100Hz from Carrier   |         | -93     |         | dBc/Hz |
| $\Phi_n(1k)$   |  |                              | 1kHz from Carrier  |         | -122    |         | dBc/Hz |
| $\Phi_n(10k)$  |  |                              | 10kHz from Carrier   |         | -135    |         | dBc/Hz |
| $\Phi_n(100k)$ |  |                              | 100kHz from Carrier  |         | -138    |         | dBc/Hz |
| $\Phi_n(1M)$   |  |                              | 1MHz from Carrier  |         | -146    |         | dBc/Hz |
| $\Phi_n(10M)$  |  |                              | 10MHz from Carrier   |         | -155    |         | dBc/Hz |
| $t_{JIT(cc)}$  | Cycle-to-Cycle Jitter;<br><a href="#">NOTE 2</a>     |                              | $f_{OUT} = 100MHz$   |         |         | 35      | ps     |
|                |  |                              | $f_{OUT} = 125MHz$   |         |         | 35      | ps     |
| $t_{sk(o)}$    | Output Skew;<br><a href="#">NOTE 2, 3</a>            | QB[0:2], nQB[0:2]            |  |         |         | 40      | ps     |
| odc            | Output Duty Cycle                                    | QB[0:2], nQB[0:2]; QC5, nQC5 |  | 47      |         | 53      | %      |
| $t_R / t_F$    | Output Rise/ Fall Time                               |                              | 20% to 80%   | 100     |         | 450     | ps     |
| $t_{DIS}$      | Output Disable Time                                  |                              |  |         | 50      |         | ns     |
| $t_{EN}$       | Output Enable Time                                   |                              |  |         | 650     |         | ns     |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

NOTE: Characterized using IDT/ Fox Part #603-25-173 crystal.

NOTE 1: Refer to the phase noise plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.



**Table 6C. HCSL AC Electrical Characteristics,  $V_{DD\_X} = V_{DDO\_C} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol             | Parameter  | Test Conditions  | Minimum | Typical | Maximum | Units  |
|--------------------|--|--|---------|---------|---------|--------|
| $f_{OUT}$          | Output frequency<br>QC[0:4],<br>nQC[0:4]                       |  |         | 100     |         | MHz    |
| $t_{JIT}$          | RMS Phase Jitter (Random);<br>NOTE 1                           | $f_{OUT} = 100MHz$ ,<br>Integration Range (12kHz to 20MHz) |         | 0.27    | 0.4     | ps     |
| $\Phi n(100)$      | Single-side Band Phase<br>Noise for $f_{OUT} = 100MHz$         | 100Hz from Carrier   |         | -101    |         | dBc/Hz |
| $\Phi n(1k)$       |  | 1kHz from Carrier  |         | -123    |         | dBc/Hz |
| $\Phi n(10k)$      |  | 10kHz from Carrier   |         | -136    |         | dBc/Hz |
| $\Phi n(100k)$     |  | 100kHz from Carrier  |         | -140    |         | dBc/Hz |
| $\Phi n(1M)$       |  | 1MHz from Carrier  |         | -147    |         | dBc/Hz |
| $\Phi n(10M)$      |  | 10MHz from Carrier   |         | -153    |         | dBc/Hz |
| $t_{JIT(CC)}$      | Cycle-to-Cycle Jitter;<br>NOTE 2                               | $f_{OUT} = 100MHz$   |         |         | 50      | ps     |
| $t_{sk(o)}$        | Output Skew;<br>NOTE 2, 3                                      | QC[0:4],<br>nQC[0:4]                                       |         |         | 70      | ps     |
| $t_{DIS}$          | Output Disable Time  |  |         | 30      |         | ns     |
| $t_{EN}$           | Output Enable Time   |  |         | 55      |         | ns     |
| $V_{MAX}$          | Absolute Maximum Output<br>Voltage; NOTE 4, 5                  |  |         |         | 1150    | mV     |
| $V_{MIN}$          | Absolute Minimum Output<br>Voltage; NOTE 4, 6                  |  | -150    |         |         | mV     |
| $V_{CROSS}$        | Absolute Crossing Voltage;<br>NOTE 4, 7, 8                     |  | 200     |         | 550     | mV     |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$<br>over all edges; NOTE 4, 8, 9 |  |         |         | 140     | mV     |
| $t_{SLEW\pm}$      | Rise/Fall Edge Rate;<br>NOTE 10, 11                            | Measured between<br>-150mV to +150mV                       | 0.6     |         | 4       | V/ns   |
| odc                | Output Duty<br>Cycle   | QC[0:4].<br>nQC[0:4]                                       | 47      |         | 53      | %      |

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

NOTE: Characterized using IDT/ Fox Part #603-25-173 crystal.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to the phase noise plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

NOTE 4: Measurement taken from single-ended waveform.

NOTE 5: Defined as the maximum instantaneous voltage including overshoot.

NOTE 6: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 7: Measured at crosspoint where the instantaneous voltage value of the rising edge of QCx equals the falling edge of nQCx. See Parameter Measurement Information Section.

NOTE 8: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoint for this measurement. See Parameter Measurement Information Section.

NOTE 9: Defined as the total variation of all crossing voltage of rising QCx and falling nQCx. This is the maximum allowed variance in the  $V_{CROSS}$  for any particular system. See Parameter Measurement Information Section.

NOTE 10: Measurement taken from a differential waveform.

NOTE 11: Measured from -150mV to +150mV on the differential waveform (derived from QCx minus nQCx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

See Parameter Measurement Information Section.

**Table 6D. PCI Express Jitter Specifications,  $V_{DD\_X} = V_{DDO\_C} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

| Symbol                                | Parameter  | Test Conditions   | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---------------------------------------|--|---|---------|---------|---------|-----------------------------|-------|
| $t_j$<br>(PCIe Gen 1)                 | Phase Jitter<br>Peak-to-Peak;<br><a href="#">NOTE 1, 4</a> | $f = 100MHz$ , 25MHz Crystal Input<br>Evaluation Band: 0Hz - Nyquist<br>(clock frequency/2) |         | 7.56    | 12.0    | 86.0                        | ps    |
| $t_{REFCLK\_HF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter RMS;<br><a href="#">NOTE 2, 4</a>             | $f = 100MHz$ , 25MHz Crystal Input<br>High Band: 1.5MHz - Nyquist<br>(clock frequency/2)    |         | 0.58    | 1.0     | 3.1                         | ps    |
| $t_{REFCLK\_LF\_RMS}$<br>(PCIe Gen 2) | Phase Jitter RMS;<br><a href="#">NOTE 2, 4</a>             | $f = 100MHz$ , 25MHz Crystal Input<br>Low Band: 10kHz - 1.5MHz                              |         | 0.05    | 1.0     | 3.0                         | ps    |
| $t_{REFCLK\_RMS}$<br>(PCIe Gen 3)     | Phase Jitter RMS;<br><a href="#">NOTE 3, 4</a>             | $f = 100MHz$ , 25MHz Crystal Input<br>Evaluation Band: 0Hz - Nyquist<br>(clock frequency/2) |         | 0.11    | 0.25    | 0.8                         | ps    |

NOTE:  $V_{DD\_X}$  denotes,  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DD\_XTAL}$ .

NOTE: Characterized using IDT/ Fox Part #603-25-173 crystal.

NOTE: Measurements done on QC[0:4]. nQC[0:4] output pairs.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.

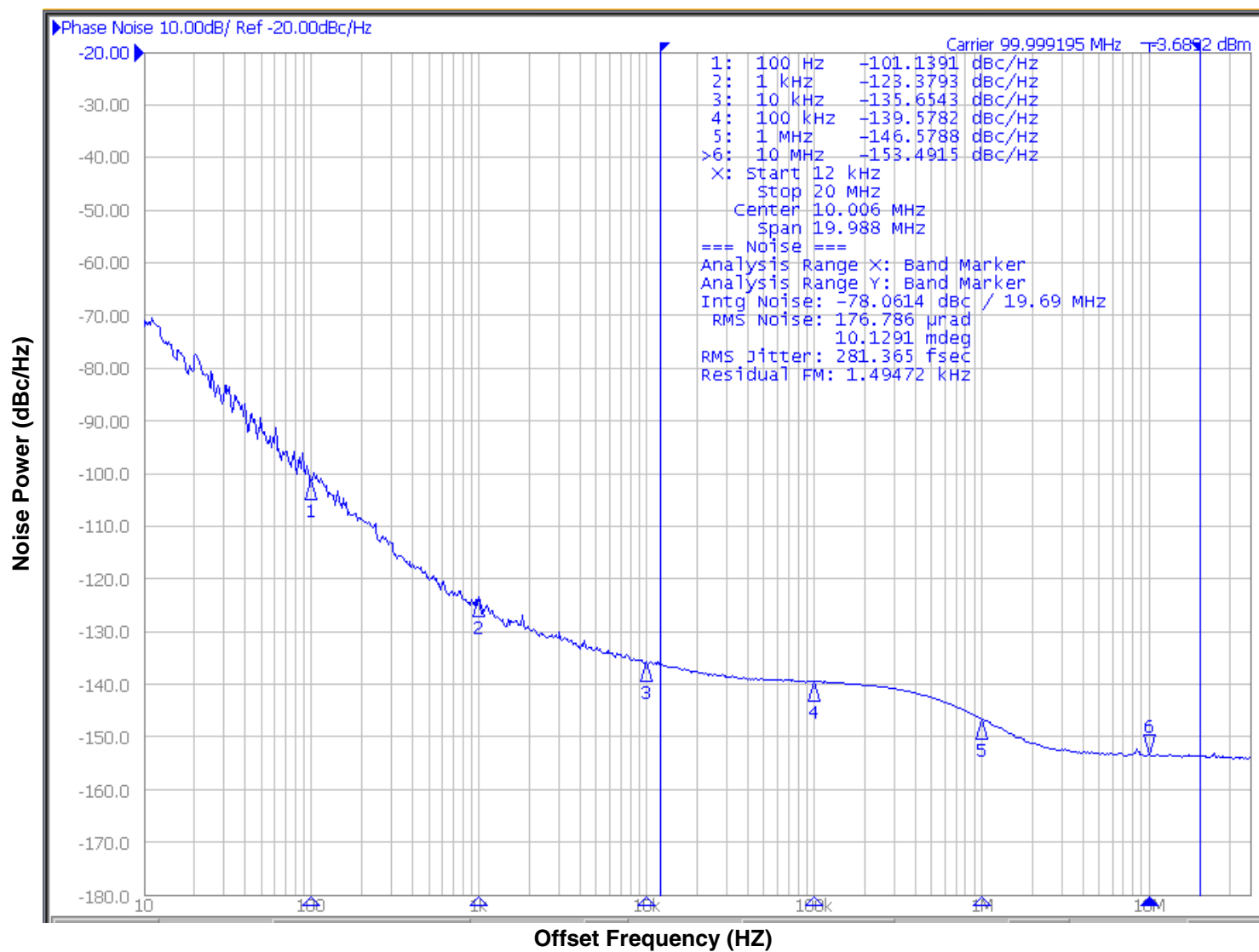
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of  $10^6$  clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

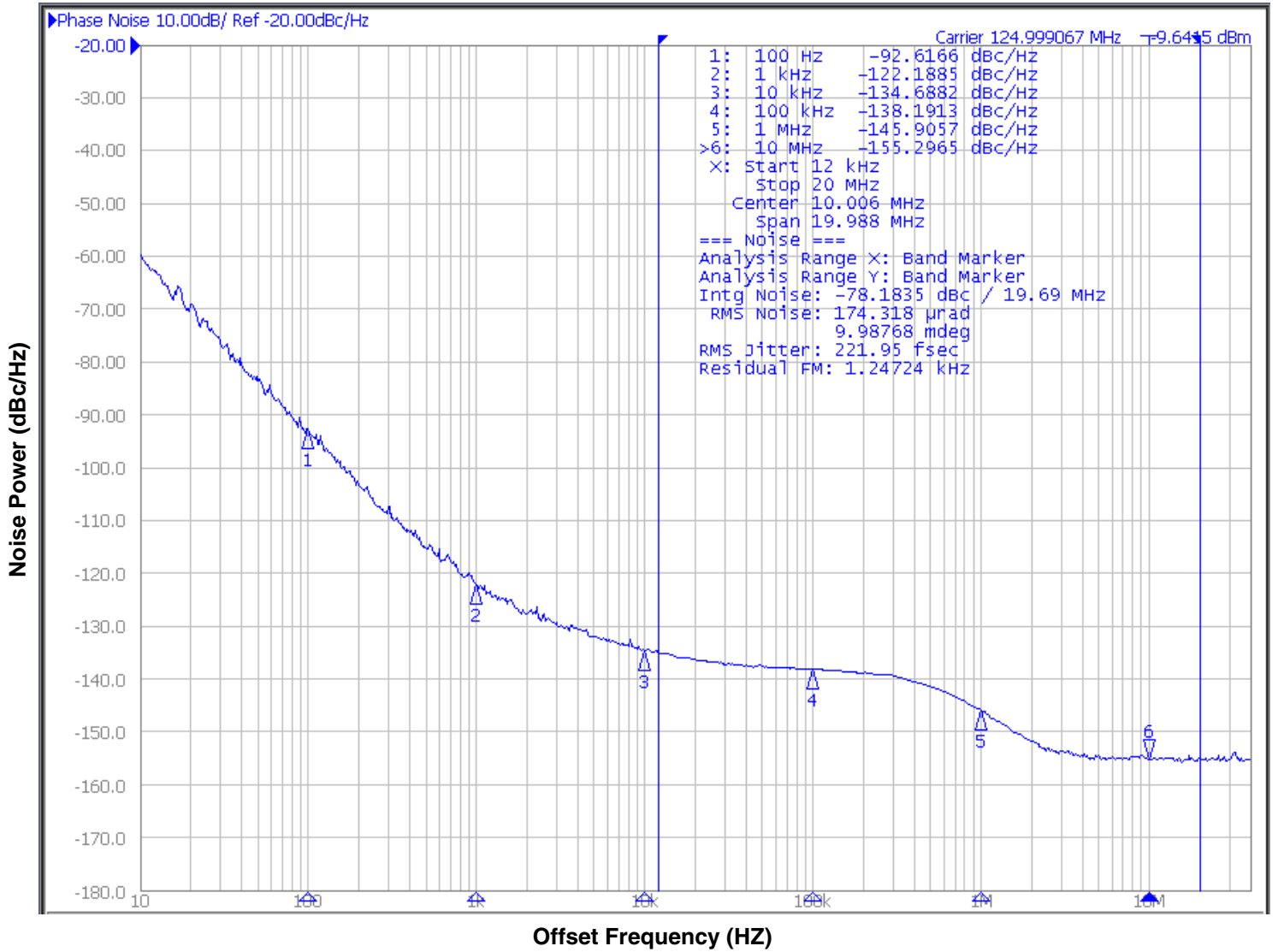
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

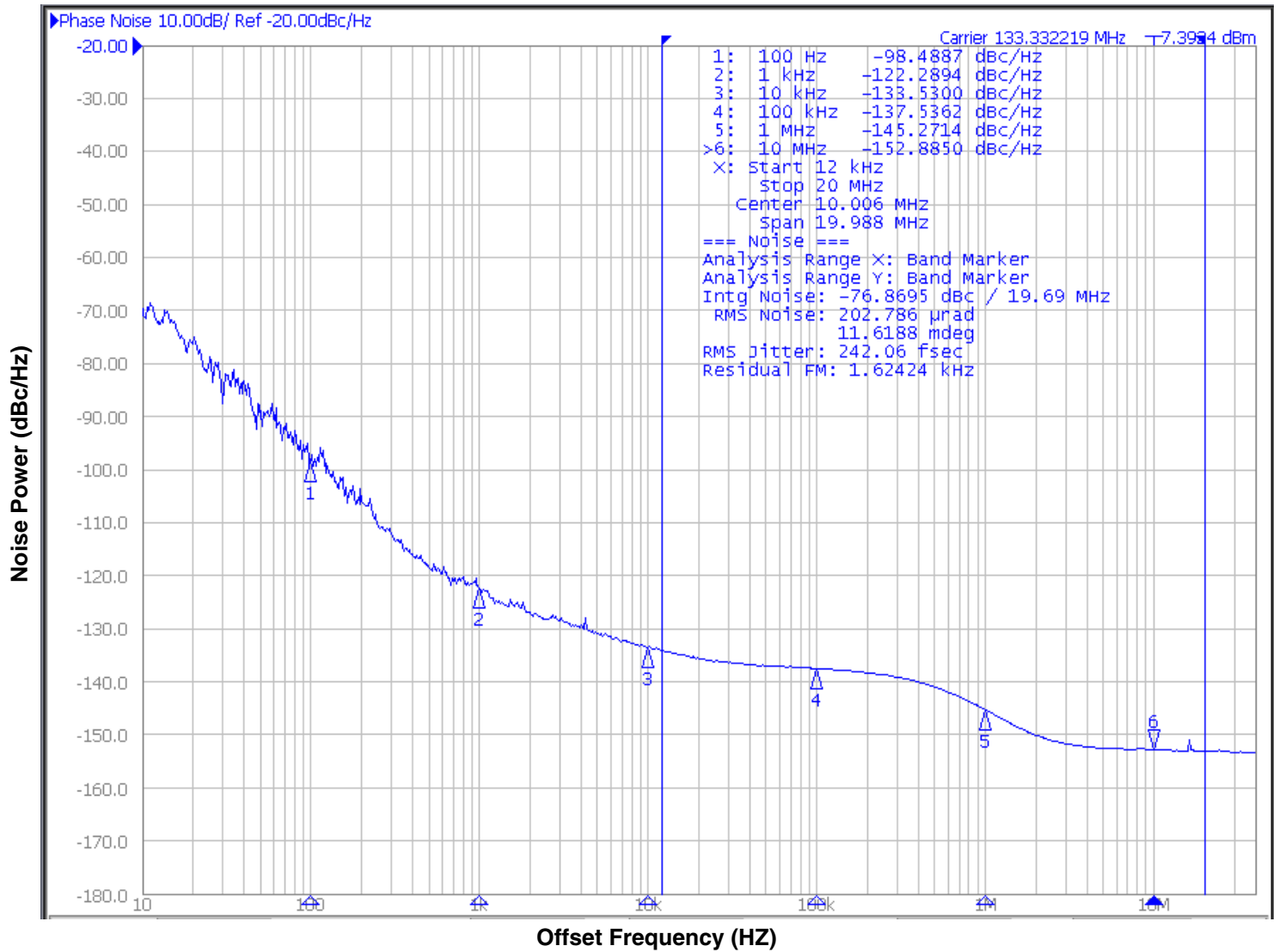
## HCSL Typical Phase Noise at 100MHz



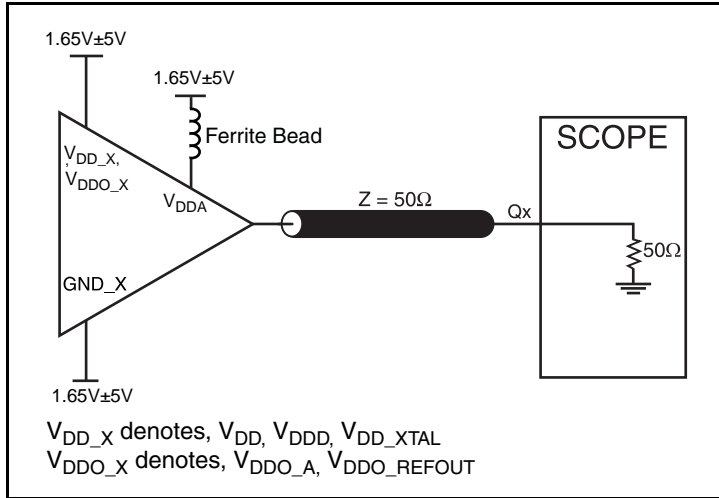
### LVDS Typical Phase Noise at 125MHz



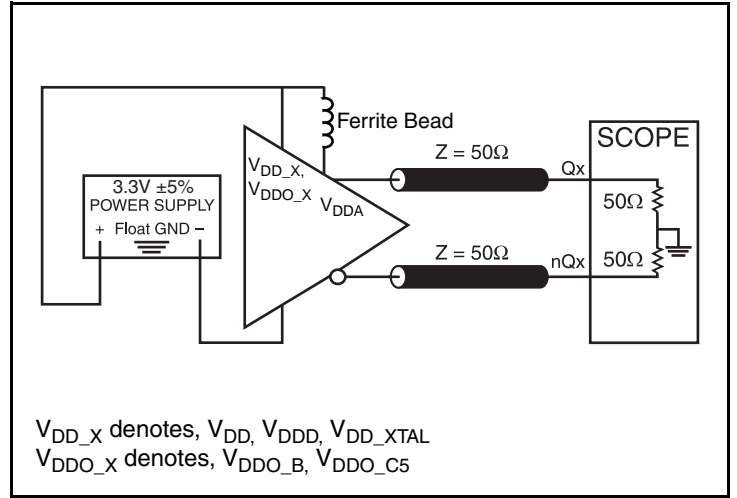
### LVCMOS Typical Phase Noise at 133.33MHz



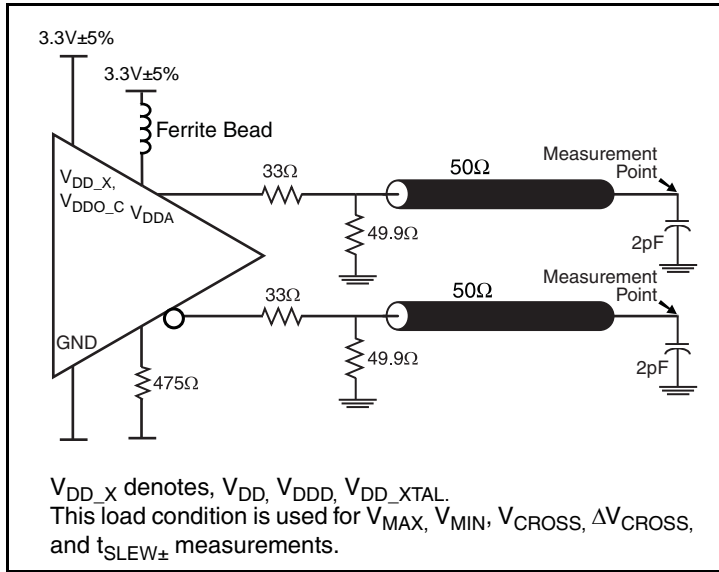
## Parameter Measurement Information



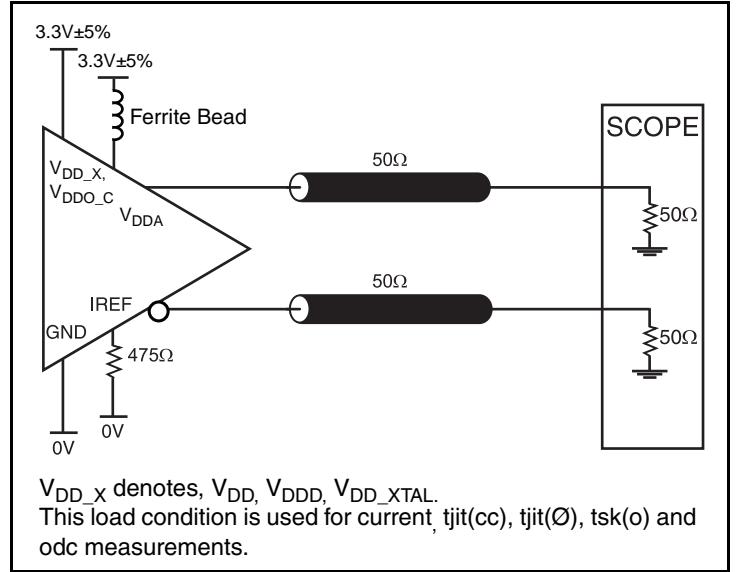
**LVC MOS Output Load Test Circuit**



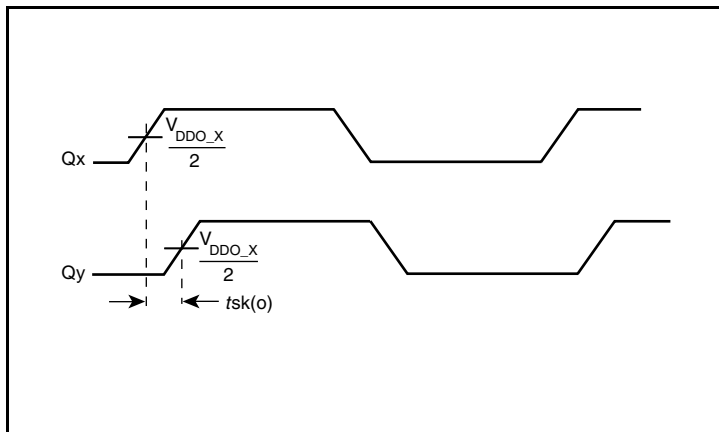
**LVDS Output Load Test Circuit**



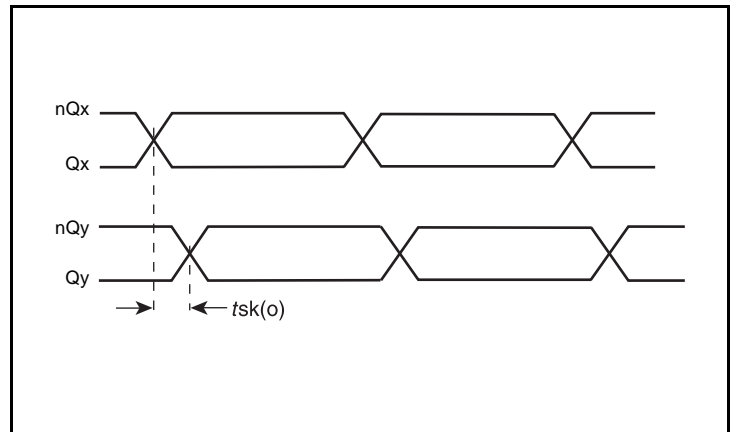
**HCSL Output Load Test Circuit**



**HCSL Output Load Test Circuit**

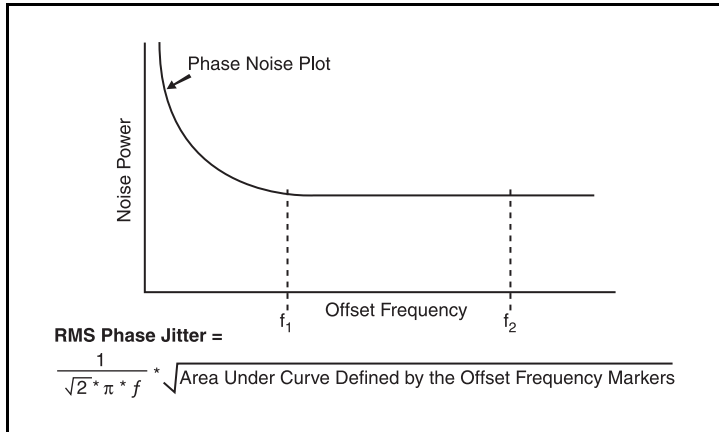


**LVC MOS Output Skew**

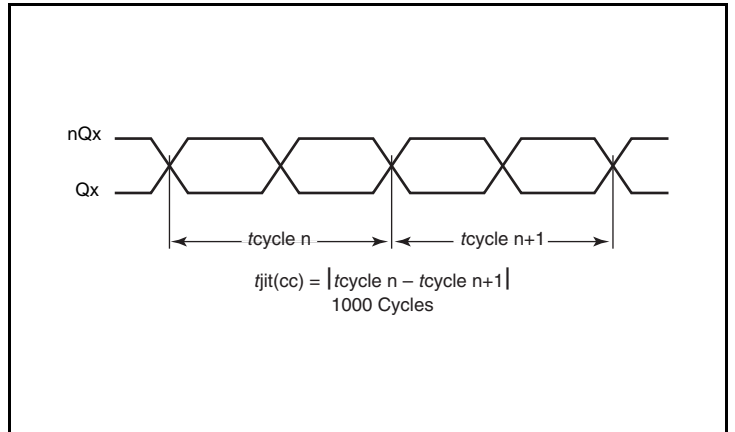


**Output Skew (Differential Outputs)**

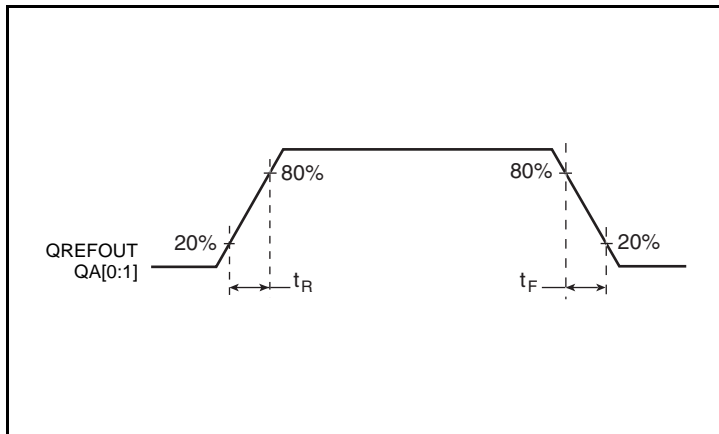
## Parameter Measurement Information, continued



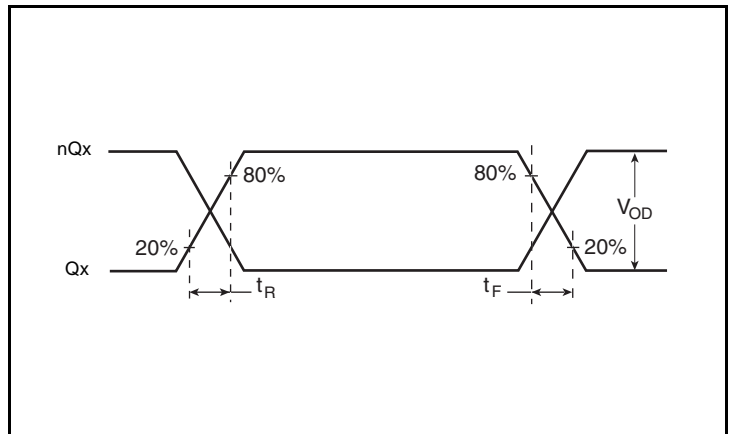
RMS Phase Jitter



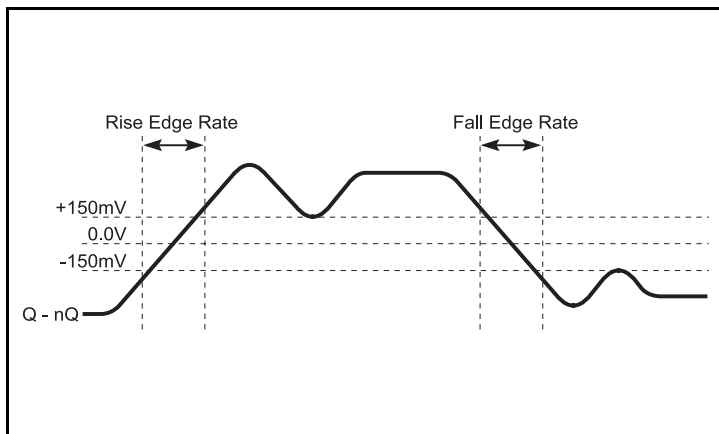
Cycle-to-Cycle Jitter (Differential Output)



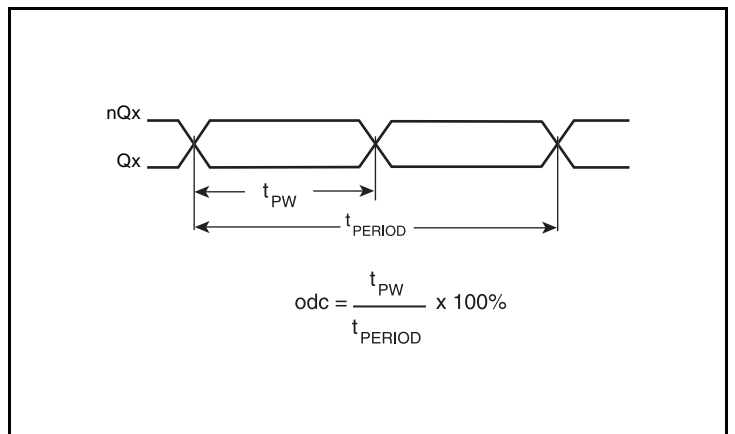
LVCMOS Output Rise/Fall Time



LVDS Output Rise/Fall Time

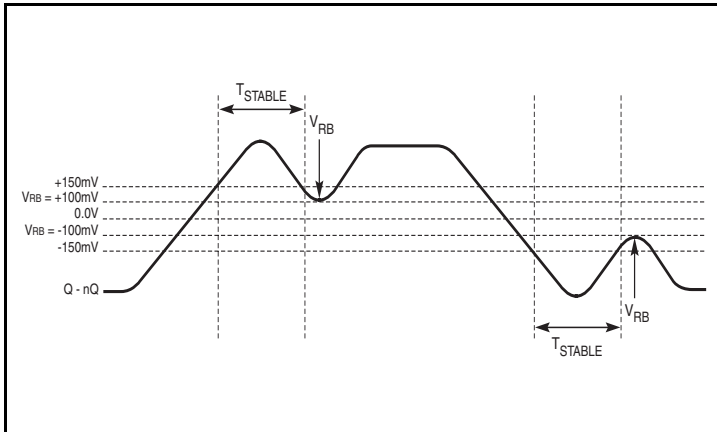


HCSL Output Points for Rise/Fall Edge Rate



Differential Output Duty Cycle

## Parameter Measurement Information, continued



HCSL Output Measurement Points for Ringback



## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. There should be no trace attached.

##### LVDS Outputs

All unused LVDS outputs can be either left floating or terminated with 100 $\Omega$  across. If they are left floating, there should be no trace attached.

##### HCSL Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### Power Supply Sequence Requirement

The 8V49N211 has a power supply sequence requirement.

This device requires that  $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DD\_XTAL}$ , and  $V_{DDD}$  are powered simultaneously.

This device has been characterized using the recommended power supply filtering techniques in the Schematic Example.

## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

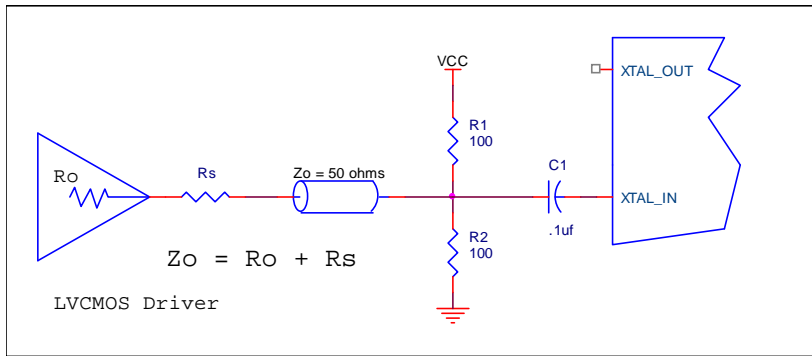


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

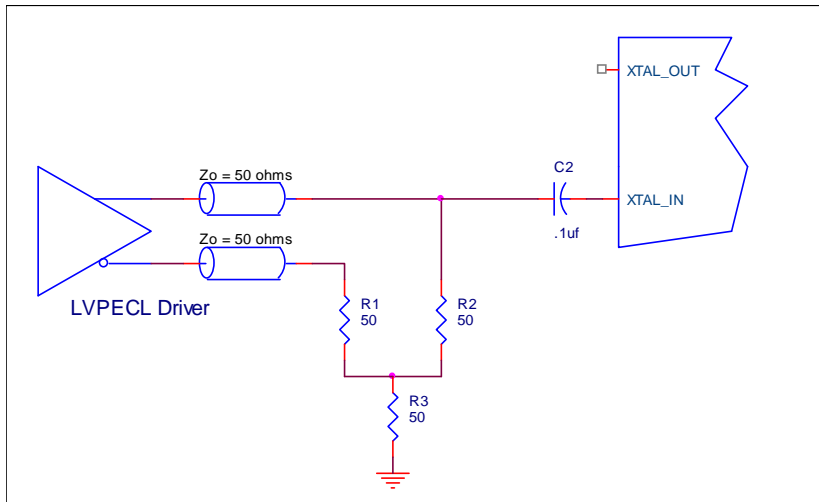
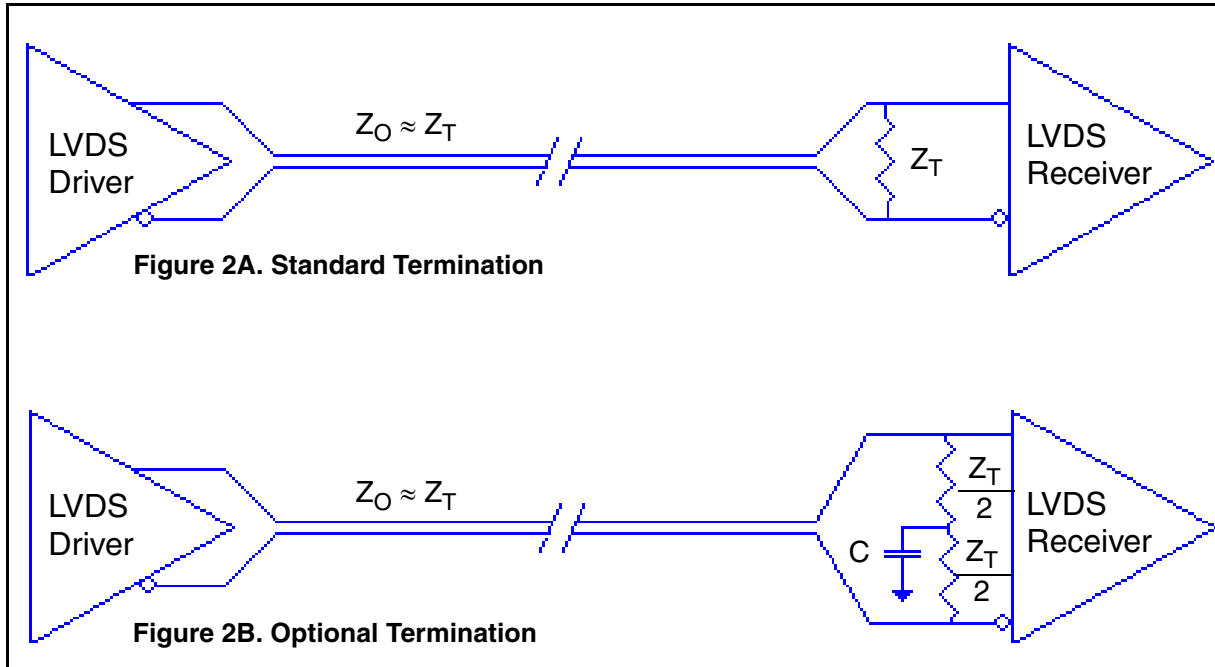


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

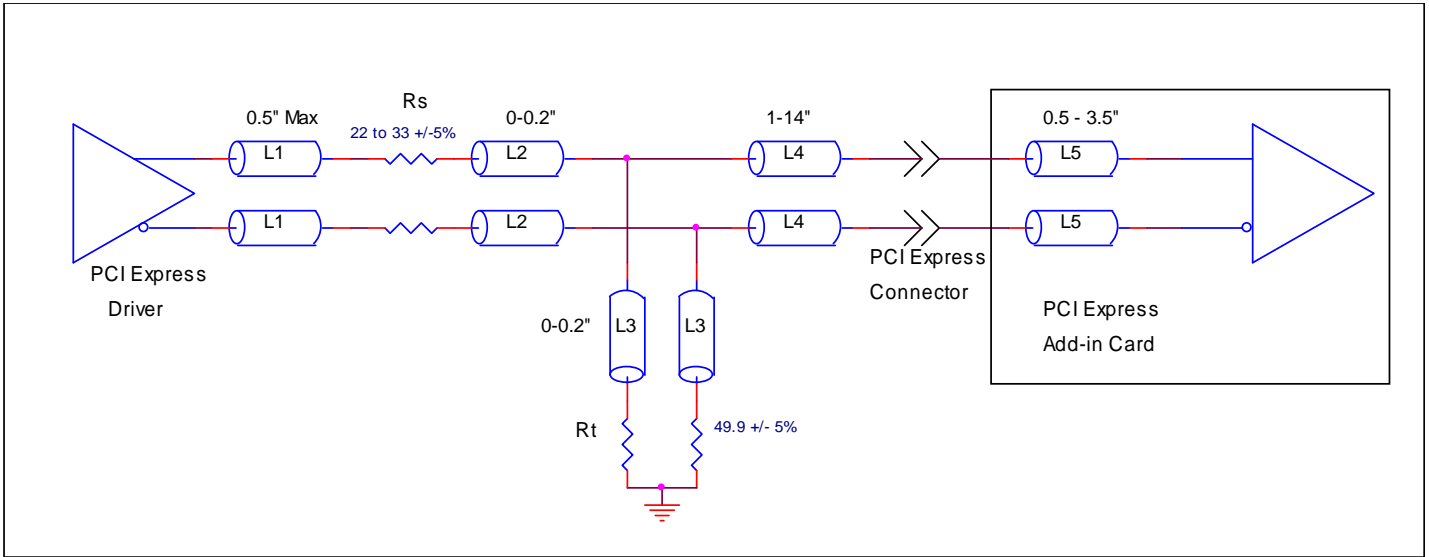


### LVDS Termination

## Recommended Termination

Figure 3A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

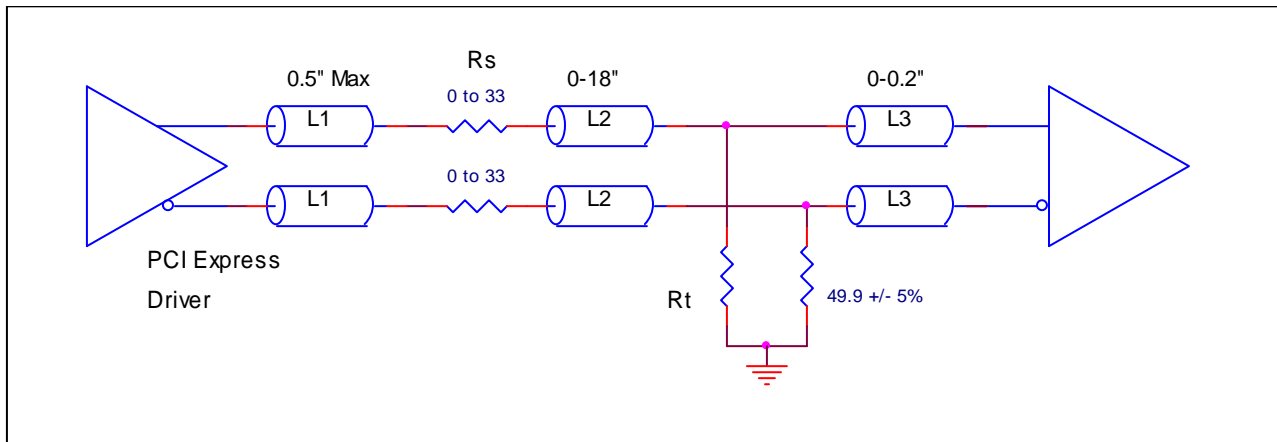
All traces should be 50Ω impedance single-ended or 100Ω differential.



**Figure 3A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)**

Figure 3B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.



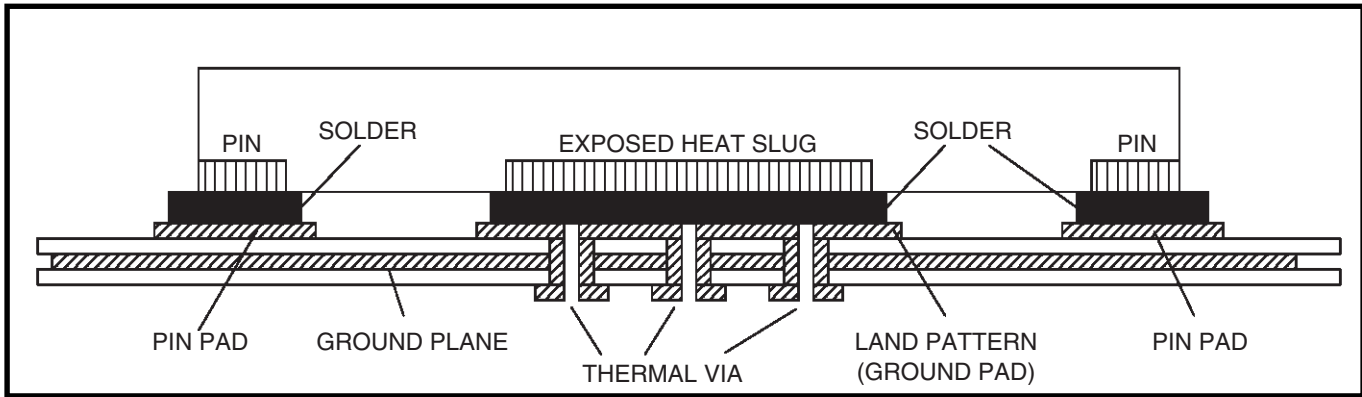
**Figure 3B. Recommended Termination (where a point-to-point connection can be used)**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

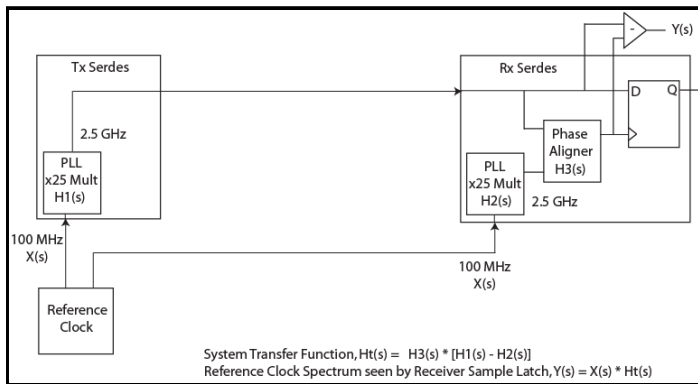
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

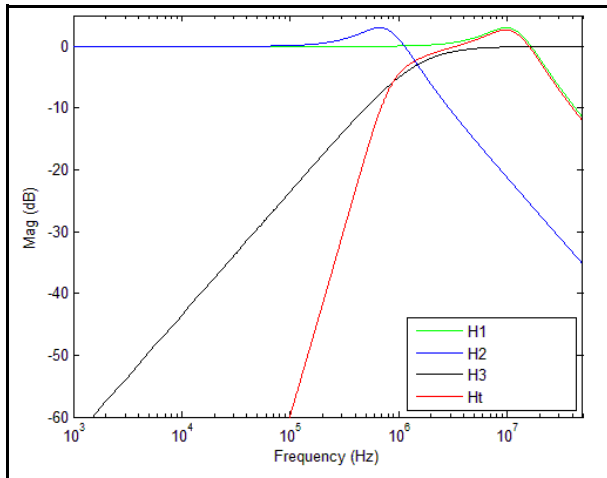
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on  $X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$ .



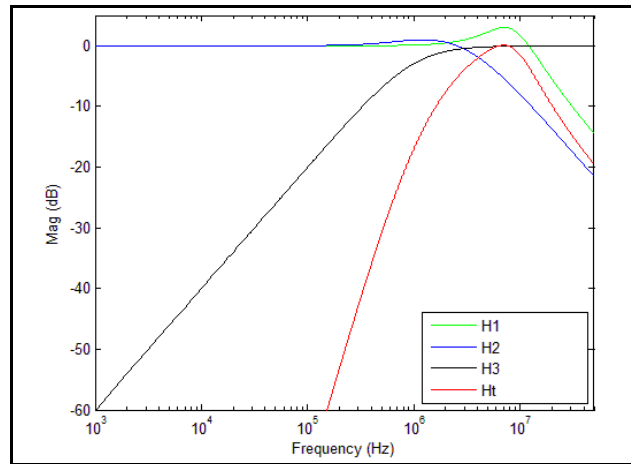
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g. for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

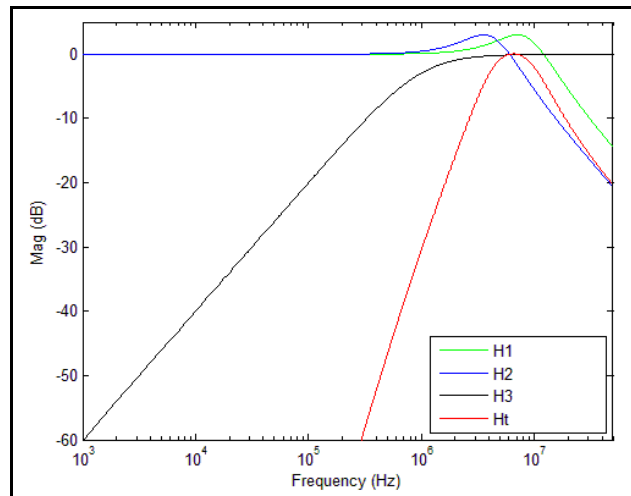


PCI Express Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

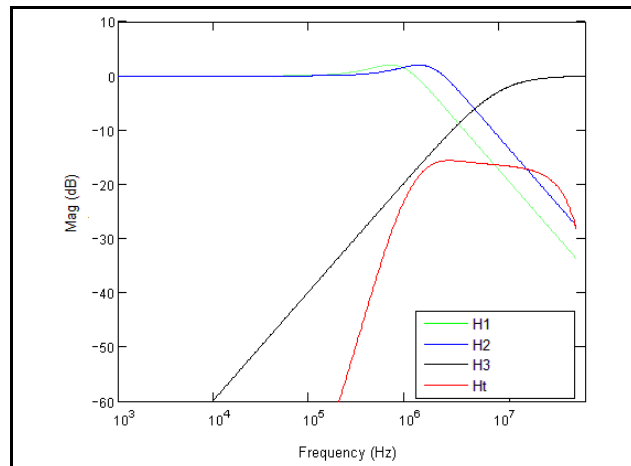


PCI Express Gen 2A Magnitude of Transfer Function



PCI Express Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCI Express Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

## Schematic Layout

Figure 5 shows an example 8V49N211 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. Input and output terminations shown are intended as examples only and may not represent the exact user configuration.

In this example a 12pF parallel resonant 25MHz crystal (IDT/ FOX Part #603-25-173) is used with the recommended load caps  $C1 = C2 = 2\text{pF}$ . Use a single point ground connection for the two load caps as shown in the schematic. The load caps are recommended for frequency accuracy, but these may be adjusted for different board layouts. Crystals with different load capacities may be used, but the load capacitors will have to be changed accordingly. If different crystal types are used, please consult IDT for recommendations.

Crystal layout is very important to minimize capacitive coupling between the crystal pads and leads and other metal in the circuit board. Capacitive coupling to other conductors has two adverse effects; it reduces the oscillator frequency leaving less tuning margin and noise coupling from power planes and logic transitions on signal traces can pull the phase of the crystal resonance, inducing jitter. Routing I<sup>2</sup>C under the crystal is a very common layout error, based on the assumption that it is a low frequency signal and will not affect the crystal oscillation. In fact, I<sup>2</sup>C transition times are short enough to capacitively couple into the crystal if they are routed close enough to the crystal traces.

In layout, all capacitive coupling to the crystal from any signal trace is to be minimized, that is to the XTAL\_IN and XTAL\_OUT pins, traces to the crystal pads, the crystal pads and the tuning capacitors. Using a crystal on the top layer as an example, void all signal and power layers under the crystal connections between the top layer and the ground plane used by the 8V49N211. Then calculate the parasitic capacity to the ground and determine if it is large enough to preclude tuning the oscillator. If the coupling is excessive, particularly if the first layer under the crystal is a ground plane, a layout option is to void the ground plane and all deeper layers until the next ground plane is

reached. The ground connection of the tuning capacitors should first be made between the capacitors on the top layer, then a single ground via is dropped to connect the tuning cap ground to the ground plane as close to the 8V49N211 as possible as shown in the schematic.

The schematic example shows two different HCSL output terminations; the standard termination for the case in which the HCSL receiver is on the same PCB as the 8V49N211 as well as the termination for an attached PCIe add-in card.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V49N211 provides separate  $V_{DD}$ ,  $V_{DDD}$ ,  $V_{DDA}$ ,  $V_{DD\_XTAL}$  and  $V_{DDO\_REF}$ ,  $V_{DDO\_A}$ ,  $V_{DDO\_B}$ ,  $V_{DDO\_C}$ , and  $V_{DDO\_C5}$  pins to isolate any high speed switching noise at the outputs from coupling into the internal PLL.

In order to achieve the best possible filtering, it is highly recommended that the 0.1 $\mu\text{F}$  capacitors be placed on the 8V49N211 side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10 $\mu\text{F}$  capacitors and the 0.1 $\mu\text{F}$  capacitors connected directly to 3.3V can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

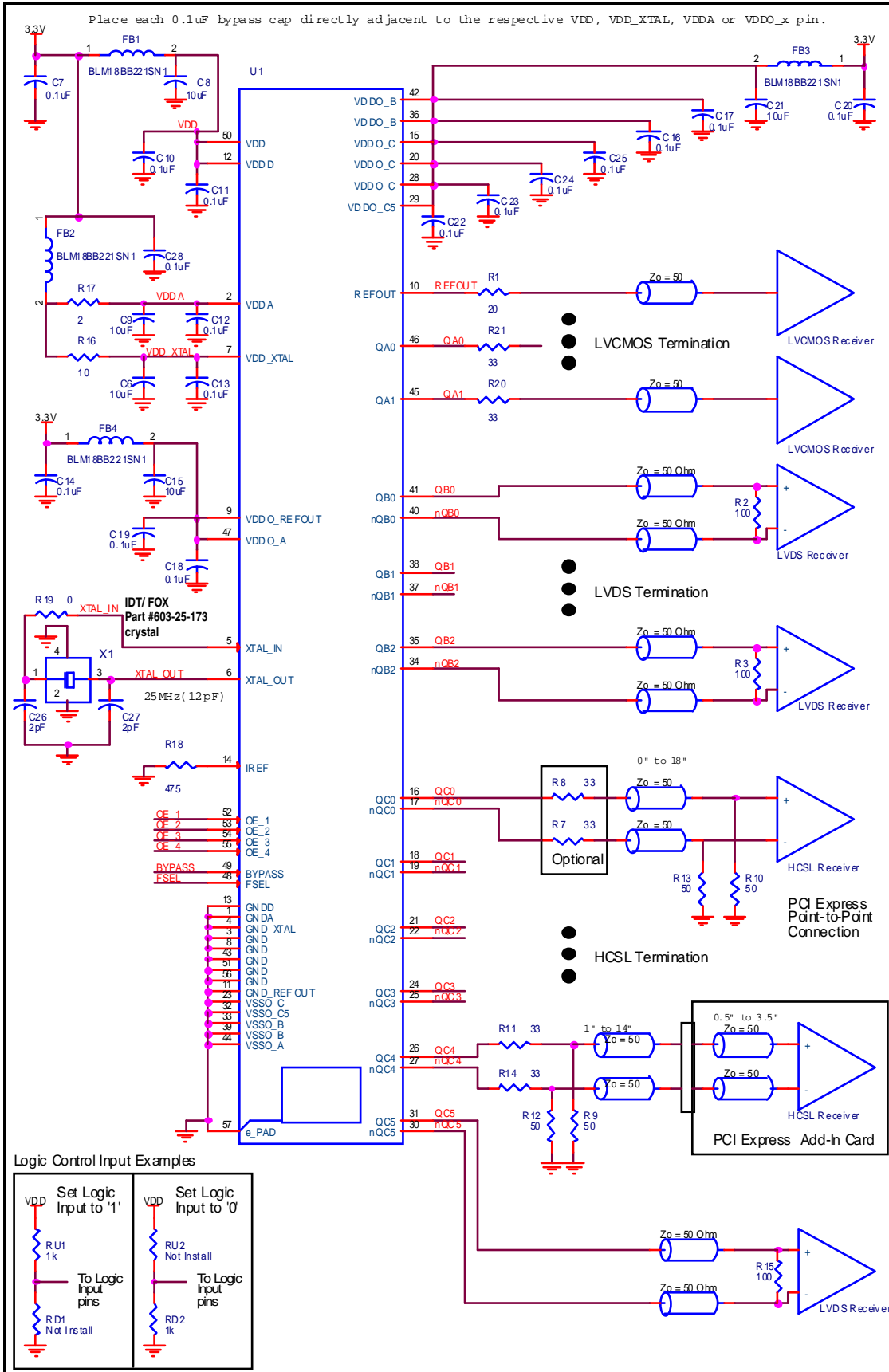


Figure 5. 8V49N211 Schematic Example



## Power Considerations

This section provides information on power dissipation and junction temperature for the 8V49N211. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8V49N211 is the sum of the core power plus the power dissipation due to the loading. The following is the power dissipation for  $V_{DD\_MAX} = 3.3V + 5\% = 3.465V$ , which gives worst case results at 85°C.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the outputs.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_X\_MAX} + I_{DDA\_MAX}) = 3.465V * (132mA + 58mA) = \mathbf{658.35mW}$
- HCSL Output Power (output)<sub>MAX</sub> = **44.5mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $5 * 44.5mW = \mathbf{222.5mW}$   
LVDS and LVCMOS Outputs Power (output)<sub>MAX</sub> =  $3.465V * 115mA = 398.475mW$

**Total Power<sub>MAX</sub> = 658.35mW + 222.5mW + 398.475mW = 1279.325mW**

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, the temperature at the junction of the bond wire and bond pad, directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T<sub>j</sub>, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 30.5°C/W per Table 7 below.

Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 1.279\text{W} * 30.5^\circ\text{C/W} = 124^\circ\text{C. This is below the limit of } 125^\circ\text{C.}$$

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

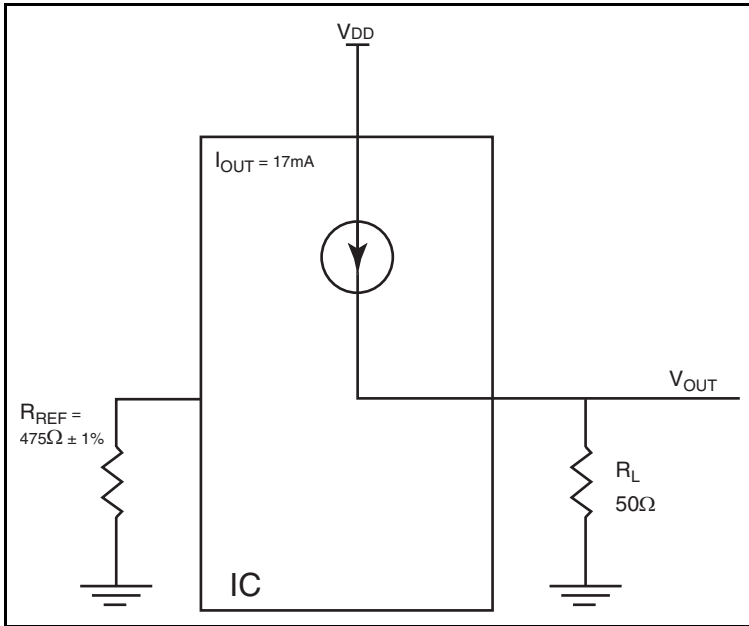
**Table 7. Thermal Resistance  $\theta_{JA}$  for 56 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 30.5°C/W | 26.4°C/W | 24.7°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate power dissipation on the IC per HCSL output pairs.

HCSL output driver circuit and termination are shown in *Figure 6*.



**Figure 6. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at  $V_{DD\_MAX}$ .

$$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$$

since  $V_{OUT} = I_{OUT} * R_L$

$$\begin{aligned} \text{Power} &= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT} \\ &= (3.465V - 17mA * 50\Omega) * 17mA \end{aligned}$$

Total Power Dissipation per output pair = 44.5mW

## Reliability Information

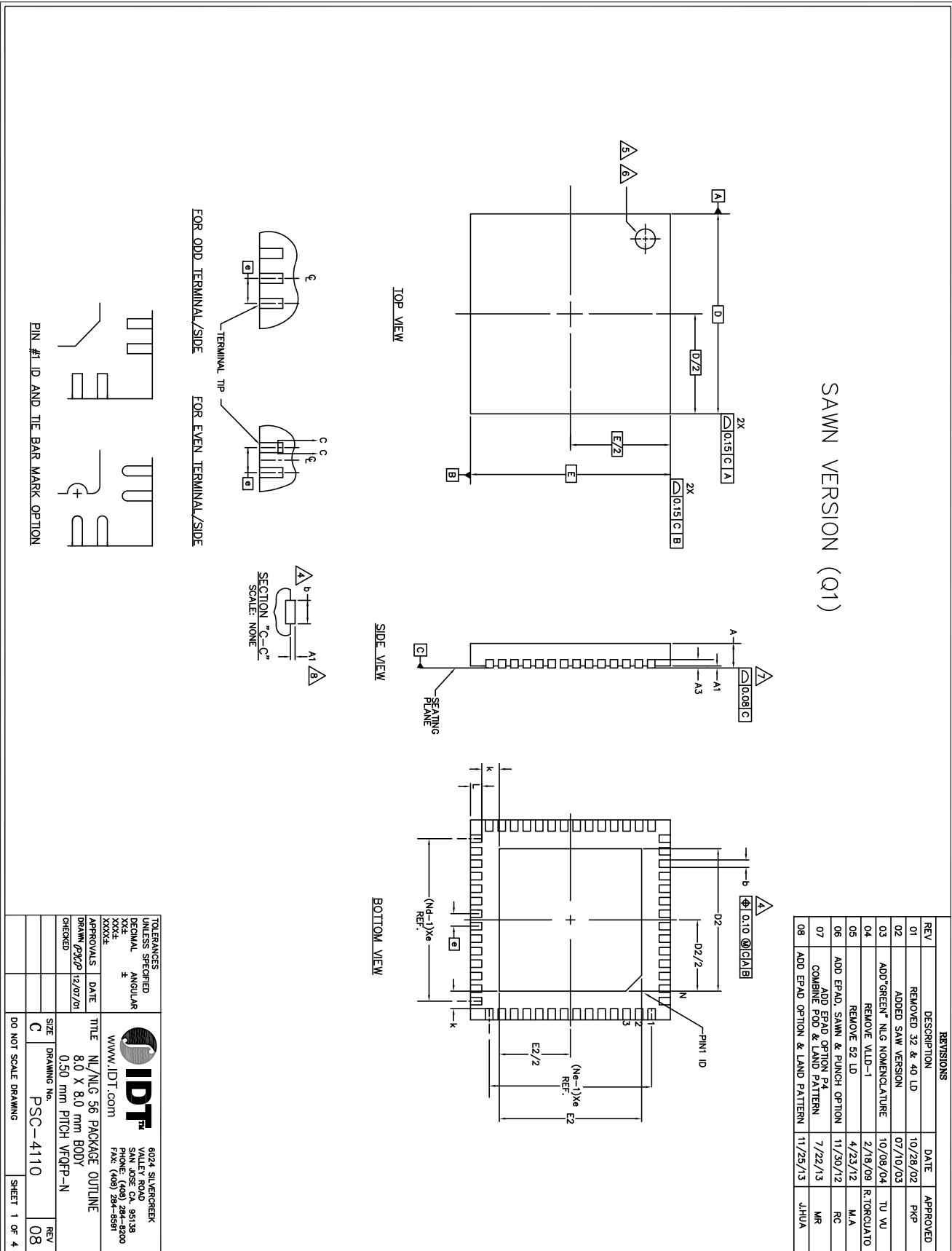
**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 56 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow                  |           |          |          |
|---|-----------|----------|----------|
| Meters per Second                           | 0         | 1        | 2        |
| Multi-Layer PCB, JEDEC Standard Test Boards | 30.5 °C/W | 26.4°C/W | 24.7°C/W |

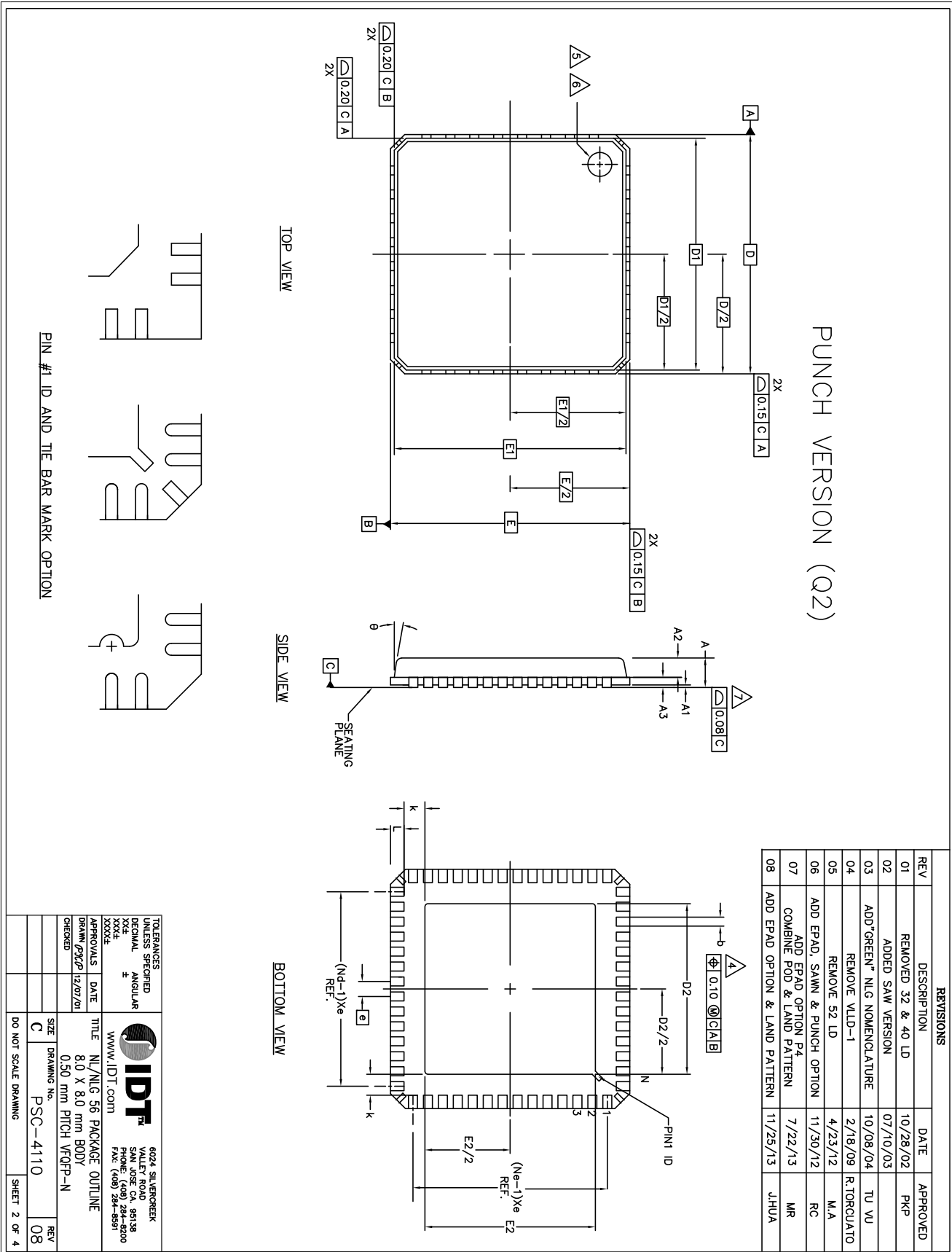
## Transistor Count

The transistor count for 8V49N211 is: 174,888

# 56 Lead VFQFN Package Outline and Package Dimensions



56 Lead VFQFN Package Outline and Package Dimensions, continued



56 Lead VFQFN Package Outline and Package Dimensions, continued

| REVISIONS |   |          |             |
|-----------|---|----------|-------------|
| REV       | DESCRIPTION                                       | DATE     | APPROVED    |
| 01        | REMOVED 32 & 40 LD                                | 10/28/02 | PRP         |
| 02        | ADDED S&M VERSION                                 | 07/10/03 | TU YU       |
| 03        | ADD CROWN* NLG NOMENCLATURE                       | 10/09/04 | TU YU       |
| 04        | REMOVE VLD-1                                      | 2/19/09  | R.TORIGIATO |
| 05        | REMOVE 52 LD                                      | 4/23/12  | M.A         |
| 06        | ADD EPAD, S&M & PUNCH OPTION                      | 11/20/12 | RC          |
| 07        | ADD EPAD OPTION P4<br>COMBINE FOOT & LAND PATTERN | 7/22/13  | HR          |
| 08        | ADD EPAD OPTION & LAND PATTERN                    | 11/25/13 | JHKA        |

PUNCH OPTION

| Q         |      |            |      |
|-----------|------|------------|------|
| DIMENSION | MIN. | NOM.       | MAX. |
| P         | -    | -          | 0.60 |
| D1        | -    | 7.75 BASIC | -    |
| E1        | -    | 7.75 BASIC | -    |
| A2        | -    | 0.65       | 0.70 |

EPAD OPTION


| DIMENSION | P1   |      |      | P2   |      |      | P3   |      |      | P4   |      |      |
|-----------|------|------|------|------|------|------|------|------|------|------|------|------|
|           | MIN  | NOM  | MAX  | MIN  | NOM  | MAX  | MIN  | NOM  | MAX  | MIN  | NOM  | MAX  |
| E2        | 6.15 | 6.30 | 6.45 | 6.45 | 6.45 | 6.45 | 6.60 | 6.75 | 5.05 | 5.20 | 5.35 | 5.80 |
| D2        | 6.15 | 6.30 | 6.45 | 6.45 | 6.45 | 6.45 | 6.60 | 6.75 | 4.35 | 4.50 | 4.65 | 5.80 |
|           |      |      |      |      |      |      |      |      |      |      |      | 5.90 |
|           |      |      |      |      |      |      |      |      |      |      |      | 6.00 |

| P5        |      |      |      |
|-----------|------|------|------|
| DIMENSION | MIN  | NOM  | MAX  |
| E2        | 5.95 | 6.05 | 6.15 |
| D2        | 5.95 | 6.05 | 6.15 |

COMMON DIMENSION

| DIMENSION | MIN.            | NOM. | MAX. |
|-----------|-----------------|------|------|
| Q         | 0.50 BSC        |      |      |
| N         | 56              |      |      |
| Nd        | 14              |      |      |
| Ne        | 14              |      |      |
| L         | 0.30            | 0.40 | 0.50 |
| b         | 0.18            | 0.25 | 0.30 |
| D2        | SEE EPAD OPTION |      |      |
| E2        | SEE EPAD OPTION |      |      |
| A         | 0.80            | 0.9  | 1.00 |
| A1        | 0.00            | 0.02 | 0.05 |
| A3        | 0.20 REF.       |      |      |
| D         | 8.00 BSC        |      |      |
| E         | 8.00 BSC        |      |      |
| θ         | -               | -    | 12°  |
| k         | 0.20            | -    | -    |

- NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M, - 1994.
  2. N IS THE NUMBER OF TERMINALS.  
Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &  
Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
  3. ALL DIMENSIONS ARE IN MILLIMETERS.
  4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
  5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
  6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
  7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
  8. APPLIED ONLY FOR TERMINALS.
  9. NOT AN ACTUAL IO.

|                             |                                 |   |
|-----------------------------|---------------------------------|---|
| TOLERANCES UNLESS SPECIFIED |                                 | <br>6024 SILVERCREEK VALLEY ROAD<br>SAN JOSE CA, 95138<br>PHONE (408) 284-8200<br>FAX (408) 284-8881 |
| DECIMAL                     | ANGULAR                         |   |
| XXXX                        | Z                               |   |
| XXXXX                       |                                 |   |
| WWW.IDT.COM                 | TITLE N/ NLG 56 PACKAGE OUTLINE |   |
| APPROVALS                   | DATE                            | SIZE 8.0 X 8.0 mm BODY  |
| DRAWN 09/20/07              | 12/07/01                        | 0.50 mm PITCH VFQFP-N   |
| CHECKED                     |                                 | DRAWING No. PSC-4110  |
|                             |                                 | REV 08  |
|                             |                                 | SHEET 3 OF 4  |

## Ordering Information

Table 9. Ordering Information Table

| Part/Order Number | Marking         | Package                  | Shipping Packaging | Temperature   |
|-------------------|-----------------|--------------------------|--------------------|---------------|
| 8V49N211NLGI      | IDT8V49N211NLGI | Lead-Free, 56-lead VFQFN | Tray               | -40°C to 85°C |
| 8V49N211NLGI8     | IDT8V49N211NLGI | Lead-Free, 56-lead VFQFN | Tape & Reel        | -40°C to 85°C |

## Revision History Sheet

| Rev | Table | Page   | Description of Change   | Date    |
|-----|-------|--|---|---------|
| B   |       | 1  | Features Section - updated Crystal bullet.                          | 5/29/15 |
|     | T5    | 6  | Crystal Characteristics Table - added note.                         |         |
|     | T6A   | 7  | LVC MOS AC Electrical Characteristics Table - updated Crystal note. |         |
|     | T6B   | 8  | LVDS AC Electrical Characteristics Table - updated Crystal note.    |         |
|     | T6C   | 9  | HCSL AC Electrical Characteristics Table - updated Crystal note.    |         |
|     | T6D   | 10   | PCI Express Jitter Specifications Table - updated Crystal note.     |         |
|     |       | 23   | Schematic Layout - Updated first sentence in second paragraph.      |         |
|     | 24    | Schematic Example - updated Crystal information. |   |         |
|     |       |  |   |         |
|     |       |  |   |         |





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