SYNCHRONOUS ETHERNET PLL

8V89307

DATASHEET

Revision 8
April 12, 2016

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FEATURES

HIGHLIGHTS

- Features 15 mHz to 560 Hz bandwidth
- Provides node clock for ITU-T G.8261/G.8262 Synchronous Ethernet (SyncE)
- Supports GR-253-CORE (OC-192) and ITU-T G.813 (STM-64) jitter generation requirements
- Provides clocks for 1 Gigabit and 10 Gigabit Ethernet applications

MAIN FEATURES

- Provides an integrated single-chip solution for Synchronous Equipment Timing Source, including Stratum 3, 4E, 4, SMC, EEC-Option 1 and EEC-Option 2 Clocks
- Supports 1PPS input and output
- Employs PLL architecture to feature excellent jitter performance and minimize the number of external components
- Supports programmable DPLL bandwidth (15 mHz to 560 Hz) and damping factor (1.2 to 20 in 5 steps)
- Supports $1.1X10^{-5}$ ppm absolute holdover accuracy and $4.4X10^{-8}$ ppm instantaneous holdover accuracy
- Provides 2 differential output clocks whose frequencies cover from 1Hz (1PPS) to 644.53125 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS outputs
  - Includes 25.78125 MHz, 128.90625 MHz and 161.1328125 MHz for CMOS outputs
  - Includes 25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential outputs
  - Includes 25.78125 MHz, 128.90625 MHz, 161.1328125 MHz, 322.265625 MHz and 644.53125 MHz for differential outputs
- Provides 1 single ended output clock whose frequencies cover from 1 Hz (1PPS) to 156.25 MHz
- Provides 2 differential input clocks whose frequency cover from 1 Hz (1PPS) to 625 MHz
  - Includes 25 MHz, 125 MHz and 156.25 MHz for CMOS inputs
  - Includes 25 MHz, 125 MHz, 156.25 MHz, 312.5 MHz and 625 MHz for differential inputs
- Provides 1 single ended input clock whose frequencies cover from 1 Hz (1PPS) to 156.25 MHz
- Supports Forced or Automatic operating mode switch controlled by an internal state machine
- Automatic state machine supports Free- Run, Locked and Holdover
- Supports manual and automatic selected input clock switch
- Supports automatic hitless selected input clock switch on clock failure
- Supports Telcordia GR-1244-CORE, Telcordia GR-253-CORE, ITU-T G.812, ITU-T G.8262, ITU-T G.813 and ITU-T G.783 recommendations

OTHER FEATURES

- Microprocessor interface modes: I2C and Serial
- IEEE 1149.1 JTAG Boundary Scan
- Single 3.3 V operation with 5 V tolerant CMOS I/Os
- 72-pin QFN package, green package options available

APPLICATIONS

- 1 Gigabit Ethernet and 10 Gigabit Ethernet
- Synchronous Ethernet equipment
- Core and access IP switches / routers
- Gigabit and terabit IP switches / routers
- IP and ATM core switches and access equipment
- Broadband and multi-service access equipment

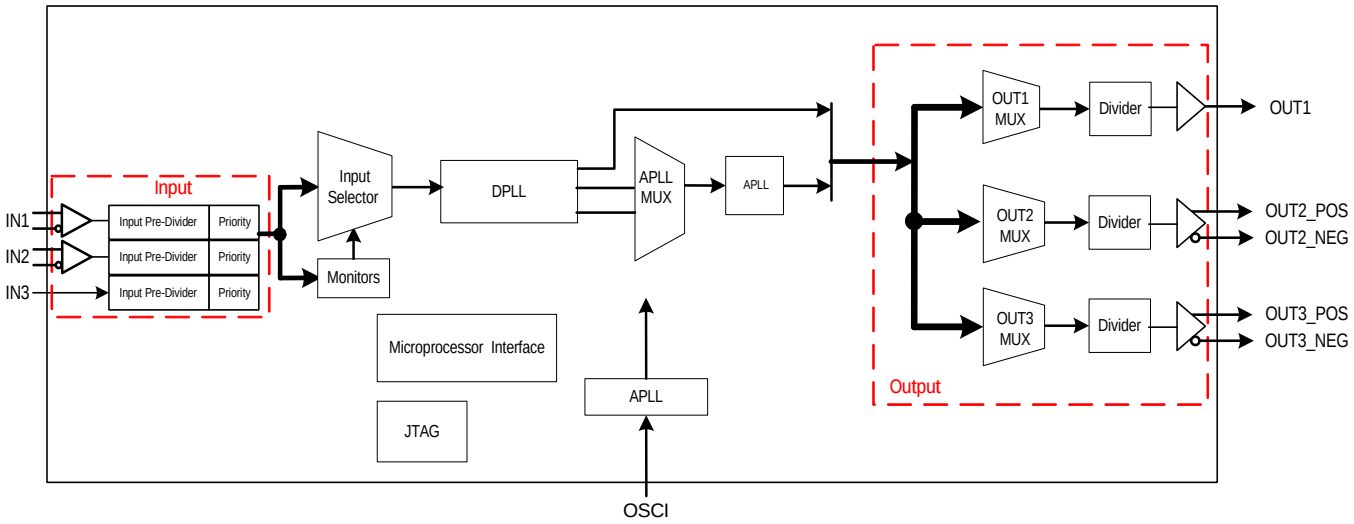

Figure 1. Functional Block Diagram

DESCRIPTION

The 8V89307 is an integrated solution for the Synchronous Equipment Timing Source supporting EEC-Option1, EEC-Option2 clocks in Synchronous Ethernet equipment.

The device has a high quality DPLL to provide system clocks for node timing synchronization within a Synchronous Ethernet network. It also integrates an APLL for better jitter performance.

An input clock is automatically or manually selected. It supports three primary operating modes: Free-Run, Locked and Holdover. In Free-Run mode, the DPLL refers to the master clock. In Locked mode, the DPLL locks to the selected input clock. In Holdover mode, the DPLL resorts to the frequency data acquired in Locked mode. Whatever the operating mode is, the DPLL gives a stable performance without being affected by operating conditions or silicon process variations.

The device provides programmable DPLL bandwidths: 15 mHz to 560 Hz and damping factors: 1.2 to 20 in 5 steps. Different settings cover all clock synchronization requirements.

A stable oscillator is required for the master clock in different applications. The master clock is used as a reference clock for all the internal circuits in the device. It can be calibrated within ±741 ppm.

All the read/write registers are accessed through a microprocessor interface. The device supports Serial and I2C interfaces.

1 PIN ASSIGNMENT

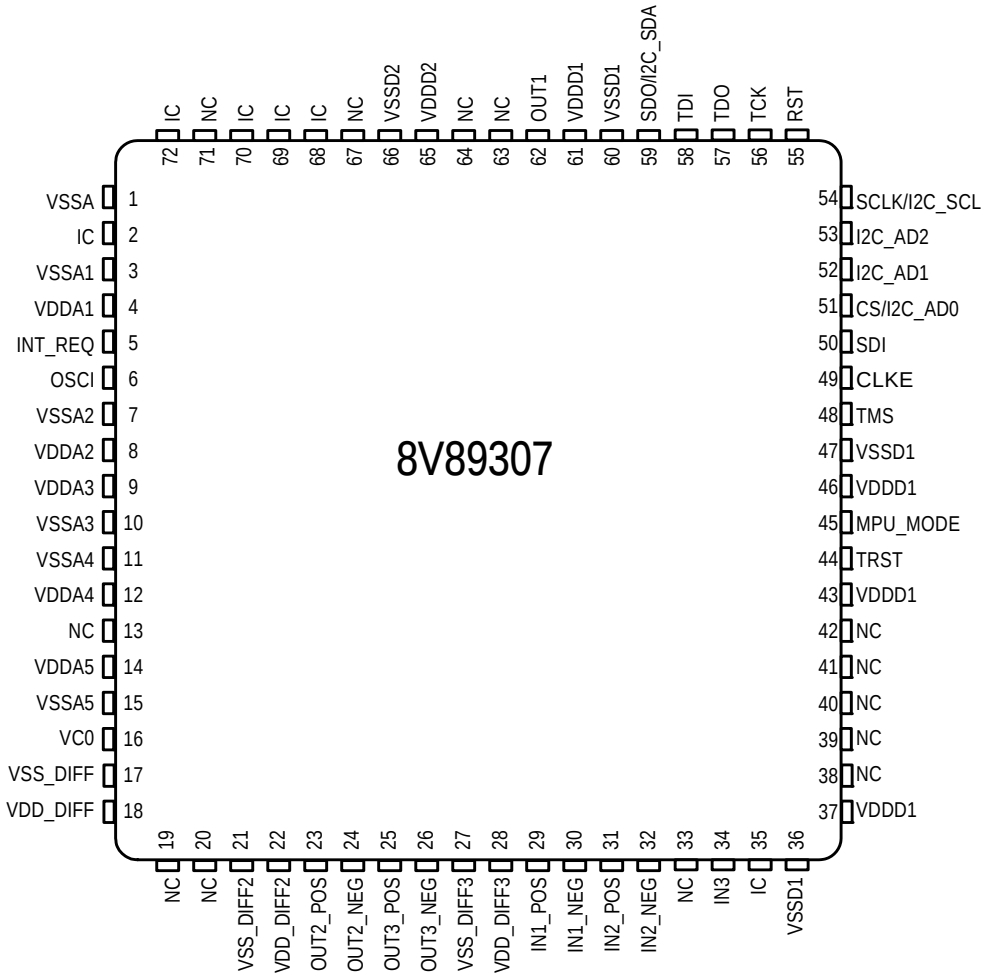

Figure 1. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Name	Pin No.	I/O	Type	Description [1, 2]
Global Control Signal				
OSCI	6	I	CMOS	OSCI: Crystal Oscillator Master Clock A nominal 12.8000 MHz clock provided by a crystal oscillator is input on this pin. It is the master clock for the device.
RST	55	I pull-up	CMOS	RST: Reset A low pulse of at least 50 µs on this pin resets the device. After this pin is high, the device will still be held in reset state for 500 ms (typical).
Input Clock				
IN1_POS IN1_NEG	29 30	I	PECL/LVDS	IN1_POS / IN1_NEG: Positive / Negative Input Clock 1 A 1PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 7.3.2.3 Single-Ended Input for Differential Input.
IN2_POS IN2_NEG	31 32	I	PECL/LVDS	IN2_POS / IN2_NEG: Positive / Negative Input Clock 2 A 1PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz or 625 MHz clock is differentially input on this pair of pins. Whether the clock signal is PECL or LVDS is automatically detected. Single-ended input for differential input is also supported. Refer to Chapter 7.3.2.3 Single-Ended Input for Differential Input.
IN3	34	I pull-down	CMOS	IN3: Input Clock 3 A 1PPS, 2 kHz, 4 kHz, N x 8 kHz [3], 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz or 156.25 MHz clock is input on this pin.
Output Clock				
OUT1	62	O	CMOS	OUT1: Output Clock 1 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 25MHz, 25.78125 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz or 156.25 MHz or 161.1328125 MHz clock is output on these pins.
OUT2_POS OUT2_NEG	23 24	O	PECL/LVDS	OUT2_POS / OUT2_NEG: Positive / Negative Output Clock 2 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125 MHz clock is differentially output on this pin pair.
OUT3_POS OUT3_NEG	25 26	O	PECL/LVDS	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 A 1PPS, 400 Hz, 2 kHz, 8 kHz, 64 kHz, N x E1 [4], N x T1 [5], N x 13.0 MHz [6], N x 3.84 MHz [7], 5 MHz, 10 MHz, 20 MHz, 25 MHz, E3, T3, 6.48 MHz, 19.44 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 128.90625 MHz, 155.52 MHz, 156.25 MHz, 161.1328125 MHz, 311.04 MHz, 312.5 MHz, 322.265625 MHz, 622.08 MHz, 625 MHz or 644.53125 MHz clock is differentially output on this pin pair.
VC0	16	O	Analog	VC0: APLL VC Output External RC filter See "APLL" on page 32 for details.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1, 2]
Microprocessor Interface				
CS / I2C_AD0	51	I/O pull-up	CMOS	CS: Chip Selection In Serial mode, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
INT_REQ	5	O	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request. The output characteristics are determined by the HZ_EN bit (b1, 0CH) and the INT_POL bit (b0, 0CH).
MPU_MODE	45	I pull-down	CMOS	MPU_MODE: Microprocessor Interface Mode Selection The device supports 2 microprocessor interface modes: I2C and Serial. During reset, these pins determine the default value of the MPU_SEL_CNFG[0] bit(b0, 7FH) as follows: 0: I2C mode 1: Serial mode After reset, these pins are general purpose inputs. The microprocessor interface mode is selected by the MPU_SEL_CNFG[0] bits (b0, 7FH). After reset de-assertion, wait 10 μs for the mode to be active. The value of this pin is always reflected by the MPU_PIN_STS[0] bits (b0, 02H).
CLKE	49	I/O pull-down	CMOS	CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. See Table 25 for details.
SDI	50	I/O pull-down	CMOS	SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. See Table 25 for details.
SDO / I2C_SDA	59	I/O pull-down	CMOS	SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data.
I2C_AD1	52	I pull-up	CMOS	I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. In Serial mode, this pin should be connected to ground.
I2C_AD2	53	I pull-up	CMOS	I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. In Serial mode, this pin should be connected to ground.
SCLK / I2C_SCL	54	I pull-down	CMOS	SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1, 2]
JTAG (per IEEE 1149.1)				
TRST	44	I pull-down	CMOS	TRST: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
TMS	48	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
TCK	56	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
TDI	58	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
TDO	57	O	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning. This pin can indicate the interrupt of DPLL selected input clock fail, as determined by the LOS_FLAG_ON_TDO bit (b6, 0BH). Refer to Chapter 3.8.1 Input Clock Validity for details.
Power & Ground				
VDDD1	37,43, 46, 61	Power	-	VDDD1: Digital Core Power.
VDDD2	65	Power	-	VDDD2: CMOS CLK Output Power
VDD_DIFF	18	Power	-	VDD_DIFF: Differential I/O Power Supply
VDD_DIFF3	28	Power	-	VDD_DIFF3: Differential I/O Power Supply
VDD_DIFF2	22	Power	-	VDD_DIFF2: Differential I/O Power Supply
VSSD1	36, 47, 60	Ground	-	VSSD1: Digital Core Ground
VSSD2	66	Ground	-	VSSD2: CMOS CLK Output Ground
VSS_DIFF	17	Ground	-	VSS_DIFF: Differential I/O Ground
VSS_DIFF3	27	Ground	-	VSS_DIFF3: Differential I/O Ground
VSS_DIFF2	21	Ground	-	VSS_DIFF2: Differential I/O Ground
VSSA	1	Ground	-	VSSA: Common Ground
VSSA1 VSSA2 VSSA3 VSSA4 VSSA5	3 7 10 11 15	Ground	-	VSSAn: APLL Ground
VDDA1 VDDA2 VDDA3 VDDA4 VDDA5	4 8 9 12 14	Power	-	VDDAn: APLL Power

Table 1: Pin Description (Continued)

Name	Pin No.	I/O	Type	Description [1, 2]
Others				
IC	72	-	-	IC: Internal Connected Internal Use. These pins should be connected to ground for normal operation.
IC	2, 35, 68, 69, 70	-	-	IC: Internal Connected Internal Use. These pins should be left open for normal operation.
NC	13, 19, 20, 33, 38, 39, 40, 41, 42, 63, 64, 67, 71	-	-	NC: Not Connected These pins are not connected

Note:
1. All the unused input pins should be connected to ground; the output of all the unused output pins are don't-care.
2. The contents in the brackets indicate the position of the register bit/bits.
3. N x 8 kHz: $1 \leq N \leq 19440$.
4. N x E1: N = 1, 2, 3, 4, 6, 8, 12, 16
5. N x T1: N = 1, 2, 3, 4, 6, 8, 12, 16, 24
6. N x 13.0 MHz: N = 1, 2
7. N x 3.84 MHz: N = 1, 2, 4, 8

3 FUNCTIONAL DESCRIPTION

3.1 RESET

The reset operation resets all registers and state machines to their default value or status.

After power on, the device must be reset for normal operation.

For a complete reset, the RST pin must be asserted low for at least 50 µs. After the RST pin is pulled high, the device will still be in reset state for 250 ms (typical). If the RST pin is held low continuously, the device remains in reset state.

3.2 MASTER CLOCK

A nominal 12.8000 MHz clock, provided by a crystal oscillator, is input on the OSCI pin. This clock is provided for the device as a master clock. The master clock is used as a reference clock for all the internal circuits. A better active edge of the master clock is selected by the OSC_EDGE bit to improve jitter and wander performance.

In fact, an offset from the nominal frequency may be input on the OSCI pin. This offset can be compensated by setting the NOMINAL_-FREQ_VALUE[23:0] bits. The calibration range is within ±741 ppm.

The crystal oscillator should be chosen accordingly to meet GR-1244-CORE, GR-253-CORE, ITU-T G.8262, ITU-T G.812 and ITU-T G.813.

Table 2: Related Bit / Register in Chapter 3.2

Bit	Register	Address (Hex)
NOMINAL_FREQ_VALUE[23:0]	NOMINAL_FREQ[23:16]_CNFG, NOMINAL_FREQ[15:8]_CNFG, NOMINAL_FREQ[7:0]_CNFG	06, 05, 04
OSC_EDGE	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A

3.3 INPUT CLOCKS

The device provide 3 input clock ports and supports the following types of input:

- PECL/LVDS
- CMOS

The 8V89307 supports Telecom and Ethernet frequencies from 1PPS up to 625 MHz. It supports 1PPS, 2 kHz, 4 kHz, N x 8 kHz, 1.544 MHz (SONET) / 2.048 MHz (SDH), 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25 MHz, 25.92 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 155.52 MHz, 156.25 MHz, 311.04 MHz, 312.5 MHz, 622.08 MHz and 625 MHz frequencies.

IN3 supports CMOS input signal only.

IN1 and IN2 support PECL/LVDS input signal and automatically detect whether the signal is PECL or LVDS.

To lock to 10 MHz then first set 12E1_GPS_E3_T3_SEL[1:0] to GPS mode in DPLL & APLL Path Configuration Register, address 55H. 8V89307 supports single-ended input for differential input.

3.4 INPUT CLOCK PRE-DIVIDER

Each input clock is assigned an internal Pre-Divider. The Pre-Divider is used to divide the clock frequency down to the internal DPLL's required input frequency, which is no more than 38.88 MHz.

For IN1 ~ IN3, the DPLL required frequency is set by the corresponding IN_FREQ[3:0] bits.

Each Pre-Divider consists of a DivN Divider and a Lock 8k Divider,. IN1 and IN2 also include a HF (High Frequency) Divider. Figure 2 shows a block diagram of the pre-dividers for an input clock and Table 3 shows the Pre-Divider Functions.

When the Lock 8k Divider is used, the input clock is divided down to 8 kHz internally; the PRE_DIVN_VALUE [14:0] bits are not required. Lock 8k Divider can be used for 1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz input clock frequency and the corresponding IN_FREQ[3:0] bits should be set to match the input frequency.

For 2 kHz, 4 kHz or 8 kHz input clock frequency only, the Pre-Divider should be bypassed by setting IN1_DIV[1:0] bits / IN2_DIV[1:0] bits = 0, DIRECT_DIV bit = 0, and LOCK_8K bit = 0. The corresponding IN_FREQ[3:0] bits should be set to match the input frequency. The input clock can be inverted, as determine by the IN_2K_4K_8K_INV bit.

The HF Divider, which is only available for IN1 and IN2, should be used when the input clock is higher than (>) 155.52 MHz. The input clock can be divided by 4, 5 or can bypass the HF Divider, as determined by the IN1_DIV[1:0]/IN2_DIV[1:0] bits correspondingly.

Either the DivN Divider or the Lock 8k Divider can be used or both can be bypassed, as determined by the DIRECT_DIV bit and the LOCK_8K bit.

When the DivN Divider is used for INn ($1 \leq n \leq 3$), the division factor setting should observe the following order:

1. *Select an input clock by the PRE_DIV_CH_VALUE[3:0] bits;*
2. *Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits;*
3. *Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.*

Once the division factor is set for the input clock selected by the PRE_DIV_CH_VALUE[3:0] bits, it is valid until a different division factor is set for the same input clock. The division factor is calculated as follows:

Division Factor = (the frequency of the clock input to the DivN Divider ÷ the frequency of the DPLL required clock set by the IN_FREQ[3:0] bits) - 1

The DivN Divider can only divide the input clock whose frequency is less than or equal to (≤) 155.52 MHz.

The Pre-Divider configuration and the division factor setting depend on the input clock on one of the IN1 ~ IN3 pins and the DPLL required clock. Here is an example:

The input clock on the IN2 pin is 622.08 MHz; the DPLL required clock is 6.48 MHz by programming the IN_FREQ[3:0] bits of register IN2 to '0010'. Do the following step by step to divide the input clock:

1. *Use the HF Divider to divide the clock down to 155.52 MHz:*
   622.08 ÷ 155.52 = 4, so set the IN2_DIV[1:0] bits to '01';
2. *Use the DivN Divider to divide the clock down to 6.48 MHz:*
   Set the PRE_DIV_CH_VALUE[3:0] bits to '0110';
   Set the DIRECT_DIV bit in Register IN2_CNFG to '1' and the LOCK_8K bit in Register IN2_CNFG to '0';
   155.52 ÷ 6.48 = 24; 24 - 1 = 23, so set the PRE_DIVN_VALUE[14:0] bits to '10111'.

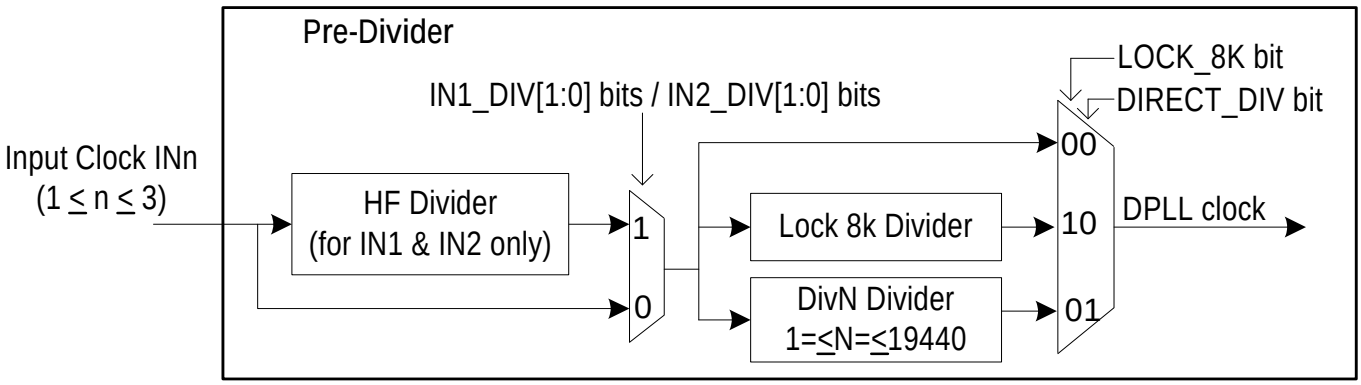

Figure 2. Pre-Divider for An Input Clock

Table 3: Pre-Divider Function

Pre-Divider	Input Clock INn Frequency	Control Register	Register/ Address[1]
HF- Divider[2]	>155.52 MHz	IN1_DIV[1:0] IN2_DIV[1:0]	IN1_IN2_HF_DIV_CNFG (18)
Divider Bypassed	1 Hz, 2kHz, 4kHz, 8kHz, 1.544 MHz, 2.048 MHz, 6.25 MHz, 6.48 MHz, 10 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz	IN_FREQ[3:0] – set to match input Clock INn frequency. LOCK_8K= 0'b; DIRECT_DIV= 0'b (Bypass Dividers)	IN1_CNFG ~ IN3_CNFG (16, 19, 1A)
Lock 8K Divider	1.544 MHz, 2.048 MHz, 6.48 MHz, 19.44 MHz, 25.92 MHz or 38.88 MHz	IN_FREQ[3:0] – set to match input Clock INn frequency. LOCK_8K= 1'b; DIRECT_DIV= 0'b (select Lock 8k Divider)	IN1_CNFG ~ IN3_CNFG (16, 19, 1A)
DivN	Nx8kHz (1 ≤ N ≤ 19440) *Example:* *25 MHz = 3125 x 8 kHz*	LOCK_8K= 0'b; DIRECT_DIV= 1'b (select DivN Divider) IN_FREQ[3:0] – set to the DPLL required frequency. ('0000': 8 kHz (default)) PRE_DIV_CH_VALUE[3:0] PRE_DIVN_VALUE[14:0] *Example:* *25 MHz = 3125 x 8kHz* *Division Factor = 3125 -1= 3124 Dec (or 0C34h)* *PRE_DIVN_VALUE[7:0]= 34h* *PRE_DIVN_VALUE[14:8]= 0Ch*	IIN1_CNFG ~ IN3_CNFG (16, 19, 1A) PRE_DIV_CH_CNFG (23) PRE_DIVN[14:8]_CNFG (25), PRE_DIVN[7:0]_CNFG (24)

Note 1: Please see register description for details.
Note 2: For 156.25 MHz, 312.5 MHz and 625 MHz differential input clock frequency, the divider mode should be DivN with IN_FREQ[3:0] = '1100': 6.25 MHz.

3.5 INPUT CLOCK QUALITY MONITORING

The qualities of all the input clocks are always monitored in the following aspects:

- Activity
- Frequency

Activity and frequency monitoring are conducted on all the input clocks.

The qualified clocks are available for DPLL selection. The selected input clocks monitored further. Refer to Chapter 3.7 Selected Input Clock Monitoring for details.

3.5.1 ACTIVITY MONITORING

Activity is monitored by using an internal leaky bucket accumulator, as shown in Figure 3.

Each input clock is assigned an internal leaky bucket accumulator. The input clock is monitored for each period of 128 ms, the internal leaky bucket accumulator is increased by 1 when an event is detected; and it is decreased by 1 when no event is detected within the period set by the decay rate. The event is that an input clock drifts outside (>) ±500 ppm with respect to the master clock within a 128 ms period.

There are four configurations (0 - 3) for a leaky bucket accumulator. The leaky bucket configuration for an input clock is selected by the corresponding BUCKET_SEL[1:0] bits. Each leaky bucket configuration consists of four elements: upper threshold, lower threshold, bucket size and decay rate.

The bucket size is the capability of the accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected. The upper threshold is a point above which a no-activity alarm is raised. The lower threshold is a point below which the no-activity alarm is cleared. The decay rate is a certain period during which the accumulator decreases by 1 if no event is detected.

The leaky bucket configuration is programmed by one of four groups of register bits: the BUCKET_SIZE_n_DATA[7:0] bits, the UPPER_THRESHOLD_n_DATA[7:0] bits, the LOWER_THRESHOLD_n_DATA[7:0] bits and the DECAY_RATE_n_DATA[1:0] bits respectively; 'n' is 0 ~ 3.

The no-activity alarm status of the input clock is indicated by the INn_NO_ACTIVITY_ALARM bit ($3 \geq n \geq 1$).

The input clock with a no-activity alarm is disqualified for clock selection for the DPLL.

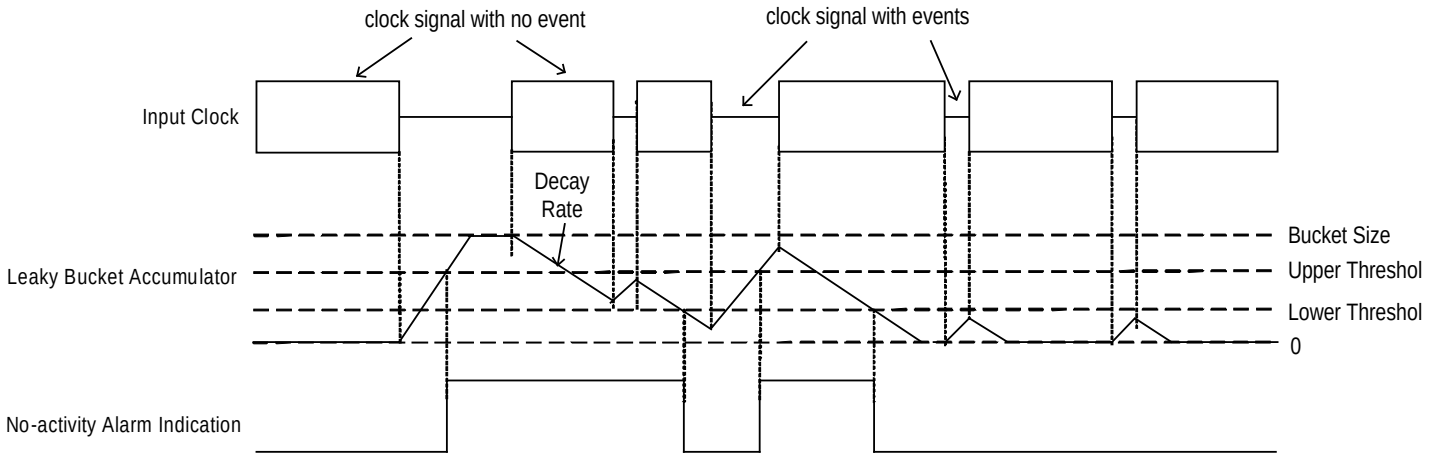

Figure 3. Input Clock Activity Monitoring

3.5.2 FREQUENCY MONITORING

Frequency is monitored by comparing the input clock with a reference clock. The reference clock can be derived from the master clock or the output of the DPLL, as determined by the FREQ_MON_CLK bit.

Each reference clock has a hard frequency monitor and a soft frequency monitor. Both monitors have two thresholds, rejecting threshold and accepting threshold, which are set in HARD_FREQ_MON_THRESHOLD[7:0] and SOFT_FREQ_MON_THRESHOLD[7:0]. So four frequency alarm thresholds are set for frequency monitoring: Hard Alarm Accepting Threshold, Hard Alarm Rejecting Threshold, Soft Alarm Accepting Threshold and Soft Alarm Rejecting Threshold.

The frequency hard alarm accepting threshold can be calculated as follows:

Frequency Hard Alarm Accepting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)

The frequency hard alarm rejecting threshold can be calculated as follows:

Frequency Hard Alarm Rejecting Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)

When the input clock frequency raises to above the hard alarm rejecting threshold, the INn_FREQ_HARD_ALARM bit ($3 \geq n \geq 1$) will alarm and indicate '1'. The alarm will remain until the frequency is down to below the hard alarm accepting threshold, then the INn_FREQ_HARD_ALARM bit will back to '0'. There is a hysteresis between frequency monitoring, refer to Figure 4. Hysteresis Frequency Monitoring

The soft alarm is indicated by the INn_FREQ_SOFT_ALARM bit ($3 \geq n \geq 1$) in the same way as hard alarm.

If the FREQ_MON_HARD_EN bit is '1', the frequency alarm status of the input clock is indicated by the INn_FREQ_HARD_ALARM bit ($3 \geq n \geq 1$). When the FREQ_MON_HARD_EN bit is '0', no frequency hard alarm is raised even if the input clock is above the frequency alarm threshold.

The input clock with a frequency hard alarm is disqualified for clock selection for the DPLL, but the soft alarm don't affect the clock selection for the DPLL.

In addition, if the input clock is 2 kHz, 4 kHz or 8 kHz, its clock edges with respect to the reference clock are monitored. If any edge drifts outside ±5%, the input clock is disqualified for clock selection for the DPLL. The input clock is qualified if any edge drifts inside ±5%. This function is supported only when the IN_NOISE_WINDOW bit is '1'.

The frequency of each input clock with respect to the reference clock can be read by doing the following step by step:

1. *Select an input clock by setting the IN_FREQ_READ_CH[3:0] bits;*
2. *Read the value in the IN_FREQ_VALUE[7:0] bits and calculate as follows:*

   Input Clock Frequency (ppm) = IN_FREQ_VALUE[7:0] X FREQ_MON_FACTOR[3:0]

Note that the value set by the FREQ_MON_FACTOR[3:0] bits depends on the application.

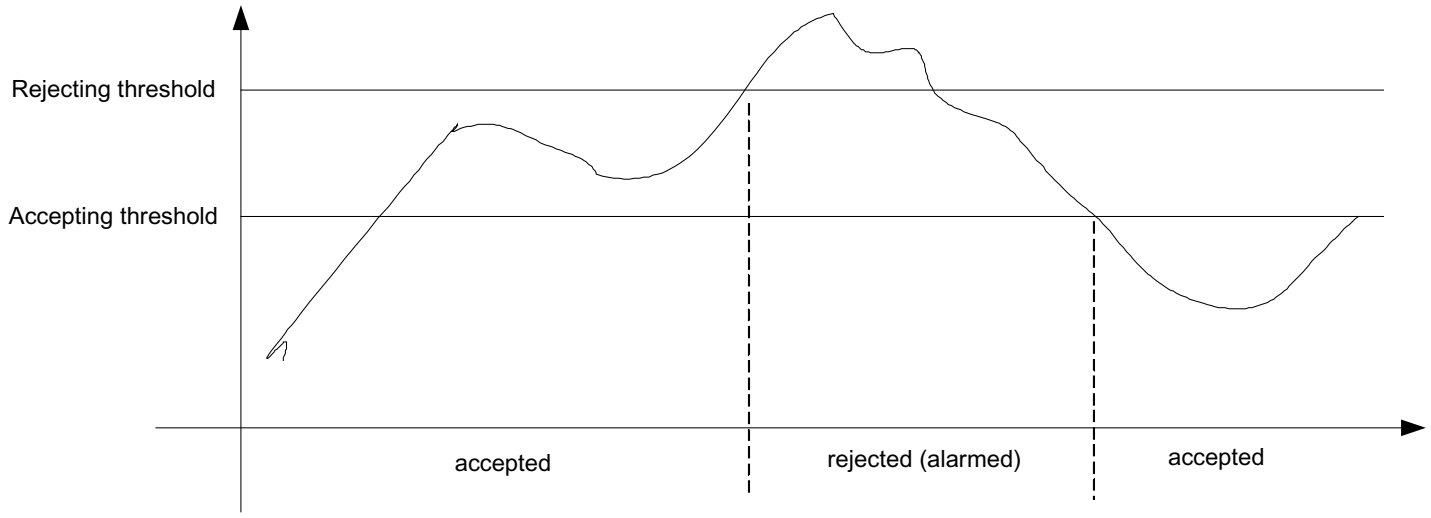

Figure 4. Hysteresis Frequency Monitoring

Table 4: Related Bit / Register in Chapter 3.5

Bit	Register	Address (Hex)
BUCKET_SIZE_n_DATA[7:0] (3 ≥ n ≥ 0)	BUCKET_SIZE_0_CNFG ~ BUCKET_SIZE_3_CNFG	33, 37, 3B, 3F
UPPER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	UPPER_THRESHOLD_0_CNFG ~ UPPER_THRESHOLD_3_CNFG	31, 35, 39, 3D
LOWER_THRESHOLD_n_DATA[7:0] (3 ≥ n ≥ 0)	LOWER_THRESHOLD_0_CNFG ~ LOWER_THRESHOLD_3_CNFG	32, 36, 3A, 3E
DECAY_RATE_n_DATA[1:0] (3 ≥ n ≥ 0)	DECAY_RATE_0_CNFG ~ DECAY_RATE_3_CNFG	34, 38, 3C, 40
BUCKET_SEL[1:0]	IN1_CNFG ~ IN3_CNFG	16, 19, 1A
INn_NO_ACTIVITY_ALARM (3 ≥ n ≥ 1)	IN1_IN2_STS ~ IN3_STS	44 ~ 45
INn_FREQ_HARD_ALARM (3 ≥ n ≥ 1)		
INn_FREQ_SOFT_ALARM (3 ≥ n ≥ 1)		
FREQ_MON_CLK	MON_SW_HS_CNFG	0B
FREQ_MON_HARD_EN		
HARD_FREQ_MON_THRESHOLD[7:0]	HARD_FREQ_MON_THRESHOLD_CNFG	2F
SOFT_FREQ_MON_THRESHOLD[7:0]	SOFT_FREQ_MON_THRESHOLD_CNFG	30
FREQ_MON_FACTOR[3:0]	FREQ_MON_FACTOR_CNFG	2E
IN_NOISE_WINDOW	PHASE_MON_CNFG	78
IN_FREQ_READ_CH[3:0]	IN_FREQ_READ_CH_CNFG	41
IN_FREQ_VALUE[7:0]	IN_FREQ_READ_STS	42

3.6 DPLL INPUT CLOCK SELECTION

The DPLL_INPUT_SEL[3:0] bits determine the input clock selection, as shown in Table 5:

Table 5: Input Clock Selection for the DPLL

Control Bit DPLL_INPUT_SEL[3:0]	Input Clock Selection
other than 0000	Forced selection
0000	Automatic selection

Forced selection is done by setting the related registers.

Automatic selection is done based on the results of input clocks quality monitoring and the related registers configuration.

3.6.1 FORCED SELECTION

In Forced selection, the selected input clock is set by the INPUT_SEL[3:0] bits. The results of input clocks quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring) do not affect the input clock selection if Forced selection is used.

3.6.2 AUTOMATIC SELECTION

In Automatic selection, the input clock selection is determined by its validity, priority and locking allowance configuration. The validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). Locking allowance is configured by the corresponding INn_VALID bit($3 \geq n \geq 1$). Refer to Figure 5. In all the qualified input clocks, the one with the highest priority is selected. The priority is set by the corresponding INn_SEL_PRIORITY[3:0] bits ($3 \geq n \geq 1$). If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

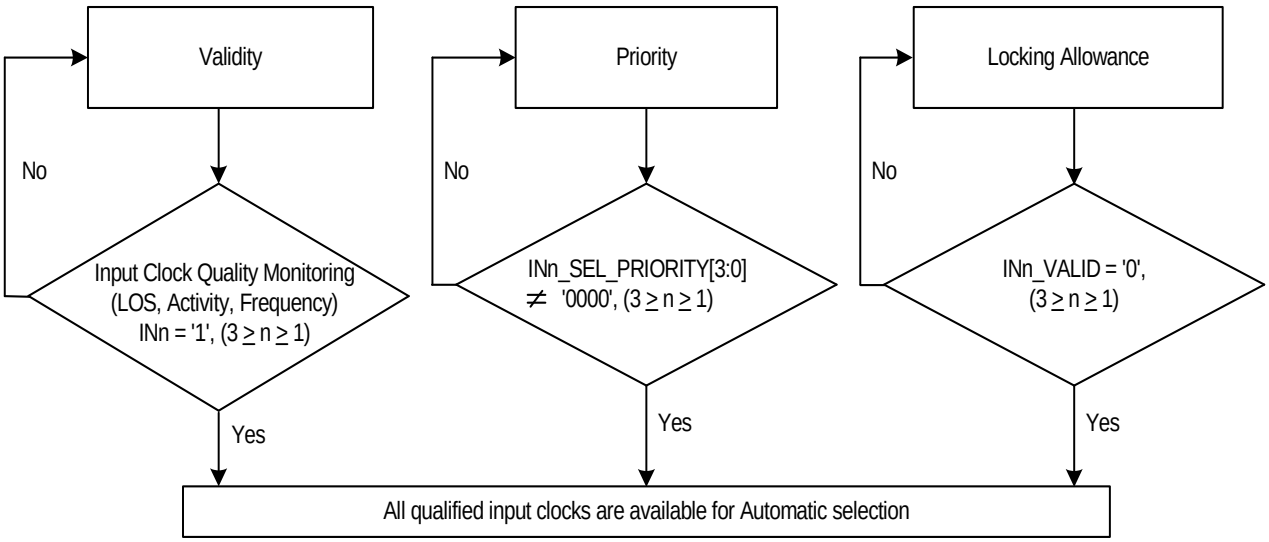

Figure 5. Qualified Input Clocks for Automatic Selection

Table 6: Related Bit / Register in Chapter 3.6

Bit	Register	Address (Hex)
DPLL_INPUT_SEL[3:0]	DPLL_INPUT_SEL_CNFG	50
INn_SEL_PRIORITY[3:0] ($3 \geq n \geq 1$)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN3_SEL_PRIORITY_CNFG	27 ~ 28
INn_VALID ($3 \geq n \geq 1$)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C
INn ($3 \geq n \geq 1$)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A,

3.7 SELECTED INPUT CLOCK MONITORING

The quality of the selected input clock is always monitored (refer to Chapter 3.5 Input Clock Quality Monitoring) and the DPLL locking status is always monitored.

3.7.1 DPLL LOCKING DETECTION

The following events is always monitored:

- Fast Loss;
- Coarse Phase Loss;
- Fine Phase Loss;
- Hard Limit Exceeding.

3.7.1.1 Fast Loss

A fast loss is triggered when the selected input clock misses 2 consecutive clock cycles. It is cleared once an active clock edge is detected.

The occurrence of the fast loss will result in the DPLL unlocked if the FAST_LOS_SW bit is '1'.

3.7.1.2 Coarse Phase Loss

The DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the coarse phase limit, a coarse phase loss is triggered. It is cleared once the phase-compared result is within the coarse phase limit.

When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 7. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to Table 8.

Table 7: Coarse Phase Limit Programming (the selected input clock of 2 kHz, 4 kHz or 8 kHz)

MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
0	don't-care	±1 UI
1	0	±1 UI
	1	set by the PH_LOS_COARSE_LIMT[3:0] bits

Table 8: Coarse Phase Limit Programming (the selected input clock of other than 2 kHz, 4 kHz and 8 kHz)

WIDE_EN	Coarse Phase Limit
0	±1 UI
1	set by the PH_LOS_COARSE_LIMT[3:0] bits

The occurrence of the coarse phase loss will result in the DPLL unlocked if the COARSE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.3 Fine Phase Loss

The DPLL compares the selected input clock with the feedback signal. If the phase-compared result exceeds the fine phase limit programmed by the PH_LOS_FINE_LIMT[2:0] bits, a fine phase loss is triggered. It is cleared once the phase-compared result is within the fine phase limit.

The occurrence of the fine phase loss will result in the DPLL unlocked if the FINE_PH_LOS_LIMT_EN bit is '1'.

3.7.1.4 Hard Limit Exceeding

Two limits are available for this monitoring. They are DPLL soft limit and DPLL hard limit. When the frequency of the DPLL output with respect to the master clock exceeds the DPLL soft / hard limit, a DPLL soft / hard alarm will be raised; the alarm is cleared once the frequency is within the corresponding limit. The occurrence of the DPLL soft alarm does not affect the DPLL locking status. The DPLL soft alarm is indicated by the corresponding DPLL_SOFT_FREQ_ALARM bit. The occurrence of the DPLL hard alarm will result in the DPLL unlocked if the FREQ_LIMT_PH_LOS bit is '1'.

The DPLL soft limit is set by the DPLL_FREQ_SOFT_LIMT[6:0] bits and can be calculated as follows:

DPLL Soft Limit (ppm) = DPLL_FREQ_SOFT_LIMT[6:0] X 0.724

The DPLL hard limit is set by the DPLL_FREQ_HARD_LIMT[15:0] bits and can be calculated as follows:

DPLL Hard Limit (ppm) = DPLL_FREQ_HARD_LIMT[15:0] X 0.0014

3.7.2 LOCKING STATUS

The DPLL locking status depends on the locking monitoring results. The DPLL is in locked state if none of the following events is triggered during 2 seconds; otherwise, the DPLL is unlocked.

- Fast Loss (the FAST_LOS_SW bit is '1');
- Coarse Phase Loss (the COARSE_PH_LOS_LIMT_EN bit is '1');
- Fine Phase Loss (the FINE_PH_LOS_LIMT_EN bit is '1');
- DPLL Hard Alarm (the FREQ_LIMT_PH_LOS bit is '1').

If the FAST_LOS_SW bit, the COARSE_PH_LOS_LIMT_EN bit, the FINE_PH_LOS_LIMT_EN bit or the FREQ_LIMT_PH_LOS bit is '0', the DPLL locking status will not be affected even if the corresponding event is triggered. If all these bits are '0', the DPLL will be in locked state in 2 seconds.

The DPLL locking status is indicated by the DPLL_LOCK

3.7.3 PHASE LOCK ALARM

A phase lock alarm will be raised when the selected input clock can not be locked in the DPLL within a certain period. This period can be calculated as follows:

Period (sec.) = TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0]

The phase lock alarm is indicated by the corresponding INn_PH_LOCK_ALARM bit ($3 \geq n \geq 1$).

The phase lock alarm can be cleared by the following two ways, as selected by the PH_ALARM_TIMEOUT bit:

- Be cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit;
- Be cleared after the period (= *TIME_OUT_VALUE[5:0] X MULTI_FACTOR[1:0] in second*) which starts from when the alarm is raised.

The selected input clock with a phase lock alarm is disqualified for the DPLL locking.

Table 9: Related Bit / Register in Chapter 3.7

Bit	Register	Address (Hex)
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B
PH_LOS_FINE_LIMT[2:0]		
FINE_PH_LOS_LIMT_EN		
MULTI_PH_8K_4K_2K_EN	PHASE_LOSS_COARSE_LIMIT_CNFG	5A
WIDE_EN		
PH_LOS_COARSE_LIMT[3:0]		
COARSE_PH_LOS_LIMT_EN		
DPLL_SOFT_FREQ_ALARM	OPERATING_STS	52
DPLL_LOCK		
DPLL_FREQ_SOFT_LIMT[6:0]	DPLL_FREQ_SOFT_LIMIT_CNFG	65
FREQ_LIMT_PH_LOS		
DPLL_FREQ_HARD_LIMT[15:0]	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG, DPLL_FREQ_HARD_LIMIT[7:0]_CNFG	67, 66
TIME_OUT_VALUE[5:0]	PHASE_ALARM_TIME_OUT_CNFG	08
MULTI_FACTOR[1:0]		
INn_PH_LOCK_ALARM ($3 \geq n \geq 1$)	IN1_IN2_STS ~ IN3_STS	44, 45
PH_ALARM_TIMEOUT	INPUT_MODE_CNFG	09

3.8 INPUT CLOCK SELECTION

If the input clock is selected by Forced selection, it can be switched by setting the related registers (refer to Chapter 3.6.1 Forced Selection) any time. In this case, whether the input clock is qualified for DPLL locking does not affect the clock switch.

When the input clock is selected by Automatic selection, the input clock switch depends on its validity, priority and locking allowance configuration. If the current selected input clock is disqualified, a new qualified input clock may be switched to.

3.8.1 INPUT CLOCK VALIDITY

For all the input clocks, the validity depends on the results of input clock quality monitoring (refer to Chapter 3.5 Input Clock Quality Monitoring). When all of the following conditions are satisfied, the input clock is valid; otherwise, it is invalid.

- No no-activity alarm (the INn_NO_ACTIVITY_ALARM bit is '0');
- No frequency hard alarm (the INn_FREQ_HARD_ALARM bit is '0');
- If the IN_NOISE_WINDOW bit is '1', all the edges of the input clock of 2 kHz, 4 kHz or 8 kHz drift inside ±5%; if the IN_NOISE_WINDOW bit is '0', this condition is ignored.
- No phase lock alarm, i.e., the INn_PH_LOCK_ALARM bit is '0';
- If the ULTR_FAST_SW bit is '1', the DPLL selected input clock misses less than (<) 2 consecutive clock cycles; if the ULTR_FAST_SW bit is '0', this condition is ignored.

The validities of all the input clocks are indicated by the INn [1] bit ($3 \geq n \geq 1$). When the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), the INn [2] bit will be set. If the INn [3] bit is '1', an interrupt will be generated.

When the selected input clock has failed, i.e., the validity of the selected input clock changes from 'valid' to 'invalid', the MAIN_REF_FAILED [1] bit will be set. If the MAIN_REF_FAILED [2] bit is '1', an interrupt will be generated. This interrupt can also be indicated by hardware - the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. When the TDO pin is used to indicate this interrupt, it will be set high when this interrupt is generated and will remain high until this interrupt is cleared.

3.8.2 INPUT CLOCK SELECTION

When the device is configured as Automatic input clock selection, Revertive and Non-Revertive switchings are supported, as selected by the REVERTIVE_MODE bit.

GR-1244 defines Revertive and Non-Revertive Reference switching. In Non-Revertive switching, a switch to an alternate reference is maintained even after the original reference has recovered from the failure that caused the switch. In Revertive switching, the clock switches back to the original reference after that reference recovers from the failure, independent of the condition of the alternate reference. In Non-Revertive switching, input clock switch is minimized.

Conditions of the qualified input clocks available for selection are:

- Valid, i.e., the INn 1 bit is '1';
- Priority enabled, i.e., the corresponding INn_SEL_PRIORITY[3:0] bits are not '0000';
- Locking to the input clock is allowed, i.e., the corresponding INn_VALID bit is '0'.

The input clock is disqualified if any of the above conditions is not satisfied.

In summary, the selected input clock can be switched by:

- Forced selection;
- Revertive switching;
- Non-Revertive switching.

3.8.2.1 Revertive Switching

In Revertive switching, the selected input clock is switched when another qualified input clock with a higher priority than the current selected input clock is available.

The selected input clock is switched if any of the following is satisfied:

- the selected input clock is disqualified;
- another qualified input clock with a higher priority than the selected input clock is available.

A qualified input clock with the highest priority is selected by revertive switching. If more than one qualified input clock INn is available and has the same priority, the input clock with the smallest 'n' is selected.

3.8.2.2 Non-Revertive Switching

In Non-Revertive switching, the DPLL selected input clock is not switched when another qualified input clock with a higher priority than the current selected input clock is available. In this case, the selected input clock is switched and a qualified input clock with the highest priority is selected only when the DPLL selected input clock is disqualified. If more than one qualified input clock is available and has the same priority, the input clock with the smallest 'n' is selected.

3.8.3 SELECTED / QUALIFIED INPUT CLOCKS INDICATION

The selected input clock is indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits.

The qualified input clocks with the three highest priorities are indicated by HIGHEST_PRIORITY_VALIDATED[3:0] bits, the SECOND_PRIORITY_VALIDATED[3:0] bits and the THIRD_PRIORITY _VALIDATED[3:0] bits respectively. If more than one input clock INn has the same priority, the input clock with the smallest 'n' is indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

When the device is configured in Automatic selection and Revertive switching is enabled, the input clock indicated by the CURRENTLY_SELECTED_INPUT[3:0] bits is the same as the one indicated by the HIGHEST_PRIORITY_VALIDATED[3:0] bits.

Table 10: Related Bit / Register in Chapter 3.8

Bit	Register	Address (Hex)
INn [1] (3 ≥ n ≥ 1)	INPUT_VALID1_STS, INPUT_VALID2_STS	4A
INn [2] (3 ≥ n ≥ 1)	INTERRUPTS1_STS, INTERRUPTS2_STS	0D
INn [3] (3 ≥ n ≥ 1)	INTERRUPTS1_ENABLE_CNFG, INTERRUPTS2_ENABLE_CNFG	10
INn_NO_ACTIVITY_ALARM (3 ≥ n ≥ 1)	IN1_IN2_STS ~ IN3_STS	44 ~ 45
INn_FREQ_HARD_ALARM (3 ≥ n ≥ 1)		
INn_PH_LOCK_ALARM (3≥ n ≥ 1)		
IN_NOISE_WINDOW	PHASE_MON_CNFG	78
ULTR_FAST_SW	MON_SW_HS_CNFG	0B
LOS_FLAG_TO_TDO		
MAIN_REF_FAILED [1]	INTERRUPTS2_STS	0E
MAIN_REF_FAILED [2]	INTERRUPTS2_ENABLE_CNFG	11
REVERTIVE_MODE	INPUT_MODE_CNFG	09
INn_SEL_PRIORITY[3:0] (3 ≥ n ≥ 1)	IN1_IN2_SEL_PRIORITY_CNFG ~ IN3_SEL_PRIORITY_CNFG	27, 28
INn_VALID (3 ≥ n ≥ 1)	REMOTE_INPUT_VALID1_CNFG, REMOTE_INPUT_VALID2_CNFG	4C
CURRENTLY_SELECTED_INPUT[3:0]	PRIORITY_TABLE1_STS	4E
HIGHEST_PRIORITY_VALIDATED[3:0]		
SECOND_PRIORITY_VALIDATED[3:0]	PRIORITY_TABLE2_STS	4F
THIRD_PRIORITY_VALIDATED[3:0]		

3.9 SELECTED INPUT CLOCK STATUS VS. DPLL OPERATING MODE

The DPLL supports three primary operating modes: Free-Run, Locked and Holdover, and three secondary, temporary operating modes: Pre-Locked, Pre-Locked2 and Lost-Phase. The operating modes of the DPLL can be switched automatically or by force, as controlled by the DPLL_OPERATING_MODE[2:0] bits.

When the operating mode is switched by force, the operating mode switch is under external control and the status of the selected input clock takes no effect to the operating mode selection.

When the operating mode is switched automatically, the internal state machines for the DPLL automatically determine the operating mode respectively.

3.9.1 SELECTED INPUT CLOCK VS. DPLL OPERATING MODE

The DPLL operating mode is controlled by the DPLL_OPERATING_-MODE[2:0] bits, as shown in Table 11:

Table 11: DPLL Operating Mode Control

DPLL_OPERATING_MODE[2:0]	DPLL Operating Mode
000	Automatic
001	Forced - Free-Run
010	Forced - Holdover
100	Forced - Locked
101	Forced - Pre-Locked2
110	Forced - Pre-Locked
111	Forced - Lost-Phase

When the operating mode is switched automatically, the operation of the internal state machine is shown in Figure 6.

Whether the operating mode is under external control or is switched automatically, the current operating mode is always indicated by the DPLL_OPERATING_MODE[2:0] bits. When the operating mode switches, the OPERATING_MODE [1] bit will be set. If the OPERATING_-MODE [2] bit is '1', an interrupt will be generated.

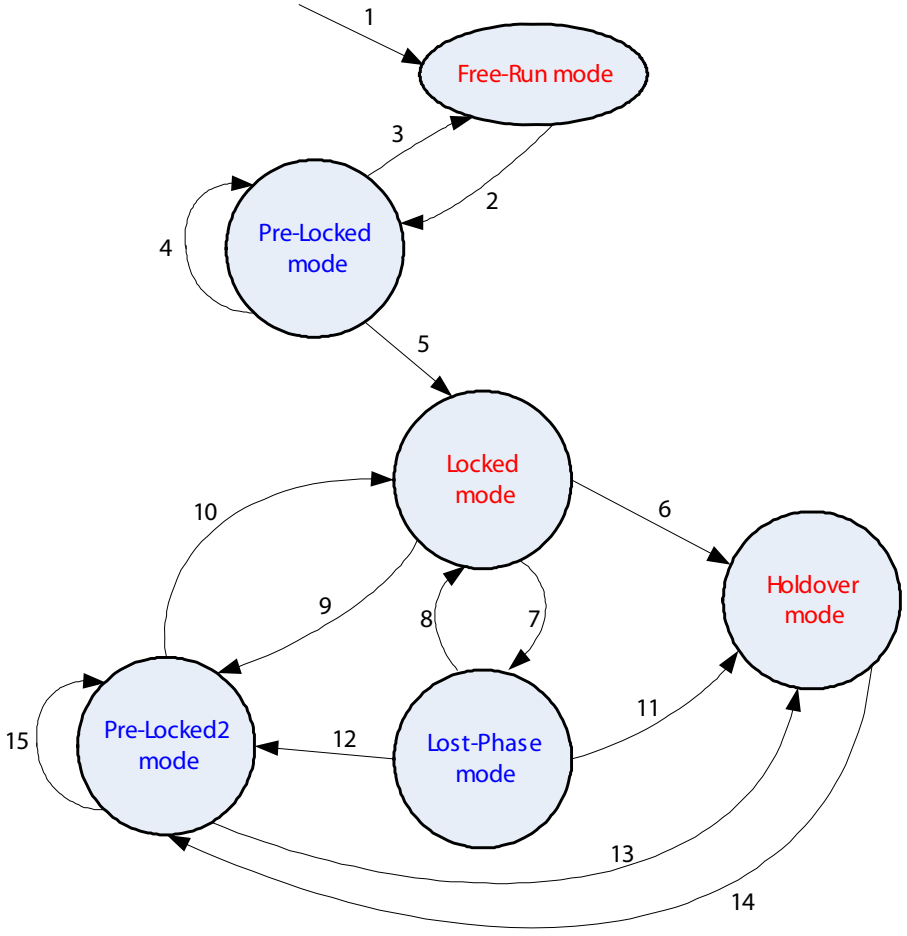

Figure 6. DPLL Selected Input Clock vs. DPLL Automatic Operating Mode

Notes to Figure 6:

1. *Reset.*
2. *An input clock is selected.*
3. *The DPLL selected input clock is disqualified AND No qualified input clock is available.*
4. *The DPLL selected input clock is switched to another one.*
5. *The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').*
6. *The DPLL selected input clock is disqualified AND No qualified input clock is available.*
7. *The DPLL selected input clock is unlocked (the DPLL_LOCK bit is '0').*
8. *The DPLL selected input clock is locked again (the DPLL_LOCK bit is '1').*
9. *The DPLL selected input clock is switched to another one.*
10. *The DPLL selected input clock is locked (the DPLL_LOCK bit is '1').*
11. *The DPLL selected input clock is disqualified AND No qualified input clock is available.*
12. *The DPLL selected input clock is switched to another one.*
13. *The DPLL selected input clock is disqualified AND No qualified input clock is available.*
14. *An input clock is selected.*
15. *The DPLL selected input clock is switched to another one.*

The causes of Item 4, 9, 12, 15 - 'the *DPLL* selected input clock is switched to another one' - are: (The *DPLL* selected input clock is disqualified AND Another input clock is switched to) OR (In Revertive switching, a qualified input clock with a higher priority is switched to) OR (The *DPLL* selected input clock is switched to another one by Forced selection).

Table 12: Related Bit / Register in Chapter 3.9

Bit	Register	Address (Hex)
DPLL_OPERATING_-MODE[2:0]	DPLL_OPERATING_-MODE_CNFG	53
DPLL_OPERATING_-MODE[2:0]	OPERATING_STS	52
DPLL_LOCK		
OPERATING_MODE [1]	INTERRUPTS2_STS	0E
OPERATING_MODE [2]	INTERRUPTS2_ENABLE_CNFG	11

3.10 DPLL OPERATING MODE

The DPLL gives a stable performance in different applications without being affected by operating conditions or silicon process variations. It integrates a PFD (Phase & Frequency Detector), a LPF (Low Pass Filter) and a DCO (Digital Controlled Oscillator), which forms a closed loop. If no input clock is selected, the loop is not closed, and the PFD and LPF do not function.

The PFD detects the phase error, including the fast loss, coarse phase loss and fine phase loss (refer to Chapter 3.7.1.1 Fast Loss to Chapter 3.7.1.3 Fine Phase Loss). The averaged phase error of the DPLL feedback with respect to the selected input clock is indicated by the CURRENT_PH_DATA[15:0] bits. It can be calculated as follows:

Averaged Phase Error (ns) = CURRENT_PH_DATA[15:0] X 0.61

The LPF filters jitter. Its 3 dB bandwidth and damping factor are programmable. A range of bandwidths and damping factors can be set to meet different application requirements. For the same bandwidth setting, a lower damping factor will decrease the locking time but will increase the overshoot.

The DCO controls the DPLL output. The frequency of the DPLL output is always multiplied on the basis of the master clock. The phase and frequency offset of the DPLL output may be locked to those of the selected input clock. The current frequency offset with respect to the master clock is indicated by the CURRENT_DPLL_FREQ[23:0] bits, and can be calculated as follows:

Current Frequency Offset (ppm) = CURRENT_DPLL_FREQ[23:0] X 0.000011

3.10.1 DPLL OPERATING MODE

The DPLL loop is closed except in Free-Run mode and Holdover mode.

For a closed loop, different bandwidths and damping factors can be used depending on DPLL locking stages: starting, acquisition and locked.

In the first two seconds when the DPLL attempts to lock to the selected input clock, the starting bandwidth and damping factor are used. They are set by the DPLL_START_BW[4:0] bits and the DPLL_START_DAMPING[2:0] bits respectively.

During the acquisition, the acquisition bandwidth and damping factor are used. They are set by the DPLL_ACQ_BW[4:0] bits and the DPLL_ACQ_DAMPING[2:0] bits respectively.

When the DPLL selected input clock is locked, the locked bandwidth and damping factor are used. They are set by the DPLL_LOCKED_BW[4:0] bits and the DPLL_LOCKED_DAMPING[2:0] bits respectively.

The corresponding bandwidth and damping factor are used when the DPLL operates in different DPLL locking stages: starting, acquisition and locked, as controlled by the device automatically.

Only the locked bandwidth and damping factor can be used regardless of the DPLL locking stage, as controlled by the AUTO_BW_SEL bit.

3.10.1.1 Free-Run Mode

In Free-Run mode, the DPLL output refers to the master clock and is not affected by any input clock. The accuracy of the DPLL output is equal to that of the master clock.

3.10.1.2 Pre-Locked Mode

In Pre-Locked mode, the DPLL output attempts to track the selected input clock.

The Pre-Locked mode is a secondary, temporary mode.

3.10.1.3 Locked Mode

In Locked mode, the DPLL selected input clock is locked. The phase and frequency offset of the DPLL output track those of the DPLL selected input clock.

In this mode, if the DPLL selected input clock is in fast loss status and the FAST_LOS_SW bit is ‘1’, the DPLL is unlocked (refer to Chapter 3.7.1.1 Fast Loss) and will enter Lost-Phase mode when the operating mode is switched automatically; if the DPLL selected input clock is in fast loss status and the FAST_LOS_SW bit is ‘0’, the DPLL locking status is not affected and the DPLL will enter Temp-Holdover mode automatically.

3.10.1.4 Temp-Holdover Mode

The DPLL will automatically enter Temp-Holdover mode with a selected input clock switch or no qualified input clock available when the operating mode switch is under external control.

In Temp-Holdover mode, the DPLL has temporarily lost the selected input clock. The DPLL operation in Temp-Holdover mode and that in Holdover mode are alike (refer to Chapter 3.10.1.6 Holdover Mode) except the frequency offset acquiring methods. See Chapter 3.10.1.6 Holdover Mode for details about the methods. The method is selected by the TEMP_HOLDOVER_MODE[1:0] bits, as shown in Table 13:

Table 13: Frequency Offset Control in Temp-Holdover Mode

TEMP_HOLDOVER_MODE[1:0]	Frequency Offset Acquiring Method
00	the same as that used in Holdover mode
01	Automatic Instantaneous
10	Automatic Fast Averaged
11	Automatic Slow Averaged

The device automatically controls the DPLL to exit from Temp-Holdover mode.

3.10.1.5 Lost-Phase Mode

In Lost-Phase mode, the DPLL output attempts to track the selected input clock.

The Lost-Phase mode is a secondary, temporary mode.

3.10.1.6 Holdover Mode

In Holdover mode, the DPLL resorts to the stored frequency data acquired in Locked mode to control its output. The DPLL output is not phase locked to any input clock. The frequency offset acquiring method is selected by the MAN_HOLDOVER bit, the AUTO_AVG bit and the FAST_AVG bit, as shown in Table 14:

Table 14: Frequency Offset Control in Holdover Mode

MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged
		1	Automatic Fast Averaged
1	don't-care		Manual

3.10.1.6.1 Automatic Instantaneous

By this method, the DPLL freezes at the operating frequency when it enters Holdover mode. The accuracy is $4.4X10^{-8}$ ppm.

3.10.1.6.2 Automatic Slow Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 110 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.6.3 Automatic Fast Averaged

By this method, an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a period of 8 minutes. The accuracy is $1.1X10^{-5}$ ppm.

3.10.1.6.4 Manual

By this method, the frequency offset is set by the HOLDOVER_FREQ[23:0] bits. The accuracy is $1.1X10^{-5}$ ppm.

The frequency offset of the DPLL output is indicated by the CURRENT_DPLL_FREQ[23:0] bits.

The device provides a reference for the value to be written to the HOLDOVER_FREQ[23:0] bits. The value to be written can refer to the value read from the CURRENT_DPLL_FREQ[23:0] bits or the HOLDOVER_FREQ[23:0] bits (refer to Chapter 3.10.1.6.5 Holdover Frequency Offset Read); or then be processed by external software filtering.

3.10.1.6.5 Holdover Frequency Offset Read

The offset value, which is acquired by Automatic Slow Averaged, Automatic Fast Averaged and is set by related register bits, can be read from the HOLDOVER_FREQ[23:0] bits by setting the READ_AVG bit and the FAST_AVG bit, as shown in Table 15.

Table 15: Holdover Frequency Offset Read

READ_AVG	FAST_AVG	Offset Value Read from HOLDOVER_FREQ[23:0]
0	don't-care	The value is equal to the one written to.
1	0	The value is acquired by Automatic Slow Averaged method, not equal to the one written to.
	1	The value is acquired by Automatic Fast Averaged method, not equal to the one written to.

The frequency offset in ppm is calculated as follows:

Holdover Frequency Offset (ppm) = HOLDOVER_FREQ[23:0] X 0.000011

3.10.1.7 Pre-Locked2 Mode

In Pre-Locked2 mode, the DPLL output attempts to track the selected input clock.

The Pre-Locked2 mode is a secondary, temporary mode.

Table 16: Related Bit / Register in Chapter 3.10

Bit	Register	Address (Hex)
CURRENT_PH_DATA[15:0]	CURRENT_DPLL_PHASE[15:8]_STS, CURRENT_DPLL_PHASE[7:0]_STS	69, 68
CURRENT_DPLL_FREQ[23:0]	CURRENT_DPLL_FREQ[23:16]_STS, CURRENT_DPLL_FREQ[15:8]_STS, CURRENT_DPLL_-FREQ[7:0]_STS	64, 63, 62
DPLL_START_BW[4:0]	DPLL_START_BW_DAMPING_CNFG	56
DPLL_START_DAMPING[2:0]		
DPLL_ACQ_BW[4:0]	DPLL_ACQ_BW_DAMPING_CNFG	57
DPLL_ACQ_DAMPING[2:0]		
_DPLL_LOCKED_BW[4:0]	DPLL_LOCKED_BW_DAMPING_CNFG	58
DPLL_LOCKED_DAMPING[2:0]		
AUTO_BW_SEL	BW_OVERSHOOT_CNFG	59
FAST_LOS_SW	PHASE_LOSS_FINE_LIMIT_CNFG	5B *
TEMP_HOLDOVER_MODE[1:0]	HOLDOVER_MODE_CNFG	5C
MAN_HOLDOVER		
AUTO_AVG		
FAST_AVG		
READ_AVG		
HOLDOVER_FREQ[23:0]	HOLDOVER_FREQ[23:16]_CNFG, HOLDOVER_FREQ[15:8]_CNFG, HOLDOVER_FREQ[7:0]_CNFG	5F, 5E, 5D

3.11 DPLL OUTPUT

The DPLL output is locked to the selected input clock. According to the phase-compared result of the feedback and the selected input clock, and the DPLL output frequency offset, the PFD output is limited and the DPLL output is frequency offset limited.

3.11.1 PFD OUTPUT LIMIT

The PFD output is limited to be within ±1 UI or within the coarse phase limit (refer to Chapter 3.7.1.2 Coarse Phase Loss), as determined by the MULTI_PH_APP bit.

3.11.2 FREQUENCY OFFSET LIMIT

The DPLL output is limited to be within the DPLL hard limit (refer to Chapter 3.7.1.4 Hard Limit Exceeding).

The integral path value can be frozen when the DPLL hard limit is reached. This function, enabled by the DPLL_LIMT bit, will minimize the subsequent overshoot when DPLL is pulling in.

3.11.3 HITLESS REFERENCE SWITCHING (HS)

When a hitless switching event is triggered, the phase offset of the selected input clock with respect to the DPLL output is measured. The device then automatically accounts for the measured phase offset and compensates an appropriate phase offset into the DPLL output so that the phase transients on the DPLL output are minimized.

A hitless switch event is triggered if any one of the following conditions occurs:

- The selected input clock switches (the HS_EN bit is '1');
- The DPLL exits from Holdover mode or Free-Run mode (the HS_EN bit is '1');

The phase transients on the DPLL output are minimized to be no more than 0.61 ns with hitless switching. The HS can also be frozen at the current phase offset by setting the HS_FREZ bit. When the HS is frozen, the device will ignore any further HS events triggered by the above two conditions, and maintain the current phase offset. When the HS is disabled, there may be a phase shift on the DPLL output and the DPLL output tracks back to 0 degree phase offset with respect to the selected input clock.

3.11.4 PHASE OFFSET SELECTION

The phase offset of the DPLL selected input clock with respect to the DPLL output can be adjusted. If the device is configured as the Master, the PH_OFFSET_EN bit determines whether the input-to-output phase offset is enabled; if the device is configured as the Slave, the input-to-output phase offset is always enabled. If enabled, the input-to-output phase offset can be adjusted by setting the PH_OFFSET[9:0] bits.

The input-to-output phase offset can be calculated as follows:

Phase Offset (ns) = PH_OFFSET[9:0] X 0.61

3.11.5 PHASE SLOPE LIMITING

To meet the phase slope requirements of Telcordia and ITU-T standards, the DPLL provides a phase slope limiting feature to limit the rate of output phase movement. The limit level is selectable via address 32 in page 1. The following options are available

- GR-1244 ST3: 81ns/1.326ms (61us/s)
- GR-1244 ST2, 3E, ST3(objective): 885ns/s
- G.813 opt1, G.8262 EEC-option 1: 7.5us/s

This feature is disabled by default.

3.11.6 FIVE PATHS OF THE DPLL OUTPUTS

The DPLL output is phase aligned with the selected input clock respectively every 125 µs period. The DPLL has five output paths.

3.11.6.1 DPLL Path

The five paths for the DPLL output are as follows:

- 77.76 MHz path - outputs a 77.76 MHz clock;
- 16E1/16T1 path - outputs a 16E1 or 16T1 clock, as selected by the IN_SONET_SDH bit;
- GSM/OBSAI/16E1/16T1 path - outputs a GSM, OBSAI, 16E1 or 16T1 clock, as selected by the GSM_OBSAI_16E1_16T1_SEL[1:0] bits;
- 12E1/GPS/E3/T3 path - outputs a 12E1, GPS, E3 or T3 clock, as selected by the 12E1_GPS_E3_T3_SEL[1:0] bits;
- 25 MHz path - outputs a 25 MHz clock.

The selected input clock is compared with the DPLL output for DPLL locking. The output can only be derived from the 77.76 MHz path or the 16E1/16T1 path. The output path is automatically selected and the output is automatically divided to get the same frequency as the selected input clock.

The DPLL outputs are provided for APLL or device output process.

Table 17: Related Bit / Register in Chapter 3.11

Bit	Register	Address (Hex)
MULTI_PH_APP	PHASE_LOSS_COARSE_LIMIT_CNFG	5A
DPLL_LIMT	DPLL_BW_OVERSHOOT_CNFG	59
HS_EN	MON_SW_HS_CNFG	0B
HS_FREZ		
PH_OFFSET_EN	PHASE_OFFSET[9:8]_CNFG	7B
PH_OFFSET[9:0]	PHASE_OFFSET[9:8]_CNFG, PHASE_OFFSET[7:0]_CNFG	7B, 7A
IN_SONET_SDH	INPUT_MODE_CNFG	09
GSM_OBSAI_16E1_16T1_SEL[1:0]	DPLL_APLL_PATH_CNFG	55
12E1_GPS_E3_T3_SEL[1:0]		

3.12 APLL

An APLL is provided for a better jitter and wander performance of the device output clocks.

The input of the APLL can be derived from one of the DPLL outputs, as selected by the APLL_PATH[3:0] bits respectively.

Both the APLL and DPLL outputs are provided for selection for the device output.

Table 18: Related Bit / Register in Chapter 3.12

Bit	Register	Address (Hex)
APLL_PATH[3:0]	DPLL_APLL_PATH_CNFG	55

3.12.1 EXTERNAL FILTER

The filter components are connected to VC0 for APLL. Choosing the correct external components and having a printed circuit board (PCB) layout is a key task for quality operation of the APLL external filter option. The APLL loop bandwidth selection table shows Rs, Cs and Cp values for recommend bandwidth. The device has been characterized using these parameters. The external loop filter components should be kept as close as possible to the device. Loop filter traces should be kept short. Other signal traces should be kept separated and not run underneath the device, and loop filter components.

Table 19: APLL Approximate Loop Bandwidth Selection

VC Filter Pin	Rs (Ω)	Cs (uF)	Cp (pF)
External component	220	2.2	510

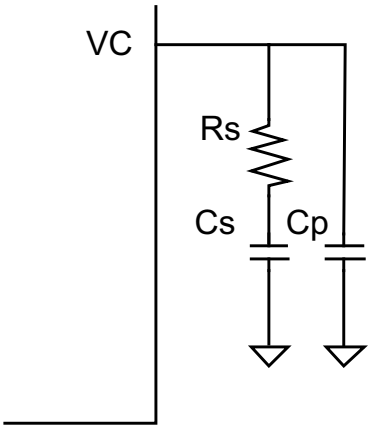

Figure 7. APLL External Filter Components

3.13 OUTPUT CLOCKS

The device supports 3 output clocks.

According to the output port technology, the output ports support the following technologies:

- PECL/LVDS;
- CMOS.

OUT1 outputs a CMOS signal.

OUT2 and OUT3 output a PECL or LVDS signal, as selected by the OUT2_PECL_LVDS bit and the OUT3_PECL_LVDS bit respectively.

The outputs on OUT1 ~ OUT3 are variable, depending on the signals

Table 20: Outputs on OUT1 ~ OUT3 if Derived from DPLL Outputs

OUTn_DIVIDER[3:0] (Output Divider) [1]	Outputs on OUT1 ~ OUT3 if Derived from DPLL Outputs [2]									
	DPLL (77.76 MHz)	DPLL 12E1	DPLL 16E1	DPLL 16T1	DPLL E3	DPLL T3	DPLL (26.0 MHz)	DPLL (25.MHz)	DPLL (30.72 MHz)	DPLL (40.0 MHz)
0000	Output is disabled (output low).									
0001										
0010		12E1	16E1	16T1	E3	T3	26 MHz	25 MHz	30.72 MHz	40 MHz
0011		6E1	8E1	8T1			13 MHz		15.36 MHz	20 MHz
0100		3E1	4E1	4T1					7.68 MHz	10 MHz
0101		2E1								
0110			2E1	2T1					3.84 MHz	5 MHz
0111		E1								
1000			E1	T1						
1001										
1010	64 kHz									
1011	8 kHz									
1100	2 kHz									
1101	400 Hz									
1110	1PPS									
1111	Output is disabled (output high).									

Note:
1. $1 \leq n \leq 3$. Each output is assigned a frequency divider.
2. E1 = 2.048 MHz, T1 = 1.544 MHz, E3 = 34.368 MHz, T3 = 44.736 MHz. The blank cell means the configuration is reserved.

Table 21: Outputs on OUT1 ~ OUT3 if Derived from APLL[1]

OUTn_DIVIDER[3:0] (Output Divider) [2]	Outputs on OUT1 ~ OUT3 if Derived from APLL Output [3]		
	SONET	ETHERNET	Ethernet *66/64
0000	Output is disabled (output low).		
0001	622.08 MHz [4]	625 MHz	625*66/64 MHz
0010	622.08 MHz [4]	625 MHz	625*66/64 MHz
0011	311.04 MHz [4]	312.5 MHz	312.5*66/64 MHz
0100	155.52 MHz	156.25 MHz	156.25*66/64 MHz
0101			
0110	77.76 MHz		
0111	51.84 MHz		
1000	38.88 MHz		
1001	25.92 MHz	125 MHz	125*66/64 MHz
1010	19.44 MHz	25 MHz	25*66/64 MHz
1011			
1100			
1101	6.48 MHz		
1110			
1111	Output is disabled (output high).		

Note:
1. For the APLL path selection, please refer to the registers DPLL_APLL_PATH_CNFG (55H) and in Chapter 6.2.7 DPLL & APLL Configuration Registers.
2. $1 \le n \le 3$. Each output is assigned a frequency divider.
3. In the APLL, the selected DPLL output may be multiplied. The blank cell means the configuration is reserved.
4. The 622.08 MHz, 625 MHz, 312.5 MHz and 311.04 MHz differential signals are only output on OUT2 and OUT3

3.13.1 1 PULSE PER SECOND

The 8V89307 can be used to lock to 1PPS input. The Bandwidth to lock to 1PPS input should be set to 15 mHz.

The 1PPS output can be locked to the input clocks instead of the 1PPS input. If there is no 1PPS input, the 1PPS output can still be generated.

The phase for the 1PPS output can be selected by setting PPS_PHASE[1:0] at the Pulse Per Second Output Configuration register (address 31H on Page 1).

The pulse width for the 1PPS output can be programmed by setting PPS_PULSE[3:0] at the Pulse Per Second Output Configuration register (address 31H on Page 1).

Table 22: Related Bit / Register in Chapter 3.13

Bit	Register	Address (Hex)
OUT2_PECL_LVDS	DIFFERENTIAL_IN_OUT_OSCI_CNFG	0A
OUT3_PECL_LVDS		
OUTn_PATH_SEL[3:0] ($1 \le n \le 3$)	OUT1_FREQ_CNFG ~ OUT3_FREQ_CNFG	6B, 70, 71
OUTn_DIVIDER[3:0] ($1 \le n \le 3$)		
IN_SONET_SDH	INPUT_MODE_CNFG	09
OUTn_INV ($1 \le n \le 3$)	OUT1_INV_CNFG, OUT2-3_INV_CNFG	73, 72
PPS_PHASE[1:0]	PPS_CNFG	31 (Page 1)
PPS_PULSE[3:0]		

3.14 INTERRUPT SUMMARY

The interrupt sources of the device are as follows:

- Input clocks for DPLL validity change
- DPLL selected input clock fail
- DPLL operating mode switch

All of the above interrupt events are indicated by the corresponding interrupt status bit. If the corresponding interrupt enable bit is set, any of the interrupts can be reported by the INT_REQ pin. The output characteristics on the INT_REQ pin are determined by the HZ_EN bit and the INT_POL bit.

Interrupt events are cleared by writing a '1' to the corresponding interrupt status bit. The INT_REQ pin will be inactive only when all the pending enabled interrupts are cleared.

In addition, the interrupt of DPLL selected input clock fail can be reported by the TDO pin, as determined by the LOS_FLAG_TO_TDO bit. Refer to Chapter 6.2.2 Interrupt Registers.

Table 23: Related Bit / Register in Chapter 3.14

Bit	Register	Address (Hex)
HZ_EN	INTERRUPT_CNFG	0C
INT_POL		
LOS_FLAG_TO_TDO	MON_SW_HS_CNFG	0B

3.15 POWER SUPPLY FILTERING TECHNIQUES

To achieve optimum jitter performance, power supply filtering is required to minimize supply noise modulation of the output clocks. The common sources of power supply noise are switch power supplies and the high switching noise from the outputs to the internal PLL. The 8V89307 provides separate VDDA1~VDDA5 power pins for the internal analog PLL. It provides VDD_DIFF, VDD_DIFF2 and VDD_DIFF3 for the differential output driver circuit. It provides VDDD1 and VDDD2 pins for the core logic as well as I/O driver circuits.

For the 8V89307, the decoupling for VDDA1~VDDA5, VDD_DIFF, VDD_DIFF2, VDD_DIFF3, VDDD1 and VDDD2 are handled individually. They should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. Figure 8 on the following page, illustrates how bypass capacitor and ferrite bead should be connected to power pins.

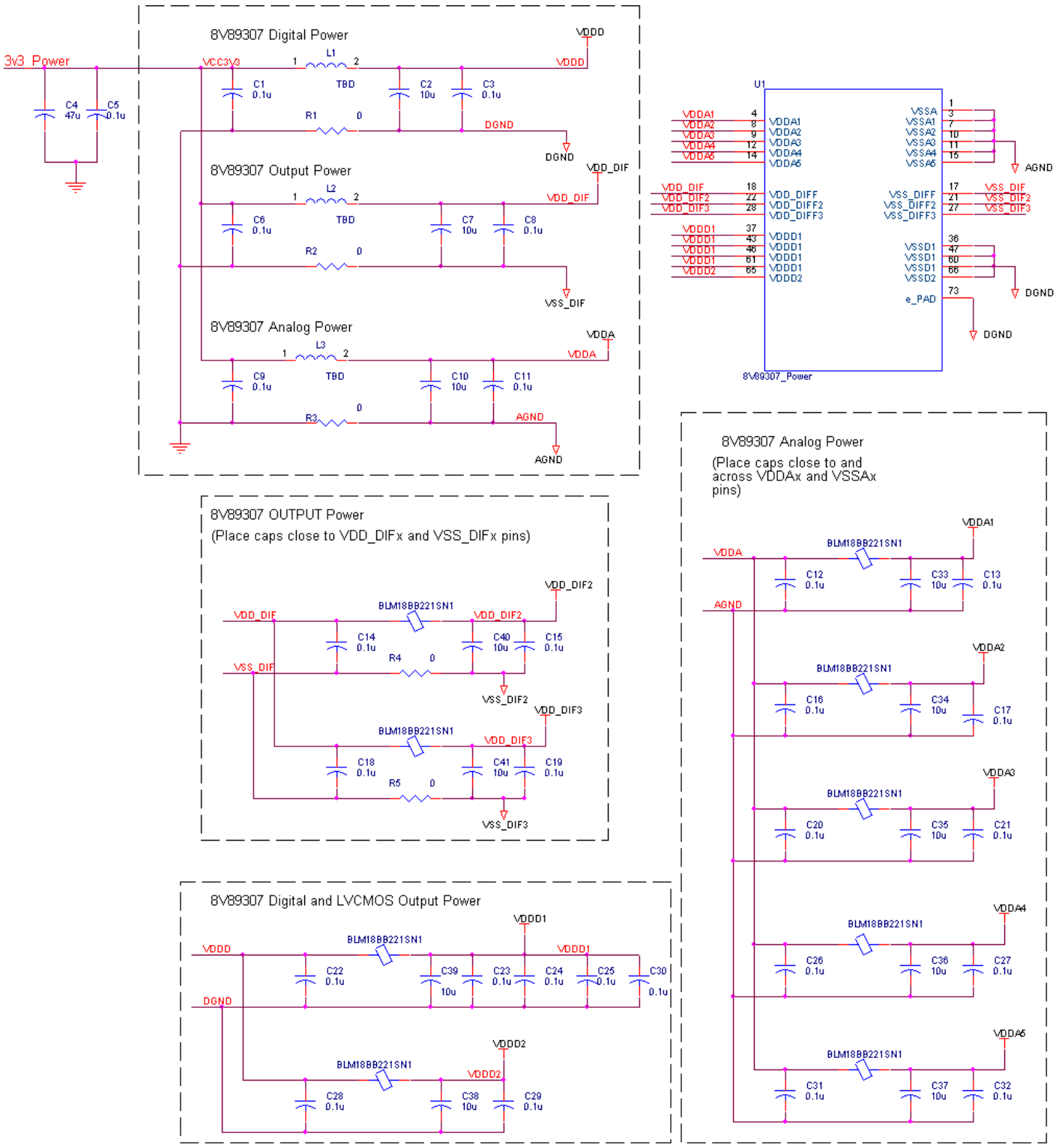

Figure 8. 8V89307 Power Decoupling Scheme

4 MICROPROCESSOR INTERFACE

The microprocessor interface provides access to read and write the registers in the device. The microprocessor interface supports the following modes:

- Serial mode.
- I2C mode

The microprocessor interface mode is selected by the MPU_SEL_CNFG[0] bits (b0, 7FH). The interface pins in different interface modes are listed in Table 24 and Table 25.

Table 24: Microprocessor Interface

MPU_SEL_CNFG[0] bits	Microprocessor Interface Mode	Interface Pins
0	I2C	I2C_AD[2:0], I2C_SDA, I2C_SCL
1	Serial	CS, SCLK, SDI, SDO, CLKE

Table 25: Microprocessor Interface Pins

PIN	MODE	
	SERIAL	I2C
SDI	INPUT	INPUT (Note 1)
CLKE	INPUT	INPUT (Note 1)
SD0/I2C_SDA	OUTPUT	INPUT/ OUTPUT
CS/I2C_AD0	INPUT	INPUT
I2C_AD1	INPUT (Note 1)	INPUT
I2C_AD2	INPUT (Note 1)	INPUT
SCLK/I2C_SCL	INPUT	INPUT
After reset de-assertion, wait 10 us for the mode to be active. Note 1: This pin is not used in this mode, this pin should be connected to ground Note 2: This pin is open drain		

4.1 SERIAL MODE

In a read operation, the active edge of SCLK is selected by CLKE. When CLKE is asserted low, data on SDO will be clocked out on the rising edge of SCLK. When CLKE is asserted high, data on SDO will be clocked out on the falling edge of SCLK.

In a write operation, data on SDI will be clocked in on the rising edge of SCLK.

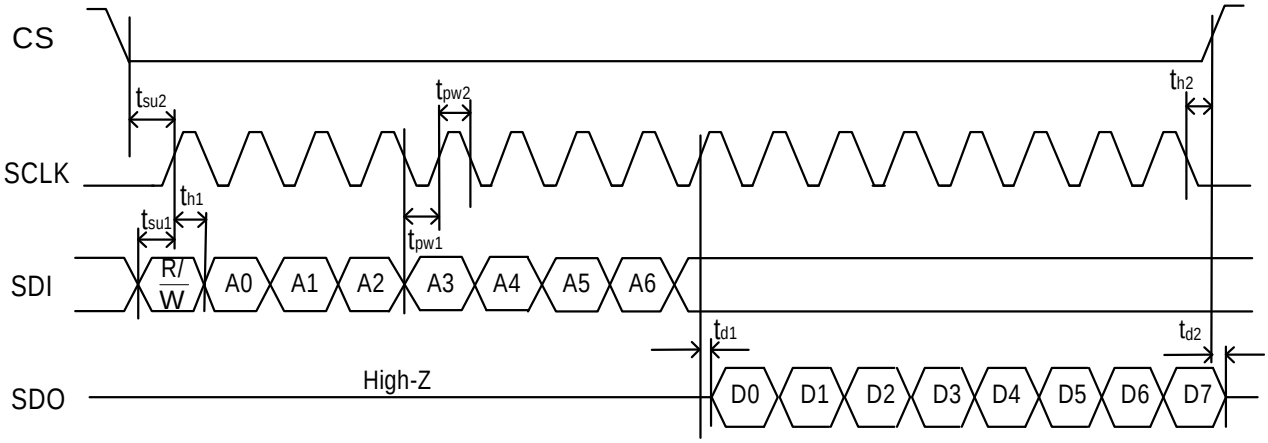

Figure 9. Serial Read Timing Diagram (CLKE Asserted Low)

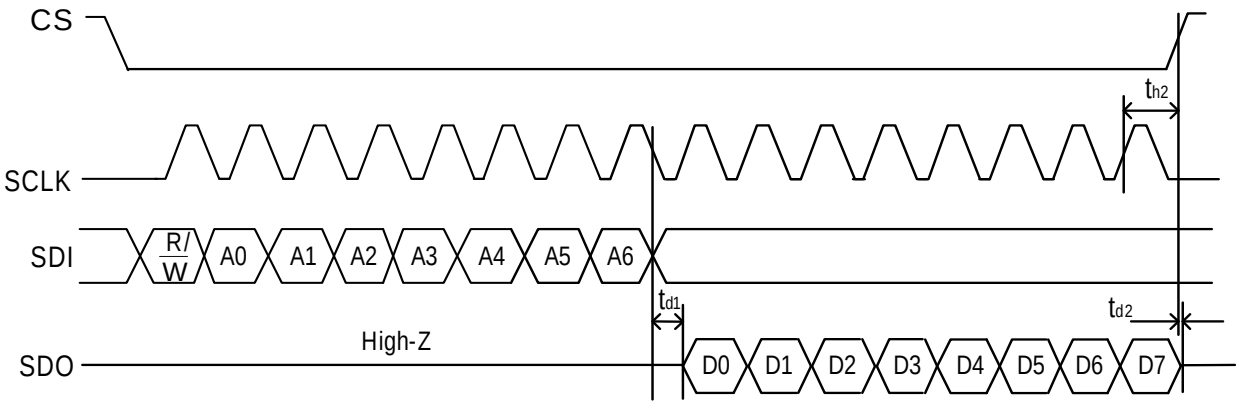

Figure 10. Serial Read Timing Diagram (CLKE Asserted High)

Table 26: Read Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid CS to valid SCLK setup time	14			ns
t_{d1}	Valid SCLK to valid data delay time		10		ns
t_{d2}	CS rising edge to SDO high impedance delay time		10		ns
t_{pw1}	SCLK pulse width low	5T+10			ns
t_{pw2}	SCLK pulse width high	5T+10			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid CS after valid SCLK hold time (CLKE = 0/1)	5			ns
t_{TI}	Time between consecutive Read-Read or Read-Write accesses (CS rising edge to CS falling edge)	10			ns

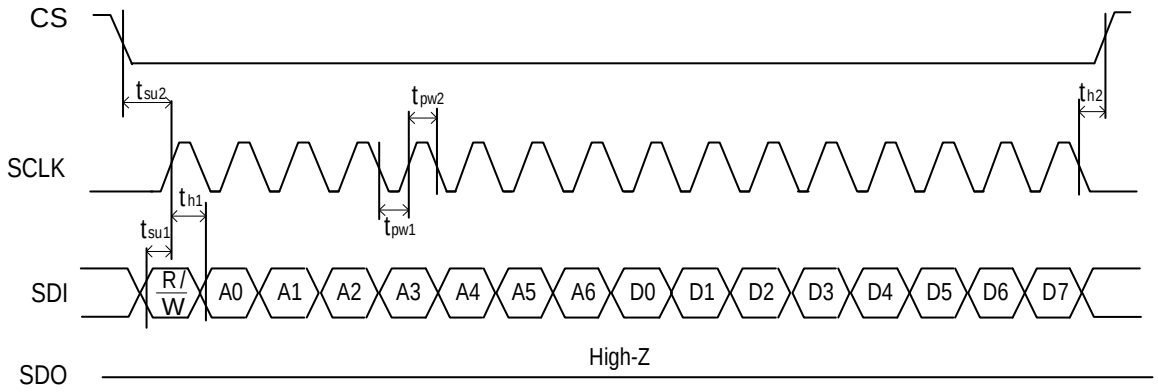

Figure 11. Serial Write Timing Diagram

Table 27: Write Timing Characteristics in Serial Mode

Symbol	Parameter	Min	Typ	Max	Unit
T	One cycle time of the master clock		12.86		ns
t_{in}	Delay of input pad		5		ns
t_{out}	Delay of output pad		5		ns
t_{su1}	Valid SDI to valid SCLK setup time	4			ns
t_{su2}	Valid CS to valid SCLK setup time	14			ns
t_{pw1}	SCLK pulse width low	5T+10			ns
t_{pw2}	SCLK pulse width high	5T+10			ns
t_{h1}	Valid SDI after valid SCLK hold time	6			ns
t_{h2}	Valid CS after valid SCLK hold time	5			ns
t_{TI}	Time between consecutive Write-Write or Write-Read accesses (CS rising edge to CS falling edge)	10			ns

4.2 I2C MODE

4.2.1 I2C DEVICE ADDRESS

The higher 4-bit address is fixed to 4'b1010. The lower 3-bit address is set by pins I2C_AD2, I2C_AD1, I2C_AD0.

4.2.2 I2C BUS TIMING

Figure 12 shows the definition of I2C bus timing.

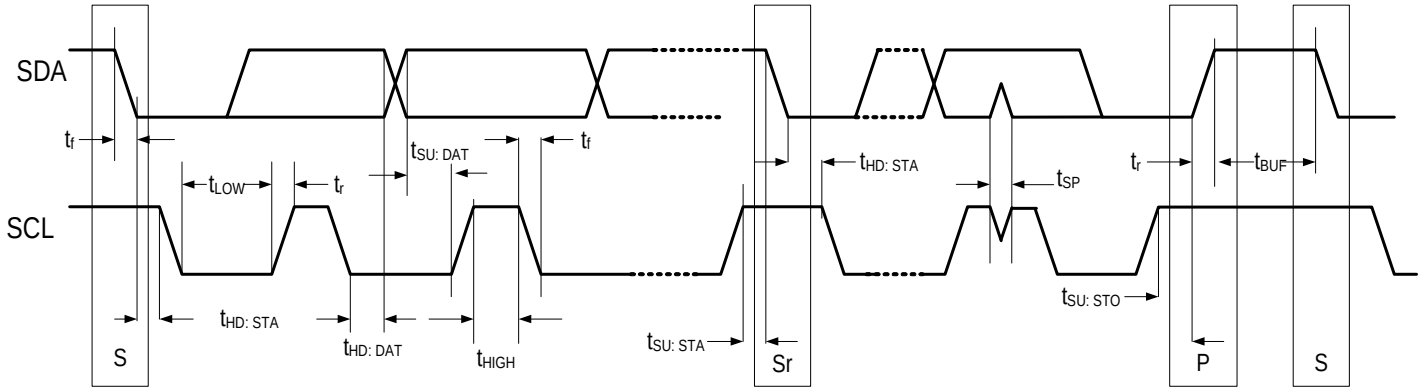

Figure 12. Definition of I2C Bus Timing

Table 28: Timing Definition for Standard Mode and Fast Mode(1)

Symbol	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL	Serial clock frequency	0	100	0	400	kHz
$t_{HD;\ STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.5	-	µs
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	µs
$t_{SU;\ STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;\ DAT}$	Data hold time: for CBUS compatible masters for I^2C-bus devices	5.0 0(2)	- 3.45(3)	- 0(2)	- 0.9(3)	µs
$t_{SU;\ DAT}$	Data set-up time	250	-	100(4)	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	20 + 0.1Cb(5)	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	20 + 0.1Cb(5)	300	ns
$t_{SU;\ STO}$	Set-up time for STOP condition	4.0	-	0.6	-	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF
V_{nL}	Noise margin at the LOW level for each connected device (Including hysteresis)	0.1VDD	-	0.1VDD	-	V
V_{nH}	Noise margin at the HIGH level for each connected device (Including hysteresis)	0.2VDD	-	0.2VDD	-	V
t_{sp}	Pulse width of spikes which must be suppressed by the input filter	0	50	0	50	ns

Note:

1. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 37)
2. A device must Internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin\ o}$f the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;\ DAT\ h}$as only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;\ DAT} \geqslant 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released.
5. C_b = total capacitance of one bus line in pF. If mixed with Hs-mode device, faster fall-times according to Table 38 allowed.

n/a = not applicable

4.2.3 SUPPORTED TRANSACTIONS

The supported types of transactions are shown below.

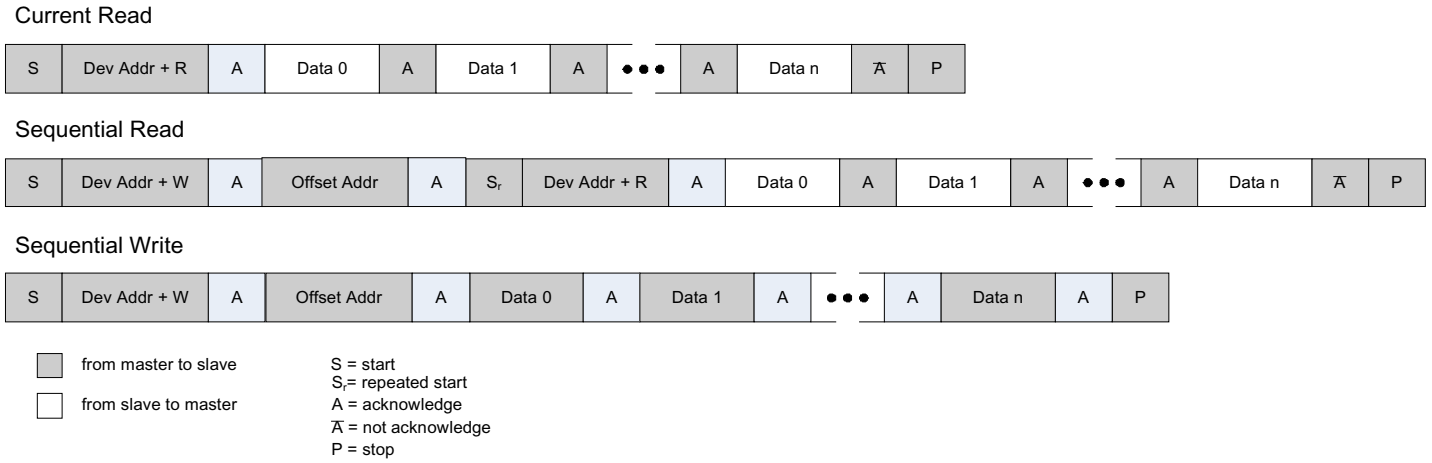

Figure 13. I2C Slave Interface Supported Transactions

Table 29: Description of I2C Slave Interface Supported Transactions

Operation	Description
Current Read	Reads a burst of data from a internal determined starting address, this starting address is equal to the last address accessed during the last read or write operation, incremented by one. If the address exceeds the address space, it will start from 0 again.
Sequential Read	Reads a burst of data from a specified address space. The starting address of the space is specified as offset address.
Sequential Write	Writes a burst of data to a specified address space, the starting address of the space is specified as offset address.

5 JTAG

This device is compliant with the IEEE 1149.1 Boundary Scan standard except the following:

- The output boundary scan cells do not capture data from the core and the device does not support EXTEST instruction;
- The TRST pin is set low by default and JTAG is disabled in order to be consistent with other manufacturers.

The JTAG interface timing diagram is shown in 8V89307 Figure 14.

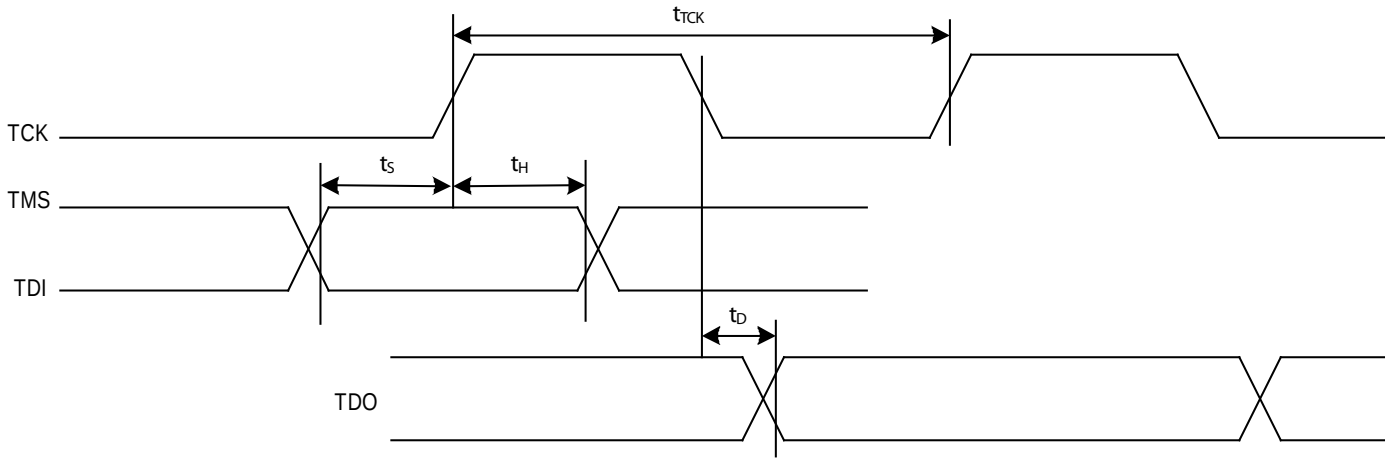

Figure 14. JTAG Interface Timing Diagram

Table 30: JTAG Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{TCK}	TCK period	100			ns
t_S	TMS / TDI to TCK setup time	25			ns
t_H	TCK to TMS / TDI Hold Time	25			ns
t_D	TCK to TDO delay time			50	ns

6 PROGRAMMING INFORMATION

After reset, all the registers are set to their default values. The registers are read or written via the microprocessor interface.

Before any write operation, the value in register PROTECTION_CNFG is recommended to be confirmed to make sure whether the write operation is enabled. The device provides 3 register protection modes:

- Protected mode: no other registers can be written except register PROTECTION_CNFG itself;
- Fully Unprotected mode: all the writable registers can be written;
- Single Unprotected mode: one more register can be written besides register PROTECTION_CNFG. After write operation (not including writing a '1' to clear a bit to '0'), the device automatically switches to Protected mode.

Writing '0' to the registers will take no effect if the registers are cleared by writing '1'.

The access of the Multi-word Registers is different from that of the Single-word Registers. Take the registers (04H, 05H and 06H) for an example, the write operation for the Multi-word Registers follows a fixed sequence. The register (04H) is configured first and the register (06H) is configured last. The three registers are configured continuously and should not be interrupted by any operation. The crystal calibration configuration will take effect after all the three registers are configured. During read operation, the register (04H) is read first and the register (06H) is read last. The crystal calibration reading should be continuous and not be interrupted by any operation.

Certain bit locations within the device register map are designated as Reserved. To ensure proper and predictable operation, bits designated as Reserved must be set with their default values.

6.1 REGISTER MAP

Table 31 depicts the register mapping. Table 32 depicts the register mapping for Page 1 registers. Page 1 is accessible only when PAGE_POINTER is set to '1' in the Page Pointer Configuration Register (address 2DH). When PAGE_POINTER is set to "0"', all registers in the range of addresses 30H through 6FH in Table 31 are selected for access and Page 1 registers in Table 40 cannot be accessed.

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
Global Control Registers										
00	ID[7:0] - Device ID 1	ID[7:0]								P 50
01	ID[15:8] - Device ID 2	ID[15:8]								P 50
02	MPU_PIN_STS - MPU_MODE[2:0] Pins Status	-	-	-	-	-	-	-	MPU_PIN_STS[0]	P 50
03	Reserved	Reserved[7:0]								P 51
04	NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1	NOMINAL_FREQ_VALUE[7:0]								P 51
05	NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2	NOMINAL_FREQ_VALUE[15:8]								P 51
06	NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3	NOMINAL_FREQ_VALUE[23:16]								P 52
08	PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration	MULTI_FACTOR[1:0]		TIME_OUT_VALUE[5:0]						P 52
09	INPUT_MODE_CNFG - Input Mode Configuration	-	-	PH_ALARM_TIMEOUT	-	-	IN_SONET_SDH	-	REVERTIVE_MODE	P 53
0A	DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration	-	-	-	-		OSC_EDGE	OUT3_PECL_LVDS	OUT2_PECL_LVDS	P 53

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
0B	MON_SW_HS_CNFG - Frequency Monitor, Input Clock Selection & HS Control	FREQ_MON_CLK	LOS_FLAG_TO_TDO	ULTR_FAST_SW	-	HS_FREZ	HS_EN	-	FREQ_MON_HARD_EN	P 54
7E	PROTECTION_CNFG - Register Protection Mode Configuration	PROTECTION_DATA[7:0]								P 54
7F	MPU_SEL_CNFG - Microprocessor Interface Mode Configuration	-	-	-	-	-	-	-	MPU_SEL_CNFG[0]	P 55
Interrupt Registers										
0C	INTERRUPT_CNFG - Interrupt Configuration	-	-	-	-	-	-	HZ_EN	INT_POL	P 56
0D	INTERRUPTS1_STS - Interrupt Status 1	-	-	IN2	IN1	-	IN3	-	-	P 56
0E	INTERRUPTS2_STS - Interrupt Status 2	OPERATING_MODE	MAIN_REF_FAILED	-	-	-	-	-	-	P 57
10	INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1	-	-	IN2	IN1		IN3	-	-	P 57
11	INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2	OPERATING_MODE	MAIN_REF_FAILED	-	-	-	-	-	-	P 58
Input Clock Frequency & Priority Configuration Registers										
16	IN3_CNFG - Input Clock 3 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 59
18	IN1_IN2_HF_DIV_CNFG - Input Clock 1 & 2 High Frequency Divider Configuration	IN2_DIV[1:0]		-	-	-	-	IN1_DIV[1:0]		P 60
19	IN1_CNFG - Input Clock 1 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 61
1A	IN2_CNFG - Input Clock 2 Configuration	DIRECT_DIV	LOCK_8K	BUCKET_SEL[1:0]		IN_FREQ[3:0]				P 62
23	PRE_DIV_CH_CNFG - DivN Divider Channel Selection	-	-	-	-	PRE_DIV_CH_VALUE[3:0]				P 63
24	PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1	PRE_DIVN_VALUE[7:0]								P 63
25	PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2	-	PRE_DIVN_VALUE[14:8]							P 64
27	IN3_SEL_PRIORITY_CNFG - Input Clock 3 Priority Configuration *	-	-	-		IN3_SEL_PRIORITY[3:0]				P 64
28	IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *	IN2_SEL_PRIORITY[3:0]				IN1_SEL_PRIORITY[3:0]				P 65
2D	PAGE_POINTER_CNFG	-	-	-	-	-	-	-	PAGE_POINTER	P 66
Input Clock Quality Monitoring Configuration & Status Registers										
2E	FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration	-	-	-	-	FREQ_MON_FACTOR[3:0]				P 66

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
2F	HARD_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Hard Input Clocks Configuration	HARD_FREQ_MON_THRESHOLD[7:4]				HARD_FREQ_MON_THRESHOLD[3:0]				P 67
30	SOFT_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Soft Input Clocks Configuration	SOFT_FREQ_MON_THRESHOLD[7:4]				SOFT_FREQ_MON_THRESHOLD[3:0]				P 67
31	UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0	UPPER_THRESHOLD_0_DATA[7:0]								P 68
32	LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0	LOWER_THRESHOLD_0_DATA[7:0]								P 68
33	BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0	BUCKET_SIZE_0_DATA[7:0]								P 68
34	DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0	-	-	-	-	-	-	DECAY_RATE_0_DATA [1:0]		P 69
35	UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1	UPPER_THRESHOLD_1_DATA[7:0]								P 69
36	LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1	LOWER_THRESHOLD_1_DATA[7:0]								P 69
37	BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1	BUCKET_SIZE_1_DATA[7:0]								P 70
38	DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1	-	-	-	-	-	-	DECAY_RATE_1_DATA [1:0]		P 70
39	UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2	UPPER_THRESHOLD_2_DATA[7:0]								P 70
3A	LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2	LOWER_THRESHOLD_2_DATA[7:0]								P 71
3B	BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2	BUCKET_SIZE_2_DATA[7:0]								P 71
3C	DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2	-	-	-	-	-	-	DECAY_RATE_2_DATA [1:0]		P 71

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
3D	UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3	UPPER_THRESHOLD_3_DATA[7:0]								P 72
3E	LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3	LOWER_THRESHOLD_3_DATA[7:0]								P 72
3F	BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3	BUCKET_SIZE_3_DATA[7:0]								P 72
40	DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3	-	-	-	-	-	-	DECAY_RATE_3_DATA [1:0]		P 73
41	IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection	-	-	-	-	IN_FREQ_READ_CH[3:0]				P 73
42	IN_FREQ_READ_STS - Input Clock Frequency Read Value	IN_FREQ_VALUE[7:0]								P 74
44	IN3_STS - Input Clock 3 Status	-	-	-	-	IN3_FREQ_SOFT_ALARM	IN3_FREQ_HARD_ALARM	IN3_NO_ACTIVITY_ALARM	IN3_PH_LOCK_ALARM	P 74
45	IN1_IN2_STS - Input Clock 1 & 2 Status	IN2_FREQ_SOFT_ALARM	IN2_FREQ_HARD_ALARM	IN2_NO_ACTIVITY_ALARM	IN2_PH_LOCK_ALARM	IN1_FREQ_SOFT_ALARM	IN1_FREQ_HARD_ALARM	IN1_NO_ACTIVITY_ALARM	IN1_PH_LOCK_ALARM	P 75
DPLL Input Clock Selection Registers										
4A	INPUT_VALID1_STS - Input Clocks Validity 1	-	-	IN2	IN1	-	IN3	-	-	P 76
4C	REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1	-	-	IN2_VALID	IN1_VALID	-	IN3_VALID	-	-	P 76
4E	PRIORITY_TABLE1_STS - Priority Status 1 *	HIGHEST_PRIORITY_VALIDATED[3:0]				CURRENTLY_SELECTED_INPUT[3:0]				P 77
4F	PRIORITY_TABLE2_STS - Priority Status 2 *	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]				SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]				P 78
50	INPUT_SEL_CNFG - Selected Input Clock Configuration	-	-	-	-	INPUT_SEL[3:0]				P 78
DPLL State Machine Control Registers										
52	OPERATING_STS - DPLL Operating Status	-	-	DPLL_SOFT_FREQ_ALARM	-	DPLL_LOCK	DPLL_OPERATING_MODE[2:0]			P 79
53	OPERATING_MODE_CNFG - DPLL Operating Mode Configuration	-	-	-	-	-	OPERATING_MODE[2:0]			P 79
DPLL & APLL Configuration Registers										
55	DPLL_APLL_PATH_CNFG - DPLL & APLL Path Configuration	APLL_PATH[3:0]				GSM_OBSAI_16E1_16T1_SEL[1:0]		12E1_GPS_E3_T3_SEL [1:0]		P 80

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
56	DPLL_START_BW_DAMPING_CNFG - DPLL Start Bandwidth & Damping Factor Configuration	DPLL_START_DAMPING[2:0]			DPLL_START_BW[4:0]					P 81
57	DPLL_ACQ_BW_DAMPING_CNFG - DPLL Acquisition Bandwidth & Damping Factor Configuration	DPLL_ACQ_DAMPING[2:0]			DPLL_ACQ_BW[4:0]					P 82
58	DPLL_LOCKED_BW_DAMPING_CNFG - DPLL Locked Bandwidth & Damping Factor Configuration	DPLL_LOCKED_DAMPING[2:0]			DPLL_LOCKED_BW[4:0]					P 83
59	BW_OVERSHOOT_CNFG - DPLL Bandwidth Overshoot Configuration	AUTO_BW_SEL	-	-	-	DPLL_LIMT	-	-	-	P 84
5A	PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *	COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT[3:0]				P 85
5B	PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *	FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT[2:0]			P 86
5C	HOLDOVER_MODE_CNFG - DPLL Holdover Mode Configuration	MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLDOVER_MODE[1:0]		-	-	P 87
5D	HOLDOVER_FREQ[7:0]_CNFG - DPLL Holdover Frequency Configuration 1	HOLDOVER_FREQ[7:0]								P 87
5E	HOLDOVER_FREQ[15:8]_CNFG - DPLL Holdover Frequency Configuration 2	HOLDOVER_FREQ[15:8]								P 88
5F	HOLDOVER_FREQ[23:16]_CNFG - DPLL Holdover Frequency Configuration 3	HOLDOVER_FREQ[23:16]								P 88
62	CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *	CURRENT_DPLL_FREQ[7:0]								P 88
63	CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *	CURRENT_DPLL_FREQ[15:8]								P 89
64	CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *	CURRENT_DPLL_FREQ[23:16]								P 89
65	DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration	FREQ_LIMT_PH_LOS	DPLL_FREQ_SOFT_LIMT[6:0]							P 89
66	DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1	DPLL_FREQ_HARD_LIMT[7:0]								P 90

Table 31: Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
67	DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2	DPLL_FREQ_HARD_LIMT[15:8]								P 90
68	CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *	CURRENT_PH_DATA[7:0]								P 90
69	CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *	CURRENT_PH_DATA[15:8]								P 90
Output Configuration Registers										
6B	OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration	OUT1_PATH_SEL[3:0]				OUT1_DIVIDER[3:0]				P 92
6C	Reserved	Reserved [7:0]								P 92
6D	Reserved	Reserved [7:0]								P 92
6E	Reserved	Reserved [7:0]								P 93
6F	Reserved	Reserved [7:0]								P 93
70	OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration	OUT2_PATH_SEL[3:0]				OUT2_DIVIDER[3:0]				P 93
71	OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration	OUT3_PATH_SEL[3:0]				OUT3_DIVIDER[3:0]				P 94
72	OUT2-3_INV_CNFG - Output Clock2 and 3 Invert Configuration	-	-	-	-	-	-	OUT3_INV	OUT2_INV	P 94
73	OUT1_INV_CNFG - Output Clock 1 Invert Configuration	Reserved [7:1]							OUT1_INV	P 95
Phase Offset Control Registers										
78	PHASE_MON_CNFG - Phase Transient Monitor Configuration	IN_NOISE_WINDOW	-	-	-	-	-	-	-	P 96
79	Reserved	Reserved [7:0]								P 51
7A	PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1	PH_OFFSET[7:0]								P 96
7B	PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2	PH_OFFSET_EN	-	-	-	-	-	PH_OFFSET[9:8]		P 97

Table 32: Page 1 Register List and Mapping

Address (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reference Page
30	DFS_OFF_CNFG - Digital Frequency Synthesizer Configuration	DFS_OFF[3]	DFS_OFF [2]	DFS_OFF[1]	DFS_OFF [0]	Reserved[3:0]				P 97
31	PPS_CNFG - 1 Pulse Per Second Configuration	-	-	PPS_PHASE[1:0]		PPS_PULSE[3:0]				P 98
32	PH_SLOPE_CNFG - Phase Slope Limiting	-	-	-	-	PH_SLOPE[1:0]		-	-	P 99
33	ICP_CTRL_CNFG_REG - APLL Charge Pump Current Configuration	-	-	-	ICP_CTRL_CODE[4:0]					P 99

6.2 REGISTER DESCRIPTION

6.2.1 GLOBAL CONTROL REGISTERS

ID[7:0] - Device ID 1

Address: 00H
Type: Read
Default Value: 10010001

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bit	Name	Description
7 - 0	ID[7:0]	Refer to the description of the ID[15:8] bits (b7~0, 01H).

ID[15:8] - Device ID 2

Address: 01H
Type: Read
Default Value: 00110011

7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit	Name	Description
7 - 0	ID[15:8]	The value in the ID[15:0] bits are pre-set, representing the identification number for the 8V89307.

MPU_PIN_STS - MPU_MODE[2:0] Pins Status

Address: 02H
Type: Read
Default Value: XXXXXXXX

7	6	5	4	3	2	1	0
-	-	-	-	-	-		MPU_PIN_STS0

Bit	Name	Description
7 - 1	-	Reserved.
0	MPU_PIN_STS[0]	This bit indicates the value of the MPU_MODE pin. The default value of this bit is determined by the MPU_MODE pin during reset. 0: I2C mode 1: Serial mode

Reserved

Address: 03H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 00111100 for normal operation.

NOMINAL_FREQ[7:0]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 1

Address: 04H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VALUE7	NOMINAL_-FREQ_VALUE6	NOMINAL_-FREQ_VALUE5	NOMINAL_-FREQ_VALUE4	NOMINAL_-FREQ_VALUE3	NOMINAL_-FREQ_VALUE2	NOMINAL_-FREQ_VALUE1	NOMINAL_-FREQ_VALUE0

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[7:0]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[15:8]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 2

Address: 05H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VAL-UE15	NOMINAL_-FREQ_VAL-UE14	NOMINAL_-FREQ_VAL-UE13	NOMINAL_-FREQ_VAL-UE12	NOMINAL_-FREQ_VAL-UE11	NOMINAL_-FREQ_VAL-UE10	NOMINAL_-FREQ_VALUE9	NOMINAL_-FREQ_VALUE8

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[15:8]	Refer to the description of the NOMINAL_FREQ_VALUE[23:16] bits (b7~0, 06H).

NOMINAL_FREQ[23:16]_CNFG - Crystal Oscillator Frequency Offset Calibration Configuration 3

Address: 06H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
NOMINAL_-FREQ_VAL-UE23	NOMINAL_-FREQ_VAL-UE22	NOMINAL_-FREQ_VAL-UE21	NOMINAL_-FREQ_VAL-UE20	NOMINAL_-FREQ_VAL-UE19	NOMINAL_-FREQ_VAL-UE18	NOMINAL_-FREQ_VAL-UE17	NOMINAL_-FREQ_VAL-UE16

Bit	Name	Description
7 - 0	NOMINAL_FREQ_VALUE[23:16]	The NOMINAL_FREQ_VALUE[23:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.0000884, the calibration value for the master clock in ppm will be gotten. For example, the frequency offset on OSCI is +3 ppm. Though -3 ppm should be compensated, the calibration value is calculated as +3 ppm: 3 ÷ 0.0000884 = 33937 (Dec.) = 8490 (Hex); So '008490' should be written into these bits. The calibration range is within ±741 ppm.

PHASE_ALARM_TIME_OUT_CNFG - Phase Lock Alarm Time-Out Configuration

Address: 08H
Type: Read / Write
Default Value: 00110010

7	6	5	4	3	2	1	0
MULTI_FAC-TOR1	MULTI_FAC-TOR0	TIME_OUT_VALUE5	TIME_OUT_VALUE4	TIME_OUT_VALUE3	TIME_OUT_VALUE2	TIME_OUT_VALUE1	TIME_OUT_VALUE0

Bit	Name	Description
7 - 6	MULTI_FACTOR[1:0]	These bits determine a factor which has a relationship with a period in seconds. A phase lock alarm will be raised if the DPLL selected input clock is not locked in DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised). Refer to the description of the TIME_OUT_VALUE[5:0] bits (b5~0, 08H). 00: 2 (default) 01: 4 10: 8 11: 16
5 - 0	TIME_OUT_VALUE[5:0]	These bits represent an unsigned integer. If the value in these bits is multiplied by the value in the MULTI_FACTOR[1:0] bits (b7~6, 08H), a period in seconds will be gotten. A phase lock alarm will be raised if the DPLL selected input clock is not locked in DPLL within this period. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', the phase lock alarm will be cleared after this period (starting from when the alarm is raised).

INPUT_MODE_CNFG - Input Mode Configuration

Address: 09H
Type: Read / Write
Default Value: 101000X0

7	6	5	4	3	2	1	0
-	-	PH_ALARM_-TIMEOUT	-	-	IN_SON-ET_SDH	-	REVERTIVE_-MODE

Bit	Name	Description
7-6	-	Reserved
5	PH_ALARM_TIMEOUT	This bit determines how to clear the phase lock alarm. 0: The phase lock alarm will be cleared when a '1' is written to the corresponding INn_PH_LOCK_ALARM bit (b4/0, 43H~49H). 1: The phase lock alarm will be cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised. (default)
4 - 3	-	Reserved
2	IN_SONET_SDH	This bit selects the SDH or SONET network type. 0: SDH. The DPLL required clock is 2.048 MHz when the IN_FREQ[3:0] bits (b3~0, 16H & 19H~1AH) are '0001'; the DPLL output from the 16E1/16T1 path is 16E1. 1: SONET. The DPLL required clock is 1.544 MHz when the IN_FREQ[3:0] bits (b3~0, 16H & 19H~1AH) are '0001'; the DPLL output from the 16E1/16T1 path is 16T1.
1	-	Reserved
0	REVERTIVE_MODE	This bit selects Revertive or Non-Revertive switching for the DPLL. 0: Non-Revertive switching. (default) 1: Revertive switching.

DIFFERENTIAL_IN_OUT_OSCI_CNFG - Differential Input / Output Port & Master Clock Configuration

Address: 0AH
Type: Read / Write
Default Value: XXXXX001

7	6	5	4	3	2	1	0
-	-	-	-	-	OSC_EDGE	OUT3_PECL_LVDS	OUT2_PECL_LVDS

Bit	Name	Description
7 - 3	-	Reserved.
2	OSC_EDGE	This bit selects a better active edge of the master clock. 0: The rising edge. (default) 1: The falling edge.
1	OUT3_PECL_LVDS	This bit selects a port technology for OUT3. 0: LVDS. (default) 1: PECL.
0	OUT2_PECL_LVDS	This bit selects a port technology for OUT2. 0: LVDS. 1: PECL. (default)

MON_SW_HS_CNFG - Frequency Monitor, Input Clock Selection & HS Control

Address: 0BH
Type: Read / Write
Default Value: 100001X1

7	6	5	4	3	2	1	0
FREQ_MON_-CLK	LOS_-FLAG_TO_TDO	ULTR_FAST_SW	-	HS_FREZ	HS_EN	-	FRE-Q_MON_HARD_EN

Bit	Name	Description
7	FREQ_MON_CLK	The bit selects a reference clock for input clock frequency monitoring. 0: The output of the DPLL. 1: The master clock. (default)
6	LOS_FLAG_TO_TDO	The bit determines whether the interrupt of DPLL selected input clock fail - is reported by the TDO pin. 0: Not reported. TDO pin is used as JTAG test data output which complies with IEEE 1149.1. (default) 1: Reported. TDO pin mimics the state of the MAIN_REF_FAILED bit (b6, 0EH) and does not strictly comply with IEEE 1149.1.
5	ULTR_FAST_SW	This bit determines whether the DPLL selected input clock is valid when missing 2 consecutive clock cycles or more. 0: Valid. (default) 1: Invalid.
4	-	Reserved.
3	HS_FREZ	This bit is valid only when the HS is enabled by the HS_EN bit (b2, 0BH). It determines whether HS is frozen at the current phase offset when a HS event is triggered. 0: Not frozen. (default) 1: Frozen. Further HS events are ignored and the current phase offset is maintained.
2	HS_EN	This bit determines whether HS is enabled when the DPLL selected input clock switch or the DPLL exiting from Holdover mode or Free-Run mode occurs. 0: Disabled. 1: Enabled. (default)
1	-	Reserved.
0	FREQ_MON_HARD_EN	This bit determines whether the frequency hard alarm is enabled when the frequency of the input clock with respect to the reference clock is above the frequency hard alarm threshold. The reference clock can be the output of DPLL or the master clock, as determined by the FREQ_MON_CLK bit (b7, 0BH). 0: Disabled. 1: Enabled. (default)

PROTECTION_CNFG - Register Protection Mode Configuration

Address: 7EH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
PROTEC-TION_DATA7	PROTEC-TION_DATA6	PROTEC-TION_DATA5	PROTEC-TION_DATA4	PROTEC-TION_DATA3	PROTEC-TION_DATA2	PROTEC-TION_DATA1	PROTEC-TION_DATA0

Bit	Name	Description
7 - 0	PROTECTION_DATA[7:0]	These bits select a register write protection mode. 00000000 - 10000100, 10000111 - 11111111: Protected mode. No other registers can be written except this register. 10000101: Fully Unprotected mode. All the writable registers can be written. (default) 10000110: Single Unprotected mode. One more register can be written besides this register. After write operation (not including writing a '1' to clear the bit to '0'), the device automatically switches to Protected mode.

MPU_SEL_CNFG - Microprocessor Interface Mode Configuration

Address: 7FH
Type: Read / Write
Default Value: XXXXXXXX

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	MPU_SEL_CNFG

Bit	Name	Description
7 - 3	-	Reserved.
0	MPU_SEL_CNFG[0]	This bit selects a microprocessor interface mode: 0: I2C mode. 1: Serial mode. The default value of this bit is determined by the MPU_MODE pin during reset.

6.2.2 INTERRUPT REGISTERS

INTERRUPT_CNFG - Interrupt Configuration

Address: 0CH
Type: Read / Write
Default Value: XXXXXX10

7	6	5	4	3	2	1	0
-	-	-	-	-	-	HZ_EN	INT_POL

Bit	Name	Description
7 - 2	-	Reserved.
1	HZ_EN	This bit determines the output characteristics of the INT_REQ pin. 0: The output on the INT_REQ pin is high/low when the interrupt is active; the output is the opposite when the interrupt is inactive. 1: The output on the INT_REQ pin is high/low when the interrupt is active; the output is in high impedance state when the interrupt is inactive. (default)
0	INT_POL	This bit determines the active level on the INT_REQ pin for an active interrupt indication. 0: Active low. (default) 1: Active high.

INTERRUPTS1_STS - Interrupt Status 1

Address: 0DH
Type: Read / Write
Default Value: 11111111

7	6	5	4	3	2	1	0
-	-	IN2	IN1	-	IN3	-	-

Bit	Name	Description
7-6	-	Reserved
5 - 4	INn	This bit indicates the validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’) for the corresponding INn; i.e., whether there is a transition (from ‘0’ to ‘1’ or from ‘1’ to ‘0’) on the corresponding INn bit (b5~2, 4AH), $1 \le n \le 2$. 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a ‘1’.
3	-	Reserved
2	IN3	This bit indicates the validity changes (from ‘valid’ to ‘invalid’ or from ‘invalid’ to ‘valid’) for the corresponding IN2; i.e., whether there is a transition (from ‘0’ to ‘1’ or from ‘1’ to ‘0’) on the corresponding IN3 bit (b5~2, 4AH). 0: Has not changed. 1: Has changed. (default) This bit is cleared by writing a ‘1’.
1-0	-	Reserved

INTERRUPTS2_STS - Interrupt Status 2

Address: 0EH
Type: Read / Write
Default Value: 00111111

7	6	5	4	3	2	1	0
OPERATING_MODE	MAIN_REF_FAILED	-	-	-	-	-	-

Bit	Name	Description
7	OPERATING_MODE	This bit indicates the operating mode switch for the DPLL; i.e., whether the value in the DPLL_OPERATING_MODE[2:0] bits (b2~0, 52H) changes. 0: Has not switched. (default) 1: Has switched. This bit is cleared by writing a '1'.
6	MAIN_REF_FAILED	This bit indicates whether the DPLL selected input clock has failed. The DPLL selected input clock fails when its validity changes from 'valid' to 'invalid'; i.e., when there is a transition from '1' to '0' on the corresponding INn bit (4AH, 4BH). 0: Has not failed. (default) 1: Has failed. This bit is cleared by writing a '1'.
5-0	-	Reserved

INTERRUPTS1_ENABLE_CNFG - Interrupt Control 1

Address: 10H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
-	-	IN2	IN1	-	IN3	-	-

Bit	Name	Description
7-6	-	Reserved
5 - 4	INn	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding INn bit (b5~2, 0DH) is '1', $1 \le n \le 2$. 0: Disabled. (default) 1: Enabled.
3	-	Reserved
2	IN3	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the input clock validity changes (from 'valid' to 'invalid' or from 'invalid' to 'valid'), i.e., when the corresponding IN3 bit (b5~2, 0DH) is '1'. 0: Disabled. (default) 1: Enabled.
1-0	-	Reserved

INTERRUPTS2_ENABLE_CNFG - Interrupt Control 2

Address: 11H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
OPERATING_MODE	MAIN_REF_FAILED	-	-	-	-	-	-

Bit	Name	Description
7	OPERATING_MODE	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the DPLL operating mode switches, i.e., when the OPERATING_MODE bit (b7, 0EH) is '1'. 0: Disabled. (default) 1: Enabled.
6	MAIN_REF_FAILED	This bit controls whether the interrupt is enabled to be reported on the INT_REQ pin when the DPLL selected input clock has failed; i.e., when the MAIN_REF_FAILED bit (b6, 0EH) is '1'. 0: Disabled. (default) 1: Enabled.
5-0	-	Reserved

6.2.3 INPUT CLOCK FREQUENCY & PRIORITY CONFIGURATION REGISTERS

IN3_CNFG - Input Clock 3 Configuration

Address: 16H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 16H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 16H), determines whether the DivN Divider or the Lock 8k Divider is used for IN3. DIRECT_DIV bit / LOCK_8K bit / Used Divider 0 / 0 / Both bypassed (default) 0 / 1 / Lock 8k Divider 1 / 0 / DivN Divider 1 / 1 / Reserved
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN3. 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN3. 0000: 8 kHz. (default) 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: 1PPS. 1100: 6.25 MHz. 1101: 10MHz. 1110 ~ 1111: Reserved. For IN3, the required frequency should not be set higher than that clock.

IN1_IN2_HF_DIV_CNFG - Input Clock 1 & 2 High Frequency Divider Configuration

Address: 18H
Type: Read / Write
Default Value: 00XXXX00

7	6	5	4	3	2	1	0
IN2_DIV1	IN2_DIV0	-	-	-	-	IN1_DIV1	IN1_DIV0

Bit	Name	Description
7 - 6	IN2_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN2 frequency division. 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.
5 - 2	-	Reserved.
1 - 0	IN1_DIV[1:0]	These bits determine whether the HF Divider is used and what the division factor is for IN1 frequency division. 00: Bypassed. (default) 01: Divided by 4. 10: Divided by 5. 11: Reserved.

IN1_CNFG - Input Clock 1 Configuration

Address: 19H
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 19H).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 19H), determines whether the DivN Divider or the Lock 8k Divider is used for IN1. DIRECT_DIV bit / LOCK_8K bit / Used Divider 0 / 0 / Both bypassed (default) 0 / 1 / Lock 8k Divider 1 / 0 / DivN Divider 1 / 1 / Reserved
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN1. 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN1. 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: 1PPS. 1100: 6.25 MHz. 1101: 10MHz. 1110 ~ 1111: Reserved. The required frequency should not be set higher than that clock.

IN2_CNFG - Input Clock 2 Configuration

Address: 1AH
Type: Read / Write
Default Value: 00000011

7	6	5	4	3	2	1	0
DIRECT_DIV	LOCK_8K	BUCKET_SEL1	BUCKET_SEL0	IN_FREQ3	IN_FREQ2	IN_FREQ1	IN_FREQ0

Bit	Name	Description
7	DIRECT_DIV	Refer to the description of the LOCK_8K bit (b6, 1AH).
6	LOCK_8K	This bit, together with the DIRECT_DIV bit (b7, 1AH), determines whether the DivN Divider or the Lock 8k Divider is used for IN2.
5 - 4	BUCKET_SEL[1:0]	These bits select one of the four groups of leaky bucket configuration registers for IN2. 00: Group 0; the addresses of the configuration registers are 31H ~ 34H. (default) 01: Group 1; the addresses of the configuration registers are 35H ~ 38H. 10: Group 2; the addresses of the configuration registers are 39H ~ 3CH. 11: Group 3; the addresses of the configuration registers are 3DH ~ 40H.
3 - 0	IN_FREQ[3:0]	These bits set the DPLL required frequency for IN2. 0000: 8 kHz. 0001: 1.544 MHz (when the IN_SONET_SDH bit (b2, 09H) is '1') / 2.048 MHz (when the IN_SONET_SDH bit (b2, 09H) is '0'). 0010: 6.48 MHz. 0011: 19.44 MHz. (default) 0100: 25.92 MHz. 0101: 38.88 MHz. 0110 ~ 1000: Reserved. 1001: 2 kHz. 1010: 4 kHz. 1011: 1PPS. 1100: 6.25 MHz. 1101: 10 MHz. 1110 ~ 1111: Reserved. For IN2, the required frequency should not be set higher than that clock.

DIRECT_DIV bit	LOCK_8K bit	Used Divider
0	0	Both bypassed (default)
0	1	Lock 8k Divider
1	0	DivN Divider
1	1	Reserved

PRE_DIV_CH_CNFG - DivN Divider Channel Selection

Address: 23H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	PRE_DIV_CH_VALUE3	PRE_DIV_CH_VALUE2	PRE_DIV_CH_VALUE1	PRE_DIV_CH_VALUE0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	PRE_DIV_CH_VALUE[3:0]	This register is an indirect address register for Register 24H and 25H. These bits select an input clock. The value set in the PRE_DIVN_VALUE[14:0] bits (25H, 24H) is available for the selected input clock. 0000: Reserved. (default) 0001, 0010: Reserved. 0011: IN3. 0100: Reserved. 0101: IN1. 0110: IN2. 0111 - 1111: Reserved.

PRE_DIVN[7:0]_CNFG - DivN Divider Division Factor Configuration 1

Address: 24H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
PRE_DIVN_ VALUE7	PRE_DIVN_ VALUE6	PRE_DIVN_ VALUE5	PRE_DIVN_ VALUE4	PRE_DIVN_ VALUE3	PRE_DIVN_ VALUE2	PRE_DIVN_ VALUE1	PRE_DIVN_ VALUE0

Bit	Name	Description
7 - 0	PRE_DIVN_VALUE[7:0]	Refer to the description of the PRE_DIVN_VALUE[14:8] bits (b6~0, 25H).

PRE_DIVN[14:8]_CNFG - DivN Divider Division Factor Configuration 2

Address: 25H
Type: Read / Write
Default Value: X0000000

7	6	5	4	3	2	1	0
-	PRE_DIVN_ VALUE14	PRE_DIVN_ VALUE13	PRE_DIVN_ VALUE12	PRE_DIVN_ VALUE11	PRE_DIVN_ VALUE10	PRE_DIVN_ VALUE9	PRE_DIVN_ VALUE8

Bit	Name	Description
7	-	Reserved.
6 - 0	PRE_DIVN_VALUE[14:8]	If the value in the PRE_DIVN_VALUE[14:0] bits is plus 1, the division factor for an input clock will be gotten. The input clock is selected by the PRE_DIV_CH_VALUE[3:0] bits (b3~0, 23H). A value from '0' to '4BEF' (Hex) can be written into, corresponding to a division factor from 1 to 19440. The others are reserved. So the DivN Divider only supports an input clock whose frequency is less than or equal to (≤) 155.52 MHz. The division factor setting should observe the following order: 1. Write the lower eight bits of the division factor to the PRE_DIVN_VALUE[7:0] bits. 2. Write the higher eight bits of the division factor to the PRE_DIVN_VALUE[14:8] bits.

IN3_SEL_PRIORITY_CNFG - Input Clock 3 Priority Configuration *

Address: 27H
Type: Read / Write
Default Value: 01010100

7	6	5	4	3	2	1	0
	-	-	-	IN3_SEL_ PRIORITY3	IN3_SEL_ PRIORITY2	IN3_SEL_ PRIORITY1	IN3_SEL_ PRIORITY0

Bit	Name	Description
7 - 4	-	Reserved
3 - 0	IN3_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding IN3. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. (default) 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

IN1_IN2_SEL_PRIORITY_CNFG - Input Clock 1 & 2 Priority Configuration *

Address: 28H
Type: Read / Write
Default Value: 01110110

7	6	5	4	3	2	1	0
IN2_SEL_ PRIORITY3	IN2_SEL_ PRIORITY2	IN2_SEL_ PRIORITY1	IN2_SEL_ PRIORITY0	IN1_SEL_ PRIORITY3	IN1_SEL_ PRIORITY2	IN1_SEL_ PRIORITY1	IN1_SEL_ PRIORITY0

Bit	Name	Description
7 - 4	IN2_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding IN2. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. 0111: Priority 7. (default) 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.
3 - 0	IN1_SEL_PRIORITY[3:0]	These bits set the priority of the corresponding IN1. 0000: Disable INn for automatic selection. 0001: Priority 1. 0010: Priority 2. 0011: Priority 3. 0100: Priority 4. 0101: Priority 5. 0110: Priority 6. (default) 0111: Priority 7. 1000: Priority 8. 1001: Priority 9. 1010: Priority 10. 1011: Priority 11. 1100: Priority 12. 1101: Priority 13. 1110: Priority 14. 1111: Priority 15.

PAGE_POINTER_CNFG - Page Pointer Configuration

Address: 2DH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	PAGE_POINTER

Bit	Name	Description
7 - 2	-	Reserved
1	-	Reserved - must be set to 0 for normal operation
0	PAGE_POINTER	Page pointer (0 default) 0: page0 can be operated 1: page1 can be operated

6.2.4 INPUT CLOCK QUALITY MONITORING CONFIGURATION & STATUS REGISTERS

FREQ_MON_FACTOR_CNFG - Factor of Frequency Monitor Configuration

Address: 2EH
Type: Read / Write
Default Value: XXXX1011

7	6	5	4	3	2	1	0
-	-	-	-	FREQ_MON_ FACTOR3	FREQ_MON_ FACTOR2	FREQ_MON_ FACTOR1	FREQ_MON_ FACTOR0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	FREQ_MON_FACTOR[3:0]	These bits determine a factor. The factor has a relationship with the frequency hard alarm threshold in ppm (refer to the description of the HARD_FREQ_MON_THRESHOLD[7:0] bits (b7~0, 2FH)) and with the frequency of the input clock with respect to the master clock in ppm (refer to the description of the IN_FREQ_VALUE[7:0] bits (b7~0, 42H)). The factor represents the accuracy of the frequency monitor and should be set according to the requirements of different applications. 0000: 0.0032. 0001: 0.0064. 0010: 0.0127. 0011: 0.0257. 0100: 0.0514. 0101: 0.103. 0110: 0.206. 0111: 0.412. 1000: 0.823. 1001: 1.646. 1010: 3.292. 1011: 3.81. (default) 1100 - 1111: 4.6.

HARD_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Hard Input Clocks Configuration

Address: 2FH
Type: Read / Write
Default Value: 00100011

7	6	5	4	3	2	1	0
HARD_FREQ_MON_THRESHOLD7	HARD_FREQ_MON_THRESHOLD6	HARD_FREQ_MON_THRESHOLD5	HARD_FREQ_MON_THRESHOLD4	HARD_FREQ_MON_THRESHOLD3	HARD_FREQ_MON_THRESHOLD2	HARD_FREQ_MON_THRESHOLD1	HARD_FREQ_MON_THRESHOLD0

Bit	Name	Description
7 - 4	HARD_FREQ_MON_THRESHOLD[7:4]	These bits are the accepting threshold of reference clock monitoring. The frequency hard alarm threshold in ppm is calculated as follows: *Frequency Hard Alarm Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.
3 - 0	HARD_FREQ_MON_THRESHOLD[3:0]	These bits are the rejecting threshold of reference clock monitoring. The frequency hard alarm threshold in ppm is calculated as follows: *Frequency Hard Alarm Threshold (ppm) = (HARD_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.

SOFT_FREQ_MON_THRESHOLD_CNFG - Frequency Monitor Threshold for Soft Input Clocks Configuration

Address: 30H
Type: Read / Write
Default Value: 00100011

7	6	5	4	3	2	1	0
SOFT_FREQ_MON_THRESHOLD7	SOFT_FREQ_MON_THRESHOLD6	SOFT_FREQ_MON_THRESHOLD5	SOFT_FREQ_MON_THRESHOLD4	SOFT_FREQ_MON_THRESHOLD3	SOFT_FREQ_MON_THRESHOLD2	SOFT_FREQ_MON_THRESHOLD1	SOFT_FREQ_MON_THRESHOLD0

Bit	Name	Description
7 - 4	SOFT_FREQ_MON_THRESHOLD[7:4]	These bits are the accepting threshold of reference clock monitoring. The frequency soft alarm threshold in ppm is calculated as follows: *Frequency Soft Alarm Threshold (ppm) = (SOFT_FREQ_MON_THRESHOLD[7:4] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.
3 - 0	SOFT_FREQ_MON_THRESHOLD[3:0]	These bits are the rejecting threshold of reference clock monitoring. The frequency soft alarm threshold in ppm is calculated as follows: *Frequency Soft Alarm Threshold (ppm) = (SOFT_FREQ_MON_THRESHOLD[3:0] + 1) X FREQ_MON_FACTOR[3:0] (b3~0, 2EH)* This threshold is symmetrical about zero.A value of 0010 bin corresponds to an alarm limit of +/- 11.43 ppm.

UPPER_THRESHOLD_0_CNFG - Upper Threshold for Leaky Bucket Configuration 0

Address: 31H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_0_DATA7	UPPER_-THRESH-OLD_0_DATA6	UPPER_-THRESH-OLD_0_DATA5	UPPER_-THRESH-OLD_0_DATA4	UPPER_-THRESH-OLD_0_DATA3	UPPER_-THRESH-OLD_0_DATA2	UPPER_-THRESH-OLD_0_DATA1	UPPER_-THRESH-OLD_0_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_0_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_0_CNFG - Lower Threshold for Leaky Bucket Configuration 0

Address: 32H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_0_DATA7	LOWER_-THRESH-OLD_0_DATA6	LOWER_-THRESH-OLD_0_DATA5	LOWER_-THRESH-OLD_0_DATA4	LOWER_-THRESH-OLD_0_DATA3	LOWER_-THRESH-OLD_0_DATA2	LOWER_-THRESH-OLD_0_DATA1	LOWER_-THRESH-OLD_0_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_0_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_0_CNFG - Bucket Size for Leaky Bucket Configuration 0

Address: 33H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_0_DATA7	BUCKET_-SIZE_0_DATA6	BUCKET_-SIZE_0_DATA5	BUCKET_-SIZE_0_DATA4	BUCKET_-SIZE_0_DATA3	BUCKET_-SIZE_0_DATA2	BUCKET_-SIZE_0_DATA1	BUCKET_-SIZE_0_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_0_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_0_CNFG - Decay Rate for Leaky Bucket Configuration 0

Address: 34H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_0_DATA1	DECAY_RATE_0_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_0_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_1_CNFG - Upper Threshold for Leaky Bucket Configuration 1

Address: 35H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_THRESHOLD_1_DATA7	UPPER_THRESHOLD_1_DATA6	UPPER_THRESHOLD_1_DATA5	UPPER_THRESHOLD_1_DATA4	UPPER_THRESHOLD_1_DATA3	UPPER_THRESHOLD_1_DATA2	UPPER_THRESHOLD_1_DATA1	UPPER_THRESHOLD_1_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_1_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_1_CNFG - Lower Threshold for Leaky Bucket Configuration 1

Address: 36H
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_THRESHOLD_1_DATA7	LOWER_THRESHOLD_1_DATA6	LOWER_THRESHOLD_1_DATA5	LOWER_THRESHOLD_1_DATA4	LOWER_THRESHOLD_1_DATA3	LOWER_THRESHOLD_1_DATA2	LOWER_THRESHOLD_1_DATA1	LOWER_THRESHOLD_1_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_1_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_1_CNFG - Bucket Size for Leaky Bucket Configuration 1

Address: 37H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_1_DATA7	BUCKET_-SIZE_1_DATA6	BUCKET_-SIZE_1_DATA5	BUCKET_-SIZE_1_DATA4	BUCKET_-SIZE_1_DATA3	BUCKET_-SIZE_1_DATA2	BUCKET_-SIZE_1_DATA1	BUCKET_-SIZE_1_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_1_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_1_CNFG - Decay Rate for Leaky Bucket Configuration 1

Address: 38H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_1_DATA1	DECAY_RATE_1_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_1_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_2_CNFG - Upper Threshold for Leaky Bucket Configuration 2

Address: 39H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_2_DATA7	UPPER_-THRESH-OLD_2_DATA6	UPPER_-THRESH-OLD_2_DATA5	UPPER_-THRESH-OLD_2_DATA4	UPPER_-THRESH-OLD_2_DATA3	UPPER_-THRESH-OLD_2_DATA2	UPPER_-THRESH-OLD_2_DATA1	UPPER_-THRESH-OLD_2_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_2_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_2_CNFG - Lower Threshold for Leaky Bucket Configuration 2

Address: 3AH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_2_DATA7	LOWER_-THRESH-OLD_2_DATA6	LOWER_-THRESH-OLD_2_DATA5	LOWER_-THRESH-OLD_2_DATA4	LOWER_-THRESH-OLD_2_DATA3	LOWER_-THRESH-OLD_2_DATA2	LOWER_-THRESH-OLD_2_DATA1	LOWER_-THRESH-OLD_2_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_2_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_2_CNFG - Bucket Size for Leaky Bucket Configuration 2

Address: 3BH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_2_DATA7	BUCKET_-SIZE_2_DATA6	BUCKET_-SIZE_2_DATA5	BUCKET_-SIZE_2_DATA4	BUCKET_-SIZE_2_DATA3	BUCKET_-SIZE_2_DATA2	BUCKET_-SIZE_2_DATA1	BUCKET_-SIZE_2_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_2_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_2_CNFG - Decay Rate for Leaky Bucket Configuration 2

Address: 3CH
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_2_DATA1	DECAY_RATE_2_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_2_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator: 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

UPPER_THRESHOLD_3_CNFG - Upper Threshold for Leaky Bucket Configuration 3

Address: 3DH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
UPPER_-THRESH-OLD_3_DATA7	UPPER_-THRESH-OLD_3_DATA6	UPPER_-THRESH-OLD_3_DATA5	UPPER_-THRESH-OLD_3_DATA4	UPPER_-THRESH-OLD_3_DATA3	UPPER_-THRESH-OLD_3_DATA2	UPPER_-THRESH-OLD_3_DATA1	UPPER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	UPPER_THRESHOLD_3_DATA[7:0]	These bits set an upper threshold for the internal leaky bucket accumulator. When the number of the accumulated events is above this threshold, a no-activity alarm is raised.

LOWER_THRESHOLD_3_CNFG - Lower Threshold for Leaky Bucket Configuration 3

Address: 3EH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
LOWER_-THRESH-OLD_3_DATA7	LOWER_-THRESH-OLD_3_DATA6	LOWER_-THRESH-OLD_3_DATA5	LOWER_-THRESH-OLD_3_DATA4	LOWER_-THRESH-OLD_3_DATA3	LOWER_-THRESH-OLD_3_DATA2	LOWER_-THRESH-OLD_3_DATA1	LOWER_-THRESH-OLD_3_DATA0

Bit	Name	Description
7 - 0	LOWER_THRESHOLD_3_DATA[7:0]	These bits set a lower threshold for the internal leaky bucket accumulator. When the number of the accumulated events is below this threshold, the no-activity alarm is cleared.

BUCKET_SIZE_3_CNFG - Bucket Size for Leaky Bucket Configuration 3

Address: 3FH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
BUCKET_-SIZE_3_DATA7	BUCKET_-SIZE_3_DATA6	BUCKET_-SIZE_3_DATA5	BUCKET_-SIZE_3_DATA4	BUCKET_-SIZE_3_DATA3	BUCKET_-SIZE_3_DATA2	BUCKET_-SIZE_3_DATA1	BUCKET_-SIZE_3_DATA0

Bit	Name	Description
7 - 0	BUCKET_SIZE_3_DATA[7:0]	These bits set a bucket size for the internal leaky bucket accumulator. If the number of the accumulated events reach the bucket size, the accumulator will stop increasing even if further events are detected.

DECAY_RATE_3_CNFG - Decay Rate for Leaky Bucket Configuration 3

Address: 40H
Type: Read / Write
Default Value: XXXXXX01

7	6	5	4	3	2	1	0
-	-	-	-	-	-	DECAY_RATE_3_DATA1	DECAY_RATE_3_DATA0

Bit	Name	Description
7 - 2	-	Reserved.
1 - 0	DECAY_RATE_3_DATA[1:0]	These bits set a decay rate for the internal leaky bucket accumulator. 00: The accumulator decreases by 1 in every 128 ms with no event detected. 01: The accumulator decreases by 1 in every 256 ms with no event detected. (default) 10: The accumulator decreases by 1 in every 512 ms with no event detected. 11: The accumulator decreases by 1 in every 1024 ms with no event detected.

IN_FREQ_READ_CH_CNFG - Input Clock Frequency Read Channel Selection

Address: 41H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	IN_FREQ_READ_CH3	IN_FREQ_READ_CH2	IN_FREQ_READ_CH1	IN_FREQ_READ_CH0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	IN_FREQ_READ_CH[3:0]	These bits select an input clock, the frequency of which with respect to the reference clock can be read. 0000: Reserved. (default) 0001- 0010: reserved. 0011: IN3. 0100:Reserved. 0101: IN1. 0110: IN2. 0111 - 1111: reserved.

IN_FREQ_READ_STS - Input Clock Frequency Read Value

Address: 42H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
IN_FREQ_ VALUE7	IN_FREQ_ VALUE6	IN_FREQ_ VALUE5	IN_FREQ_ VALUE4	IN_FREQ_ VALUE3	IN_FREQ_ VALUE2	IN_FREQ_ VALUE1	IN_FREQ_ VALUE0

Bit	Name	Description
7 - 0	IN_FREQ_VALUE[7:0]	These bits represent a 2's complement signed integer. If the value is multiplied by the value in the FREQ_MON_FACTOR[3:0] bits (b3~0, 2EH), the frequency of an input clock with respect to the reference clock in ppm will be gotten. The input clock is selected by the IN_FREQ_READ_CH[3:0] bits (b3~0, 41H). The value in these bits is updated every 16 seconds, starting when an input clock is selected.

IN3_STS - Input Clock 3 Status

Address: 44H
Type: Read
Default Value: 01100110

7	6	5	4	3	2	1	0
-	-	-	-	IN3_FREQ_ SOFT_ALARM	IN3_FREQ_ HARD_ALARM	IN3_NO_ ACTIVITY_ALARM	IN3_PH_LOCK_ ALARM

Bit	Name	Description
7-4	-	Reserved
3	IN3_FREQ_SOFT_ALARM	This bit indicates whether IN3 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN3_FREQ_HARD_ALARM	This bit indicates whether IN3 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN3_NO_ACTIVITY_ALARM	This bit indicates whether IN3 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN3_PH_LOCK_ALARM	This bit indicates whether IN3 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MULTI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

IN1_IN2_STS - Input Clock 1 & 2 Status

Address: 45H
Type: Read
Default Value: 01100110

7	6	5	4	3	2	1	0
IN2_FREQ_-SOFT-_ALARM	IN2_FRE-Q_HARD_ALAR M	IN2_NO_ACTIV-ITY_ALARM	IN2_PH_LOCK_ ALARM	IN1_FREQ_-SOFT_ALARM	IN1_FRE-Q_HARD_ALAR M	IN1_NO_ACTIV-ITY_ALARM	IN1_PH_LOCK_ ALARM

Bit	Name	Description
7	IN2_FREQ_SOFT_ALARM	This bit indicates whether IN2 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
6	IN2_FREQ_HARD_ALARM	This bit indicates whether IN2 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
5	IN2_NO_ACTIVITY_ALARM	This bit indicates whether IN2 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
4	IN2_PH_LOCK_ALARM	This bit indicates whether IN2 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_-TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MUL-TI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.
3	IN1_FREQ_SOFT_ALARM	This bit indicates whether IN1 is in frequency soft alarm status. 0: Input frequency within soft accept region. 1: Input frequency over the soft reject region.
2	IN1_FREQ_HARD_ALARM	This bit indicates whether IN1 is in frequency hard alarm status. 0: Input frequency within hard accept region. 1: Input frequency over the hard reject region.
1	IN1_NO_ACTIVITY_ALARM	This bit indicates whether IN1 is in no-activity alarm status. 0: No no-activity alarm. 1: In no-activity alarm status. (default)
0	IN1_PH_LOCK_ALARM	This bit indicates whether IN1 is in phase lock alarm status. 0: No phase lock alarm. (default) 1: In phase lock alarm status. If the PH_ALARM_TIMEOUT bit (b5, 09H) is '0', this bit is cleared by writing '1' to this bit; if the PH_ALARM_-TIMEOUT bit (b5, 09H) is '1', this bit is cleared after a period (= *TIME_OUT_VALUE[5:0] (b5~0, 08H) X MUL-TI_FACTOR[1:0] (b7~6, 08H) in second*) which starts from when the alarm is raised.

6.2.5 IDPLL INPUT CLOCK SELECTION REGISTERS

INPUT_VALID1_STS - Input Clocks Validity 1

Address: 4AH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
-	-	IN2	IN1	-	IN3	-	-

Bit	Name	Description
7-6	-	Reserved
5-4	INn	This bit indicates the validity of the corresponding INn., 2≤n≤1. 0: Invalid. (default) 1: Valid.
3	-	Reserved
2	IN3	This bit indicates the validity of the corresponding IN3. 0: Invalid. (default) 1: Valid.
1-0	-	Reserved

REMOTE_INPUT_VALID1_CNFG - Input Clocks Validity Configuration 1

Address: 4CH
Type: Read / Write
Default Value: 11111111

7	6	5	4	3	2	1	0
-	-	IN2_VALID	IN1_VALID	-	IN3_VALID	-	-

Bit	Name	Description
7 - 6	-	Reserved.
5 - 4	INn_VALID	This bit controls whether the corresponding INn, 1≤n≤2, is allowed to be locked for automatic selection. 0: Enabled. 1: Disabled. (default)
3	-	Reserved.
2	IN3_VALID	This bit controls whether the corresponding IN3 is allowed to be locked for automatic selection. 0: Enabled. 1: Disabled. (default)
1 - 0	-	Reserved.

PRIORITY_TABLE1_STS - Priority Status 1 *

Address: 4EH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
HIGHEST_PRIORITY_VALIDATED3	HIGHEST_PRIORITY_VALIDATED2	HIGHEST_PRIORITY_VALIDATED1	HIGHEST_PRIORITY_VALIDATED0	CURRENTLY_SELECTED_INPUT3	CURRENTLY_SELECTED_INPUT2	CURRENTLY_SELECTED_INPUT1	CURRENTLY_SELECTED_INPUT0

Bit	Name	Description
7 - 4	HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the highest priority. 0000: No input clock is qualified. (default) 0001-0010: Reserved. 0011: IN3. 0100: Reserved. 0101: IN1. 0110: IN2. 0111- 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b5-2, 4CH) bit is '0'.
3 - 0	CURRENTLY_SELECTED_INPUT[3:0]	These bits indicate the selected input clock. 0000: No input clock is selected (default) 0001-0010: Reserved. 0011: IN3. 0100: Reserved. 0101: IN1. 0110: IN2. 0111-1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b5-2, 4CH) bit is '0'.

PRIORITY_TABLE2_STS - Priority Status 2 *

Address: 4FH
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
THIRD_HIGHEST_PRIORITY_VALIDATED3	THIRD_HIGHEST_PRIORITY_VALIDATED2	THIRD_HIGHEST_PRIORITY_VALIDATED1	THIRD_HIGHEST_PRIORITY_VALIDATED0	SECOND_HIGHEST_PRIORITY_VALIDATED3	SECOND_HIGHEST_PRIORITY_VALIDATED2	SECOND_HIGHEST_PRIORITY_VALIDATED1	SECOND_HIGHEST_PRIORITY_VALIDATED0

Bit	Name	Description
7 - 4	THIRD_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the third highest priority. 0000: No input clock is qualified. (default) 0001-0010: Reserved. 0011: IN3. 0100: Reserved. 0101: IN1. 0110: IN2. 0111- 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b5-2, 4CH) bit is '0'.
3 - 0	SECOND_HIGHEST_PRIORITY_VALIDATED[3:0]	These bits indicate a qualified input clock with the second highest priority. 0000: No input clock is qualified. (default) 0001-0010: Reserved. 0011: IN3. 0100: Reserved. 0101: IN1. 0110: IN2. 0111- 1111: Reserved. Note that the input clock is indicated by these bits only when the corresponding INn (b5-2, 4CH) bit is '0'.

INPUT_SEL_CNFG - Selected Input Clock Configuration

Address: 50H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	INPUT_SEL3	INPUT_SEL2	INPUT_SEL1	INPUT_SEL0

Bit	Name	Description
7 - 4	-	Reserved.
3 - 0	INPUT_SEL[3:0]	This bit determines DPLL input clock selection. 0000: Automatic selection. (default) 0001- 0010: Reserved. 0011: Forced selection - IN3 is selected. 0100: Reserved. 0101: Forced selection - IN1 is selected. 0110: Forced selection - IN2 is selected. 0111 - 1111: Reserved.

6.2.6 DPLL STATE MACHINE CONTROL REGISTERS

OPERATING_STS - DPLL Operating Status

Address: 52H
Type: Read
Default Value: 10000001

7	6	5	4	3	2	1	0
-	-	DPLL_SOFT_-FREQ_ALARM	-	DPLL_LOCK	DPLL_OPERAT-ING_MODE2	DPLL_OPERAT-ING_MODE1	DPLL_OPERAT-ING_MODE0

Bit	Name	Description
7-6	-	Reserved
5	DPLL_SOFT_FREQ_ALARM	This bit indicates whether the DPLL is in soft alarm status. 0: No DPLL soft alarm. (default) 1: In DPLL soft alarm status.
4	-	Reserved
3	DPLL_LOCK	This bit indicates the DPLL locking status. 0: Unlocked. (default) 1: Locked.
2 - 0	DPLL_OPERATING_MODE[2:0]	These bits indicate the current operating mode of DPLL. 000: Reserved. 001: Free-Run. (default) 010: Holdover. 011: Reserved. 100: Locked. 101: Pre-Locked2. 110: Pre-Locked. 111: Lost-Phase.

OPERATING_MODE_CNFG - DPLL Operating Mode Configuration

Address: 53H
Type: Read / Write
Default Value: XXXX0000

7	6	5	4	3	2	1	0
-	-	-	-	-	OPERATING_MODE2	OPERATING_MODE1	OPERATING_MODE0

Bit	Name	Description
7 - 3	-	Reserved.
2 - 0	OPERATING_MODE[2:0]	These bits control the DPLL operating mode. 000: Automatic. (default) 001: Forced - Free-Run. 010: Forced - Holdover. 011: Reserved. 100: Forced - Locked. 101: Forced - Pre-Locked2. 110: Forced - Pre-Locked. 111: Forced - Lost-Phase.

6.2.7 DPLL & APLL CONFIGURATION REGISTERS

DPLL_APLL_PATH_CNFG - DPLL & APLL Path Configuration

Address: 55H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
APLL_PATH3	APLL_PATH2	APLL_PATH1	APLL_PATH0	GSM_OBSAI_ 16E1_16T1_SEL1	GSM_OBSAI_ 16E1_16T1_SEL0	12E1_G-PS_E3_T3_-SEL1	12E1_G-PS_E3_T3_-SEL0

Bit	Name	Description
7 - 4	APLL_PATH[3:0]	These bits select reference clock path and output clock rate of the APLL. 0000: Lock to DPLL, output 622.08 MHz (default) 0001- 0111: Reserved 1000: Lock to DPLL, output 625 MHz 1001: Lock to DPLL, output 625 MHz*66/64 1010-1111: Reserved.
3 - 2	GSM_OBSAI_16E1_16T1_SEL[1:0]	These bits select an output clock from the DPLL GSM/OBSAI/16E1/16T1 path. 00: 16E1. 01: 16T1. 10: GSM. 11: OBSAI.
1 - 0	12E1_GPS_E3_T3_SEL[1:0]	These bits select an output clock from the DPLL 12E1/GPS/E3/T3 path. 00: 12E1. 01: GPS 10: E3. 11: T3.

DPLL_START_BW_DAMPING_CNFG - DPLL Start Bandwidth & Damping Factor Configuration

Address: 56H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
DPLL_START_DAMPING2	DPLL_START_DAMPING1	DPLL_START_DAMPING0	DPLL_START_BW4	DPLL_START_BW3	DPLL_START_BW2	DPLL_START_BW1	DPLL_START_BW0

Bit	Name	Description
7 - 5	DPLL_START_DAMPING[2:0]	These bits set the starting damping factor for DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	DPLL_START_BW[4:0]	These bits set the starting bandwidth for DPLL. 00000- 00100: Reserved 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

DPLL_ACQ_BW_DAMPING_CNFG - DPLL Acquisition Bandwidth & Damping Factor Configuration

Address: 57H
Type: Read / Write
Default Value: 01101111

7	6	5	4	3	2	1	0
DPLL_ACQ_ DAMPING2	DPLL_ACQ_ DAMPING1	DPLL_ACQ_ DAMPING0	DPLL_ACQ_ BW4	DPLL_ACQ_ BW3	DPLL_ACQ_ BW2	DPLL_ACQ_ BW1	DPLL_ACQ_ BW0

Bit	Name	Description
7 - 5	DPLL_ACQ_DAMPING[2:0]	These bits set the acquisition damping factor for DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	DPLL_ACQ_BW[4:0]	These bits set the acquisition bandwidth for DPLL. 00000 - 00100: Reserved 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. (default) 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

DPLL_LOCKED_BW_DAMPING_CNFG - DPLL Locked Bandwidth & Damping Factor Configuration

Address: 58H
Type: Read / Write
Default Value: 01101011

7	6	5	4	3	2	1	0
DPLL_LOCKED_DAMPING2	DPLL_LOCKED_DAMPING1	DPLL_LOCKED_DAMPING0	DPLL_LOCKED_BW4	DPLL_LOCKED_BW3	DPLL_LOCKED_BW2	DPLL_LOCKED_BW1	DPLL_LOCKED_BW0

Bit	Name	Description
7 - 5	DPLL_LOCKED_DAMPING[2:0]	These bits set the locked damping factor for DPLL. 000: Reserved. 001: 1.2. 010: 2.5. 011: 5. (default) 100: 10. 101: 20. 110, 111: Reserved.
4 - 0	DPLL_LOCKED_BW[4:0]	These bits set the locked bandwidth for DPLL. 00000 - 00100: Reserved 00101: 15 mHz. 00110: 30 mHz. 00111: 60 mHz. 01000: 0.1 Hz. 01001: 0.3 Hz. 01010: 0.6 Hz. 01011: 1.2 Hz. (default) 01100: 2.5 Hz. 01101: 4 Hz. 01110: 8 Hz. 01111: 18 Hz. 10000: 35 Hz. 10001: 70 Hz. 10010: 560 Hz. 10011 ~ 11111: Reserved.

BW_OVERSHOOT_CNFG - DPLL Bandwidth Overshoot Configuration

Address: 59H
Type: Read / Write
Default Value: 1XXX1XXX

7	6	5	4	3	2	1	0
AUTO_BW_SEL	-	-	-	DPLL_LIMT	-	-	-

Bit	Name	Description
7	AUTO_BW_SEL	This bit determines whether starting or acquisition bandwidth / damping factor is used for the DPLL. 0: The starting and acquisition bandwidths / damping factors are not used. Only the locked bandwidth / damping factor is used regardless of the DPLL locking stage. 1: The starting, acquisition or locked bandwidth / damping factor is used automatically depending on different DPLL locking stages. (default)
6 - 4	-	Reserved.
3	DPLL_LIMT	This bit determines whether the integral path value is frozen when the DPLL hard limit is reached. 0: Not frozen. 1: Frozen. It will minimize the subsequent overshoot when DPLL is pulling in. (default)
2 - 0	-	Reserved.

PHASE_LOSS_COARSE_LIMIT_CNFG - Phase Loss Coarse Detector Limit Configuration *

Address: 5AH
Type: Read / Write
Default Value: 10000101

7	6	5	4	3	2	1	0
COARSE_PH_LOS_LIMT_EN	WIDE_EN	MULTI_PH_APP	MULTI_PH_8K_4K_2K_EN	PH_LOS_COARSE_LIMT3	PH_LOS_COARSE_LIMT2	PH_LOS_COARSE_LIMT1	PH_LOS_COARSE_LIMT0

Bit	Name	Description
7	COARSE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the coarse phase loss will result in the DPLL unlocked. 0: Disabled. 1: Enabled. (default)
6	WIDE_EN	Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH).
5	MULTI_PH_APP	This bit determines whether the PFD output of the DPLL is limited to ±1 UI or is limited to the coarse phase limit. 0: Limited to ±1 UI. (default) 1: Limited to the coarse phase limit. When the selected input clock is of 2 kHz, 4 kHz or 8 kHz, the coarse phase limit depends on the MULTI_PH_8K_4K_2K_EN bit, the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits; when the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH) for details.
4	MULTI_PH_8K_4K_2K_EN	This bit, together with the WIDE_EN bit (b6, 5AH) and the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH), determines the coarse phase limit when the selected input clock is of 2 kHz, 4 kHz or 8 kHz. When the selected input clock is of other frequencies but 2 kHz, 4 kHz and 8 kHz, the coarse phase limit depends on the WIDE_EN bit and the PH_LOS_COARSE_LIMT[3:0] bits.
3 - 0	PH_LOS_COARSE_LIMT[3:0]	These bit set the coarse phase limit. The limit is used only in some cases. Refer to the description of the MULTI_PH_8K_4K_2K_EN bit (b4, 5AH). 0000: ±1 UI. 0001: ±3 UI. 0010: ±7 UI. 0011: ±15 UI. 0100: ±31 UI. 0101: ±63 UI. (default) 0110: ±127 UI. 0111: ±255 UI. 1000: ±511 UI. 1001: ±1023 UI. 1010-1111: Reserved.

Selected Input Clock	MULTI_PH_8K_4K_2K_EN	WIDE_EN	Coarse Phase Limit
2 kHz, 4 kHz or 8 kHz	0	don't-care	±1 UI
	1	0	±1 UI
		1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).
other than 2 kHz, 4 kHz and 8 kHz	don't-care	0	±1 UI
		1	set by the PH_LOS_COARSE_LIMT[3:0] bits (b3~0, 5AH).

PHASE_LOSS_FINE_LIMIT_CNFG - Phase Loss Fine Detector Limit Configuration *

Address: 5BH
Type: Read / Write
Default Value: 10XXX010

7	6	5	4	3	2	1	0
FINE_PH_LOS_LIMT_EN	FAST_LOS_SW	-	-	-	PH_LOS_FINE_LIMT2	PH_LOS_FINE_LIMT1	PH_LOS_FINE_LIMT0

Bit	Name	Description
7	FINE_PH_LOS_LIMT_EN	This bit controls whether the occurrence of the fine phase loss will result in the DPLL unlocked. 0: Disabled. 1: Enabled. (default)
6	FAST_LOS_SW	This bit controls whether the occurrence of the fast loss will result in the DPLL unlocked. 0: Does not result in the DPLL unlocked. The DPLL will enter Temp-Holdover mode automatically. (default) 1: Results in the DPLL unlocked. The DPLL will enter Lost-Phase mode if the DPLL operating mode is switched automatically.
5 - 3	-	Reserved.
2 - 0	PH_LOS_FINE_LIMT[2:0]	These bits set a fine phase limit. 000: 0. 001: ± (45 ° ~ 90 °). 010: ± (90 ° ~ 180 °). (default) 011: ± (180 ° ~ 360 °). 100: ± (20 ns ~ 25 ns). 101: ± (60 ns ~ 65 ns). 110: ± (120 ns ~ 125 ns). 111: ± (950 ns ~ 955 ns).

HOLDOVER_MODE_CNFG - DPLL Holdover Mode Configuration

Address: 5CH
Type: Read / Write
Default Value: 010001XX

7	6	5	4	3	2	1	0
MAN_HOLDOVER	AUTO_AVG	FAST_AVG	READ_AVG	TEMP_HOLD-OVER_MODE1	TEMP_HOLD-OVER_MODE0	-	-

Bit	Name	Description
7	MAN_HOLDOVER	Refer to the description of the FAST_AVG bit (b5, 5CH).
6	AUTO_AVG	Refer to the description of the FAST_AVG bit (b5, 5CH).
5	FAST_AVG	This bit, together with the AUTO_AVG bit (b6, 5CH) and the MAN_HOLDOVER bit (b7, 5CH), determines a frequency offset acquiring method in DPLL Holdover Mode.
4	READ_AVG	This bit controls the holdover frequency offset reading, which is read from the HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH). 0: The value read from the HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is equal to the one written to them. (default) 1: The value read from the HOLDOVER_FREQ[23:0] bits (5FH ~ 5DH) is not equal to the one written to them. The value is acquired by Automatic Slow Averaged method if the FAST_AVG bit (b5, 5CH) is '0'; or is acquired by Automatic Fast Averaged method if the FAST_AVG bit (b5, 5CH) is '1'.
3 - 2	TEMP_HOLDOVER_MODE[1:0]	These bits determine the frequency offset acquiring method in DPLL Temp-Holdover Mode. 00: The method is the same as that used in DPLL Holdover mode. 01: Automatic Instantaneous. (default) 10: Automatic Fast Averaged. 11: Automatic Slow Averaged.
1 - 0	-	Reserved.

MAN_HOLDOVER	AUTO_AVG	FAST_AVG	Frequency Offset Acquiring Method
0	0	don't-care	Automatic Instantaneous
	1	0	Automatic Slow Averaged (default)
		1	Automatic Fast Averaged
1	don't-care		Manual

HOLDOVER_FREQ[7:0]_CNFG - DPLL Holdover Frequency Configuration 1

Address: 5DH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
HOLDOVER_FREQ7	HOLDOVER_FREQ6	HOLDOVER_FREQ5	HOLDOVER_FREQ4	HOLDOVER_FREQ3	HOLDOVER_FREQ2	HOLDOVER_FREQ1	HOLDOVER_FREQ0

Bit	Name	Description
7 - 0	HOLDOVER_FREQ[7:0]	Refer to the description of the HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

HOLDOVER_FREQ[15:8]_CNFG - DPLL Holdover Frequency Configuration 2

Address: 5EH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
HOLDOVER_FREQ15	HOLDOVER_FREQ14	HOLDOVER_FREQ13	HOLDOVER_FREQ12	HOLDOVER_FREQ11	HOLDOVER_FREQ10	HOLDOVER_FREQ9	HOLDOVER_FREQ8

Bit	Name	Description
7 - 0	HOLDOVER_FREQ[15:8]	Refer to the description of the HOLDOVER_FREQ[23:16] bits (b7~0, 5FH).

HOLDOVER_FREQ[23:16]_CNFG - DPLL Holdover Frequency Configuration 3

Address: 5FH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
HOLDOVER_FREQ23	HOLDOVER_FREQ22	HOLDOVER_FREQ21	HOLDOVER_FREQ20	HOLDOVER_FREQ19	HOLDOVER_FREQ18	HOLDOVER_FREQ17	HOLDOVER_FREQ16

Bit	Name	Description
7 - 0	HOLDOVER_FREQ[23:16]	The HOLDOVER_FREQ[23:0] bits represent a 2's complement signed integer. The value read from these bits multiplied by 0.000011 is the frequency offset automatically slow or fast averaged or manually set, as determined by the READ_AVG bit (b4, 5CH) and the FAST_AVG bit (b5, 5CH).

CURRENT_DPLL_FREQ[7:0]_STS - DPLL Current Frequency Status 1 *

Address: 62H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_DPLL_FREQ7	CURRENT_DPLL_FREQ6	CURRENT_DPLL_FREQ5	CURRENT_DPLL_FREQ4	CURRENT_DPLL_FREQ3	CURRENT_DPLL_FREQ2	CURRENT_DPLL_FREQ1	CURRENT_DPLL_FREQ0

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[7:0]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[15:8]_STS - DPLL Current Frequency Status 2 *

Address: 63H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_ DPLL_FREQ15	CURRENT_ DPLL_FREQ14	CURRENT_ DPLL_FREQ13	CURRENT_ DPLL_FREQ12	CURRENT_ DPLL_FREQ11	CURRENT_ DPLL_FREQ10	CURRENT_ DPLL_FREQ9	CURRENT_ DPLL_FREQ8

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[15:8]	Refer to the description of the CURRENT_DPLL_FREQ[23:16] bits (b7~0, 64H).

CURRENT_DPLL_FREQ[23:16]_STS - DPLL Current Frequency Status 3 *

Address: 64H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_ DPLL_FREQ23	CURRENT_ DPLL_FREQ22	CURRENT_ DPLL_FREQ21	CURRENT_ DPLL_FREQ20	CURRENT_ DPLL_FREQ19	CURRENT_ DPLL_FREQ18	CURRENT_ DPLL_FREQ17	CURRENT_ DPLL_FREQ16

Bit	Name	Description
7 - 0	CURRENT_DPLL_FREQ[23:16]	The CURRENT_DPLL_FREQ[23:0] bits represent a 2's complement signed integer. If the value in these bits is multiplied by 0.000011, the current frequency offset of the DPLL output in ppm with respect to the master clock will be gotten.

DPLL_FREQ_SOFT_LIMIT_CNFG - DPLL Soft Limit Configuration

Address: 65H
Type: Read / Write
Default Value: 10001100

7	6	5	4	3	2	1	0
FREQ_LIMT_ PH_LOS	DPLL_FREQ_ SOFT_LIMT6	DPLL_FREQ_ SOFT_LIMT5	DPLL_FREQ_ SOFT_LIMT4	DPLL_FREQ_ SOFT_LIMT3	DPLL_FREQ_ SOFT_LIMT2	DPLL_FREQ_ SOFT_LIMT1	DPLL_FREQ_ SOFT_LIMT0

Bit	Name	Description
7	FREQ_LIMT_PH_LOS	This bit determines whether the DPLL in hard alarm status will result in it unlocked. 0: Disabled. 1: Enabled. (default)
6 - 0	DPLL_FREQ_SOFT_LIMT[6:0]	These bits represent an unsigned integer. If the value is multiplied by 0.724, the DPLL soft limit for the DPLL in ppm will be gotten. The DPLL soft limit is symmetrical about zero.

DPLL_FREQ_HARD_LIMIT[7:0]_CNFG - DPLL Hard Limit Configuration 1

Address: 66H
Type: Read / Write
Default Value: 10101011

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT7	DPLL_FREQ_HARD_LIMT6	DPLL_FREQ_HARD_LIMT5	DPLL_FREQ_HARD_LIMT4	DPLL_FREQ_HARD_LIMT3	DPLL_FREQ_HARD_LIMT2	DPLL_FREQ_HARD_LIMT1	DPLL_FREQ_HARD_LIMT0

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[7:0]	Refer to the description of the DPLL_FREQ_HARD_LIMT[15:8] bits (b7~0, 67H).

DPLL_FREQ_HARD_LIMIT[15:8]_CNFG - DPLL Hard Limit Configuration 2

Address: 67H
Type: Read / Write
Default Value: 00011001

7	6	5	4	3	2	1	0
DPLL_FREQ_HARD_LIMT15	DPLL_FREQ_HARD_LIMT14	DPLL_FREQ_HARD_LIMT13	DPLL_FREQ_HARD_LIMT12	DPLL_FREQ_HARD_LIMT11	DPLL_FREQ_HARD_LIMT10	DPLL_FREQ_HARD_LIMT9	DPLL_FREQ_HARD_LIMT8

Bit	Name	Description
7 - 0	DPLL_FREQ_HARD_LIMT[15:8]	The DPLL_FREQ_HARD_LIMT[15:0] bits represent an unsigned integer. If the value is multiplied by 0.0014, the DPLL hard limit for the DPLL in ppm will be gotten. The DPLL hard limit is symmetrical about zero.

CURRENT_DPLL_PHASE[7:0]_STS - DPLL Current Phase Status 1 *

Address: 68H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA7	CURRENT_PH_DATA6	CURRENT_PH_DATA5	CURRENT_PH_DATA4	CURRENT_PH_DATA3	CURRENT_PH_DATA2	CURRENT_PH_DATA1	CURRENT_PH_DATA0

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[7:0]	Refer to the description of the CURRENT_PH_DATA[15:8] bits (b7~0, 69H).

CURRENT_DPLL_PHASE[15:8]_STS - DPLL Current Phase Status 2 *

Address: 69H
Type: Read
Default Value: 00000000

7	6	5	4	3	2	1	0
CURRENT_PH_DATA15	CURRENT_PH_DATA14	CURRENT_PH_DATA13	CURRENT_PH_DATA12	CURRENT_PH_DATA11	CURRENT_PH_DATA10	CURRENT_PH_DATA9	CURRENT_PH_DATA8

Bit	Name	Description
7 - 0	CURRENT_PH_DATA[15:8]	The CURRENT_PH_DATA[15:0] bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the averaged phase error of the DPLL feedback with respect to the selected input clock in ns will be gotten.

6.2.8 OUTPUT CONFIGURATION REGISTERS

OUT1_FREQ_CNFG - Output Clock 1 Frequency Configuration

Address: 6BH
Type: Read / Write
Default Value: 00001011

7	6	5	4	3	2	1	0
OUT1_PATH_SEL3	OUT1_PATH_SEL2	OUT1_PATH_SEL1	OUT1_PATH_SEL0	OUT1_DIVID-ER3	OUT1_DIVID-ER2	OUT1_DIVID-ER1	OUT1_DIVID-ER0

Bit	Name	Description
7 - 4	OUT1_PATH_SEL[3:0]	These bits select an input to OUT1. 0000 ~ 0010: The output of APLL. (default: 0000) 0011: DPLL ETH path 0100: The output of DPLL 77.76 MHz path. 0101: The output of DPLL 12E1/GPS/E3/T3 path. 0110: The output of DPLL 16E1/16T1 path. 0111: The output of DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1111: Reserved
3 - 0	OUT1_DIVIDER[3:0]	These bits select a division factor of the divider for OUT1. The output frequency is determined by the division factor and the signal derived from the DPLL or from the APLL output (selected by the OUT1_PATH_SEL[3:0] bits (b7~4, 6BH)). If the signal is derived from one of the DPLL outputs, please refer to Table 20 for the division factor selection. If the signal is derived from the APLL output, please refer to Table 21 for the division factor selection. OUT1 default frequency is 12.96MHz.

Reserved

Address: 6CH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 00000000 for normal operation.

Reserved

Address: 6DH
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 00000000 for normal operation.

Reserved

Address: 6EH
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 00000000 for normal operation.

Reserved

Address: 6FH
Type: Read / Write
Default Value: 00000100

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 00000000 for normal operation.

OUT2_FREQ_CNFG - Output Clock 2 Frequency Configuration

Address:70H
Type: Read / Write
Default Value: 00000110

7	6	5	4	3	2	1	0
OUT2_PATH_-SEL3	OUT2_PATH_-SEL2	OUT2_PATH_-SEL1	OUT2_PATH_-SEL0	OUT2_DIVID-ER3	OUT2_DIVID-ER2	OUT2_DIVID-ER1	OU26_DIVID-ER0

Bit	Name	Description
7 - 4	OUT2_PATH_SEL[3:0]	These bits select an input to OUT2. 0000 ~ 0010: The output of APLL. (default: 0000) 0011: DPLL ETH path 0100: The output of DPLL 77.76 MHz path. 0101: The output of DPLL 12E1/GPS/E3/T3 path. 0110: The output of DPLL 16E1/16T1 path. 0111: The output of DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1111: Reserved.
3 - 0	OUT2_DIVIDER[3:0]	These bits select a division factor of the divider for OUT2. The output frequency is determined by the division factor and the signal derived from DPLL or from the APLL output (selected by the OUT2_PATH_SEL[3:0] bits (b7~4, 70H)). If the signal is derived from one of the DPLL outputs, please refer to Table 20 for the division factor selection. If the signal is derived from the APLL output, please refer to Table 21 for the division factor selection.

OUT3_FREQ_CNFG - Output Clock 3 Frequency Configuration

Address:71H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
OUT3_PATH_SEL3	OUT3_PATH_SEL2	OUT3_PATH_SEL1	OUT3_PATH_SEL0	OUT3_DIVID-ER3	OUT3_DIVID-ER2	OUT3_DIVID-ER1	OUT3_DIVID-ER0

Bit	Name	Description
7 - 4	OUT3_PATH_SEL[3:0]	These bits select an input to OUT3. 0000 ~ 0010: The output of APLL. (default: 0000) 0011: DPLL ETH path 0100: The output of DPLL 77.76 MHz path. 0101: The output of DPLL 12E1/GPS/E3/T3 path. 0110: The output of DPLL 16E1/16T1 path. 0111: The output of DPLL GSM/OBSAI/16E1/16T1 path. 1000 ~ 1111: Reserved
3 - 0	OUT3_DIVIDER[3:0]	These bits select a division factor of the divider for OUT3. The output frequency is determined by the division factor and the signal derived from DPLL or from the APLL output (selected by the OUT3_PATH_SEL[3:0] bits (b7~4, 71H)). If the signal is derived from one of the DPLL outputs, please refer to Table 20 for the division factor selection. If the signal is derived from the APLL output, please refer to Table 21 for the division factor selection.

OUT2-3_INV_CNFG - Output Clock2 and 3 Invert Configuration

Address:72H
Type: Read / Write
Default Value: 01000000

7	6	5	4	3	2	1	0
-	-	-	-	-	-	OUT3_INV	OUT2_INV

Bit	Name	Description
7-2	-	Reserved
1	OUT3_INV	This bit determines whether the output on OUT3 is inverted. 0: Not inverted. (default) 1: Inverted.
0	OUT2_INV	This bit determines whether the output on OUT2 is inverted. 0: Not inverted. (default) 1: Inverted.

OUT1_INV_CNFG - Output Clock 1 Invert Configuration

Address:73H
Type: Read / Write
Default Value: 01000000

7	6	5	4	3	2	1	0
Reserved[7:1]							OUT1_INV

Bit	Name	Description
7 - 1	Reserved[7:1]	Reserved. These bits must be set to 0000000 for normal operation.
0	OUT1_INV	This bit determines whether the output on OUT1 is inverted. 0: Not inverted. (default) 1: Inverted.

6.2.9 PHASE OFFSET CONTROL REGISTERS

PHASE_MON_CNFG - Phase Transient Monitor Configuration

Address:78H
Type: Read / Write
Default Value: 0X000110

7	6	5	4	3	2	1	0
IN_NOISE_WINDOW	-	-	-	-	-	-	

Bit	Name	Description
7	IN_NOISE_WINDOW	This bit determines whether the input clock whose edge respect to the reference clock is outside ±5% is enabled to be selected for DPLL. 0: Disabled. (default) 1: Enabled.
6-0	-	Reserved.

Reserved

Address: 79H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
Reserved[7:0]							

Bit	Name	Description
7 - 0	Reserved[7:0]	Reserved. These bits must be set to 01001000 for normal operation.

PHASE_OFFSET[7:0]_CNFG - Phase Offset Configuration 1

Address:7AH
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
PH_OFFSET7	PH_OFFSET6	PH_OFFSET5	PH_OFFSET4	PH_OFFSET3	PH_OFFSET2	PH_OFFSET1	PH_OFFSET0

Bit	Name	Description
7 - 0	PH_OFFSET[7:0]	Refer to the description of the PH_OFFSET[9:8] bits (b1~0, 7BH).

PHASE_OFFSET[9:8]_CNFG - Phase Offset Configuration 2

Address:7BH
Type: Read / Write
Default Value: 0XXXXX00

7	6	5	4	3	2	1	0
PH_OFF-SET_EN	-	-	-	-	-	PH_OFFSET9	PH_OFFSET8

Bit	Name	Description
7	PH_OFFSET_EN	This bit determines whether the input-to-output phase offset is enabled. If the device is configured as the Master, the input-to-output phase offset: 0: Disabled. (default) 1: Enabled. If the device is configured as the Slave, the input-to-output phase offset is always enabled.
6 - 2	-	Reserved.
1 - 0	PH_OFFSET[9:8]	These bits represent a 2's complement signed integer. If the value is multiplied by 0.61, the input-to-output phase offset in ns to adjust will be gotten.

6.3 PAGE 1 REGISTERS DESCRIPTION

DFS_OFF_CNFG - Digital Frequency Synthesizer Configuration

Address:30H
Type: Read / Write
Default Value: 00000000

7	6	5	4	3	2	1	0
DFS_OFF[3]	DFS_OFF[2]	DFS_OFF[1]	DFS_OFF[0]	Reserved[3:0]			

Bit	Name	Description
7	DFS_OFF[3]	ETH (default 0) 0: enable 1: disable
6	DFS_OFF[2]	12E1/GPS/E3/T3 (default 0) 0: enable 1: disable
5	DFS_OFF[1]	16E1/16T1 (default 0) 0: enable 1: disable
4	DFS_OFF[0]	GSM/OBSA1/16E1/16T1 (default 0) 0: enable 1: disable
3-0	Reserved[3:0]	Reserved. These bits must be set to 1111 for normal operation.

PPS_CNFG - 1 Pulse Per Second Configuration

Address:31H
Type: Read / Write
Default Value: 00001000

7	6	5	4	3	2	1	0
-	-	PPS_PHASE[1:0]		PPS_PULSE[3:0]			

Bit	Name	Description
7 - 6	-	Reserved
5 - 4	PPS_PHASE[1:0]	Phase position: 00: 0 degree (on target, sync to input (default) 01: 50ns delayed (half period of 10 MHz) 10: 100ns delayed (one period of 10 MHz) 11: reserved
3 - 0	PPS_PULSE[3:0]	For FRSYNC_8K_1PPS and for MFRSYNC_2K_1PPS Pulse width, the following settings apply: 0000: 0.5s (50% duty cycle) 0001: 100ns 0010: 200ns 0011: 400ns 0100: 800ns 0101: 1µs 0110: 20µs 0111: 50µs 1000: 100µs (default) 1001: 200µs 1010: 400µs 1011: 600µs 1100: 800µs 1101: 1ms 1110: 10ms 1111: 100ms For OUTn ($1 \leq n \leq 3$) 1PPS output Pulse width, the following settings apply: 0000: 0.5s (50% duty cycle) 0001: 100ns 0010: 200ns 0011: 400ns 0100: 800ns 0101: 1µs 0110: 20µs 0111: 50µs 1000: 100µs (default) 1001: 200µs 1010: 400µs 1011: 1.2ms 1100: 800µs 1101: 0.5s 1110: 0.5s 1111: 0.5s

PH_SLOPE_CNFG - Phase Slope Limiting

Address:32H
Type: Read / Write
Default Value: 00001111

7	6	5	4	3	2	1	0
-	-	-	-	PH_SLOPE[1]	PH_SLOPE[0]	-	-

Bit	Name	Description
7-4	-	Reserved (default 0000)
3-2	PH_SLOPE[1:0]	DPLL Phase slope selection (default 11): 00: GR-1244 ST3: 61µs/s 01: GR-1244 ST2, 3E, ST3 (objective): 885ns/s (loop bandwidth must be set to less than 8Hz in address register 58H) 10: G.813 opt1, G.8262: 7.5µs/s (loop bandwidth must be set to less than 35Hz in address register 58H) 11: no limitation
1-0	-	Reserved (default 11)

ICP_CTRL_CNFG_REG - APLL Charge Pump Current Configuration

Address:33H
Type: Read / Write
Default Value: 00001010

7	6	5	4	3	2	1	0
-	-	-	ICP_CTRL_CODE[4]	ICP_CTRL_CODE[3]	ICP_CTRL_CODE[2]	ICP_CTRL_CODE[1]	ICP_CTRL_CODE[0]

Bit	Name	Description
7-5	-	Reserved (default 000)
4-0	ICP_CTRL_CODE[4:0]	APLL charge pump current selection 01010: 40 uA (default)

7 ELECTRICAL SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATING

Table 33: Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage VDD	-0.5	5.5	V
V_{IN}	Input Voltage (non-supply pins)		5.5	V
V_{OUT}	Output Voltage (non-supply pins)		5.5	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STOR}	Storage Temperature	-50	150	°C
CDM Classification – Class III (JESD22 - C101) HBM Classification – Class 2 (JESD22-A114)				

7.2 RECOMMENDED OPERATION CONDITIONS

Table 34: Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power Supply (DC voltage) VDD	3.135	3.3	3.465	V	
T_A	Ambient Temperature Range	-40	25	85	°C	
I_{DD}	Supply Current		270		mA	Exclude the loading current and power
P_{TOT}	Total Power Dissipation		0.9	1.35	W	

7.3 I/O SPECIFICATIONS

7.3.1 CMOS INPUT / OUTPUT PORT

Table 35: CMOS Input Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
I_{IN}	Input Current			±10	µA	

Table 36: CMOS Input Port with Internal Pull-Up Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_U	Pull-Up Resistor		50		KΩ	
I_{IN}	Input Current			±150	µA	

Table 37: CMOS Input Port with Internal Pull-Down Resistor Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input Voltage High	2			V	
V_{IL}	Input Voltage Low			0.8	V	
P_D	Pull-Down Resistor		50		KΩ	
I_{IN}	Input Current			±15	µA	

Table 38: CMOS Output Port Electrical Characteristics

Application Pin	Parameter	Description	Min	Typ	Max	Unit	Test Condition
Output Clock	V_{OH}	Output Voltage High	2.4			V	I_{OH} = -4 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL} = 4 mA
	t_R	Rise time		2.2		ns	15 pF
	t_F	Fall time		2.2		ns	15 pF
Other Output	V_{OH}	Output Voltage High	2.4			V	I_{OH} = -2 mA
	V_{OL}	Output Voltage Low			0.4	V	I_{OL}= 2 mA
	t_R	Rise Time			20	ns	50 pF
	t_F	Fall Time			20	ns	50 pF

7.3.2 PECL / LVDS INPUT / OUTPUT PORT

7.3.2.1 PECL Input / Output Port

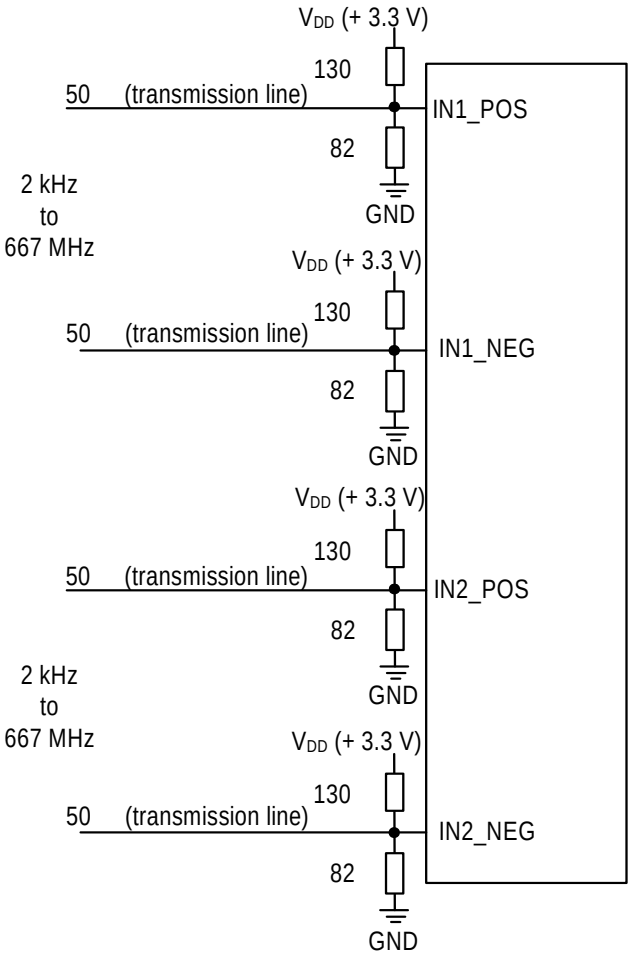

Figure 15. Recommended PECL Input Port Line Termination

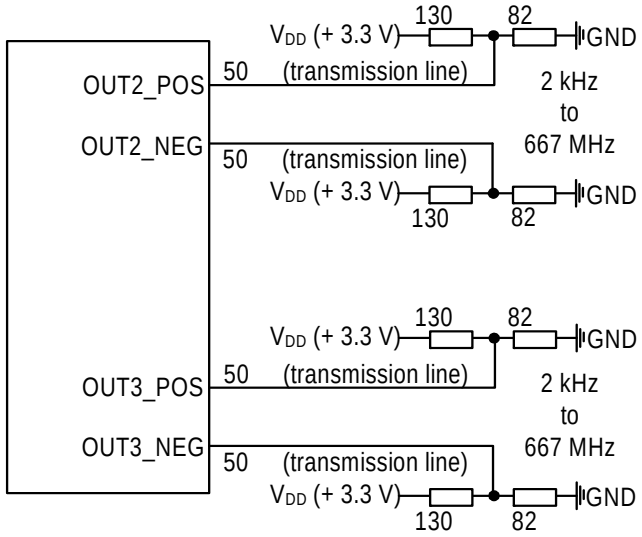

Figure 16. Recommended PECL Output Port Line Termination

Table 39: PECL Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage, Differential Inputs	V_{DD} - 2.5		V_{DD} - 0.5	V	
V_{IH}	Input High Voltage, Differential Inputs	V_{DD} - 2.4		V_{DD} - 0.4	V	
V_{ID}	Input Differential Voltage	0.1		1.4	V	
V_{IL_S}	Input Low Voltage, Single-ended Input	V_{SS}		V_{DD} - 1.5	V	
V_{IH_S}	Input High Voltage, Single-ended Input	V_{DD} - 1.3		V_{DD}	V	
I_{IH}	Input High Current, Input Differential Voltage			10	µA	
I_{IL}	Input Low Current, Input Differential Voltage	-10			µA	
V_{OL}	Output Voltage Low	1.15		1.75	V	
V_{OH}	Output Voltage High	1.95		2.55	V	
V_{OD}	Output Differential Voltage	650		850	mV	
t_{RISE}	Output Rise time (20% to 80%)		178	300	pS	
t_{FALL}	Output Fall time (20% to 80%)		176	300	pS	
t_{SKEW}	Output Differential Skew		80	150	pS	

NOTE:
1. Assuming a differential input voltage of at least 100 mV.
2. Unused differential input terminated to V_{DD} - 1.4 V.
3. with 50Ω load on each pin to V_{DD} - 2 V, i.e. 82 to GND and 103 to V_{DD}.

7.3.2.2 LVDS Input / Output Port

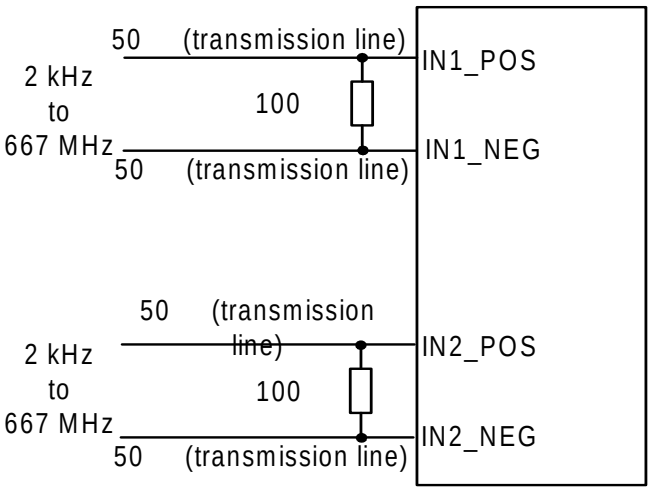

Figure 17. Recommended LVDS Input Port Line Termination

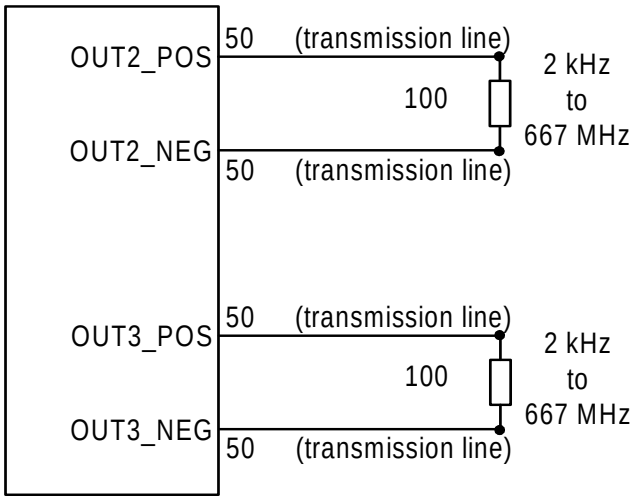

Figure 18. Recommended LVDS Output Port Line Termination

Table 40: LVDS Input / Output Port Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit	Test Condition
V_{CM}	Input Common-mode Voltage Range	200	1200	2200	mV	
V_{DIFF}	Input Peak Differential Voltage	100	350	900	mV	
V_{IDTH}	Input Differential Threshold	-100		100	mV	
R_{TERM}	External Differential Termination Impedance		100		Ω	
V_{OH}	Output Voltage High	1250		1650	mV	R_{LOAD} = 100 Ω ± 1%
V_{OL}	Output Voltage Low	850		1250	mV	R_{LOAD} = 100 Ω ± 1%
V_{OD}	Differential Output Voltage	247	400	454	mV	R_{LOAD} = 100 Ω ± 1%
V_{OS}	Output Offset Voltage	1095		1405	V	R_{LOAD} = 100 Ω ± 1%
R_O	Differential Output Impedance	80		120	Ω	V_{CM} = 1.0 V or 1.4 V
ΔR_O	R_O Mismatch between A and B			20	%	V_{CM} = 1.0 V or 1.4 V
ΔV_{OD}	Change in V_{OD} between Logic 0 and Logic 1			50	mV	R_{LOAD} = 100 Ω ± 1%
ΔV_{OS}	Change in V_{OS} between Logic 0 and Logic 1			50	mV	R_{LOAD} = 100 Ω ± 1%
I_{SA}, I_{SB}	Output Current			24	mA	Driver shorted to GND
I_{SAB}	Output Current			12	mA	Driver shorted together
t_{RISE}	Output Rise time (20% to 80%)		130	300	pS	R_{LOAD} = 100 Ω ± 1%
t_{FALL}	Output Fall time (20% to 80%)		130	300	pS	R_{LOAD} = 100 Ω ± 1%
t_{SKEW}	Output Differential Skew		80	150	pS	R_{LOAD} = 100 Ω ± 1%

7.3.2.3 Single-Ended Input for Differential Input

This is a recommended and tested interface circuit to drive differential input with a single-ended signal.

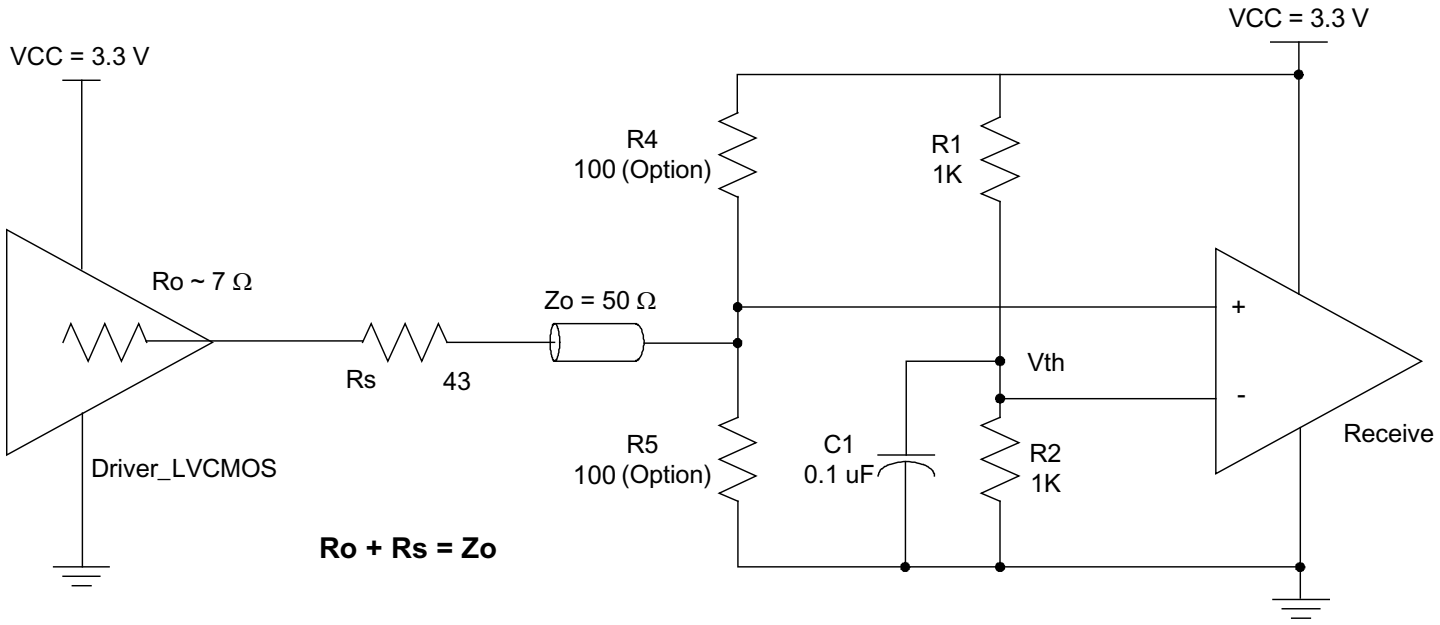

Figure 19. Example of Single-Ended Signal to Drive Differential Input

Vth = VCC*[R2/(R1+R2)]

For the example in Figure 19, R1 = R2, so Vth = VCC/2 =1.65 V

The suggested single-ended signal input:

V_{IHmax} = VCC

V_{ILmin} = 0 V

V_{swing} = 0.6 V ~ VCC

DC offset (Swing Center) = Vth/2 +/- V_{swing}*10%

7.4 JITTER PERFORMANCE

Table 41: Output Clock Jitter Generation
(jitter measured on one differential output (OUT2 or OUT3) with all other outputs disabled)

Test Definition	Output Frequency	RMS Jitter (pS) Typ	RMS Jitter (pS) Max	Note	Test Filter
25 MHz with APLL	25 MHz	1.0	1.3		12 kHz - 5 MHz
125 MHz with APLL	125 MHz	0.9	1.1		12 kHz - 20 MHz
156.25 MHz with APLL	156.25 MHz	0.9	1.2		12 kHz - 20 MHz
N x 2.048 MHz without APLL		105	150		20 Hz - 100 kHz
N x 1.544 MHz without APLL		105	150		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	105	150		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	105	150		10 Hz - 400 kHz
625 MHz with APLL	625 MHz	0.209	0.29		1.875 MHz - 20 MHz
OC-3 and STM-1 (On-chip DPLL + APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	0.8	1.3	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	2.1	ITU-T G.813 limit 0.5 UI G.813Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.5	0.8	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	77.76 MHz	0.7	1.1	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.0	2.2	ITU-T limit 0.5 UI G.813Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	155.52 MHz	0.7	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	2.2	ITU-T limit 0.5 UI G.813 Option 1Ip-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.7	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
OC-12 and STM-4 (On-chip DPLL + APLL) 77.76 MHz, 155.52 MHz, 622.08 MHz output	77.76 MHz	0.7	1.2	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.0	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
	155.52 MHz	0.7	1.2	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.0	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
	622.08 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.1	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
OC-48 and STM-16 (On-chip DPLL + APLL) 155.52 MHz, 622.08 MHz output	155.52 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-401.878 ps)	12 kHz - 20 MHz
		0.9	1.4	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.4	0.6	ITU-T G.813 Option 1	1 MHz to 20 MHz
	622.08 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 20 MHz
		0.9	1.5	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.2	0.3	ITU-T G.813 Option 1	1 MHz to 20 MHz
OC-192 and STM-64 (On-chip DPLL + APLL) 622.08 MHz Output	622.08 MHz	0.2	0.3	GR-253-CORE, ITU-T G.813 Option 2	4 MHz - 80 MHz
		0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	20 kHz - 80 MHz
		0.7	1.0	ITU-T G.813 Option 1	20 kHz - 80 MHz
NOTE: The device is locked to 25 MHz at IN3(CMOS).					

Table 42: Output Clock Jitter Generation
(jitter measured on one differential output (OUT2 or OUT3) with all other outputs enabled)

Test Definition	Output Frequency	RMS Jitter (pS) Typ	RMS Jitter (pS) Max	Note	Test Filter
25 MHz with APLL	25 MHz	1.0	1.3		12 kHz - 5 MHz
125 MHz with APLL	125 MHz	0.9	1.1		12 kHz - 20 MHz
156.25 MHz with APLL	156.25 MHz	0.9	1.2		12 kHz - 20 MHz
N x 2.048 MHz without APLL		105	150		20 Hz - 100 kHz
N x 1.544 MHz without APLL		105	150		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	105	150		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	105	150		10 Hz - 400 kHz
625 MHz with APLL	625 MHz	0.209	0.29		1.875 MHz - 20 MHz
OC-3 and STM-1 (On-chip DPLL + APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	2.2	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.6	0.9	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	77.76 MHz	0.7	1.1	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.0	2.2	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	155.52 MHz	0.7	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	2.3	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
OC-12 and STM-4 (On-chip DPLL + APLL) 77.76 MHz, 155.52 MHz, 622.08 MHz output	77.76 MHz	0.7	1.1	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.0	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
	155.52 MHz	0.7	1.2	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.0	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
	622.08 MHz	0.8	1.3	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.1	2.2	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
OC-48 and STM-16 (On-chip DPLL + APLL) 155.52 MHz, 622.08 MHz output	155.52 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-401.878 ps)	12 kHz - 20 MHz
		0.9	1.4	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.4	0.6	ITU-T G.813 Option 1	1 MHz to 20 MHz
	622.08 MHz	0.8	1.3	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 20 MHz
		0.9	1.5	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.2	0.3	ITU-T G.813 Option 1	1 MHz to 20 MHz
OC-192 and STM-64 (On-chip DPLL + APLL) 622.08 MHz output	622.08 MHz	0.2	0.3	GR-253-CORE, ITU-T G.813 Option 2	4 MHz - 80 MHz
		0.7	1.1	GR-253-CORE and ITU-T G.813 Option 2	20 kHz - 80 MHz
		0.7	1.1	ITU-T G.813 Option 1	20 kHz - 80 MHz
NOTE: The device is locked to 25MHz at IN3(CMOS).					

Table 43: Output Clock Jitter Generation
(jitter measured on CMOS output (OUT1) with all other outputs disabled)

Test Definition	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
25 MHz with APLL	25 MHz	0.9	1.3		12 kHz - 5 MHz
125 MHz with APLL	125 MHz	0.9	1.1		12 kHz - 20 MHz
156.25 MHz with APLL	156.25 MHz	0.8	1.1		12 kHz - 20 MHz
N x 2.048 MHz without APLL		105	150		20 Hz - 100 kHz
N x 1.544 MHz without APLL		105	150		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	105	150		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	105	150		10 Hz - 400 kHz
OC-3 and STM-1 (On-chip DPLL + APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	0.8	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	1.6	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.6	0.9	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	77.76 MHz	0.6	0.9	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		0.9	1.6	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	155.52 MHz	0.6	0.9	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		0.9	1.7	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
OC-12 and STM-4 (On-chip DPLL + APLL) 77.76 MHz, 155.52 MHz, 622.08MHz output	77.76 MHz	0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	1.5	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.5	0.6	ITU-T G.813 Option 1	250 kHz to 5 MHz
	155.52 MHz	0.6	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		0.9	1.5	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.3	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
OC-48 and STM-16 (On-chip DPLL + APLL) 155.52 MHz, 622.08 MHz output	155.52 MHz	0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 20 MHz
		0.8	1.2	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.4	0.5	ITU-T G.813 Option 1	1 MHz to 20 MHz
NOTE: The device is locked to 25MHz at IN3(CMOS).					

Table 44: Output Clock Jitter Generation
(jitter measured on CMOS output (OUT1) with all other outputs enabled)

Test Definition	Output Frequency	RMS Typ (pS)	RMS Max (pS)	Note	Test Filter
25 MHz with APLL	25 MHz	0.9	1.3		12 kHz - 5 MHz
125 MHz with APLL	125 MHz	0.9	1.1		12 kHz - 20 MHz
156.25 MHz with APLL	156.25 MHz	0.9	1.1		12 kHz - 20 MHz
N x 2.048 MHz without APLL		105	150		20 Hz - 100 kHz
N x 1.544 MHz without APLL		105	150		10 Hz - 40 kHz
44.736 MHz without APLL	44.736 MHz	105	150		100 Hz - 800 kHz
34.368 MHz without APLL	34.368 MHz	105	150		10 Hz - 400 kHz
OC-3 and STM-1 (On-chip DPLL + APLL) 19.44 MHz, 77.76 MHz, 155.52 MHz output	19.44 MHz	0.9	1.2	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p (1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.1	2.7	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.7	0.9	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	77.76 MHz	0.6	0.9	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p(1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.0	1.9	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
	155.52 MHz	0.6	0.9	GR-253-CORE and ITU-T G.813 Option 2 limit 0.1 UI p-p(1 UI-6430 ps)	12 kHz - 1.3 MHz
		1.0	2.3	ITU-T limit 0.5 UI G.813 Option 1I p-p (1 UI-6430 ps)	500 Hz to 1.3 MHz
		0.4	0.6	ITU-T G.813 Option 1	65 kHz to 1.3 MHz
OC-12 and STM-4 (On-chip DPLL + APLL) 77.76 MHz, 155.52 MHz, 622.08 MHz output	77.76 MHz	0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		1.0	2.4	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.5	0.6	ITU-T G.813 Option 1	250 kHz to 5 MHz
	155.52 MHz	0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 5 MHz
		0.9	2.2	ITU-T G.813 Option 1	1000 Hz to 5 MHz
		0.4	0.5	ITU-T G.813 Option 1	250 kHz to 5 MHz
OC-48 and STM-16 (On-chip DPLL + APLL) 155.52 MHz, 622.08 MHz output	155.52 MHz	0.7	1.0	GR-253-CORE and ITU-T G.813 Option 2	12 kHz - 20 MHz
		0.8	1.3	ITU-T G.813 Option 1	5000 Hz to 20 MHz
		0.4	0.6	ITU-T G.813 Option 1	1 MHz to 20 MHz
NOTE: The device is locked to 25MHz at IN3(CMOS).					

7.5 OUTPUT WANDER GENERATION

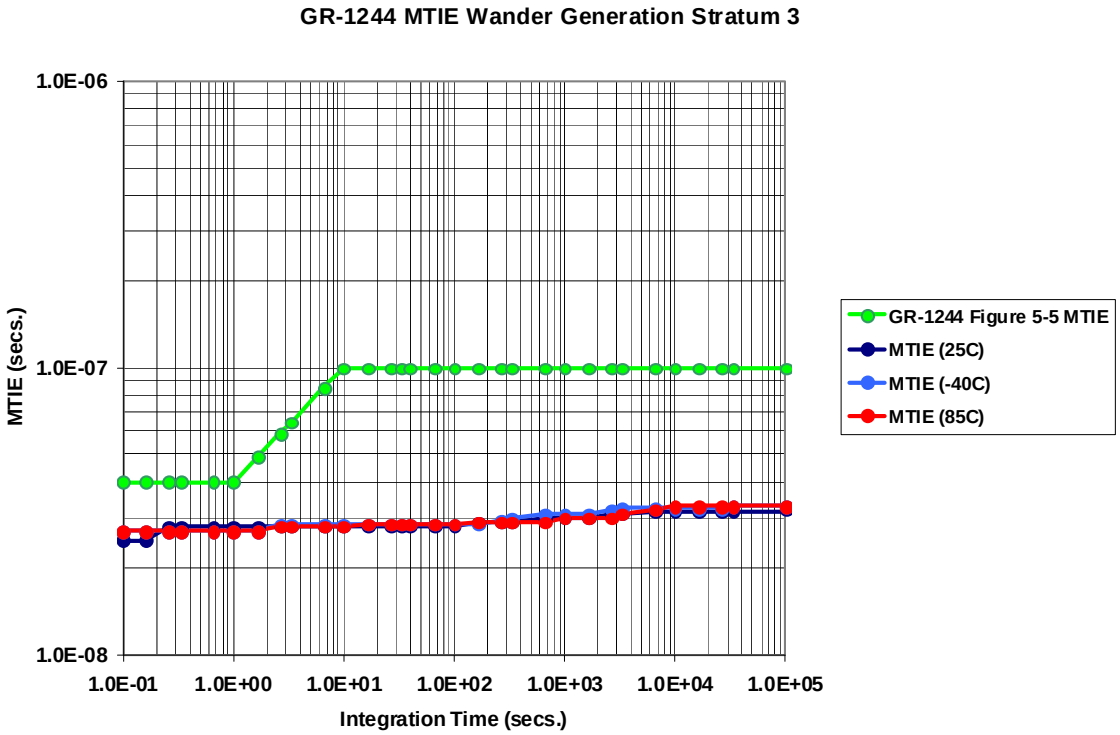

Figure 20. MTIE Output Wander Generation

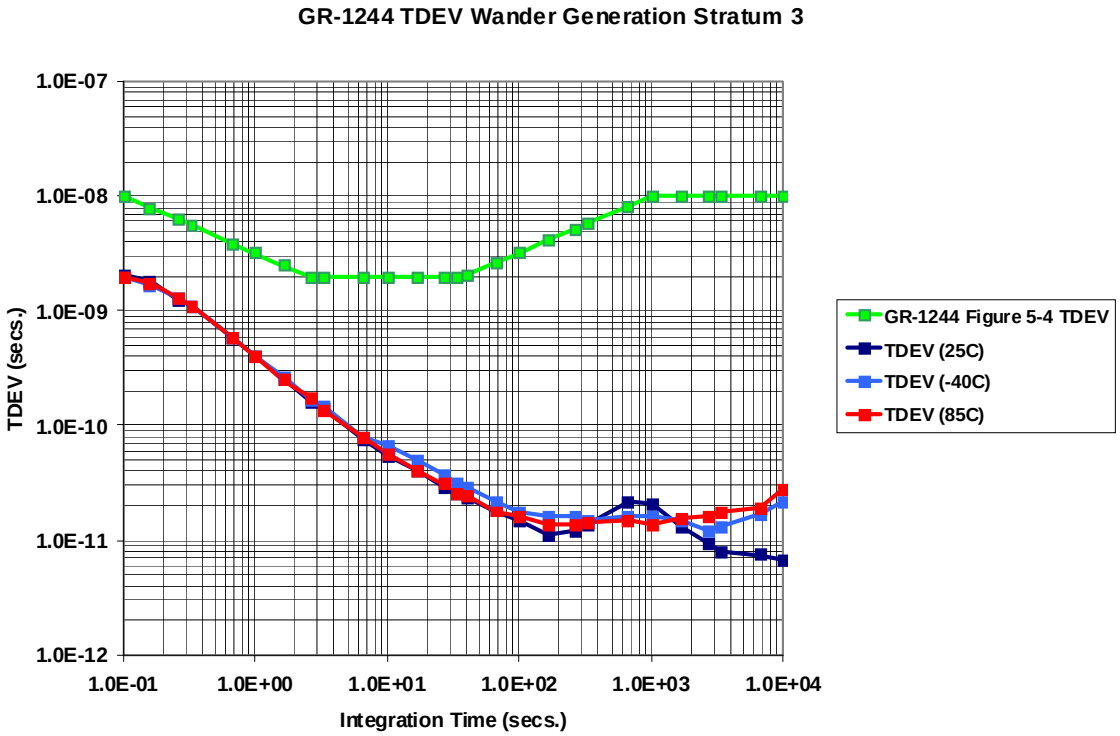

Figure 21. TDEV Output Wander Generation

7.6 INPUT / OUTPUT CLOCK TIMING

The inputs and outputs are aligned ideally. But due to the circuit delays, there is delay between the inputs and outputs.

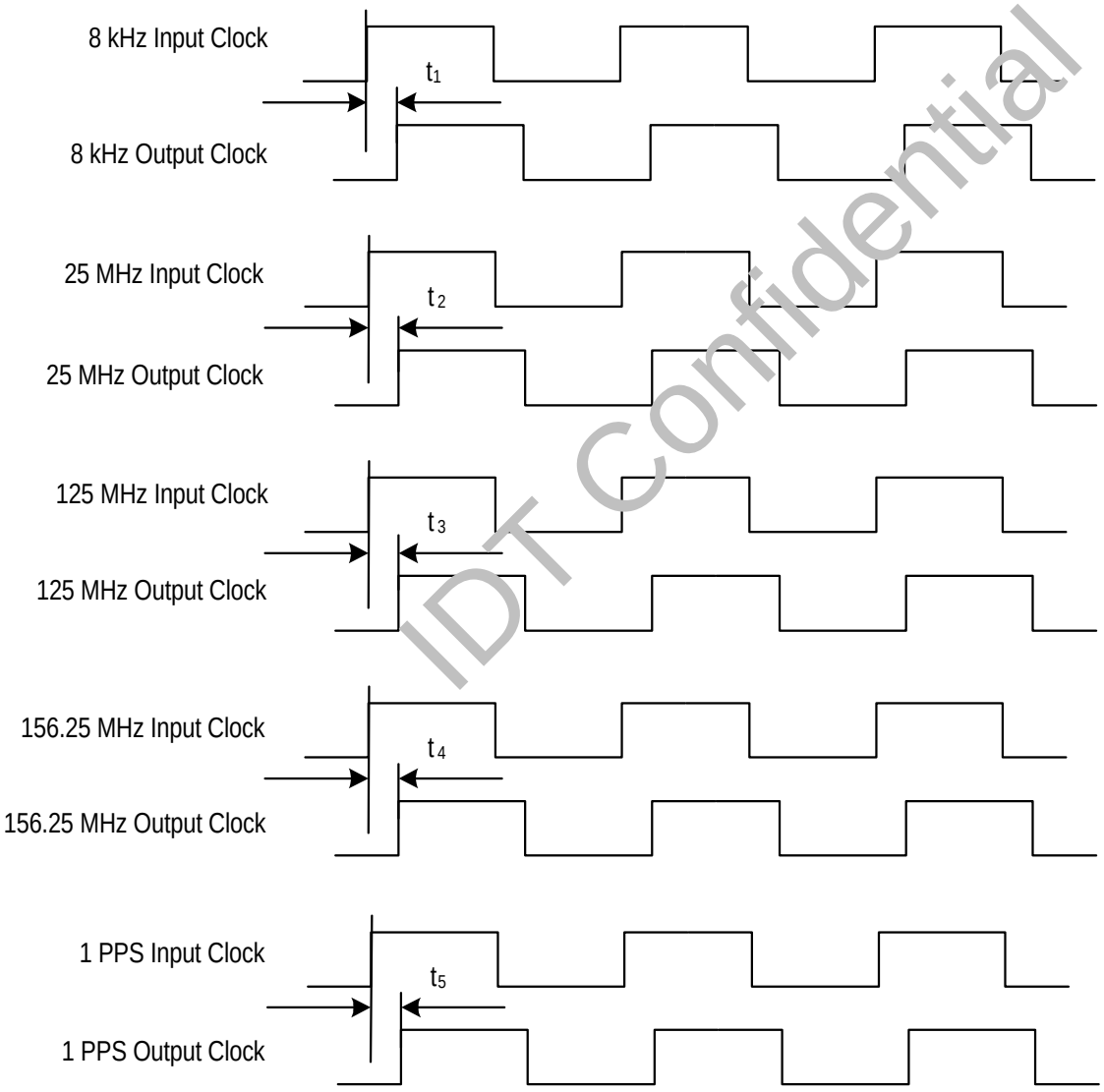

Figure 22. Input / Output Clock Timing

Table 45: Input/Output Clock Timing

Symbol	Typical Delay (ns)	Maximum Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	2	4	2
t_2	5	8	2
t_3	-2	-4	2
t_4	-2	-3.2	2
t_5	3	10	10

Note:
1. Typical delay provided as reference only.
2. Peak-to-Peak Delay Variation is the delay variation.
3. OCXO is used for 1PPS delay test.

7.7 1PPS INPUT AND OUTPUT CLOCK TIMING

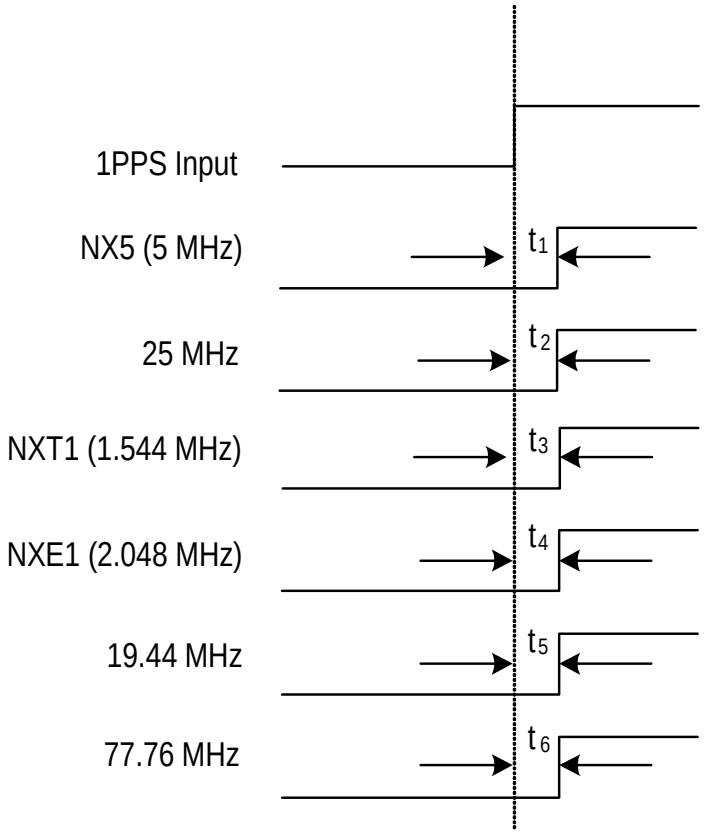

Figure 23. 1PPS Input and Output Clock Timing

Table 46: Output Clock Timing

Symbol	Typical Delay (ns)	Maximum Delay (ns)	Peak to Peak Delay Variation (ns)
t_1	2	10	10
t_2	4	10	10
t_3	2	10	10
t_4	2	10	10
t_5	4	10	10
t_6	4	10	10

Note:
1. OCXO is used for delay test.

8 THERMAL MANAGEMENT

The device operates over the industry temperature range -40°C ~ +85°C. To ensure the functionality and reliability of the device, the maximum junction temperature T_{jmax} should not exceed 125°C. In some applications, the device will consume more power and a thermal solution should be provided to ensure the junction temperature T_j does not exceed the T_{jmax}.

8.1 JUNCTION TEMPERATURE

Junction temperature T_j is the temperature of package typically at the geographical center of the chip where the device's electrical circuits are. It can be calculated as follows:

Equation 1: $T_j = T_A + P \times \theta_{JA}$

Where:

θ_{JA} = *Junction-to-Ambient Thermal Resistance of the Package*

T_j = *Junction Temperature*

T_A = *Ambient Temperature*

P = Device Power Dissipation

In order to calculate junction temperature, an appropriate θ_{JA} must be used. The θ_{JA} is shown in Table 47:

Table 47: Thermal Data

Package	Pin Count	Thermal Pad	θ_{JB} (°C/W)	θ_{JA} (°C/W) Air Flow in m/s		
				0	1	2
QFN/NLG72	72	6x6 mm ePad soldered down / 3x3 PCB vias	0.56	28.8	22.1	19.8

8.2 VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 24. The solderable area on The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

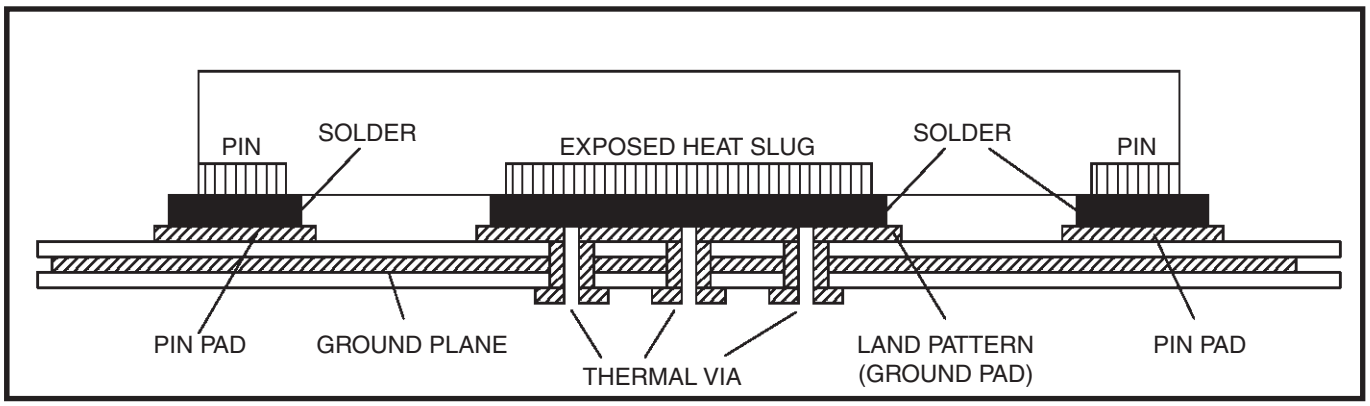

Figure 24. assembly for Expose Pad thermal Release Path (Side View)

3G	---	Third Generation
ADSL	---	Asymmetric Digital Subscriber Line
APLL	---	Analog Phase Locked Loop
ATM	---	Asynchronous Transfer Mode
BITS	---	Building Integrated Timing Supply
CMOS	---	Complementary Metal-Oxide Semiconductor
DCO	---	Digital Controlled Oscillator
DPLL	---	Digital Phase Locked Loop
DSL	---	Digital Subscriber Line
DSLAM	---	Digital Subscriber Line Access MUX
DWDM	---	Dense Wavelength Division Multiplexing
EPROM	---	Erasable Programmable Read Only Memory
ETH	---	Synchronous Ethernet System
GPS	---	Global Positioning System
GSM	---	Global System for Mobile Communications
IIR	---	Infinite Impulse Response
IP	---	Internet Protocol
ISDN	---	Integrated Services Digital Network
JTAG	---	Joint Test Action Group
LPF	---	Low Pass Filter
LVDS	---	Low Voltage Differential Signal
MTIE	---	Maximum Time Interval Error
MUX	---	Multiplexer
OBSAI	---	Open Base Station Architecture Initiative
OC-n	---	Optical Carried rate, n = 1, 3, 12, 48, 192, 768; 51 Mbit/s, 155 Mbit/s, 622 Mbit/s, 2.5 Gbit/s, 10 Gbit/s, 40 Gbit/s.
HS	---	Hiitless Switching
PDH	---	Plesiochronous Digital Hierarchy
PECL	---	Positive Emitter Coupled Logic

PFD	---	Phase & Frequency Detector
PLL	---	Phase Locked Loop
RMS	---	Root Mean Square
PRS	---	Primary Reference Source
SDH	---	Synchronous Digital Hierarchy
SEC	---	SDH / SONET Equipment Clock
SMC	---	SONET Minimum Clock
SONET	---	Synchronous Optical Network
SSU	---	Synchronization Supply Unit
STM	---	Synchronous Transfer Module
TCM-ISDN	---	Time Compression Multiplexing Integrated Services Digital Network
TDEV	---	Time Deviation
UI	---	Unit Interval
WLL	---	Wireless Local Loop

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Datasheet

PACKAGE DIMENSIONS

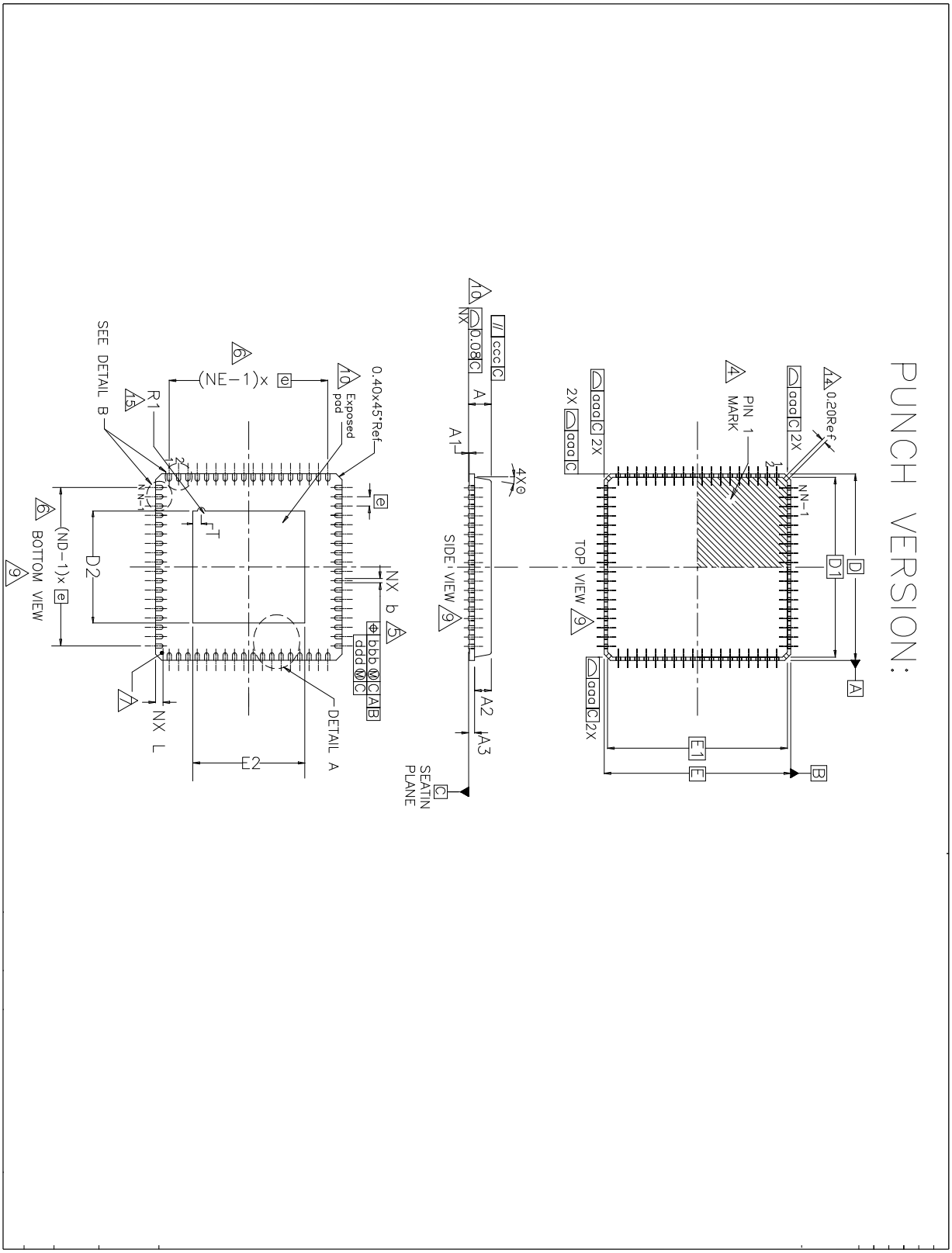


Figure 25. 72-Pin QFN Package Dimensions (a) (in Millimeters)

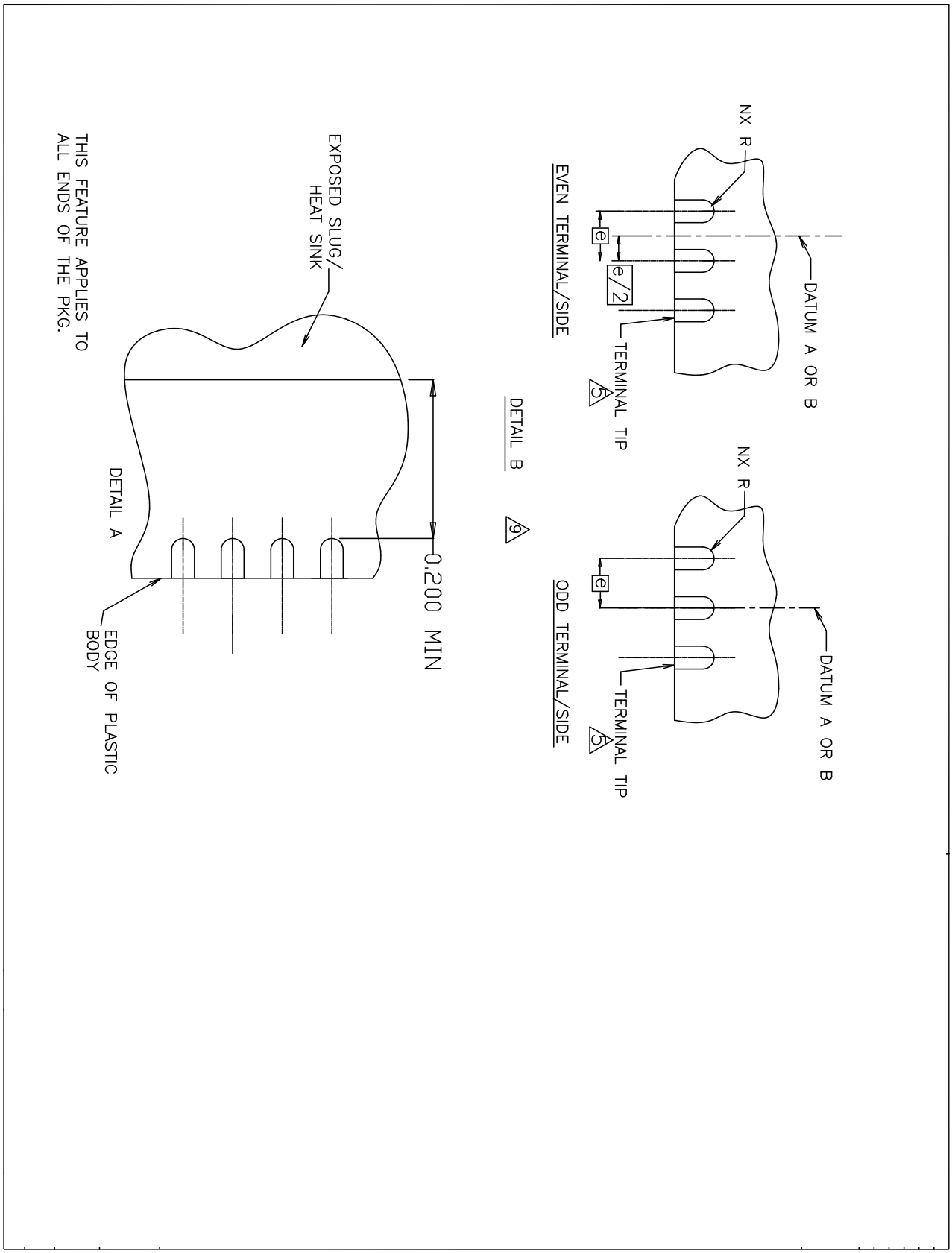


Figure 26. 72-Pin QFN Package Dimensions (b) (in Millimeters)

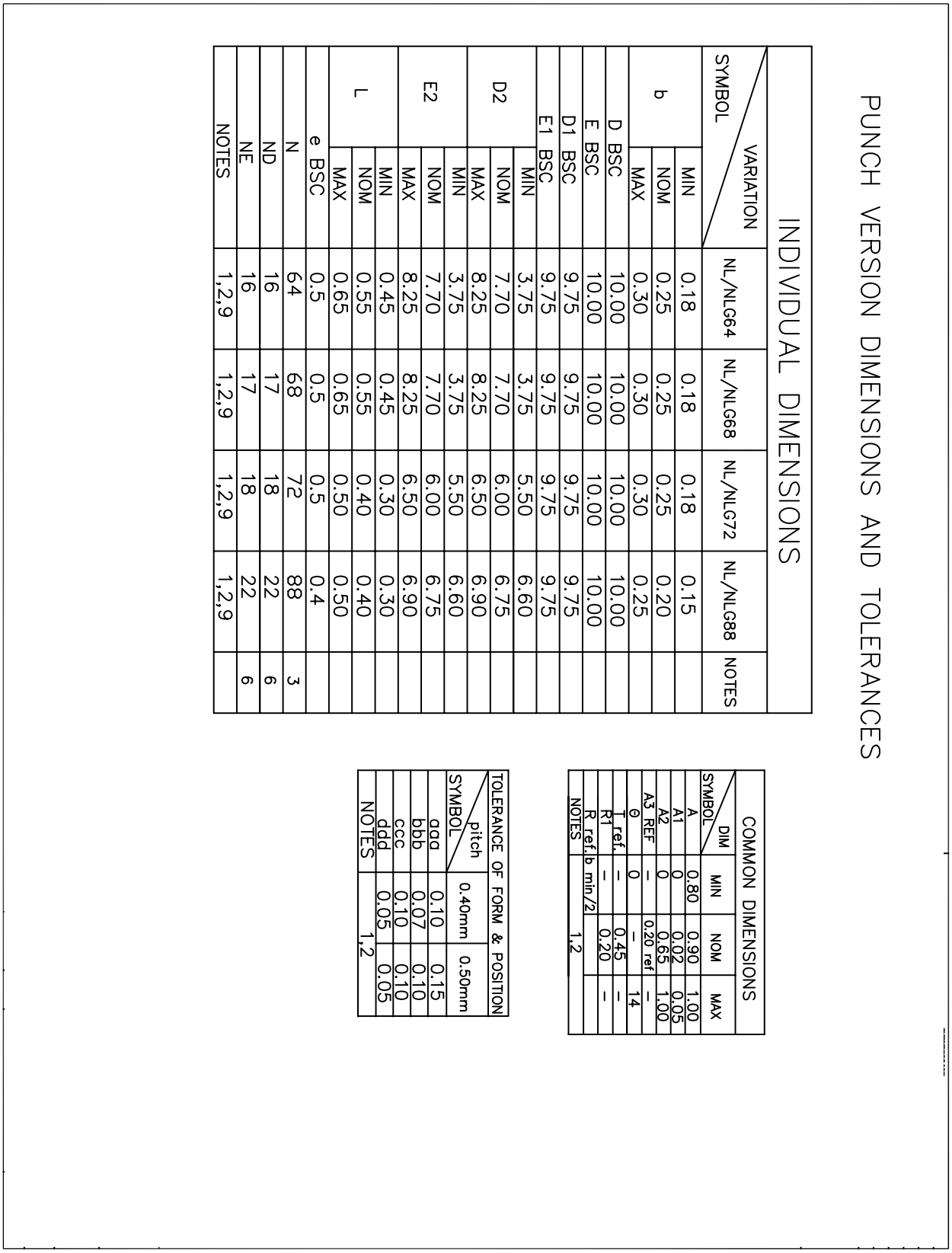


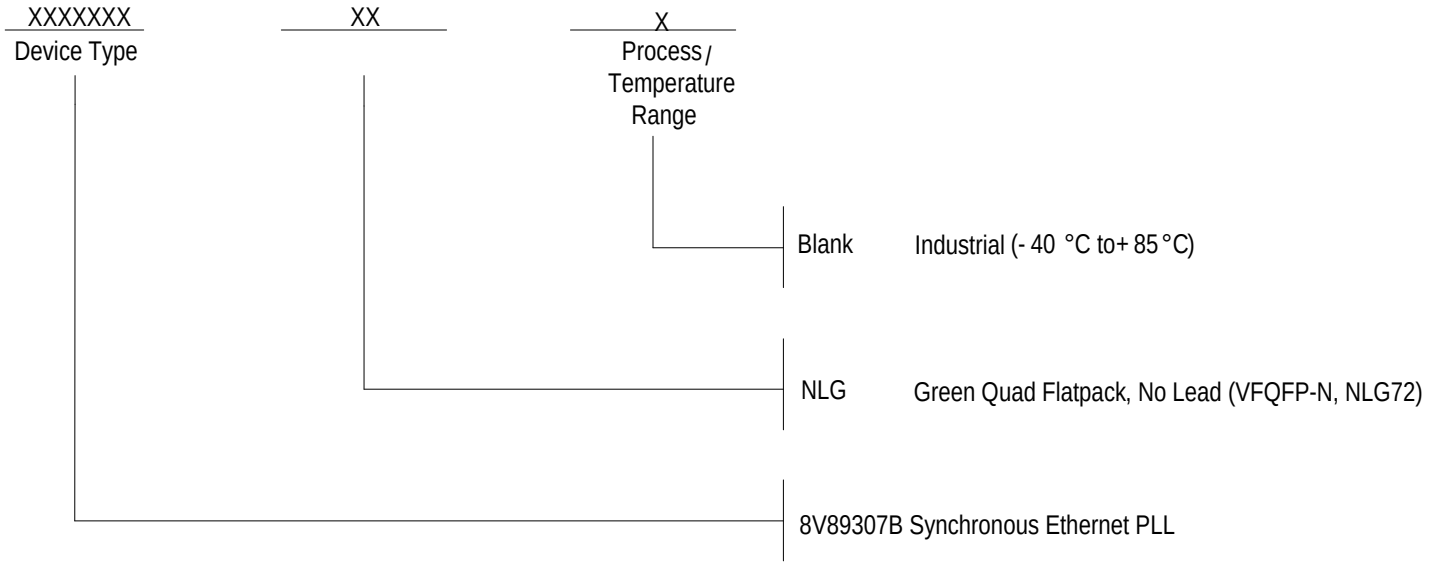
Figure 27. 72-Pin QFN Dimensions

Note:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters . All angles are in degrees.
3. N is the total number of terminals.
4. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012.Details of terminal #1 identifier are optional , but must be located within the zone indicated.The terminal #1 identifier may be a molded, marked, or metalized features.
5. Dimensions b apply to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
6. ND refer to the maximum number of terminals on D and E side.
7. Depopulation is possible in a symmetrical fashion.
8. N/A
9. For a complete set of dimensions for each variation, see the individual variation and the common dimensions and tolerances on page 6
10. Coplanarity applies to the exposed heat sink slug as well as the terminals.
11. When more than one variation (option) exists for the same profile height, body size (D x E), and pitch, then those variations will be denoted by an additional dash number (ie: -1, -2, etc.) designator to identify them. The new variations would be created from all or any of the followwing reasons lead counts, terminal lengths, and or thermal pad sizes.
12. Variation comply to JEDEC MO-220.
13. A3 is measured at side of the package in between two adjacent leads.
14. Tie bar option could be exposed or hidden.
15. The exact shape of this feature varies.

Figure 28. Package Notes

ORDERING INFORMATION



REVISION HISTORY

January 17, 2012	pages 120 - 123
May 10, 2012	pages 106, 107
July 23, 2012	page 113
August 15, 2012	pages 21, 41 - 42, 53, 55, 79
August 17, 2012	pages 33-34
March 1, 2013	pages 16 - 17, 99, 104, 115
April 12, 2016	Updated datasheet header/footer, deleted “IDT” part number prefix, deleted “Confidential” watermark

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