ADC1206S040/055/070

Single 12 bits ADC, up to 40 MHz, 55 MHz or 70 MHz

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1206S040/055/070 are a family of BiCMOS 12-bit Analog-to-Digital Converters (ADC) optimized for a wide range of applications such as cellular infrastructures, professional telecommunications, imaging, and digital radio. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 70 MHz. All static digital inputs (SH, $\overline{CE}$ and OTC) are Transistor-Transistor Logic (TTL) and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

2. Features

- 12-bit resolution
- Sampling rate up to 70 MHz
- −3 dB bandwidth of 245 MHz
- 5 V power supplies and 3.3 V output power supply
- Binary or twos complement CMOS outputs
- In-range CMOS compatible output
- TTL and CMOS compatible static digital inputs
- TTL and CMOS compatible digital outputs
- Differential AC or Positive Emitter-Coupled Logic (PECL) clock input; TTL compatible
- Power dissipation 550 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample and hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included
- −40 °C to +85 °C ambient temperature

3. Applications

High-speed analog-to-digital conversion for:

- Cellular infrastructure
- Professional telecommunication
- Digital radio
- Radar
- Medical imaging
- Fixed network
- Cable modem

- Barcode scanner
- Cable Modem Termination System (CMTS)/
  Data Over Cable Service Interface Specification (DOCSIS)

4. Quick reference data

Table 1. Quick reference data

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	3.6	V
I_{CCA}	analog supply current		-	78	87	mA
I_{CCD}	digital supply current		-	27	30	mA
I_{CCO}	output supply current	f_{clk} = 20 MHz f_i = 400 kHz	-	3	4	mA
INL	integral non-linearity	f_{clk} = 20 MHz f_i = 400 kHz	-	±2.6	±4.5	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz f_i = 400 kHz (no missing code guaranteed)	-	±0.5	+1.1 − 0.95	LSB
$f_{clk(max)}$	maximum clock frequency	ADC1206S040H	40	-	-	MHz
		ADC1206S055H	55	-	-	MHz
		ADC1206S070H	70	-	-	MHz
P_{tot}	total power dissipation	f_{clk} = 55 MHz f_i = 20 MHz	-	550	660	mW

5. Ordering information

Table 2. Ordering information

Type number	Package			Sampling frequency (MHz)
	Name	Description	Version	
ADC1206S040H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	40
ADC1206S055H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	55
ADC1206S070H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	70

6. Block diagram

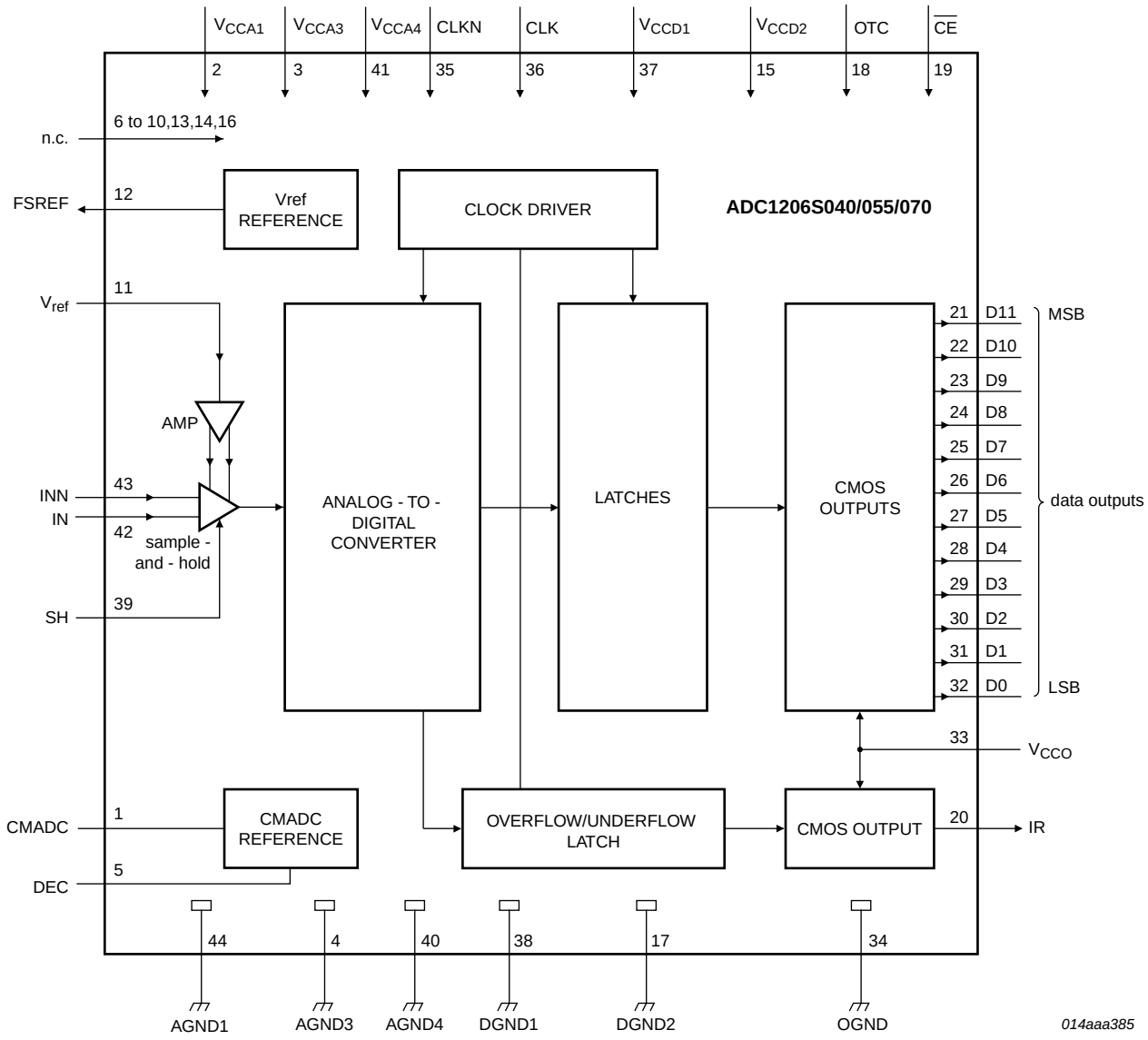


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

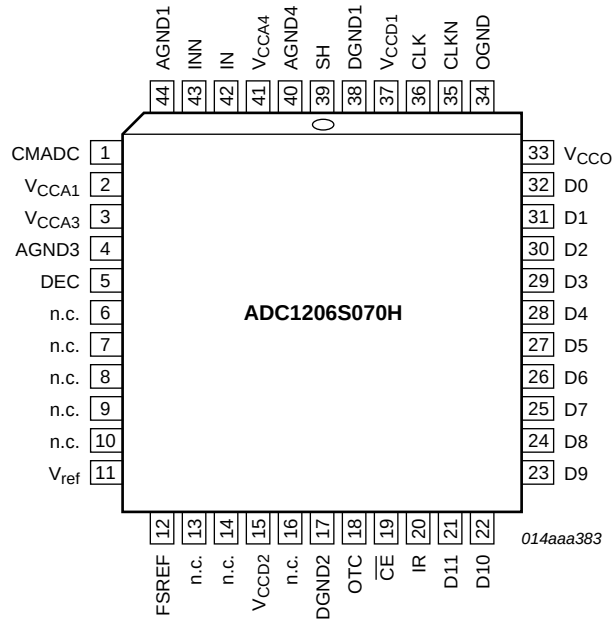


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
CMADC	1	regulator output common mode ADC input
V_{CCA1}	2	analog supply voltage 1 (5 V)
V_{CCA3}	3	analog supply voltage 3 (5 V)
AGND3	4	analog ground 3
DEC	5	decoupling node
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
V_{ref}	11	reference voltage input
FSREF	12	full-scale reference output
n.c.	13	not connected
n.c.	14	not connected
V_{CCD2}	15	digital supply voltage 2 (5 V)
n.c.	16	not connected

Table 3. Pin description *…continued*

Symbol	Pin	Description
DGND2	17	digital ground 2
OTC	18	control input twos complement output; active HIGH
$\overline{CE}$	19	chip enable input (CMOS level; active LOW)
IR	20	in-range output
D11	21	data output; bit 11 (Most Significant Bit (MSB))
D10	22	data output; bit 10
D9	23	data output; bit 9
D8	24	data output; bit 8
D7	25	data output; bit 7
D6	26	data output; bit 6
D5	27	data output; bit 5
D4	28	data output; bit 4
D3	29	data output; bit 3
D2	30	data output; bit 2
D1	31	data output; bit 1
D0	32	data output; bit 0 (Least Significant Bit (LSB))
V_{CCO}	33	output supply voltage (3.3 V)
OGND	34	output ground
CLKN	35	complementary clock input
CLK	36	clock input
V_{CCD1}	37	digital supply voltage 1 (5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V_{CCA4}	41	analog supply voltage 4 (5 V)
IN	42	analog input voltage
INN	43	complementary analog input voltage
AGND1	44	analog ground 1

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CCA}	analog supply voltage		[1]	−0.3	+7.0	V
V_{CCD}	digital supply voltage		[1]	−0.3	+7.0	V
V_{CCO}	output supply voltage		[1]	−0.3	+7.0	V
ΔV_{CC}	supply voltage difference	$V_{CCA} - V_{CCD}$		−1.0	+1.0	V
		$V_{CCD} - V_{CCO}$		−1.0	+4.0	V
		$V_{CCA} - V_{CCO}$		−1.0	+4.0	V

Table 4. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{i(IN)}$	input voltage on pin IN	referenced to AGND	0.3	V_{CCA}	V
$V_{i(INN)}$	input voltage on pin INN		0.3	V_{CCA}	V
$V_{i(clk)(p-p)}$	peak-to-peak clock input voltage	differential clock drive at pins 35 and 36	-	V_{CCD}	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C

[1] The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

10. Characteristics

Table 6. Characteristics

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = –40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Supplies							
V_{CCA}	analog supply voltage			4.75	5.0	5.25	V
V_{CCD}	digital supply voltage			4.75	5.0	5.25	V
V_{CCO}	output supply voltage			3.0	3.3	3.6	V
I_{CCA}	analog supply current		I	-	78	87	mA
I_{CCD}	digital supply current		I	-	27	30	mA
I_{CCO}	output supply current	f_{clk} = 20 MHz; f_i = 400 kHz	I	-	3	4	mA
		f_{clk} = 40 MHz; f_i = 4.43 MHz	C	-	6.2	9	mA
		f_{clk} = 55 MHz; f_i = 20 MHz	I	-	9.5	12	mA
P_{tot}	total power dissipation	f_{clk} = 55 MHz f_i = 20 MHz		-	550	660	mW

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Inputs							
CLK and CLKN referenced to DGND[2]							
V_{IL}	LOW-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.19	-	3.52	V
		TTL mode	C	0	-	0.8	V
V_{IH}	HIGH-level input voltage	PECL mode; V_{CCD} = 5 V	I	3.83	-	4.12	V
		TTL mode	C	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} or V_{CLKN} = 3.19 V	C	−10	-	-	μA
I_{IH}	HIGH-level input current	V_{CLK} or V_{CLKN} = 3.83 V	C	-	-	10	μA
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage	AC driving mode; DC voltage level = 2.5 V	C	1	1.5	2.0	V
R_i	input resistance	f_{clk} = 55 MHz	D	2	-	-	kΩ
C_i	input capacitance	f_{clk} = 55 MHz	D	-	-	2	pF
OTC, SH and $\overline{CE}$ (referenced to DGND); see Table 8 and 9							
V_{IL}	LOW-level input voltage		I	0	-	0.8	V
V_{IH}	HIGH-level input voltage		I	2.0	-	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.8 V	I	−20	-	-	μA
I_{IH}	HIGH-level input current	V_{IH} = 2.0 V	I	-	-	20	μA
IN and INN (referenced to AGND); see Table 7, $V_{ref} = V_{CCA3} - 1.75$ V							
I_{IL}	LOW-level input current	SH = HIGH	C	-	10	-	μA
I_{IH}	HIGH-level input current	SH = HIGH	C	-	10	-	μA
R_i	input resistance	f_i = 20 MHz	D	-	14	-	MΩ
C_i	input capacitance	f_i = 20 MHz	D	-	450	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{I(IN)} = V_{I(INN)}$ output code 2047	C	$V_{CCA3} - 1.7$	$V_{CCA3} - 1.6$	$V_{CCA3} - 1.2$	V
Voltage controlled regulator output CMADC							
$V_{O(cm)}$	common-mode output voltage		I	-	$V_{CCA3} - 1.6$	-	V
I_{load}	load current		I	-	1	2	mA

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Voltage input V_{ref}[3]							
V_{ref}	reference voltage	full-scale fixed voltage; f_i = 20 MHz; f_{clk} = 55 MHz	C	-	$V_{CCA3} - 1.75$	-	V
I_{ref}	reference current		C	-	0.3	10	μA
$V_{i(dif)(p-p)}$	peak-to-peak differential input voltage	$V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V	C	-	1.9	-	V
Voltage controlled regulator output FSREF							
$V_{O(ref)}$	reference output voltage	$V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V	I	-	$V_{CCA3} - 1.75$	-	V
Digital outputs D11 to D0 and IR (referenced to OGND)							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	I	0	-	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = − 0.4 mA	I	$V_{CCCO} - 0.5$	-	V_{CCO}	V
I_o	output current	3-state output level between 0.5 V and V_{CCO}	I	−20	-	+20	μA
Switching characteristics; Clock frequency f_{clk}; see Figure 3							
$f_{clk(min)}$	minimum clock frequency	SH = HIGH	C	-	-	7	MHz
$f_{clk(max)}$	maximum clock frequency	ADC1206S040H	C	40	-	-	MHz
		ADC1206S055H	I	55	-	-	MHz
		ADC1206S070H	C	70	-	-	MHz
$t_{w(clk)H}$	HIGH clock pulse width	f_i = 20 MHz	C	6.8	-	-	ns
$t_{w(clk)L}$	LOW clock pulse width	f_i = 20 MHz	C	6.8	-	-	ns
Analog signal processing; 50 % clock duty factor; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; see Table 7							
Linearity							
INL	integral non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz	I	-	±2.6	±4.5	LSB
DNL	differential non-linearity	f_{clk} = 20 MHz; f_i = 400 kHz (no missing code guaranteed)	I	-	±0.5	+1.1 − 0.95	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C; output code = 2047	C	−25	+5	+25	mV
E_G	gain error	spread from device to device; $V_{CCA} = V_{CCD}$ = 5 V; V_{CCO} = 3.3 V; T_{amb} = 25 °C	C	−7	-	+7	%FS

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Bandwidth (f_{clk} = 55 MHz)[4]							
B	bandwidth	−3 dB; full-scale input	C	220	245	-	MHz
Harmonics							
α_{2H}	second harmonic level	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	−78	-	dBFS
		f_i = 10 MHz	C	-	−77	-	dBFS
		f_i = 15 MHz	C	-	−74	-	dBFS
		f_i = 20 MHz	C	-	−71	-	dBFS
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−77	-	dBFS
		f_i = 10 MHz	C	-	−77	-	dBFS
		f_i = 15 MHz	C	-	−76	-	dBFS
		f_i = 20 MHz	I	-	−73	-	dBFS
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−76	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−70	-	dBFS
α_{3H}	third harmonic level	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−74	-	dBFS
		f_i = 20 MHz	C	-	−73	-	dBFS
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−74	-	dBFS
		f_i = 20 MHz	I	-	−72	-	dBFS
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−74	-	dBFS
		f_i = 10 MHz	C	-	−74	-	dBFS
		f_i = 15 MHz	C	-	−73	-	dBFS

Table 6. Characteristics *…continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Total harmonic distortion[5]							
THD	total harmonic distortion	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−68	-	dBFS
		f_i = 15 MHz	C	-	−68	-	dBFS
		f_i = 20 MHz	C	-	−68	-	dBFS
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−68	-	dBFS
		f_i = 15 MHz	C	-	−68	-	dBFS
		f_i = 20 MHz	I	-	−68	-	dBFS
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	−68	-	dBFS
		f_i = 10 MHz	C	-	−67	-	dBFS
		f_i = 15 MHz	C	-	−67	-	dBFS
Thermal noise (f_{clk} = 55 MHz)							
$N_{th(RMS)}$	RMS thermal noise	shorted input; SH = HIGH; f_{clk} = 55 MHz	C	-	0.45	-	LSB
Signal-to-noise ratio[6]							
S/N	signal-to-noise ratio	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	64	-	dBFS
		f_i = 20 MHz	C	-	64	-	dBFS
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	64	-	dBFS
		f_i = 20 MHz	I	-	64	-	dBFS
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	64	-	dBFS
		f_i = 10 MHz	C	-	64	-	dBFS
		f_i = 15 MHz	C	-	63	-	dBFS

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Spurious free dynamic range; see Figure 7, 13 and 14							
SFDR	spurious free dynamic range	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	72	-	dBFS
		f_i = 10 MHz	C	-	71	-	dBFS
		f_i = 15 MHz	C	-	71	-	dBFS
		f_i = 20 MHz	C	-	69	-	dBFS
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	72	-	dBFS
		f_i = 10 MHz	C	-	71	-	dBFS
		f_i = 15 MHz	C	-	71	-	dBFS
		f_i = 20 MHz	I	-	69	-	dBFS
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	70	-	dBFS
		f_i = 10 MHz	C	-	69	-	dBFS
		f_i = 15 MHz	C	-	69	-	dBFS
Effective number of bits[7]							
ENOB	effective number of bits	ADC1206S040H; (f_{clk} = 40 MHz)					
		f_i = 4.43 MHz	C	-	10.1	-	bits
		f_i = 10 MHz	C	-	10.1	-	bits
		f_i = 15 MHz	C	-	10.1	-	bits
		f_i = 20 MHz	C	-	10	-	bits
		ADC1206S055H; (f_{clk} = 55 MHz)					
		f_i = 4.43 MHz	C	-	10.1	-	bits
		f_i = 10 MHz	C	-	10.1	-	bits
		f_i = 15 MHz	C	-	10	-	bits
		f_i = 20 MHz	I	-	10	-	bits
		ADC1206S070H; (f_{clk} = 70 MHz)					
		f_i = 4.43 MHz	C	-	10	-	bits
		f_i = 10 MHz	C	-	10	-	bits
		f_i = 15 MHz	C	-	10	-	bits
Two-tone Intermodulation; (f_{clk} = 55 MHz; f_i = 20 MHz)[8]							
α_{IM}	intermodulation suppression		C	-	−68	-	dB
IMD3	third-order intermodulation distortion		C	-	−70	-	dB

Table 6. Characteristics *...continued*

V_{CCA} = V2 to V44, V3 to V4 and V41 to V40 = 4.75 V to 5.25 V; V_{CCD} = V37 to V38 and V15 to V17 = 4.75 V to 5.25 V; V_{CCO} = V33 to V34 = 3.0 V to 3.6 V; AGND and DGND shorted together; T_{amb} = −40 °C to 85 °C; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; $V_{ref} = V_{CCA3} - 1.75$ V; $V_{I(cm)} = V_{CCA3} - 1.6$ V; typical values measured at $V_{CCA} = V_{CCD}$ = 5 V and V_{CCO} = 3.3 V, T_{amb} = 25 °C and C_L = 10 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Bit error rate (f_{clk} = 55 MHz)							
BER	bit error rate	f_i = 20 MHz; V_I = ±16 LSB at code 2047	C	-	10^{-14}	-	times/sample
Timing (C_L = 10 pF)[9]							
$t_{d(s)}$	sampling delay time		C	-	0.25	1	ns
$t_{h(o)}$	output hold time		C	4	6.4	-	ns
$t_{d(o)}$	output delay time		C	-	9.0	13	ns
3-state output delay times; see Figure 4							
t_{dZH}	float to active HIGH delay time		C	-	5.1	9.0	ns
t_{dZL}	float to active LOW delay time		C	-	7.0	11	ns
t_{dHZ}	active HIGH to float delay time		C	-	9.7	14	ns
t_{dLZ}	active LOW to float delay time		C	-	9.5	13	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] The circuit has two clock inputs: CLK and CLKN. There are 5 modes of operation:

a) PECL mode 1: (DC level vary 1:1 with V_{CCD}) CLK and CLKN inputs are at differential PECL levels.

b) PECL mode 2: (DC level vary 1:1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on CLKN decoupled to GND via a 100 nF capacitor.

c) PECL mode 3: (DC level vary 1:1 with V_{CCD}) CLKN input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.

d) Differential AC driving mode 4: When driving the CLK input directly and with any AC signal of minimum 1 V (p - p) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the CLKN input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the CLKN or CLK input to DGND via a 100 nF capacitor.

e) TTL mode 1: CLK input is at TTL level and sampling is taken on the falling edge of the clock input signal. In that case the CLKN pin has to be connected to the ground.

[3] The ADC input range can be adjusted with an external reference connected to V_{ref} pin. This voltage has to be referenced to V_{CCA}; see Figure 12.

[4] The −3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.

[5] Total Harmonic Distortion (THD) is obtained with the addition of the first five harmonics:

$$THD = 20 \log \sqrt{\frac{(\alpha_{2H})^2 + (\alpha_{3H})^2 + (\alpha_{4H})^2 + (\alpha_{5H})^2 + (\alpha_{6H})^2}{(\alpha_{1H})^2}}$$

where α_{1H} is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input; see Figure 6.

[6] Signal-to-noise ratio (S/N) takes into account all harmonics above five and noise up to Nyquist frequency; see Figure 8.

[7] Effective number of bits are obtained via a fast Fourier transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to Single-to-noise-and-distortion-ratio (SINAD) is given by SINAD = ENOB × 6.02 + 1.76 dB; see Figure 5.

[8] Intermodulation measured relative to either tone with analog input frequencies of 20 and 20.1 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (−6 dB below full-scale for each input signal). IMD3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.

[9] Output data acquisition: the output data is available after the maximum delay of $t_{d(o)}$; see Figure 3.

11. Additional information relating to Table 6

Table 7. Output coding with differential inputs (typical values to AGND); $V_{I(IN)(p-p)} - V_{I(INN)(p-p)} = 1.9$ V, $V_{ref} = V_{CCA3} - 1.75$ V

Code	$V_{I(IN)(p-p)}$ (V)	$V_{I(INN)(p-p)}$	IR	Binary outputs D11 to D0	Twos complement outputs D11 to D0
Underflow	< 3.125	< 4.075	0	0000 0000 0000	10 0000 0000 00
0	3.125	4.075	1	0000 0000 0000	10 0000 0000 00
1	-	-	1	0000 0000 0001	10 0000 0000 01
↓	-	-	↓	↓	↓
2047	3.6	3.6	↓	01 1111 1111 11	11 1111 1111 11
↓	-	-	↓	↓	↓
4094	-	-	1	1111 1111 1110	0111 1111 1110
4095	4.075	3.125	1	1111 1111 1111	0111 1111 1111
Overflow	> 4.075	< 3.125	0	1111 1111 1111	0111 1111 1111

Table 8. Mode selection

OTC	$\overline{CE}$	D0 to D11 and IR
0	0	binary; active
1	0	two's complement; active
X[1]	1	high-impedance

[1] X = don't care.

Table 9. Sample-and-hold selection

SH	Sample-and-hold
1	active
0	inactive; tracking mode

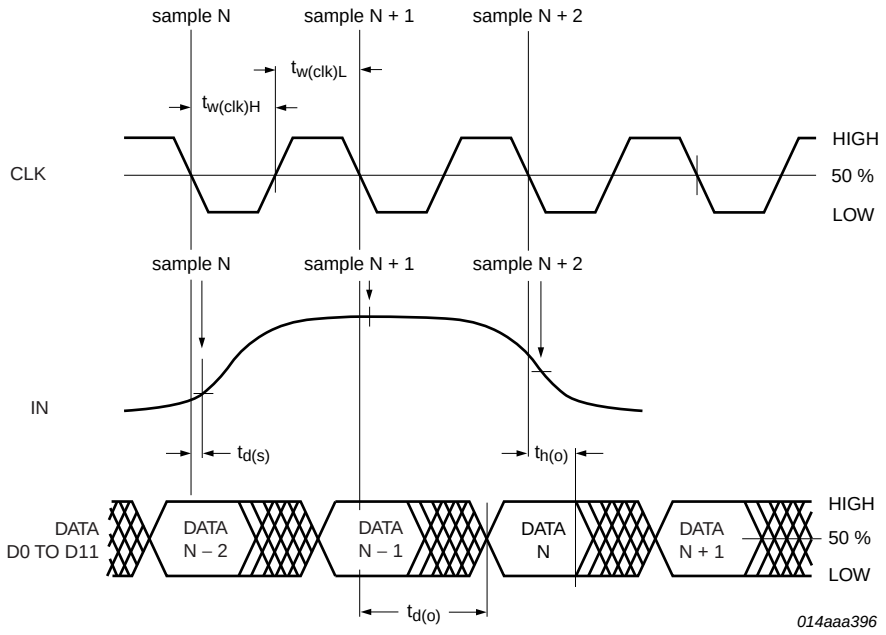
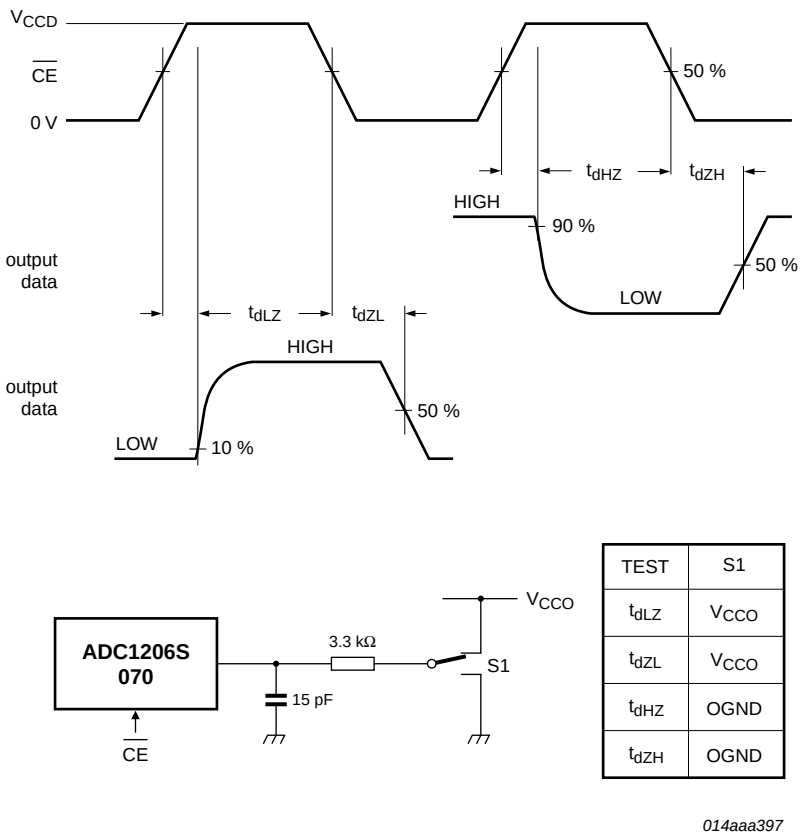


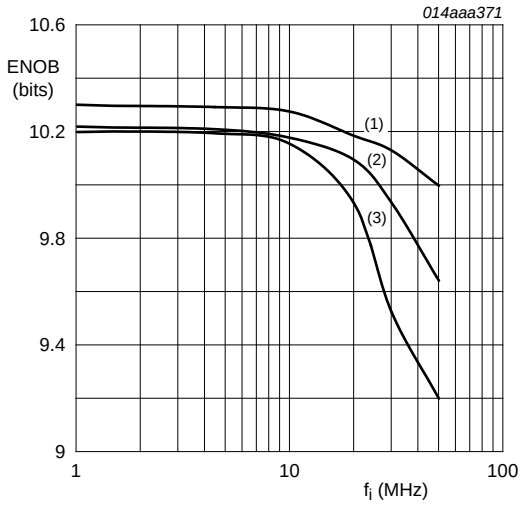
Fig 3. Timing diagram



TEST	S1
t_{dLZ}	V_{CCO}
t_{dZL}	V_{CCO}
t_{dHZ}	OGND
t_{dZH}	OGND

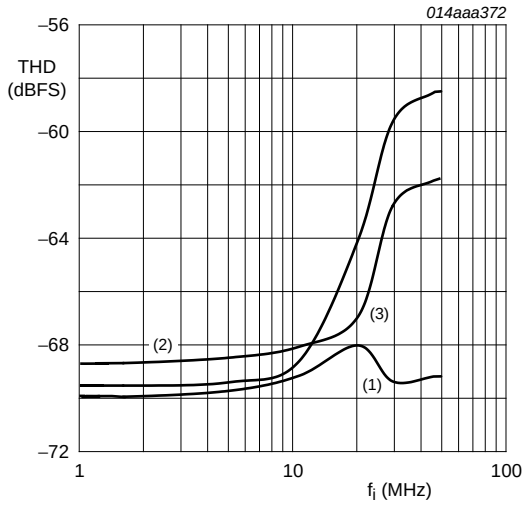
frequency on pin $\overline{CE}$ = 100 kHz

Fig 4. Timing diagram and test conditions of 3-state output delay time



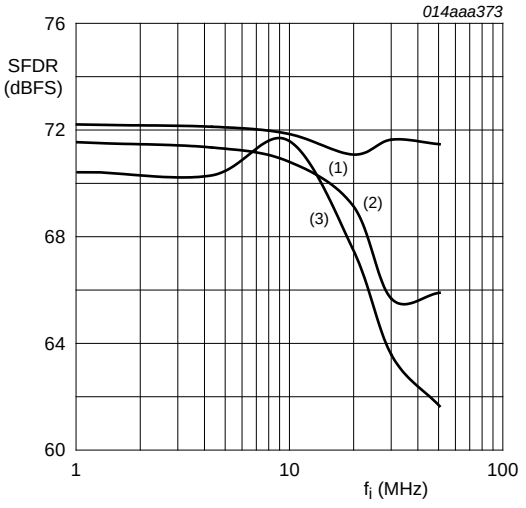
(1) 40 MHz
(2) 55 MHz
(3) 70 MHz

Fig 5. Effective Number Of Bits (ENOB) as a function of input frequency (sample device).



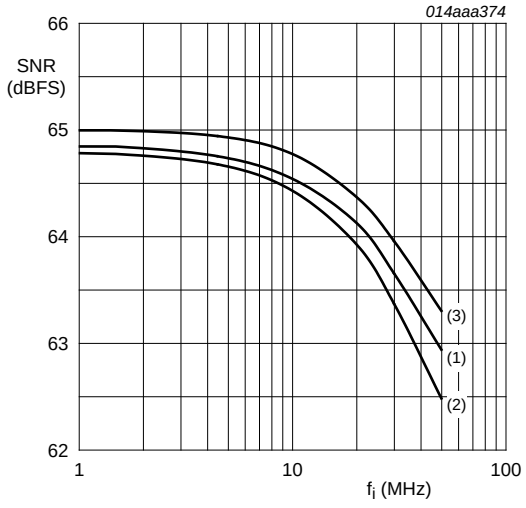
(1) 40 MHz
(2) 55 MHz
(3) 70 MHz

Fig 6. Total Harmonic Distortion (THD) as a function of input frequency (sample device).



(1) 40 MHz
(2) 55 MHz
(3) 70 MHz

Fig 7. Spurious Free Dynamic Range (SFDR) as a function of input frequency (sample device).



(1) 40 MHz
(2) 55 MHz
(3) 70 MHz

Fig 8. Signal-to-Noise ratio (S/N) as a function of input frequency (sample device).

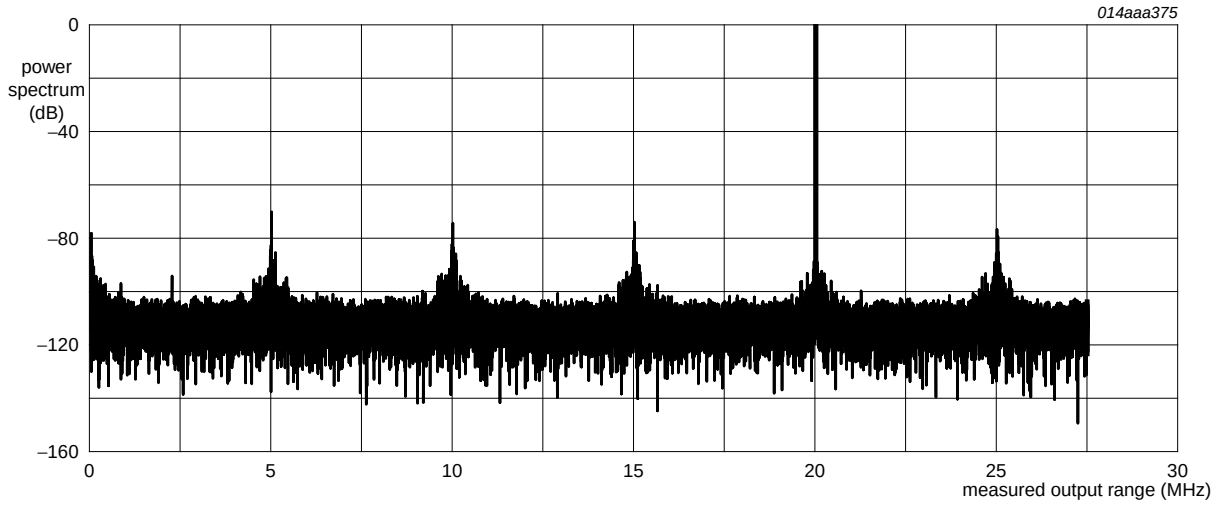


Fig 9. Single-tone; f_i = 20 MHz; f_{clk} = 55 MHz.

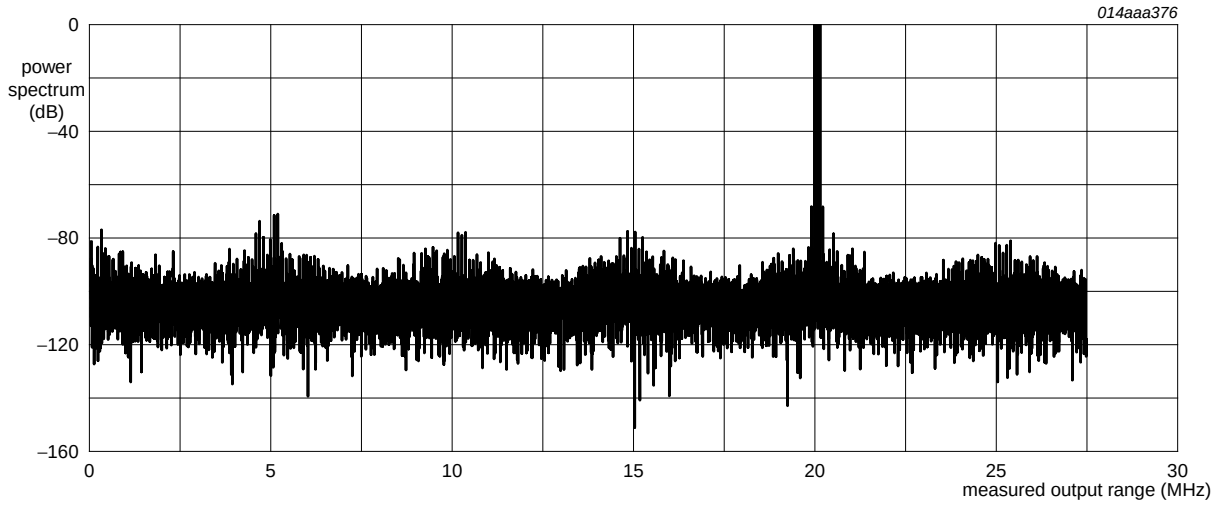


Fig 10. Two-tone; f_i 1 = 20 MHz; f_i 2 = 20.1 MHz; f_{clk} = 55 MHz.

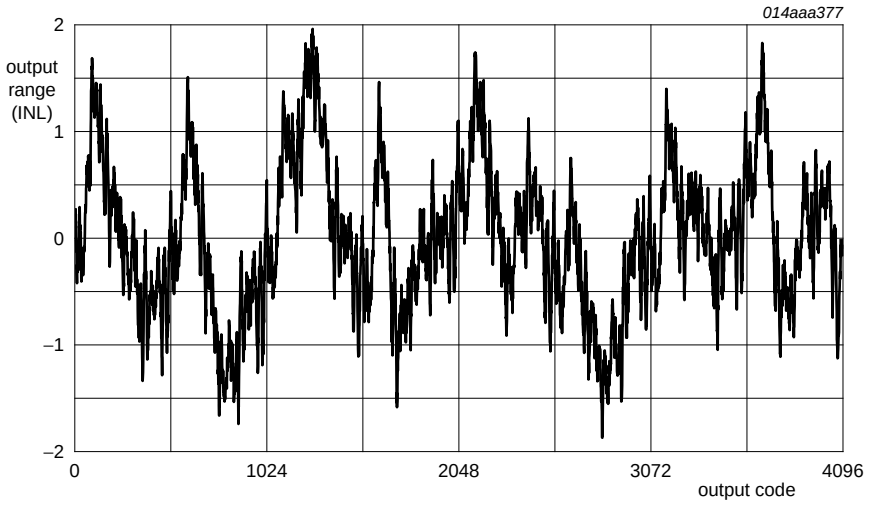


Fig 11. Integral Non-Linearity (INL)

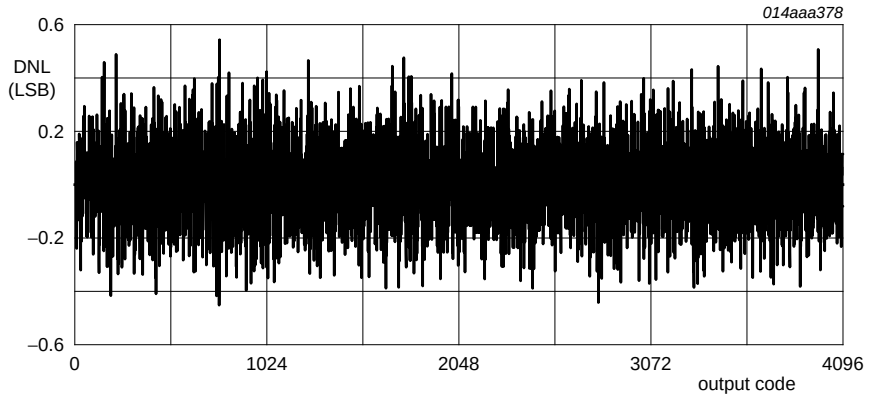
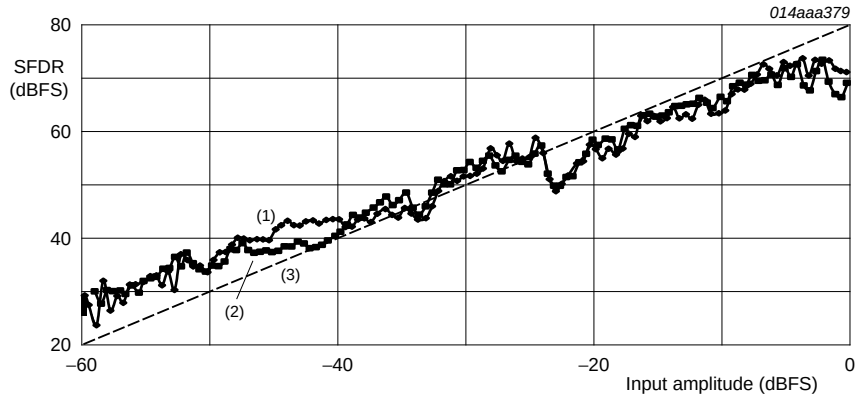


Fig 12. Differential Non-Linearity (DNL)

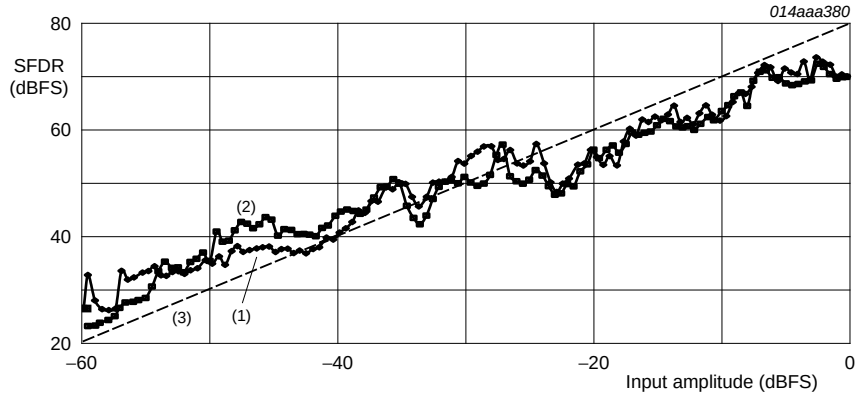


(1) f_i = 4.43 MHz

(2) f_i = 20 MHz

(3) SFDR = 80 dB

Fig 13. SFDR as a function of input amplitude; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ = 1.9 V; f_{clk} = 40 MHz

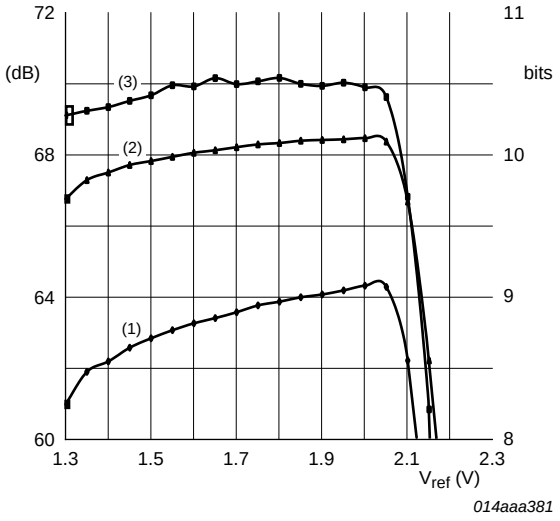


(1) f_i = 4.43 MHz

(2) f_i = 20 MHz

(3) SFDR = 80 dB

Fig 14. SFDR as a function of input amplitude; $V_{I(IN)(p-p)}$ - $V_{I(INN)(p-p)}$ = 1.9 V; f_{clk} = 55 MHz



(1) S/N

(2) ENOB

(3) SFDR

Fig 15. ENOB, SFDR and S/R as a function of V_{ref}; f_{clk} = 55 MHz; f_i = 4.43 MHz

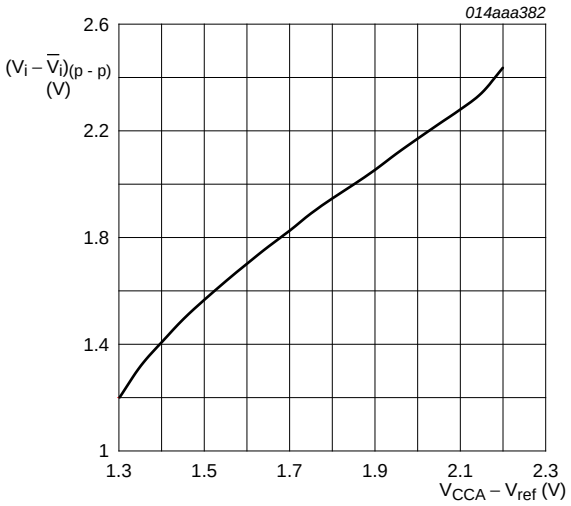
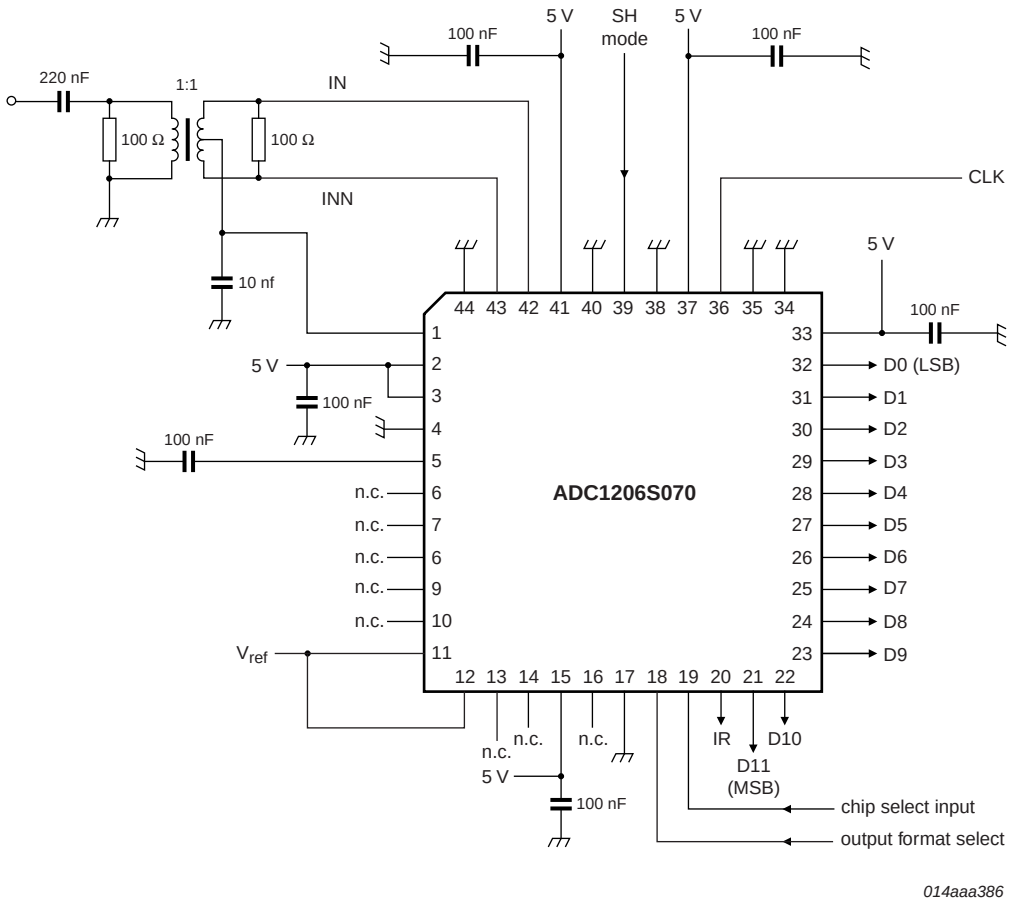


Fig 16. ADC full-scale; $V_{I(IN)(p-p)} - V_{I(INN)(p-p)}$ as a function of $V_{CCA} - V_{ref}$

12. Application information



The analog, digital and output supplies should be separated and decoupled.

Fig 17. Application diagram

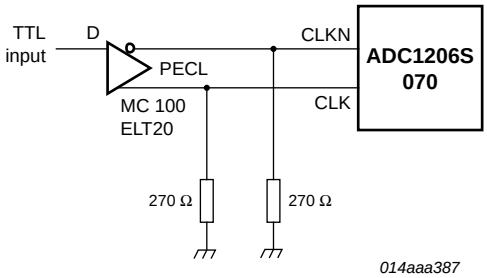


Fig 18. Application diagram for differential clock input PECL compatible using a TTL to PECL translator

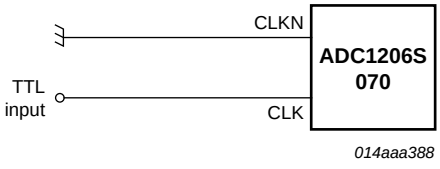
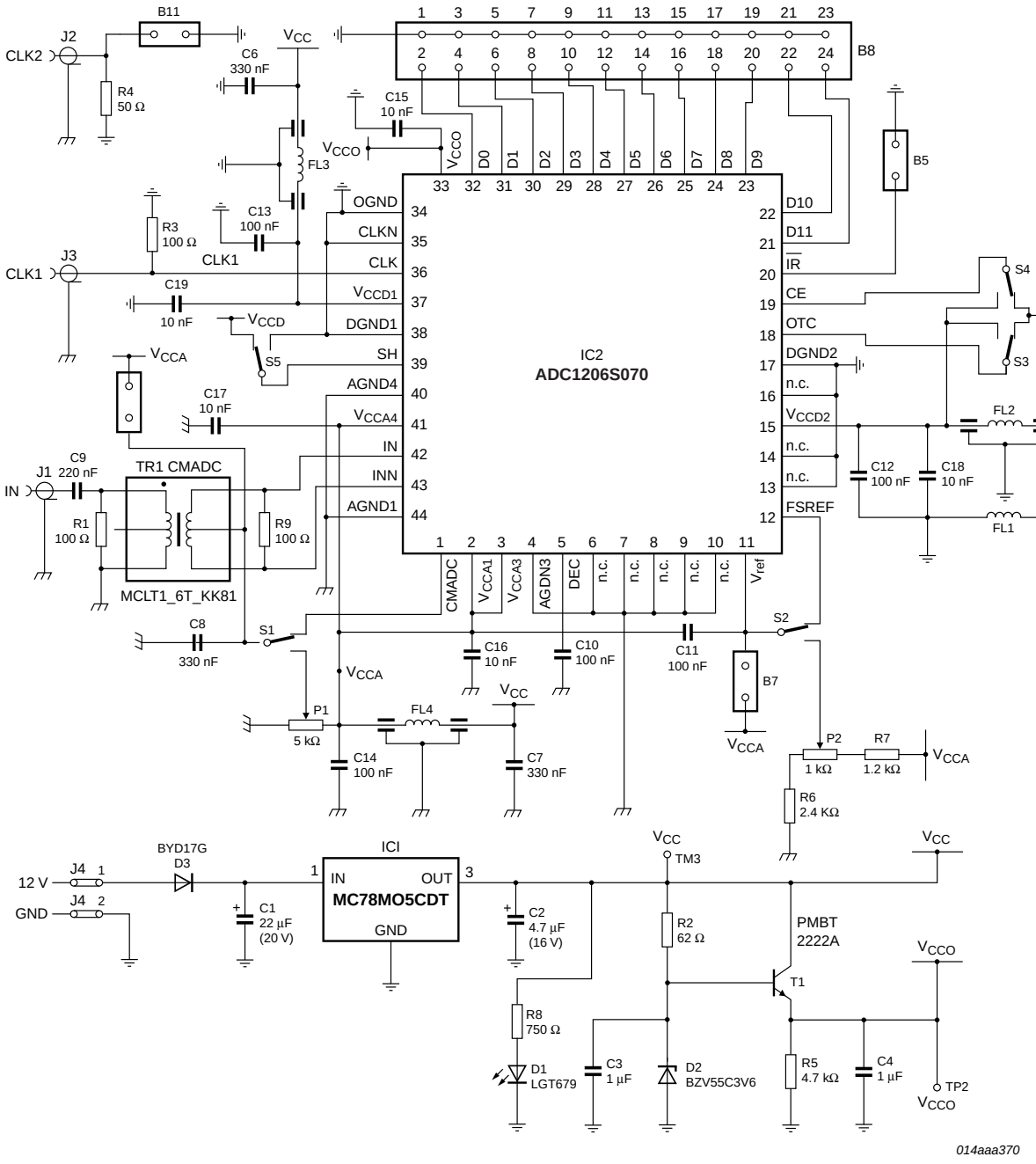


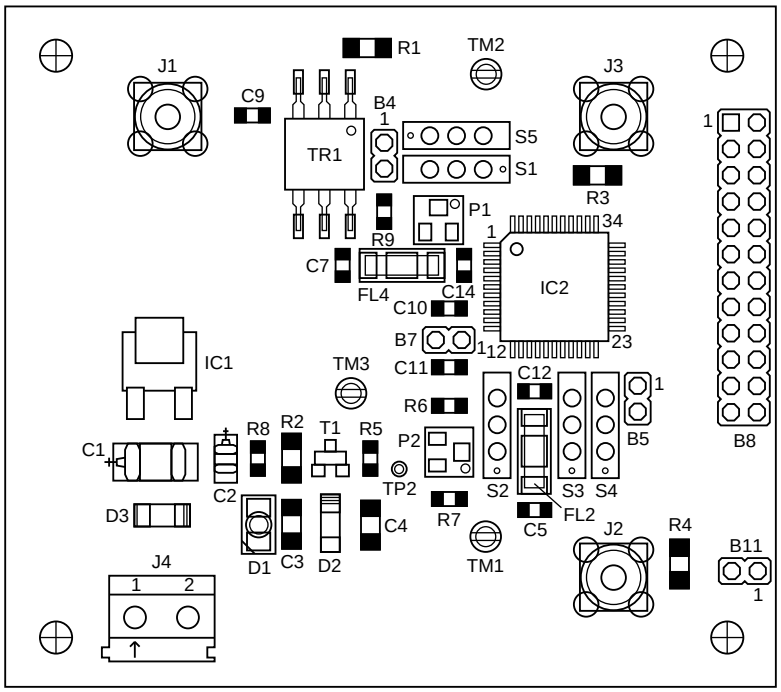
Fig 19. Application diagram for TTL single-ended clock

12.1 Demonstration board



C8 = close to TR1 pin.

Fig 20. Demonstration board schematic.



014aaa391

Fig 21. Component placement (top side).

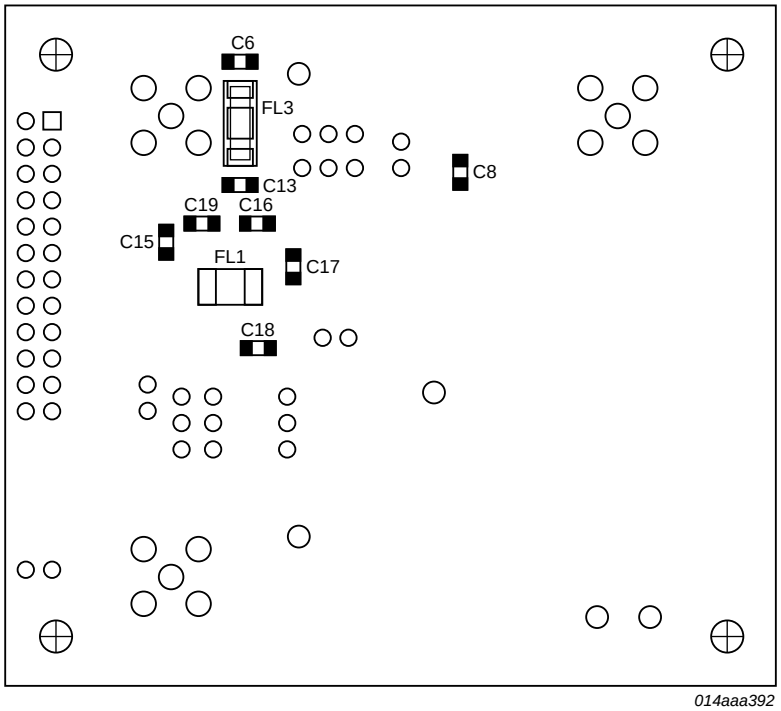


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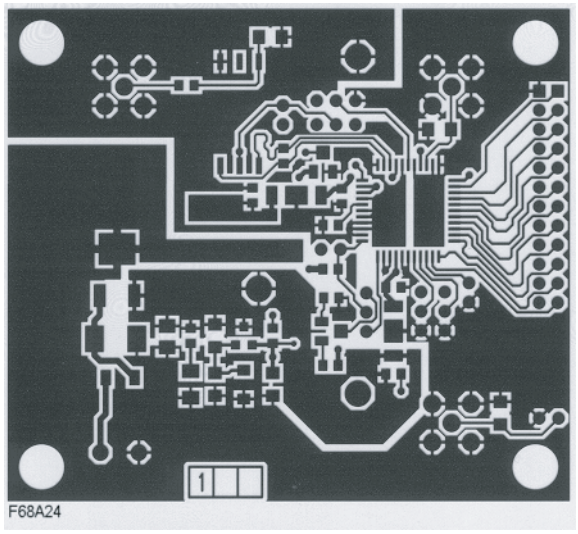
Fig 22. Component placement (underside).



014aaa393

Fig 23. PCB layout (top layer).

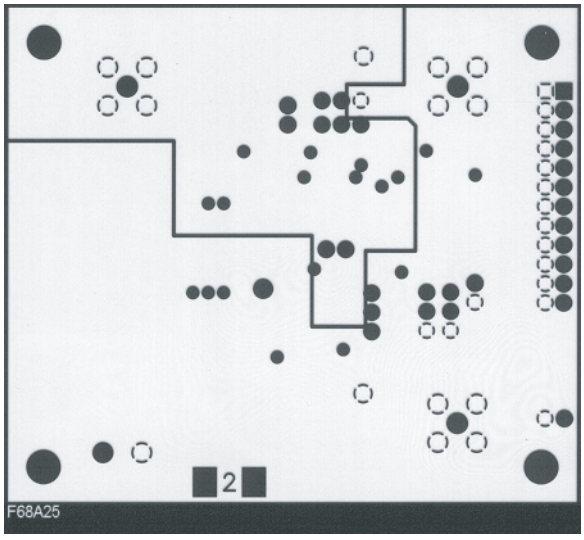


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Fig 24. PCB layout (ground layer).

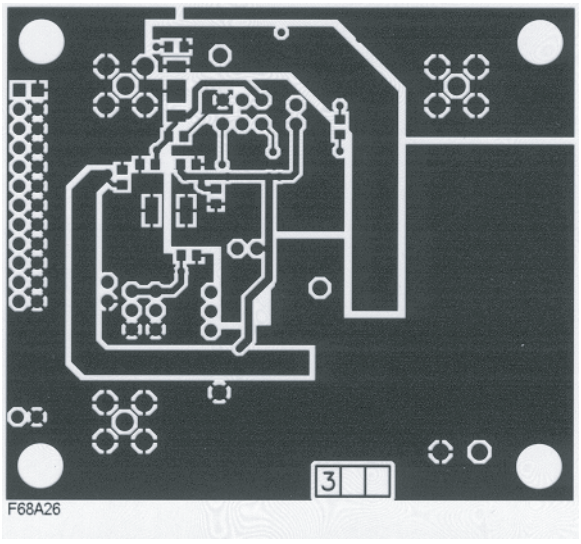

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Fig 25. PCB layout (power plane).

12.2 Alternative parts

The following alternative parts are also available:

Table 10. Alternative parts

Type number	Description		Sampling frequency
ADC1006S055	Single 10 bits ADC	[1]	55 MHz
ADC1006S070	Single 10 bits ADC	[1]	70 MHz

[1] Pin to pin compatible

12.3 Recommended companion chip

The recommended companion chip is the TDA9901 wide band differential digital controlled variable gain amplifier.

13. Support information

13.1 Non-linearities

13.1.1 Integral Non-Linearity (INL).

It is defined as the deviation of the transfer function from a best fit straight line (linear regression computation). The INL of the code i is obtained from the equation:

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S}$$

where

$i = 0 \cdot (2^n - 1)$ and

S = slope of the ideal straight line = code width; i = code value.

13.1.2 Differential Non-Linearity (DNL).

It is the deviation in code width from the value of 1 LSB. $DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S} - 1$

where $i = 0 \cdot (2^n - 2)$

13.2 Dynamic parameters (single tone)

Figure 26 shows the spectrum of a full-scale input sine wave with frequency f_t, conforming to coherent sampling (f_t/f_s = M/N, where M is the number of cycles and N is number of samples, M and N being relatively prime), and digitized by the ADC under test.

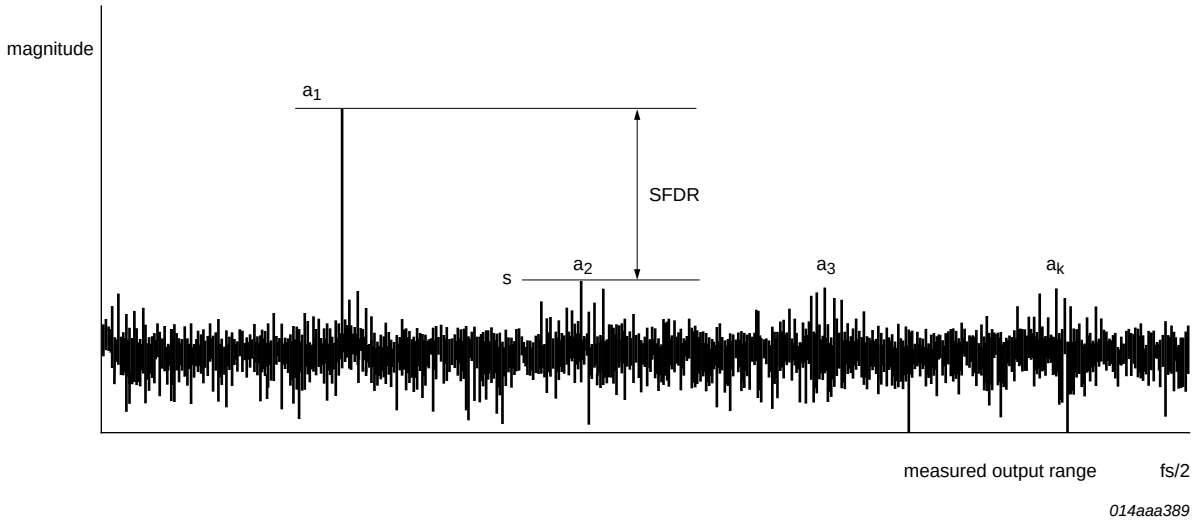


Fig 26. Spectrum of full-scale input sine wave with frequency f_t.

Remark: in the following equations, P_{noise} is the power of the terms which include the effects of random noise, non-linearities, sampling time errors, and “quantization noise”.

13.2.1 Signal-to-noise and distortion (SINAD)

The ratio of the output signal power to the noise-plus-distortion power for a given sample rate and input frequency, excluding the DC component:

$$SINAD[db] = 10log\left[\frac{P_{signal}}{P_{noise+distortion}}\right]$$

13.2.2 Effective Number Of Bits (ENOB)

It is derived from SINAD and gives the theoretical resolution an ideal ADC would require to obtain the same SINAD measured on the real ADC. A good approximation gives:

$$ENOB = (SINAD[dB] - (1 \cdot 76))/(6 \cdot 02)$$

13.2.3 Total Harmonic Distortion (THD)

The ratio of the power of the harmonics to the power of the fundamental. For k-1 harmonics the THD is: $THD[dB] = 10log\left[\frac{P_{harmonics}}{P_{signal}}\right]$

where $P_{harmonics} = \alpha|_2^2 + \alpha|_3^2 + \alpha|_k^2$

$P_{signal} = \alpha|_1^2$

The value of k is usually 6 (i.e. calculation of THD is done on the first 5 harmonics).

13.2.4 Signal-to-Noise ratio (S/N)

The ratio of the output signal power to the noise power, excluding the harmonics and the DC component. $S/N[dB] = 10log\left[\frac{P_{signal}}{P_{noise}}\right]$

13.2.5 Spurious Free Dynamic Range (SFDR)

The number SFDR specifies available signal range as the spectral distance between the amplitude of the fundamental and the amplitude of the largest spurious (harmonic and non-harmonic, excluding DC component). $SFDR[dB] = 20log\frac{\alpha_1}{max(s)}$

13.3 Intermodulation distortion

13.3.1 Spectral analysis (dual-tone)

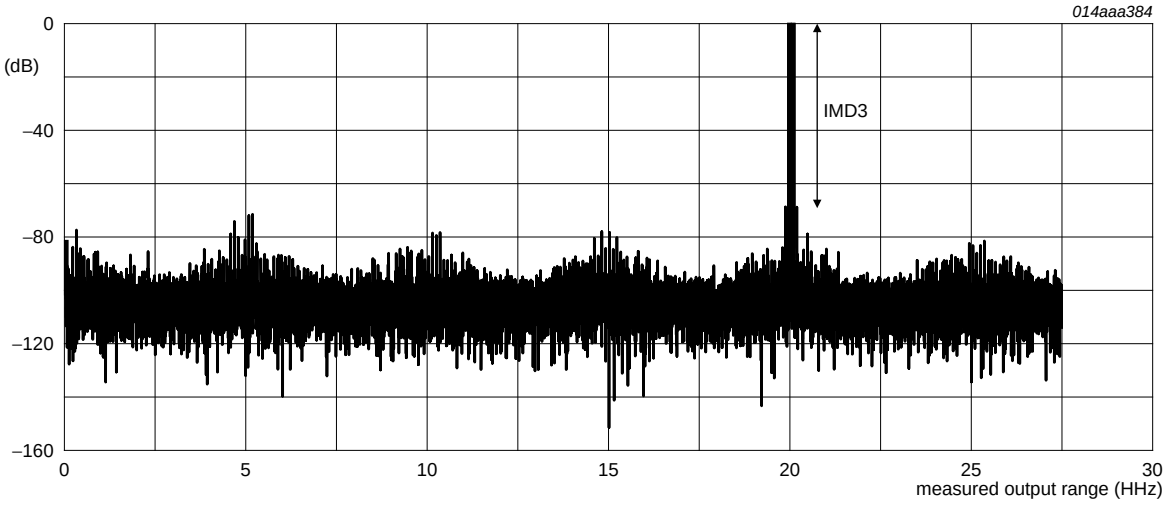


Fig 27. Spectral analysis (dual-tone)

From a dual-tone input sinusoid (f_t 1 and f_t 2, these frequencies being chosen according to the coherence criterion), the intermodulation distortion products IMD2 and IMD3 (respectively, 2nd and 3rd order components) are defined, as follows.

13.3.2 IMD2 (IMD3)

The ratio of the RMS value of either tone to the RMS value of the worst second (third) order intermodulation product.

The total intermodulation distortion IMD is given by

$$IMD[dB] = 10log\left[\frac{P_{intermod}}{P_{signal}}\right]$$

where, $P_{intermod} = \alpha|^2_{im}(f_{t1} - f_{t2}) - \alpha|^2_{im}(f_{t1} + f_{t2}) + \alpha|^2_{im}(f_{t1} - 2f_{t2}) + \alpha|^2_{im}(f_{t1} + 2f_{t2}) + \alpha|^2_{im}(2f_{t1} - f_{t2}) + \alpha|^2_{im}(2f_{t1} + f_{t2})$

$$P_{signal} = \alpha^2(f_{t1}) + \alpha^2(f_{t2})$$

and $\alpha|^2_{im}(f_t)$

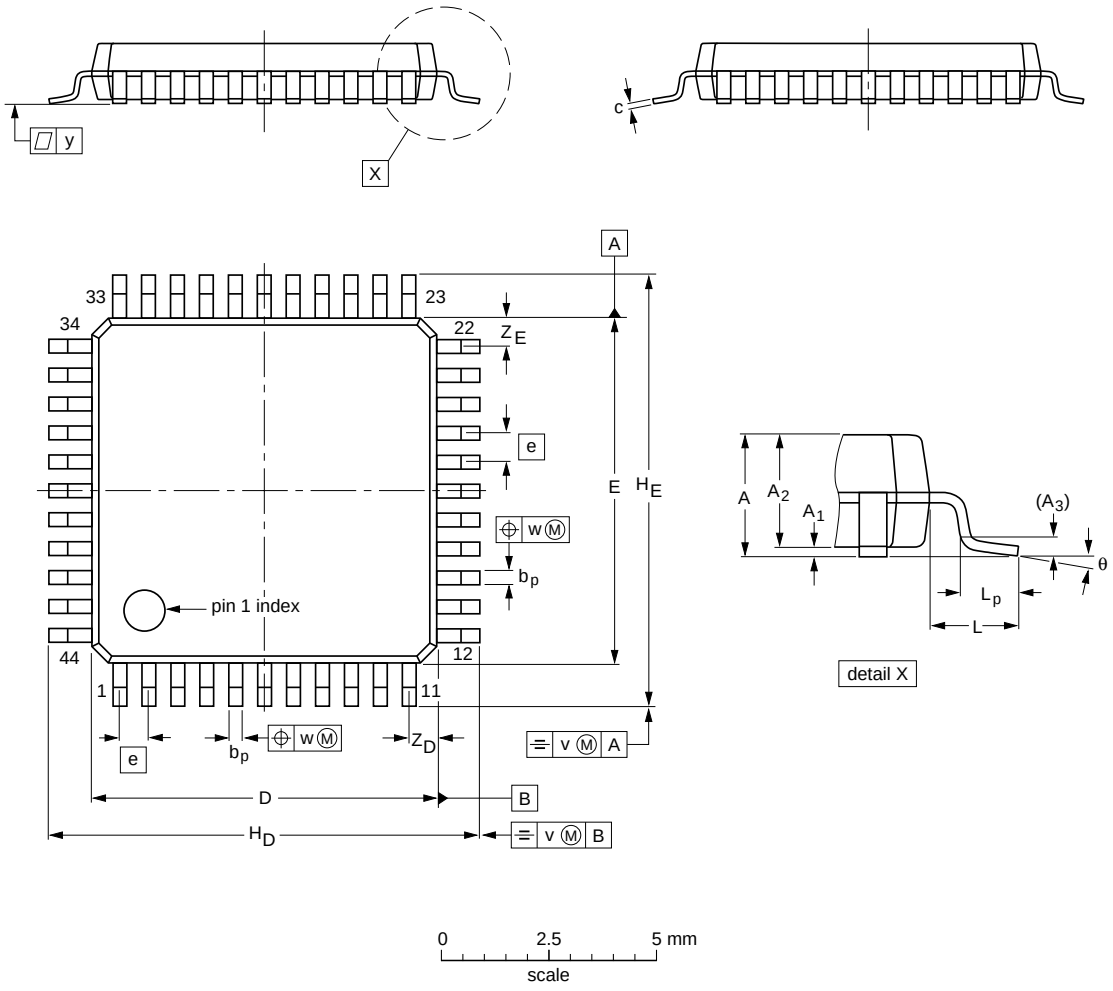
is the power in the intermodulation component at frequency f_t.

13.4 Noise Power Ratio (NPR)

When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample set.

14. Package outline

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.1	0.25 0.05	1.85 1.65	0.25	0.4 0.2	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT307-2						~~97-08-01~~ 03-02-25

Fig 28. SOT307-2 (QFP44)

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ADC1206S040_055_070_3	20120702	Product data sheet	-	ADC1206S040_055_070_2
ADC1206S040_055_070_2	20080812	Product data sheet	-	ADC1206S040_055_070_1
Modifications:	• Corrections made to DNL value in Table 1. • Corrections made to several entries in Table 6. • Corrections made to note in Figure 4.			
ADC1206S040_055_070_1	20080612	Product data sheet	-	-

16. Contact information

For more information or sales office addresses, please visit: **http://www.idt.com**

17. Contents