CCG1401 Programmable Transimpedance Amplifier

1. DESCRITPION

The CCG1401 is a universal programmable amplifier for optical sensor applications. The chip can be delivered in a QFN16 package or as a Chip Size Package (CSP) for very small PCB footprints.

2. FEATURES

- Universal amplifier for optical sensor applications
- Programmable transimpedance
- Programmable upper frequency range
- Programmable threshold voltages
- Single supply voltage
- Low current consumption
- Standby mode

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3. SCHEMATICS

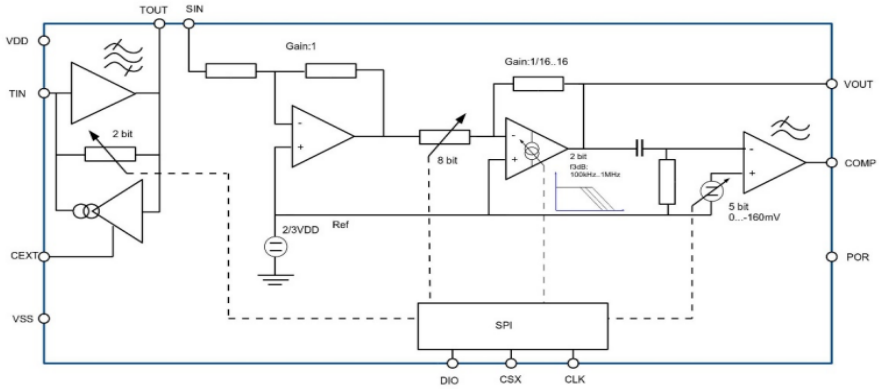
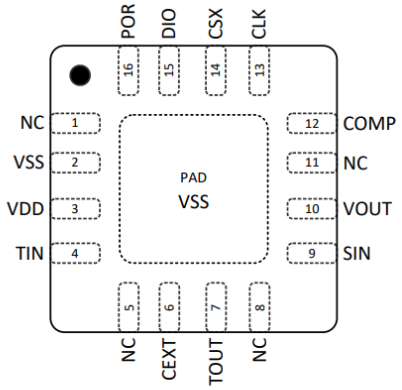


Figure 1: Block Diagram

4. PINOUT

Package QFN16



Chip Size Package

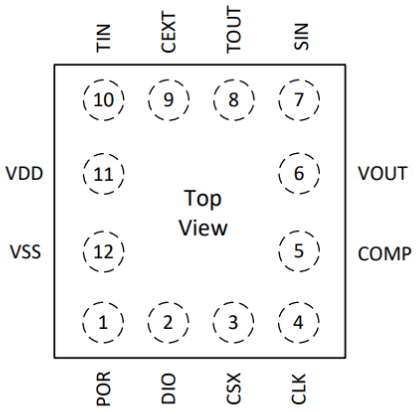


Figure 3: CCG1401 Pad configuration (CSP/Bumped Die)

PIN DESCRIPTIONS

Pin no. QFN16	Pin no. CPS	Name	Type	Function
1	-	NC	-	Not connected
2	12	VSS	PWR	Signal/PWR Ground
3	11	VDD	PWR	Power Supply
4	10	TIN	IN	Input TIA
5	-	NC	-	Not connected
6	9	CEXT	IN	External Capacitor TIA
7	8	TOUT	OUT	Output TIA
8	-	NC	-	Not connected
9	7	SIN	IN	Input SUM Amplifier
10	6	VOUT	OUT	Analog Output
11	-	NC	-	Not connected
12	5	COMP	OUT	Comparator Output
13	4	CLK	IN	Serial Interface CLOCK
14	3	CSX	IN	Serial Interface ENABLE
15	2	DIO	IN/OUT	Serial Interface DATA IN/OUT
16	1	POR	OUT	Power-ON Reset Output

Table 1: CCG1401 Pin Descriptions

5. ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are allowed for short periods of time only, otherwise product reliability degrades.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply Voltage	V_{DD}		-0.6	6	V
Total Power Dissipation	P_{TOT}	@ ϑ_{op}=125 °C		20	mW
Storage temperature range	$\vartheta_{storage}$		-55	150	ºC
Soldering Profile	$t_{soldering}$	ϑ_{sol_max}=260ºC		12	S
ESD Protection	V_{ESD}	Human Body Model JEFEC JESD22 Method A114B Class2	2		kV
Permanent current into ESD-protection diodes	I_{DC_ESD}	Only in case of forward biased ESD diodes. Input voltage above VDD or below VSS		4	mA
Reliability	MTBF	@ ϑ_{amb}=27 °C		100	FIT

Table 2: Absolute Maximum Ratings

6. ELECTRICAL CHARACTERISTICS

Electrical characteristics are valid for typical operating conditions, the whole specified temperature and supply voltage range unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating temperature range	ϑ_{op}	Ambient Temperature	-40		125	ºC
Junction temperature range	$\vartheta_{j,op}$	Junction Temperature			150	pF
Coupling capacitor between TOUT and SIN	C_{int}	Typical values are recommended. Change in value could lead to change in absolute transimpedance and bandwidth		0.32		nF
External capacitor @CEXT[1] to Ground	C_{ext}	Smaller than minimum values can lead to peaking, should be avoided. Higher than typical values will change bandwidth and transimpedance value	2	5		nF
Load resistance at COMP	R_{Load_COMP}		10			kΩ
Load capacitance at COMP	C_{Load_COMP}				200	pF
Load resistance at VOUT	R_{Load_VOUT}		4.7			kΩ
Load capacitance at VOUT	C_{Load_VOUT}				100	pF

Table 3: General Parameters

Note 1: The transimpedance amplifier has a bandpass characteristic dependent from the external capacitor Cext and operating condition. The low bandpass cut-off frequency can be calculated as follows:

$$f_c = \frac{1}{2 * \pi * I_{DC,in}{}^{-(K*\ln(M)+0.06)} * 1800 * M^{Exp} * C_{ext}}$$

With:

- I_{DC_in} Transimpedance amplifier input current (formula valid range 1µA to specified max value, see 4.3. Transimpedance Input Stage)
- K Input current exponent = 0.14
- M Transimpedance control variable
- Exp Control variable exponent = -1.2
- C_{ext} External capacitor

Power Supply

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		3		5.5	V
Current Consumption	I_{DD}	VDD=5.5V, no external load currents		2.5	3	mA
Standby current	$I_{DDstandby}$	No external load currents, CSX=CLK=High			15	µA

Table 4: Power Supply

Transimpedance Input Stage/Bandwidth Limitation

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transimpedance control	M	Adjustable in three steps: 1,8,64	1	8	64	
Transimpedance ratio tolerance	ΔM/M	Deviation of ratio from step to step; IDC_IN=3µA		3	11	%
Transimpedance	R_{T3}	M=64, T=27°C, fmeas=100kHz		210		kΩ
	R_{T2}	M=8, T=27°C, fmeas=100kHz		26		kΩ

	R_{T1}	M=1, T=27°C, fmeas=100kHz		3.3		kΩ
Tolerance of transimpedance	$\Delta R_T / R_T$	M=1, 8, 64; T=27°C	-30		30	%
Temperature coefficient	TC_{RT}			700	900	Ppm/K
Tolerance of transimpedance over I_{DC_IN}	$\Delta R_T / R_{T\_IDC}$	M=64 IDC_IN=0.1µA…100µA			5	%
Transimpedance V_{DD} drift	$\Delta R_T / R_{T\_V\ DD}$	M=1, 8, 64 $3 \le V_{DD} \le 3.3V$ $3.3 \le V_{DD} \le 5.5V$			6 1	%
Input resistance	R_{I_TIA}	Load TOUT: C=320pF and R=10kΩ in series to ground			1.7	kΩ
DC input current @ TIN	I_{DC_IN}	M=64			100	µA
		M=8			800	µA
		M=1			1500	µA
Input noise current	I_{NOISE}	200 kHz noise bandwidth, 6 dB SNR @ I_{DC_IN}=1µA			2.5	pA/√H z

Table 5: Transimpedance Input Stage / Bandwidth Limitation

Programmable Amplifier / Analog Output

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input resistance	R_{I_AMP}		7	10	13	kΩ
Gain control resolution	Gain	GA=0 minimum value		1/16		
		GA=15		1		
		GA=255 maximum value		16		
3dB cut-off frequency control	f_{AMP_3dB}	GA=255, GFA=0		100		kHz
		GA=255, GFA=1		250		kHz

		GA=255, GFA=2		500		kHz
		GA=255, GFA=3		10000		kHz
Output voltage	V_{OUT}	R_{Load_VOUT}=4.7 kΩ	0.2		4.8	V
DC output voltage	V_{OUT_DC}			$2/3V_{DD}$		
Output slew rate	SR_{OUT}	3V step at pin SIN, C_{Load_VOUT}=100pF, V_{DD}=3V GA=15, GFA=0	[0.3]			V/µs
		3V step at pin SIN, C_{Load_VOUT}=100pF, VDD=3V GA=15, GFA=1	[0.6]			V/µs
		3V step at pin SIN, C_{Load_VOUT}=100pF, VDD=3V GA=15, GFA=2	[1.2]			V/µs
		3V step at pin SIN, C_{Load_VOUT}=100pF, V_{DD}=3V GA=15, GFA=3	[2.4]			V/µs

Table 6: Programmable Amplifier / Analog output

Comparator

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input offset voltage	Voffs	3σ			±8	mV
Noise filter grade time	t_{NOISE_GATE}	Toggle input voltage over threshold, comparator output doesn't reach 0.7V	80			Ns
Low limit threshold voltage	V_{SREF}	referenced to 2/3 V_{DD}, G_{SREF}=31	-186			mV
Upper limit threshold voltage					28	

Threshold voltage deviations	ΔV_{SREF}	G_{sref}=0…31			±28	mV
Threshold voltage resolution	G_{SREF}	Linear steps		5		BIT
Threshold voltage step size	V_{SREF_step}			5.1		mV
Settling time V_{SREF}	$t_{settling}$	After asserting CSX signal (low->high; SPI communication cycle)			10	µs

Table 7: Comparator

Overall System Data

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total transimpedance (Vout / Ifoto)	R_{TT}	M=64, Gain=1/16 @ fmeas=100kHz	8.5			kΩ
		M=64, Gain=16 @ fmeas=100kHz			3500	
		M=8, Gain=1/16 @ fmeas=100kHz	1.0			
		M=8, Gain=16 @ fmeas=100kHz 430			430	
		M=1, Gain=1/16 @ fmeas=100kHz 0	0.145			
		M=1, Gain=16 @ fmeas=100kHz			54.5	
Temperature coefficient R_{TT}	TCR_{TT}				600	ppm/K
Total transimpedance V_{DD} drift	$\Delta R_{TT}/R_{TT}$	M=1, 8, 64 3≤VDD≤3.3V			2	%

		3.3≤VDD≤5.5V			1	
Settling time after overdrive input TIN	t_{set}	100 times overdrive, $\Delta V_{OUT,DC}$ / $V_{OUT,DC}$ = 1% M=1, 8, 64, GA=15		30	55	µs
Band limiting frequency	f_l	M=1, 8, 64	20		40	kHz
	f_u		170		270	kHz
Low frequency suppression	a_{100}	@100Hz	-50	-70		dB
Dead time between input and output response	t_{dead}	VDD=5V, I_{DC_IN}=10µA, G_{SREF}=0, M=1, Pulse current=25µA Monitor pin VOUT t_{dead} consists mainly of t_{prop}		1.2	2.8	µs
Switching time from standby to operation	t_{sw_01}	C_{ext} = 5nF		150	200	µs
Switching time from operation to standby	t_{sw_10}				20	µs
Start-up time	t_{start}	After reaching VDD=3V			2	ms

Table 8: Overall System Data

Power on Reset

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power-on threshold	V_{POR_on}	POR signal goes high @ V_{DD} = V_{POR_on}	2.4	2.6	2.8	V
Power-off threshold	V_{POR_off}	POR signal goes low @ V_{DD} = V_{POR_off}	2.2	2.45	2.7	V
Hysteresis	V_{POR_hyst}		100	160	230	mV

Table 9: Power ON Reset

Logic Output Comp

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low output voltage	V_{OL}	I_{OUT}=4mA, V_{DD}=3…5V No input signal			0.8	V
High output voltage	V_{OH_5V}	POR signal goes low @ $V_{DD} = V_{POR\_off}$	2.2	2.45	2.7	V
Hysteresis	V_{POR_hyst}		100	160	230	mV

Table 10: Logic Output COMP

Logic Input (DIO, CLK, CSX)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low input voltage	V_{IL_3V}	V_{DD}=3.0V			0.5	V
	V_{IL_5V}	V_{DD}=5.0V			0.8	
Low input voltage	V_{IH_3V}	V_{DD}=3.0V	1.5			V
	V_{IH_5V}	V_{DD}=5.0V	2.2			
Input capacitance	C_{in_d}				40	pF
Frequency at CLK	f_{CLK}				4	MHz

Table 11: Logic Input (DIO, CLK, CSX)

7. FUNCTION DESCRIPTION

SPI and Digital Control

A synchronous serial interface receives data from an external controller via DIO, CLK and CSX. This interface consists of a 10-bit shift register, 2-bit header and 8 bit data. Each positive slope at CLK shifts the value at DIO into the shift register. With a positive slope at CSX the 8 data bits of the shift register are transferred to the address register or a parameter register depending on the value of the header. A data package with header “00” selects a parameter register. Following data packages with header “01” are intended for the previously selected register. To read out the registers content, the header needs to be “10”. DIO changes then its functionality from input to output and DIO pin has to be released. Data can be shifted out with the positive edge of CLK. Sampling of data should occur on the negative edge. Maximum frequency when reading is 50 kHz. The output data starts with the register content at address 0, followed by the one at address 1 and ends with the content of register 4. After transfer of the last bit, when CSX goes high, DIO changes its functionality back to input behavior. The DIO-behavior is visualized by the internal signal DOUT_EN in the timing diagram. Standby modus of analog circuitry can be selected by register (see 0) and alternatively by setting CSX=High and CLK=High. The SPI is not affected by standby operation. The comparator threshold can be controlled by register content and setting DIO=High for using the register SREF1 (see 5.4.4) or setting DIO=Low for using register SREF2 (see 5.4.5). Take into consideration that this mechanism does not work during an SPI-transfer.

SPI Timing

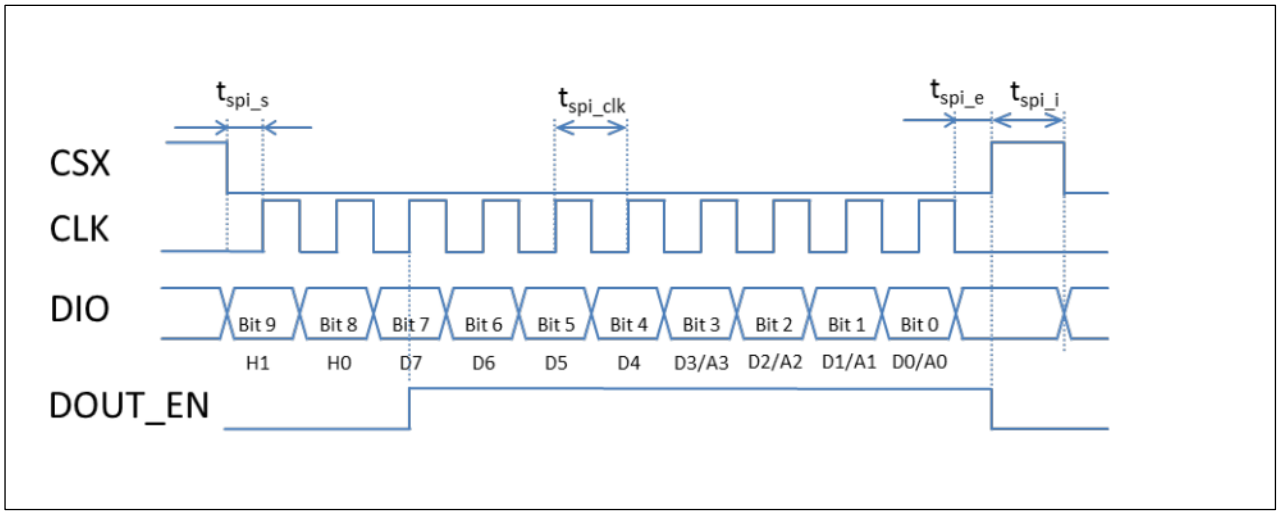


Figure 4: Timing Diagram

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SPI Clock Frequency	f_{SPI}				4	MHz
SPI Clock Period	t_{SPI_CLK}		250			ns
SPI Start Clock after select	t_{SPI_S}		125			ns
SPI End of Select after Clock	t_{SPI_E}		125			ns
SPI Idle between Access	t_{SPI_I}		250			ns

Table 12: SPI Timing

After Power-on all register defaults are in logical state “High”, except CIRC_DIS in CTRL-register (see 0).

SPI Protocol

10 bit shift register: 2 bit header, 8 bit data/address

Bit	9	8	7	6	5	4	3	2	1	0
Denotation	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
Message type 0 (SPI-Write address)	‘0’	‘0’	-	-	-	-	A3	A2	A1	A0
Message type 1 (SPI-Write address)	‘0’	‘1’	D7	D6	D5	D4	D3	D2	D1	D0
Message type 2 (SPI-Read data)	‘1’	‘0’	D7	D6	D5	D4	D3	D2	D1	D0

Register Descriptions

Register Definitions

0x1	Gain
0x2	SREF1
0x3	SREF2
0x4	CTRL

Table 13: Register Definitions

TIA- Transimpedance Register

Bit	7 : 2	1 : 0
Name	-	TI
Reset	0xFF	

Table 14: TIA

Address: 0x1

GA Programmable amplifier gain adjustment

Gain = (GA+1)/16
0d: Gain = 1/16
15d: Gain = 1
255d: Gain = 16 (default)

GAIN - Programmable Gain Register

Bit	7 : 0
Name	GA
Reset	0xFF

Table 15: GAIN

Address: 0x1

GA Programmable amplifier gain adjustment

Gain = (GA+1)/16
0d: Gain = 1/16
15d: Gain = 1
255d: Gain = 16 (default)

SREF1- Programmable threshold voltage Register #1

Bit	7 : 5	4 : 0
Name	-	SREF1
Reset	0xFF	

Table 16: SREF1

Address: 0x2

SREF1 Comparator threshold voltage 1

Defines the comparator threshold voltage referenced to 2/3 VDD
Vsref ≈ SREF1 * -5.1mV
DIO = high

SREF2- Programmable threshold voltage Register #2

Bit	7 : 5	4 : 0
Name	-	SREF2
Reset	0xFF	

Table 17: SREF2

Address: 0x3

SREF1 Comparator threshold voltage 2

Defines the comparator threshold voltage referenced to 2/3 VDD
Vsref ≈ SREF2 * -5.1mV
DIO = low

CTRL – General Control Register

Bit	7	6	5 : 2	1 : 0
Name	COMP_DIS	CIRC_DIS	-	GFA
Reset	0xBF (0b10111111)			

Table 18: CTRL

Address: 0x4

GFA Programmable summing amplifier 3dB frequency control adjustment

0d -> GFA=0
1d -> GFA=1
2d -> GFA=2
3d -> GFA=3

CIRC_DIS Circuit disable (standby mode)

0d -> circuit is enabled (This is the default value! Keep in mind that this is the only bit that is initialized with ‘0’)
1d -> circuit is disabled

COMP_DIS Comparator output disable

0d -> comparator output is enabled
1d -> comparator output is disabled

8. APPLICATION NOTES

Application with Photodiode Sensor

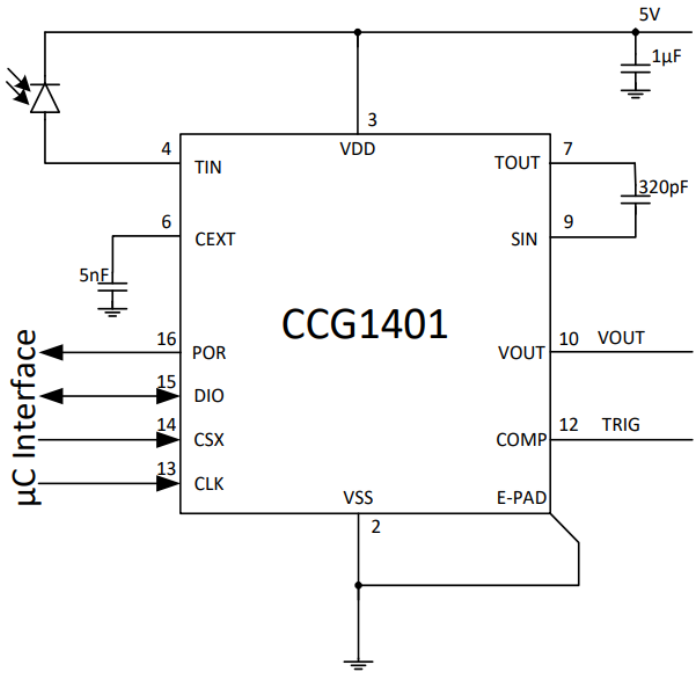
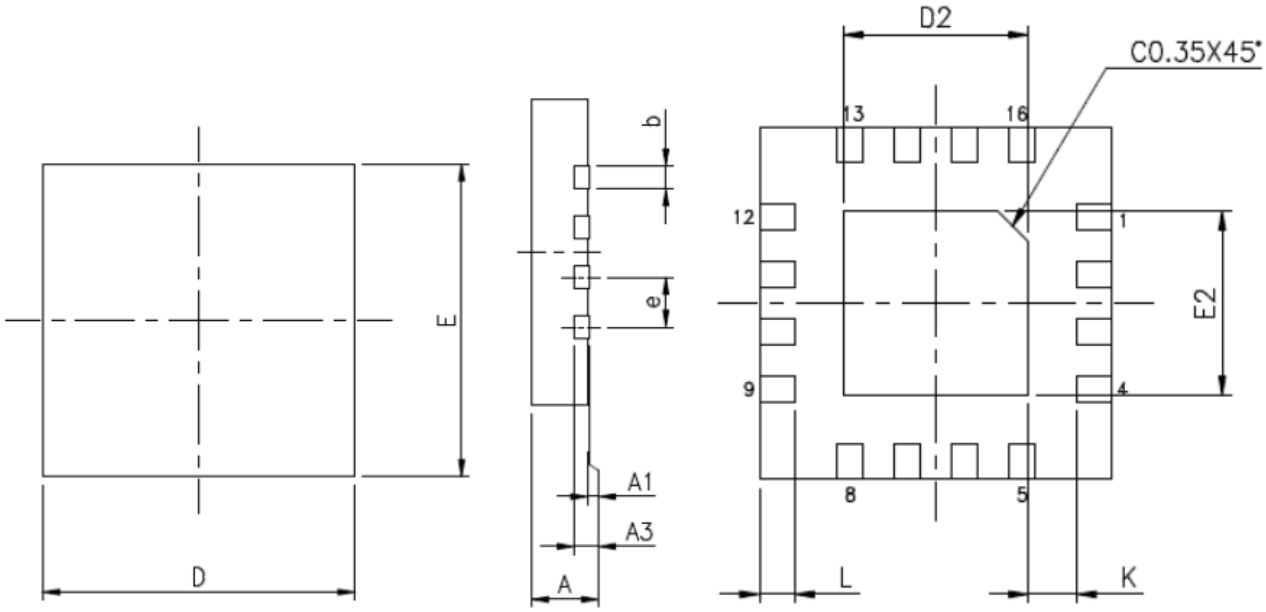


Figure 4: Optical Application

9. PACKAGE OUTLINE

QFN16 Package



Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
Min	0.70	0.00	0.20 REF.	0.25	4.00 BSC	4.00 BSC	0.65 BSC.	0.35	0.20	2.00	2.00
Nom.	0.75	0.02		0.30				0.40	-	2.10	2.10
Max	0.80	0.05		0.35				0.45	-	2.20	2.20

UNIT : mm

NOTES :

1. JEDEC OUTLINE : N/A.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 5: QFN16 Package

CSP 12 Package

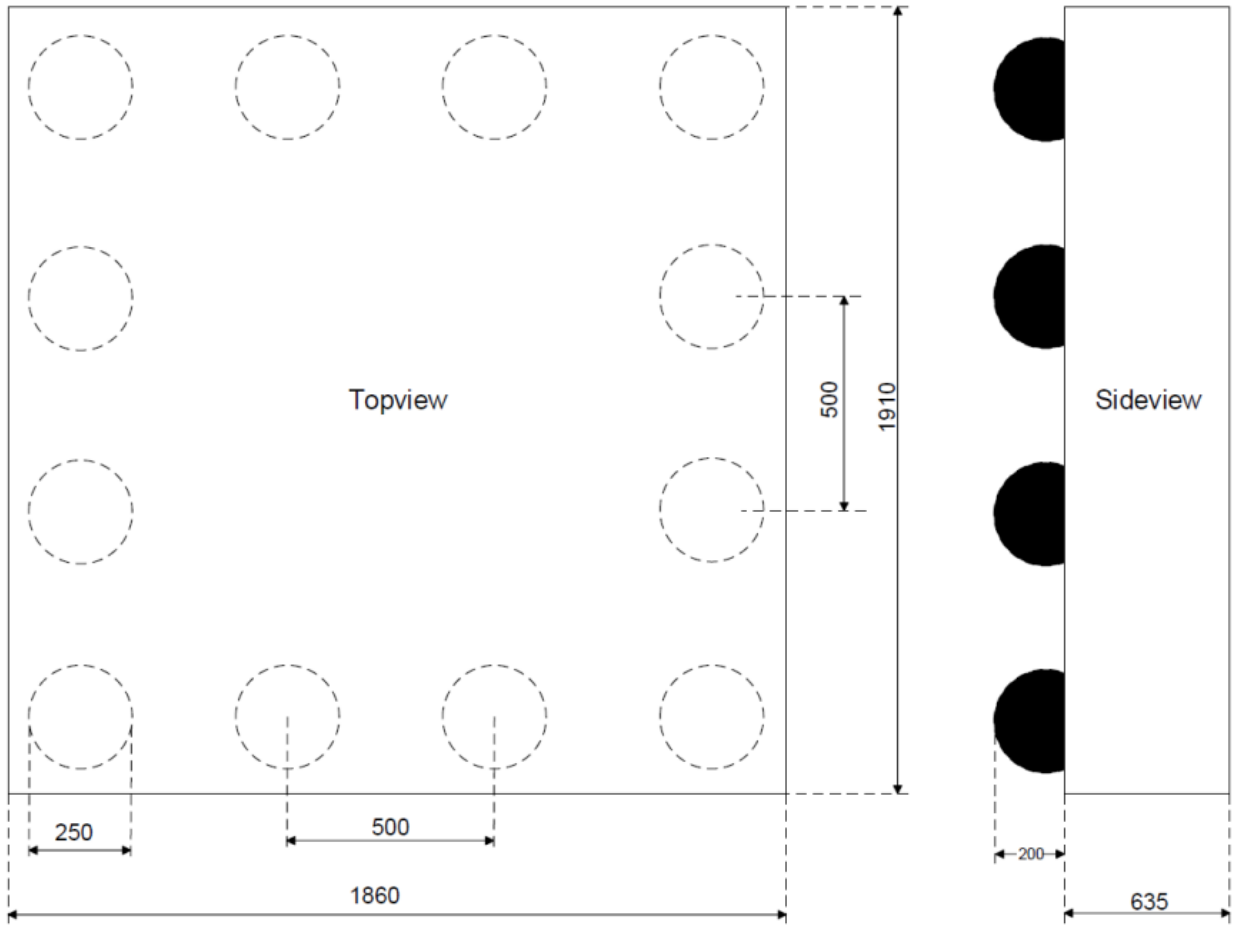
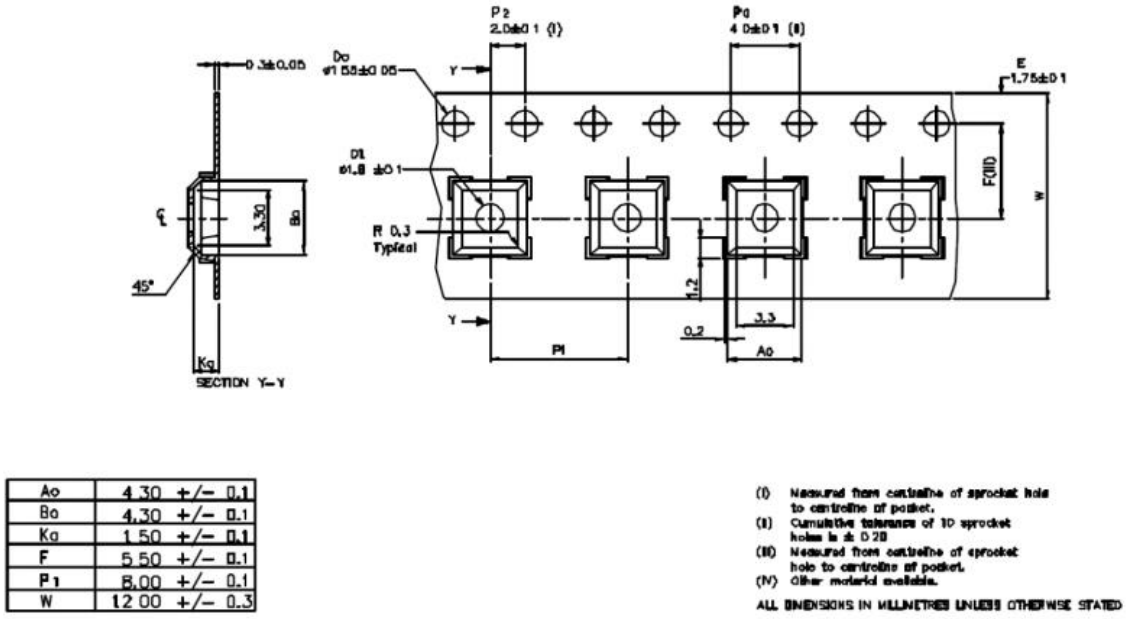


Figure 6: CSP12 Package

10. TAPE AND REEL INFORMATION

Tape QFN16 Package



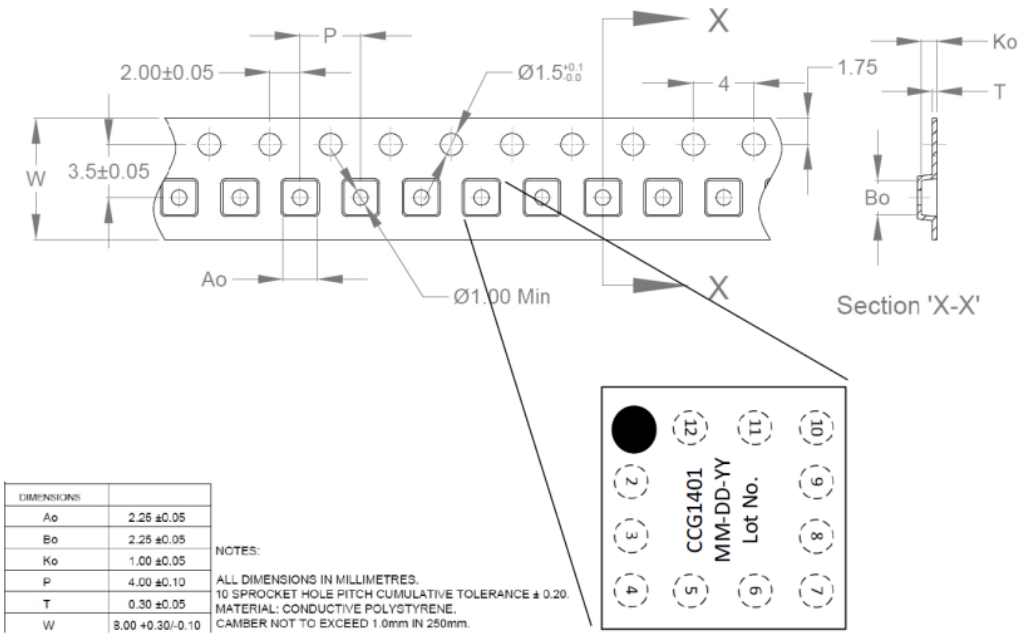
Ao	4.30 +/- 0.1
Bo	4.30 +/- 0.1
Ko	1.50 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Figure 7: QFN16 Tape Dimensions

Tape CSP Package

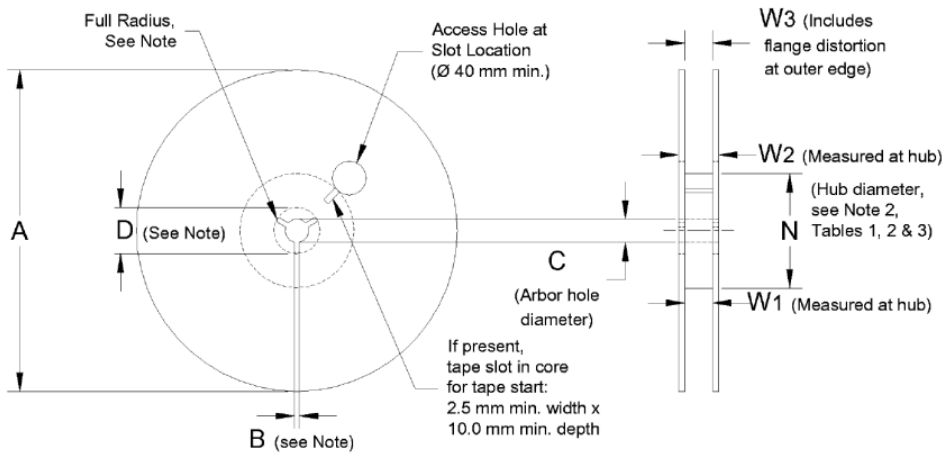


DIMENSIONS	
Ao	2.26 ±0.05
Bo	2.25 ±0.05
Ko	1.00 ±0.05
P	4.00 ±0.10
T	0.30 ±0.05
W	8.00 +0.30/-0.10

NOTES:
ALL DIMENSIONS IN MILLIMETRES.
10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.20.
MATERIAL: CONDUCTIVE POLYSTYRENE.
CAMBER NOT TO EXCEED 1.0mm IN 250mm.

Figure 8: CSP Tape Dimensions

Reel Information QFN16

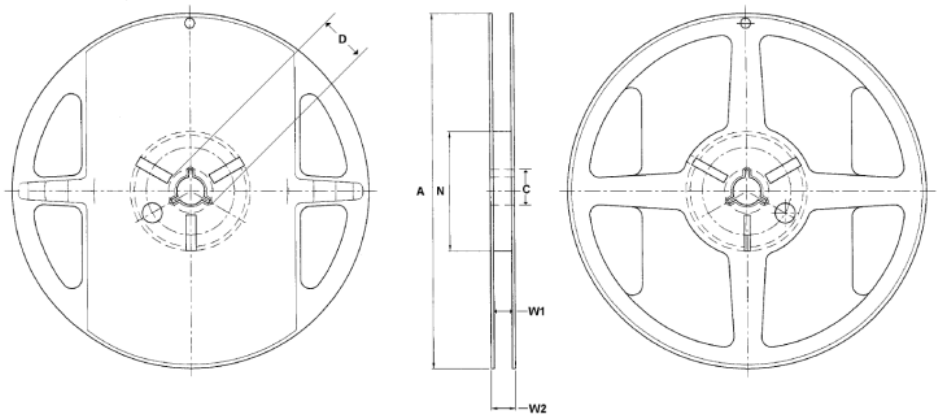


Note: Drive spokes optional; if used, dimensions B and D shall apply.

Symbol	A	B	C	D	W_1 QFN16
Min	-	1.5	12.8	20.2	13.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	13.75

Figure 9: Reel Dimensions QFN16

Reel Information CSP



Tape Width	A Diameter	C	D (min)	N Hub	W1	W2 (max)
8	178	13.5	20.2	60	9	11.5
	+/- 1.0	+/-0.5		+0.1 -0.0	+/- 0.5	

Figure 10: Reel Dimensions CSP

11. ORDERING INFORMATION

Part	Order No.	Package	Delivery	Quantity
CCG1401	CCG1401_QFN16	QFN16	Tape & Reel	5,000 per reel
CCG1401	CCG1401_CSP	CSP	Tape & Reel	3,000 per reel

Table 19: Ordering Information

12. REVISION HISTORY

Revision	Date	Description
2.5	21-Feb-2022	Rebrand
2.4	31-Oct-2019	Updated template
2.3	07-Feb-2018	Added CSP outline and tape, reel drawing CSP
2.2	03-Apr-2017	Updated document number
2.1	13-Oct-2016	Correct Pinning in 2.1-2.3 and QFN pitch 0.65 Introduction of Start-up time (4.6) Fix condition for switch time operation – standby Changed description of (TI) transimpedance gain default value Fixed description for summing amplifier gain (GFA)

(Rev.5.0-1 October 2020

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

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