DA16200

Ultra-Low-Power Wi-Fi SoC

General Description

The DA16200 is a highly integrated ultra-low-power Wi-Fi® system on a chip (SoC), which contains an 802.11b/g/n radio (PHY), a baseband processor, a media access controller (MAC), on-chip memory, and a host networking application processor, all on a single silicon die.

The SoC enables full offload capabilities, running the entire networking stack on chip so that no external network processor, CPU, or microcontroller is required, while many other SoCs optionally use a microcontroller.

The DA16200 is a synthesis of breakthrough ultra-low power technologies that enables extremely low power operation in the SoC. The DA16200 shuts down every micro element of the chip that is not in use, which allows a near zero level of power consumption when not actively transmitting or receiving data. Such low power operation can extend the battery life up to a year or more depending on the application. The DA16200 also enables ultra-low power transmitting and receiving modes when the SoC needs to be awake to exchange information with other devices. Advanced algorithms enable staying asleep until the exact moment required to wake up to transmit or receive.

The SoC is built from the ground up for the Internet of Things (IoT) and is ideal for door locks, thermostats, sensors, pet trackers, asset trackers, sprinkler systems, connected lighting, video cameras, video doorbells, wearables, and other IoT devices.

Key Features

- Highly integrated ultra-low-power Wi-Fi® system on chip
- Full offload: SoC runs full networking OS and TCP/IP stack
- Wi-Fi processor
- IEEE 802.11b/g/n, 1×1, 20 MHz channel bandwidth, 2.4 GHz
- On-chip PA, LNA, and RF switch
- Wi-Fi security: WPA/WPA2-Enterprise/Personal, WPA2 SI, WPA3 SAE, and OWE
- Vendor EAP types: EAP-TTLS/MSCHAPv2, PEAPv0/EAP-MSCHAPv2, PEAPv1, EAP-FAST, and EAP-TLS
- Operating modes: Station and Soft AP
- WPS-PIN/PBC for easy Wi-Fi provisioning
- Connection manager for autonomous and fast Wi-Fi connections
- Bluetooth coexistence
- Antenna switching diversity
- Built-in 4-channel auxiliary ADC for sensor interfaces
- 12-bit SAR ADC: single-ended four channels
- Direct code execution from the external serial flash memory (XIP)
- Hardware accelerators
- General hardware CRC engine
- Hardware zeroing function for fast booting
- Pseudo random number generator (PRNG)
- Complete software stack
- Comprehensive networking software stack
- Provides TCP/IP stack in the form of network socket APIs
- Advanced security
- Secure booting
- Secure debugging using JTAG/SWD and UART ports
- Secure asset storage
- Built-in hardware crypto engines for advanced security
- TLS/DTLS security protocol functions
- Crypto engine for key deliberate generic security functions: AES (128,192,256), DES/3DES, SHA1/224/256, RSA, DH, ECC, CHACHA, and TRNGProvides dynamic auto switching function
- Support various interfaces
- eMMC/SD expanded memory
- SDIO Host/Slave function
- QSPI for external flash control
- Three UARTs
- SPI Master/Slave interface
- I2C Master/Slave interface
- I2S for digital audio streaming
- 4-channel PWM

- Individually programmable, multiplexed GPIO pins
- JTAG and SWD
- Wi-Fi Alliance® certifications:
- Wi-Fi CERTIFIED™ b/g/n
- WPA™ - Enterprise, Personal
- WPA2™ - Enterprise, Personal
- WPA3™ - Enterprise, Personal
- Wi-Fi Enhanced Open™
- WMM
- WMM - Power Save
- Wi-Fi Protected Setup™
- CPU core subsystem
- Arm® Cortex®-M4F core w/clock frequency of 30~160 MHz
- ROM: 256 kB
- SRAM: 512 kB
- OTP: 2 kB
- Retention Memory: 48 kB
- Power management unit
- On-Chip RTC
- Wake-up control of fast booting or full booting with minimal initialization time
- Integrated DC-DC and LDOs
- Supports three ultra-low-power Sleep modes
- Clock source
- 40 MHz crystal (± 20 ppm) for master clock (initial + temp + aging)
- 32.768 kHz crystal (± 250 ppm) for RTC clock
- Integrated 32 kHz RC oscillator
- Supply
- Single operating voltage: 2.1 V to 3.6 V (typical: 3.3 V)
- Digital I/O Supply Voltage: 1.8 V/3.3 V
- Blackout and brownout detector
- Package type
- 6 mm × 6 mm, 0.4 mm pitch, 48-Pin, QFN
- 3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP
- Operating temperature range
- -40 °C to 85 °C

Applications

- Security systems
- Door locks
- Thermostats
- Garage door openers
- Blinds
- Lighting control
- Sprinkler systems
- Video camera security systems
- Smart appliances
- Video doorbell
- Asset tracker

System Diagram

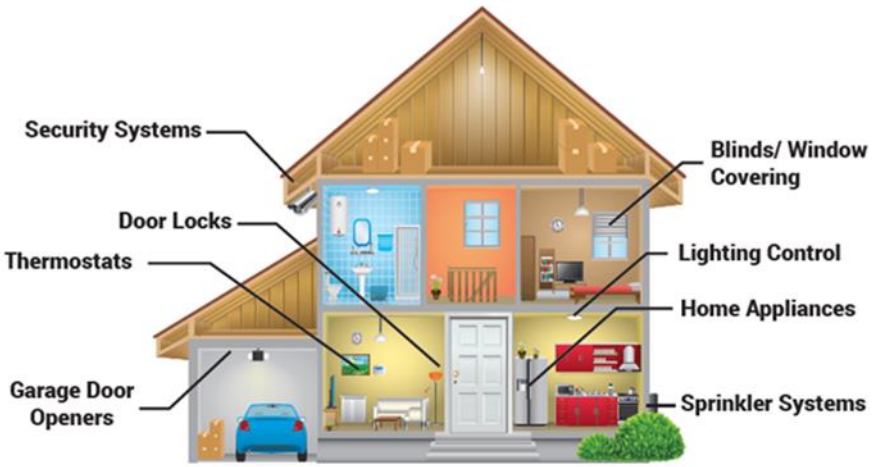

Figure 1. System diagram

Contents

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Tables

1. Terms and Definitions

API	Application Programming Interface
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IoT	Internet of Things
JTAG	Joint Test Action Group
LDO	Low-Dropout Regulator
LLI	Linked-List Item
NVIC	Nested Vectored Interrupt Controller
NVRAM	Non-Volatile RAM
PLL	Phase-Locked Loop
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
QSPI	Quad-Lane SPI
RTC	Real-Time Clock
RWC	Read Wait Control
MRC	Maximum Ratio Combining
MSL	Moisture Sensitivity Level
SAR ADC	Successive Approximation Analog-to-Digital Converter
SPI	Serial Peripheral Interface
SRAM	Static Random-Access Memory
SW	Software
SWD	Serial Wire Debug
TAP	Test Access Port
UART	Universal Asynchronous Receivers and Transmitter
XIP	eXecute in Place

2. References

[1] ARM® Cortex®-M4 Processor Technical Reference Manual.

[2] UM-WI-046, DA16200 DA16600 FreeRTOS SDK Programmer Guide, User Manual, Renesas Electronics.

[3] ITU-T O.150, General Requirements for Instrumentation for Performance Measurements on Digital Transmission Equipment, 1996.

[4] Arm TrustZone® CryptoCell-312, Software Integrators Manual, Revision r1p1.

[5] IEEE Standard 1149.1, Test Access Port and Boundary-Scan Architecture.

[6] AMBA AHB Bus Specification, Revision 3.0. (https://developer.arm.com/documentation/ihi0033/bb)

Note 1 References are for the latest published version, unless otherwise indicated.

3. Block Diagram

Figure 2 shows the DA16200 hardware block diagram.

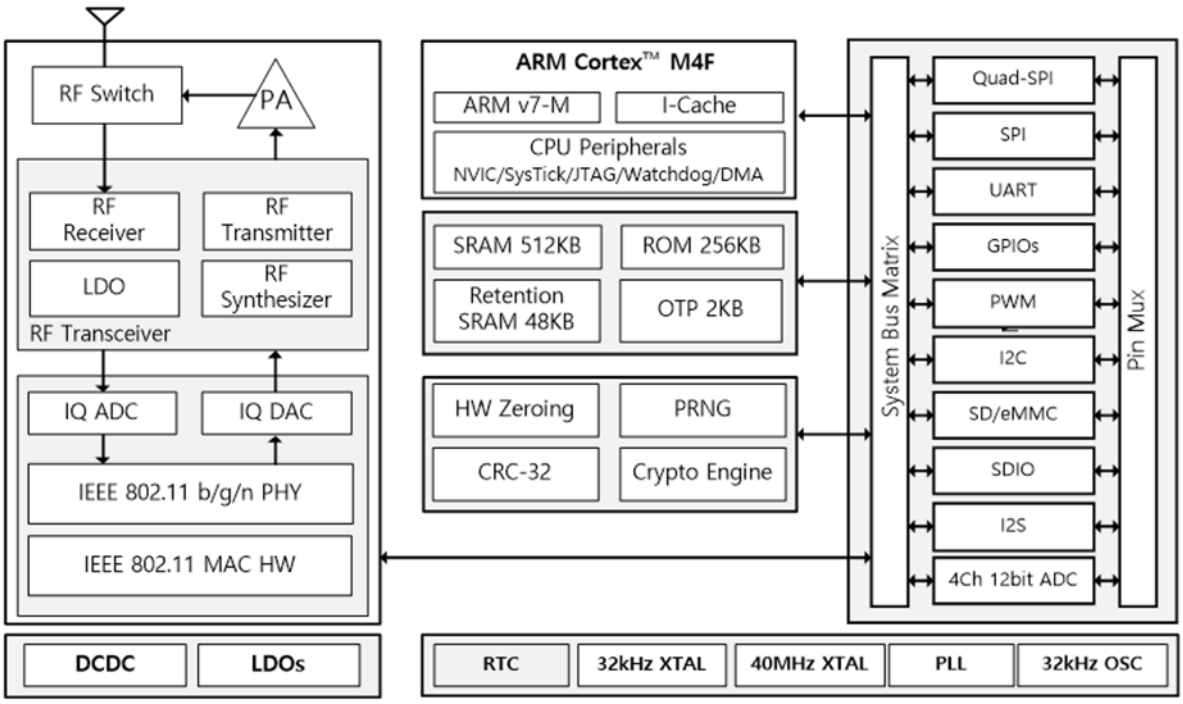

Figure 2. Hardware block diagram

Figure 3 shows the DA16200 software block diagram.

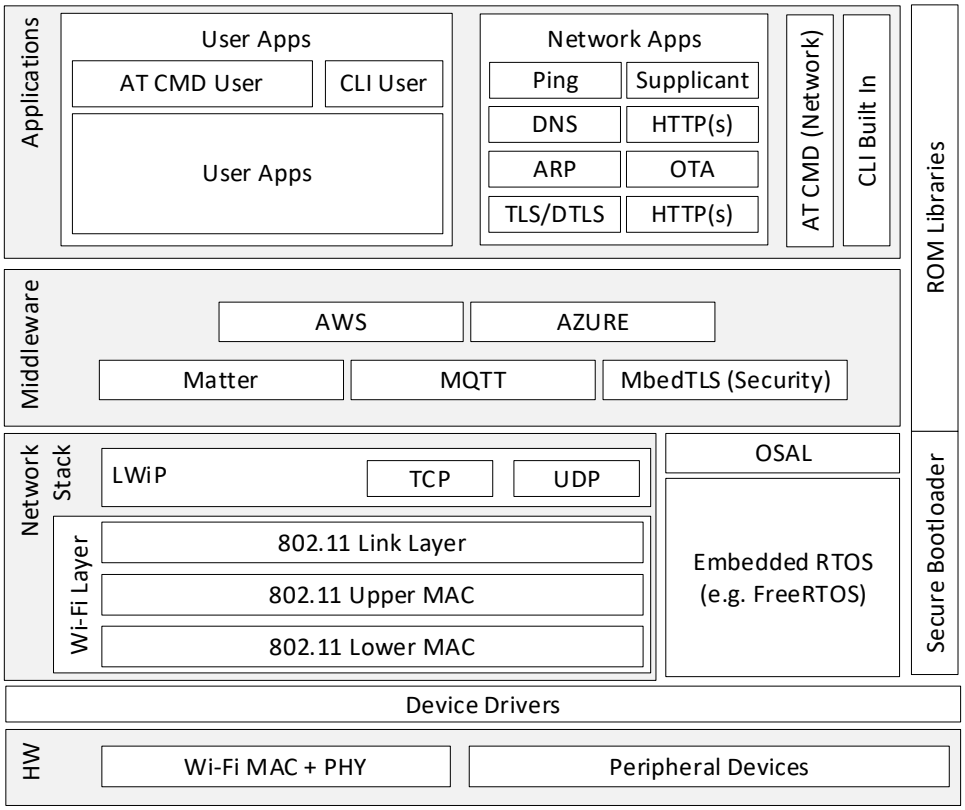

Figure 3. Software block diagram

The following descriptions are about the software block diagram:

- Kernel layer
  - Real Time Operating System
- The Network Stack layer is divided into four layers:
  - Lower MAC
    - Software module to control/handle hardware Wi-Fi MAC/PHY and interfaces with Upper MAC layer
  - Upper MAC
    - Software module to control/handle Wi-Fi control/handle to interface with supplicant
    - Wi-Fi Link layer: Interface layer between Upper MAC and supplicant
    - Supplicant: Software module to control/management to operate Wi-Fi operation
  - Network subsystem layer
    - Used to control/handle network operation
    - Main protocols are IP, TCP, and UDP
    - Other necessary protocols are supported
  - Security layer
    - Crypto operation engine is ported to use crypto hardware engine
- TLS/TCP and DTLS/UDP APIs are supported to handle security operation:
  - User application layer
    - Various sample code is available in the SDK – the sample code shows how to use the supported APIs
    - TCP Client/Server, UDP Client/Server, TLS Client/Server
    - HTTP/HTTPs download, OTA Update usage, and MQTT usage
- Customer applications can be included and implemented easily in the SDK.

4. Pinout

4.1 48-Pin QFN

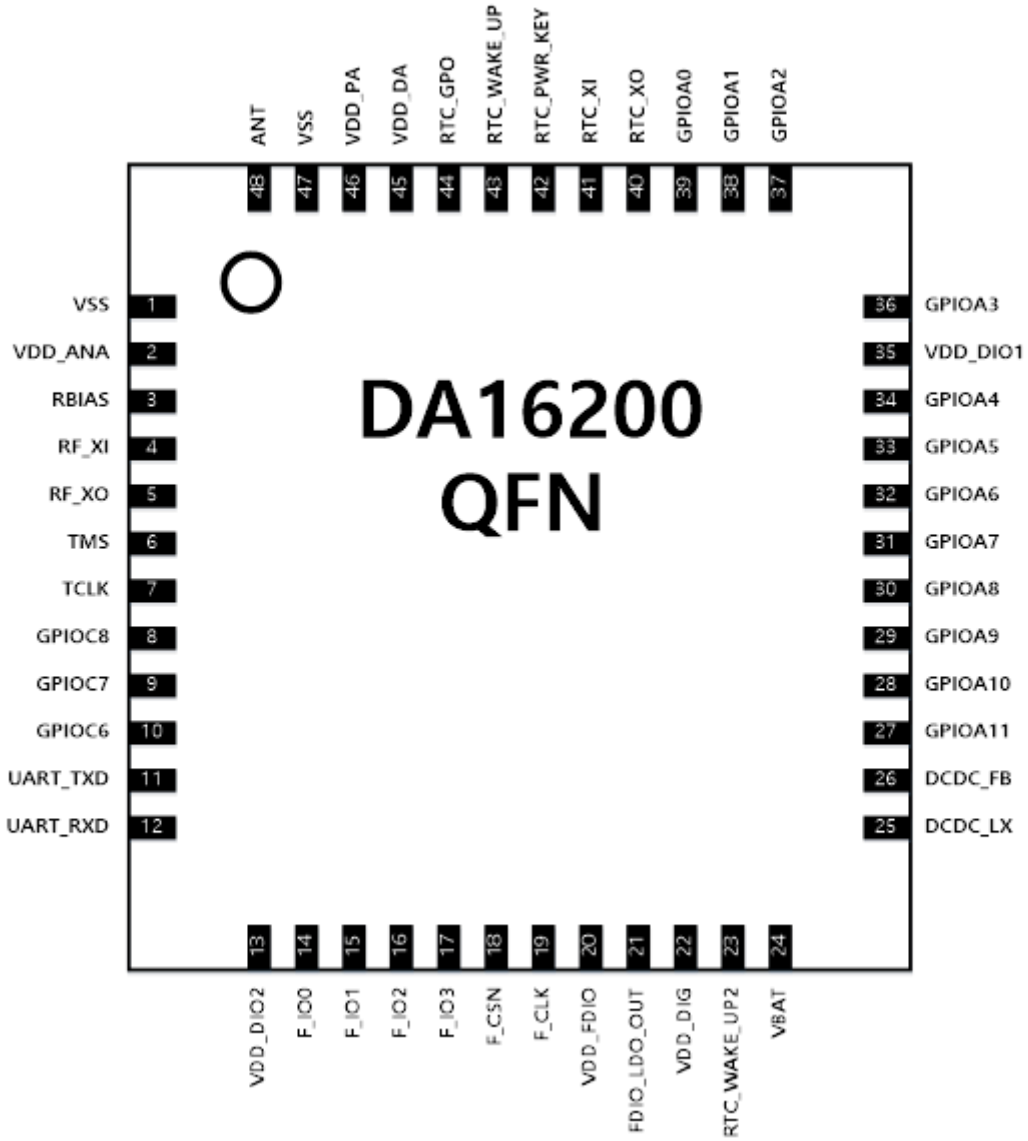

Figure 4. DA16200 QFN48 pinout diagram (top view)

4.2 72-Pin fcCSP

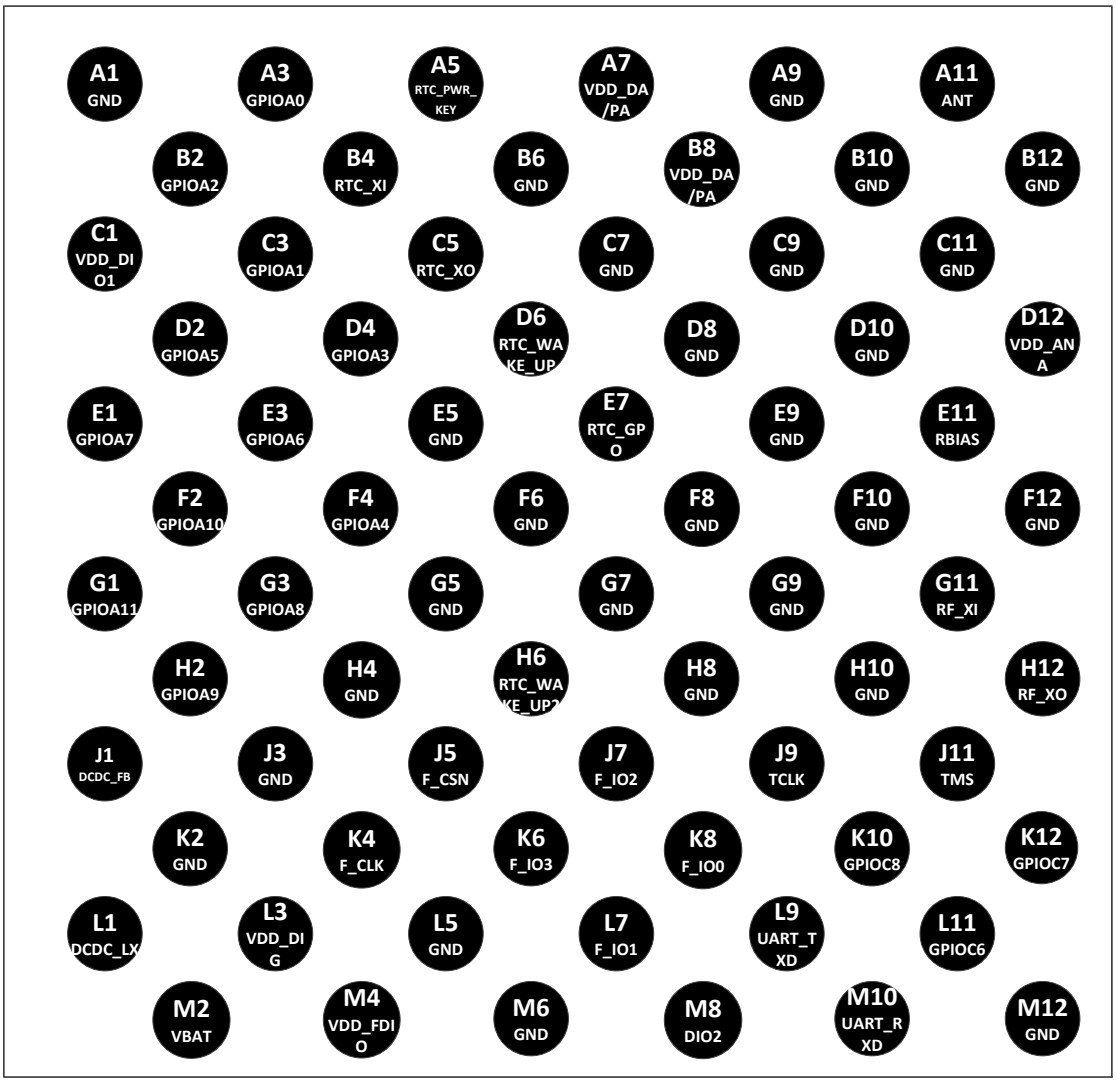

Figure 5. DA16200 fcCSP72 pinout diagram (top view)

Table 1. Pin description

QFN #pin	fcCSP #pin	Pin name	Type (Table 2)	Drive (mA)	Initial state (Note 1)	Description
1		GND	GND	-	-	Ground
2	D12	VDD_ANA	VDD	-	-	RF VDD
3	E11	RBIAS	AIO	-	-	External reference resistor pin
4	G11	RF_XI	AI	-	-	40 MHz crystal clock input
5	H12	RF_XO	AO	-	-	40 MHz crystal clock output
6	J11	TMS	DIO	2/4/8/12	I-PU	JTAG I/F, SWDIO
7	J9	TCLK	DIO	2/4/8/12	I-PD	JTAG I/F, SWCLK, General Purpose I/O
8	K10	GPIOC8	DIO	2/4/8/12	I-PD	General Purpose I/O
9	K12	GPIOC7	DIO	2/4/8/12	I-PD	General Purpose I/O
10	L11	GPIOC6	DIO	2/4/8/12	I-PD	General Purpose I/O
11	L9	UART_TXD	DO	2/4/8/12	O	UART transmit data
12	M10	UART_RXD	DI	2/4/8/12	I	UART receive data
13	M8	VDD_DIO2	VDD	-	-	Supply power for digital I/O GPIOC6~GPIOC8, TMS/TCLK, TXD/RXD

QFN #pin	fcCSP #pin	Pin name	Type (Table 2)	Drive (mA)	Initial state (Note 1)	Description
14	K8	F_IO0	DIO	-	-	External Flash Memory I/F
15	L7	F_IO1	DIO	-	-	External Flash Memory I/F
16	J7	F_IO2	DIO	-	-	External Flash Memory I/F
17	K6	F_IO3	DIO	-	-	External Flash Memory I/F
18	J5	F_CSN	DIO	-	-	External Flash Memory I/F
19	K4	F_CLK	DIO	-	-	External Flash Memory I/F
20	M4	VDD_FDIO	VDD	-	-	Flash I/O Power
21		FDIO_LDO_OUT	AIO	-	-	LDO output for Flash and I/O. Connect output to external cap.
22	L3	VDD_DIG	VDD	-	-	LDO output for Digital I/O. Connect output to external cap.
23	H6	RTC_WAKE_UP2	DI	-	DI (Note 2)	RTC block wake-up signal
24	M2	VBAT	VDD	-	-	Supply power for internal DC-DC, DIO_LDO, and analog IP
25	L1	DCDC_LX	AIO	-	-	Connection from power MOSFETs to the Inductor in internal DC-DC
26	J1	DCDC_FB	AIO	-	-	Feedback voltage from the output of the power supply in internal DC-DC
27	G1	GPIOA11	DIO	2/4/8/12	I-PD	General Purpose I/O
28	F2	GPIOA10	DIO	2/4/8/12	I-PD	General Purpose I/O
29	H2	GPIOA9	DIO	2/4/8/12	I-PD	General Purpose I/O
30	G3	GPIOA8	DIO	2/4/8/12	I-PD	General Purpose I/O
31	E1	GPIOA7	DIO	2/4/8/12	I-PD	General Purpose I/O
32	E3	GPIOA6	DIO	2/4/8/12	I-PD	General Purpose I/O
33	D2	GPIOA5	DIO	2/4/8/12	I-PD	General Purpose I/O
34	F4	GPIOA4	DIO	2/4/8/12	I-PD	General Purpose I/O
35	C1	VDD_DIO1	VDD	-	-	Supply power for digital I/O GPIOA0~GPIOA11
36	D4	GPIOA3	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
37	B2	GPIOA2	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
38	C3	GPIOA1	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
39	A3	GPIOA0	AI/DIO	2/4/8/12	I-PD	Aux.ADC input/General Purpose I/O
40	C5	RTC_XO	AO	-	AO	32.768 kHz crystal clock output
41	B4	RTC_XI	AI	-	AI	32.768 kHz crystal clock input
42	A5	RTC_PWR_KEY	DI	-	DI	RTC block enable signal
43	D6	RTC_WAKE_UP	DI	-	DI (Note 2)	RTC block wake-up signal
44	E7	RTC_GPO	DO	-	DO	General Purpose Output
45	A7, B8	VDD_DA	VDD	-	-	TX DA power and RTC block power
46		VDD_PA	VDD	-	-	Supply power for integrated power amplifier
47		GND	GND	-	-	Ground
48	A11	ANT	AI	-	-	ANT
fcCSP GND Pin: A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, E5, E9, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12						

Note 1 Status of RTC_PWR_KEY is asserted, and digital power (VDD_DIG) is stable.

Note 2 When this pin is used, an external pull-down resistor is needed, and if the pin is not used, it should remain open.

Table 2. Pin type definition

Pin type	Description	Pin type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PU	Pull-up resistor (fixed)	GND	Ground
PU	Pull-up resistor (fixed)	PD	Pull-down resistor (fixed)

4.3 Pin Multiplexing

The DA16200 provides various I/O interfaces to support many kinds of applications. To reduce the number of external pins required, the DA16200 uses pin multiplexing to assign these I/O interfaces to specific pins as shown in Table 3 and Table 4. There are 16 general purpose pins, each of which can be assigned alternate functions. There are four GPIO pins, GPIOA0 to GPIOA3, which support multiplexing with analog signals. See Table 133 and Table 134 for details on how to configure the pin functions.

Table 3. DA16200 pin multiplexing

Pin	JTAG	Analog	SPI master	SPI slave	I2C master	I2C slave	SDIO slave	SDeMMC
GPIOA0	-	CH0	-	SPI_MISO	I2C_SDA	I2C_SDA	-	Note 1
GPIOA1	-	CH1	-	SPI_MOSI	I2C_CLK	I2C_CLK	-	SD/eMMC_WRP
GPIOA2	-	CH2	-	SPI_CSB	-	I2C_SDA	-	-
GPIOA3	-	CH3	-	SPI_CLK	-	I2C_CLK	-	-
GPIOA4	-	-	-	-	I2C_SDA	I2C_SDA	SDIO_CMD	SD/eMMC_CMD
GPIOA5	-	-	-	-	I2C_CLK	I2C_CLK	SDIO_CLK	SD/eMMC_CLK
GPIOA6	-	-	E_SPI_CSB	SPI_CSB	-	I2C_SDA	SDIO_D3	SD/eMMC_D3
GPIOA7	-	-	E_SPI_CLK	SPI_CLK	-	I2C_CLK	SDIO_D2	SD/eMMC_D2
GPIOA8	-	-	E_SPI_DIO0/ E_SPI_MOSI	SPI_MISO	I2C_SDA	-	SDIO_D1	SD/eMMC_D1
GPIOA9	-	-	E_SPI_DIO1/ E_SPI_MISO	SPI_MOSI	I2C_CLK	-	SDIO_D0	SD/eMMC_D0
GPIOA10	-	-	E_SPI_DIO2	SPI_MISO	-	-	-	SD/eMMC_WRP
GPIOA11	-	-	E_SPI_DIO3	SPI_MOSI	-	-	-	-
TCLK/GPIOA15	TCLK	-	-	-	-	-	-	-
TMS	TMS	-	-	-	-	-	-	-
UART_TXD	-	-	-	-	-	-	-	-
UART_RXD	-	-	-	-	-	-	-	-
GPIOC8	TDI	-	-	-	-	-	-	-
GPIOC7	TDO	-	-	-	-	-	-	-
GPIOC6	NTRST	-	-	-	-	-	-	-

Note 1 Analog input pin function.

Table 4. DA16200 pin multiplexing (continued)

Pin	BT coex	I2S	I2S_Clock	UART1	UART2	Muxed w/analog	Pin state (nRESET=0)	Driving strength (Default: 8 mA)
GPIOA0	-	I2S_BCLK	-	UART1_TXD	-	Yes	I-PD	2/4/8/12 mA

Pin	BT coex	I2S	I2S_Clock	UART1	UART2	Muxed w/analog	Pin state (nRESET=0)	Driving strength (Default: 8 mA)
GPIOA1	-	I2S_MCLK	-	UART1_RXD	-	Yes	I-PD	2/4/8/12 mA
GPIOA2	-	I2S_SDO	Note 1	UART1_TXD	-	Yes	I-PD	2/4/8/12 mA
GPIOA3	-	I2S_LRCK	I2S_CLK_IN	UART1_RXD	-	Yes	I-PD	2/4/8/12 mA
GPIOA4	-	I2S_BCLK	-	UART1_TXD/UART1_RTS	-	No	I-PD	2/4/8/12 mA
GPIOA5	-	I2S_MCLK	-	UART1_RXD/UART1_CTS	-	No	I-PD	2/4/8/12 mA
GPIOA6	-	I2S_SDO	-	UART1_TXD	-	No	I-PD	2/4/8/12 mA
GPIOA7	-	I2S_LRCK	-	UART1_RXD	-	No	I-PD	2/4/8/12 mA
GPIOA8	BT_SIG0	I2S_BCLK	-	-	-	No	I-PD	2/4/8/12 mA
GPIOA9	BT_SIG1	I2S_MCLK	-	-	-	No	I-PD	2/4/8/12 mA
GPIOA10	BT_SIG2	-	I2S_CLK_IN	-	UART2_TXD	No	I-PD	2/4/8/12 mA
GPIOA11	-	-	-	-	UART2_RXD	No	I-PD	2/4/8/12 mA
TCLK/GPIOA15	-	-	-	-	-	No	I-PD	2/4/8/12 mA
TMS	-	-	-	-	-	No	I-PU	2/4/8/12 mA
UART_TXD	-	-	-	-	-	No	O	2/4/8/12 mA
UART_RXD	-	-	-	-	-	No	I	2/4/8/12 mA
GPIOC8	-	-	-	-		No	I-PD	2/4/8/12 mA
GPIOC7	-	-	-	-	UART2_RXD	No	I-PD	2/4/8/12 mA
GPIOC6	-	-	-	-	UART2_TXD	No	I-PD	2/4/8/12 mA

Note 1 Analog input pin function.

5. Electrical Specifications

5.1 Absolute Maximum Ratings

Table 5. Absolute maximum ratings

Parameter	QFN pins	fcCSP pins	Min	Max	Unit
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2, A7, B8	-0.2	3.7	V
VDD_DIO1	35	C1	-0.2	3.7	V
VDD_DIO2	13	M8	-0.2	3.7	V
VDD_FDIO	20	M4	-0.2	3.7	V
FDIO_LDO_OUT	21	-	-0.2	3.7	V
VDD_DIG	22	L3	-0.1	1.22	V
VDD_ANA	2	D12	-0.1	1.55	V
Operating temperature range (TA)	-	-	-40	+85	°C
Storage temperature range	-	-	-40	+150	°C

5.2 Recommended Operating Conditions

Table 6. Recommended operating conditions

Parameter	QFN pins	fcCSP pins	Min	Typ	Max	Unit
VBAT, VDD_DA, VDD_PA	24, 45, 46	M2, A7, B8 (Note 1)	2.1	-	3.6	V
VDD_DA, VDD_PA	-	A7, B8 (Note 2)	-	1.45	-	V
VDD_DIO1	35	C1	1.62	-	3.6	V
VDD_DIO2	13	M8	1.62	-	3.6	V
VDD_FDIO	20	M4	1.62	-	3.6	V
FDIO_LDO_OUT	21	-	1.62	-	1.92	V
VDD_DIG	22	L3	-	1.1	-	V
VDD_ANA	2	D12	-	1.37 (Note 2)	-	V
Operating temperature range (TA)	-	-	-40	-	+85	°C

Note 1 QFN, fcCSP Normal power mode.

Note 2 fcCSP Low power mode.

5.3 Electrical Characteristics

5.3.1 DC Parameters for Normal GPIOs

Table 7. DC parameters for normal GPIOs, 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.3 × DVDD	V
Input High Voltage	V_{IH}	Guaranteed logic high level	0.7 × DVDD	-	DVDD	V
Output Low Voltage	V_{OL}	DVDD = Min. (Note 1)	VSS	-	0.2 × DVDD	V
Output High Voltage	V_{OH}	DVDD = Min. (Note 1)	0.8 × DVDD	-	DVDD	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-up Resistor	R_{PU}	$V_{PAD} = V_{IH}$, DIO = Min.	-	-	32.4	kΩ
Pull-down Resistor	R_{PD}	V_{PAD} = VIL, DIO = Min.	-	-	32.4	

Note 1 DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level.

Table 8. DC parameters for normal GPIOs, 3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.8	V
Input High Voltage	V_{IH}	Guaranteed logic high level	2.0	-	DVDD	V
Output Low Voltage	V_{OL}	DVDD = Min. (Note 1)	VSS	-	0.4	V
Output High Voltage	V_{OH}	DVDD = Min. (Note 1)	2.4	-	DVDD	V
Pull-up Resistor	R_{PU}	VPAD = VIH, DIO = Min.	-	-	19.4	kΩ
Pull-down Resistor	R_{PD}	$V_{PAD} = V_{IL}$, DIO = Min.	-	-	16.0	

Note 1 DVDD = 3.3 V, VDD_DIO1, VDD_DIO2 Logic Level.

5.3.2 DC Parameters for RTC Block

There are several control pins in the RTC block. For details, see Section 7.4.

Table 9. DC parameters for RTC bloc, 3.3 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.6	V
Input High Voltage	V_{IH}	Guaranteed logic high level	2.3	-	VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

Table 10. DC parameters for RTC block, 2.1 V VBAT

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.3	V
Input High Voltage	V_{IH}	Guaranteed logic high level	1.6	-	VBAT	V

(RTC block: RTC_PWR_KEY, RTC_WAKE_UP, RTC_WAKE_UP2)

5.3.3 DC Parameters for Digital Wake-up

Several GPIOs can be used for wake-up. For details, see Section 7.4.1. To use digital wake-up, the I/O voltage should not be higher than the VBAT value.

Table 11. DC parameters for digital wake-up, 3.3 V VBAT and 1.8/3.3 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.5	V
Input High Voltage	V_{IH}	Guaranteed logic high level	1.4	-	DVDD (Note 1)	V

Note 1 DVDD = 1.8/3.3 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be higher than the VBAT value.

Table 12. DC parameters for digital wake-up, 2.1 V VBAT and 1.8 V IO

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	Guaranteed logic low level	VSS	-	0.3	V
Input High Voltage	V_{IH}	Guaranteed logic high level	1.3	-	DVDD (Note 1)	V

Note 1 DVDD = 1.8 V, VDD_DIO1, VDD_DIO2 Logic Level, DVDD should not be higher than the VBAT value.

5.4 Radio Characteristics

5.4.1 WLAN Receiver Characteristics

Typical values are at T_A = +25 °C and VBAT = 3.3 V, unless otherwise specified.

Parameters are measured at the antenna pin of CH1 (2412 MHz).

Table 13. WLAN receiver characteristics – QFN

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1 Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2 Mbps DSSS	-96	-95	-93	
	11 Mbps CCK	-91	-90	-88	
	6 Mbps OFDM	-92	-91	-89	
	9 Mbps OFDM	-92	-91	-89	
	18 Mbps OFDM	-90	-89	-87	
	36 Mbps OFDM	-83	-82	-80	
	54 Mbps OFDM	-77	-76	-74	
	MCS0 (GF)	-92	-91	-89	
	MCS7 (GF)	-74	-73	-71	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

Table 14. WLAN receiver characteristics – fcCSP

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity (8% PER for 11b rates, 10% PER for 11g/11n rates)	1 Mbps DSSS	-100.5	-99.5	-97.5	dBm
	2 Mbps DSSS	-96	-95	-93	
	11 Mbps CCK	-91	-90	-88	
	6 Mbps OFDM	-92	-91	-89	
	9 Mbps OFDM	-92	-91	-89	
	18 Mbps OFDM	-90	-89	-87	
	36 Mbps OFDM	-83	-82	-80	
	54 Mbps OFDM	-77	-76	-74	
	MCS0 (GF)	-92	-91	-89	
	MCS7 (GF)	-74	-73	-71	
Maximum input level (8% PER for 11b rates, 10% PER for 11g/11n rates)	802.11b	-4	0	0	
	802.11g	-10	-4	-3	

5.4.2 WLAN Transmitter Characteristics

Typical values are at T_A = +25 °C and VBAT = 3.3 V, unless otherwise specified.

Parameters are measured at the antenna pin of CH1 (2412 MHz).

Table 15. WLAN transmitter characteristics - QFN

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power measured from IEEE spectral mask and EVM	1 Mbps DSSS	17.5	20.0	21.0	dBm
	2 Mbps DSSS	17.5	20.0	21.0	
	5.5 Mbps CCK	17.5	20.0	21.0	
	11 Mbps CCK	17.5	20.0	21.0	
	6 Mbps OFDM	16.5	19.0	20.0	
	9 Mbps OFDM	16.5	19.0	20.0	
	12 Mbps OFDM	16.5	19.0	20.0	
	18 Mbps OFDM	16.5	19.0	20.0	
	24 Mbps OFDM	15.5	18.0	19.0	
	36 Mbps OFDM	15.5	18.0	19.0	
	48 Mbps OFDM	14.0	16.5	17.5	
	54 Mbps OFDM	13.0	15.5	16.5	
	MCS0 OFDM	16.5	19.0	20.0	
	MCS7 OFDM	13.0	15.5	16.5	
Transmit center frequency accuracy		-20		+20	ppm

Table 16. WLAN transmitter characteristics – fcCSP (Normal power mode)

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	16.0	18.5	19.5	dBm
	2 Mbps DSSS	16.0	18.5	19.5	
	5.5 Mbps CCK	16.0	18.5	19.5	
	11 Mbps CCK	16.0	18.5	19.5	
	6 Mbps OFDM	15.5	18.0	19.0	
	9 Mbps OFDM	15.5	18.0	19.0	
	12 Mbps OFDM	15.5	18.0	19.0	
	18 Mbps OFDM	15.5	18.0	19.0	
	24 Mbps OFDM	14.5	17.0	18.0	
	36 Mbps OFDM	14.5	17.0	18.0	
	48 Mbps OFDM	13.0	15.5	16.5	
	54 Mbps OFDM	12.0	14.5	15.5	
	MCS0 OFDM	15.5	18.0	19.0	
	MCS7 OFDM	12.0	14.5	15.5	
Transmit center frequency accuracy	-	-20	-	+20	ppm

Table 17. WLAN transmitter characteristics – fcCSP (Low power mode)

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power measured form IEEE spectral mask and EVM	1 Mbps DSSS	7.5	9.5	10.5	dBm
	2 Mbps DSSS	7.5	9.5	10.5	
	5.5 Mbps CCK	7.5	9.5	10.5	
	11 Mbps CCK	7.5	9.5	10.5	
	6 Mbps OFDM	6.0	8.0	9.0	
	9 Mbps OFDM	6.0	8.0	9.0	
	12 Mbps OFDM	6.0	8.0	9.0	
	18 Mbps OFDM	6.0	8.0	9.0	
	24 Mbps OFDM	3.5	5.5	6.5	
	36 Mbps OFDM	3.5	5.5	6.5	
	48 Mbps OFDM	0	2.0	3.0	
	54 Mbps OFDM	0	2.0	3.0	

Parameter	Condition	Min	Typ	Max	Unit
	MCS0 OFDM	6.0	8.0	9.0	
	MCS7 OFDM	0	2.0	3.0	
Transmit center frequency accuracy	-	-20	-	+20	ppm

5.5 Current Consumption

Typical values are at T_A = +25 °C and VBAT = 3.3 V, unless otherwise specified, with CPU clock 80 MHz.

Table 18. Current consumption in active state – QFN

Parameter	Condition			Min	Typ	Max	Unit
Active	TX	1 Mbps DSSS	@ 20.0 dBm	260	280	320	mA
		6 Mbps OFDM	@ 19.0 dBm	240	260	300	
		54 Mbps OFDM	@ 15.5 dBm	180	200	240	
		MCS7	@ 15.5 dBm	180	200	240	
	RX	No signal (Note 1)		25	29	51	
		1 Mbps DSSS (Note 1)		26.5	30.5	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	38.5	54	
		MCS7		29	38.6	54	

Note 1 Low Current mode and CPU clock 30 MHz.

Table 19. Current consumption in active state – fcCSP (Normal power mode)

Parameter	Condition			Min	Typ	Max	Unit
Active	TX	1 Mbps DSSS	@ 18.5 dBm	250	270	310	mA
		6 Mbps OFDM	@ 18.0 dBm	230	250	290	
		54 Mbps OFDM	@ 14.0 dBm	190	210	250	
		MCS7	@ 14.0 dBm	190	210	250	
	RX	No signal (Note 1)		25	28.4	51	
		1 Mbps DSSS (Note 1)		26.5	29.7	53	
		1 Mbps DSSS		27	36.5	54	
		54 Mbps OFDM		29	38	54	
		MCS7		29	38	54	

Note 1 Low Current mode and CPU clock 30 MHz.

Table 20. Current consumption in active state – fcCSP (Low power mode)

Parameter	Condition			Min	Typ	Max	Unit
Active	TX	1 Mbps DSSS	@ 9.5 dBm	63	85	100	mA
		6 Mbps OFDM	@ 8.0 dBm	63	85	100	
		54 Mbps OFDM	@ 2.0 dBm	48	70	90	
		MCS7	@ 2.0 dBm	48	70	90	
	RX	No signal (Note 1)		25	28.4	51	
		1 Mbps DSSS (Note 1)		26.5	29.7	53	
		1 Mbps DSSS		27	37.5	54	
		54 Mbps OFDM		29	39.2	54	
		MCS7		29	39.2	54	

Note 1 Low Current Mode and CPU clock 30 MHz.

Table 21. Current consumption in low power operation

Parameter	Condition	Min	Typ	Max	Unit
Low power operation	Sleep mode 1	-	0.2	-	µA
	Sleep mode 2	-	1.8	-	
	Sleep mode 3	-	3.5	-	

5.6 ESD Ratings

Table 22. QFN package

Parameter	Condition	Test condition	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

Table 23. fcCSP package

Parameter	Condition	Test condition	Result
Human Body Model (HBM)	JEDEC EIA/JESD22-A114	± 2,000 V	Pass
Charge Device Mode (CDM)	JEDEC EIA/JESD22-C101	± 500 V	Pass

5.7 Brownout and Blackout

The device enters a brownout condition whenever the input voltage dips below the Vbrownout condition defined in Table 24. This condition should be considered during design of the power supply routing, especially if the SoC is operated from a battery. High-current operations, such as Wi-Fi TX operations, cause a dip in the supply voltage, potentially triggering a Brownout. The resistance includes the internal resistance of the battery, contact resistance of the battery holder (for example, four contacts for two AA batteries), wiring resistance, and PCB routing resistance.

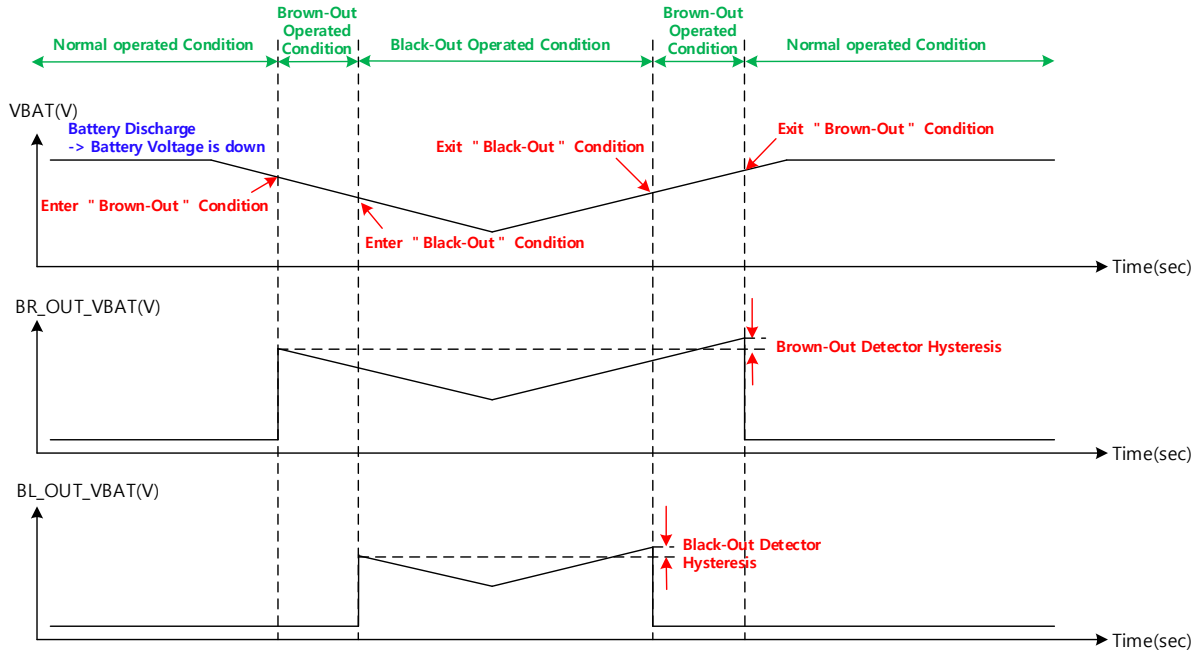

Figure 6. Brownout and blackout levels

Brownout and blackout conditions only operate in normal mode. The blackout condition is equivalent to a hardware reset event in which all states within the device are lost. Table 24 lists the brownout and blackout voltage levels.

Table 24. Brownout/blackout voltage levels

Condition	Voltage	Hysteresis	Operation
Vbrownout	2.10 V (Note 1)	90 mV	Software Control

Condition	Voltage	Hysteresis	Operation
Vblackout	1.75 V (Note 1)	90 mV	Full boot

Note 1 Recommended voltage level. Adjustable depending on the application condition.

5.8 Clock Electrical Characteristics

The DA16200 needs two clock sources. One is the 32.768 kHz clock used by the RTC block, and the other is the 40 MHz clock for the internal processor and Wi-Fi system. More specifically, the 40 MHz clock is used as a source clock for the internal PLL, while the PLL output is used for the internal processor and Wi-Fi system block.

5.8.1 RTC Clock Source

The 32.768 kHz RTC clock source is necessary for the free-running counter in the RTC block. The RTC block of the SoC contains an internal 32.768 kHz RC oscillator as well, which is used as a clock for chip initialization before the external 32.768 kHz crystal reaches the stable time in the initial stage. It is necessary to convert it into an external clock for accurate clock counting after the initialization stage. This process is executed through the register setting. Table 25 shows the suitable loading capacitor value and required tolerance. Figure 7 and Figure 8 show connections for the RTC crystal clock.

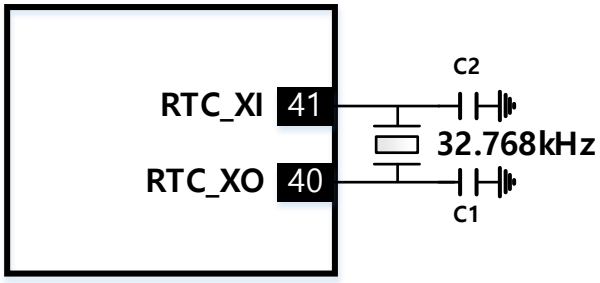

Figure 7. RTC crystal connections - QFN

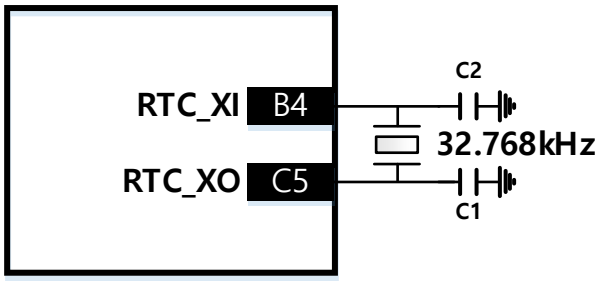

Figure 8. RTC crystal connection - fcCSP

Table 25 lists the RTC crystal requirements.

Table 25. RTC crystal requirements

Parameter	Condition	Min	Typ	Max	Unit
Frequency	-	-	32.768	-	kHz
Frequency Accuracy	Initial + temp + aging	-250	-	+250	ppm
Crystal ESR	-	-	-	100k	Ω
Load Capacitance	-	-	10	-	pF
Shunt Capacitance (Note 1)	-	-	15	-	pF

Note 1 There are no non-tunable capacitors inside so it must be adjusted using an external capacitor. External Shunt capacitors (C1, C2) have 15 pF mounted on the DA16200 module.

5.8.2 Main Clock Source

The DA16200 contains a crystal oscillator for the main clock source which supports the external crystal clock. Basically, the external clock is 40 MHz. Table 26 shows the load capacitor value and required clock tolerance for 40 MHz. Figure 9 and Figure 10 show the crystal clock connections.

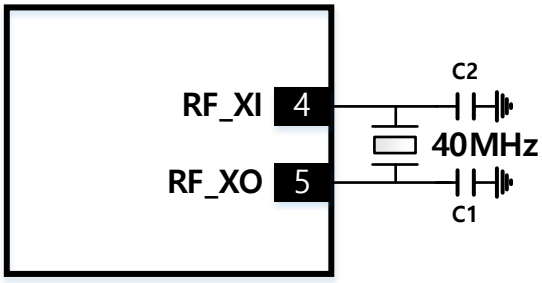

Figure 9. Crystal clock connections - QFN

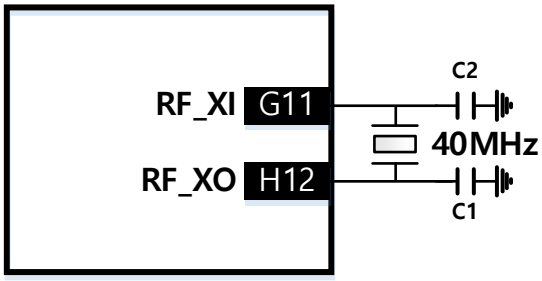

Figure 10. Crystal clock connections - fcCSP

Table 26 lists the WLAN crystal requirements.

Table 26. WLAN crystal clock requirements

Parameter	Condition	Min	Typ	Max	Unit
Frequency	-	-	40	-	MHz
Frequency Accuracy	Initial + temp + aging	-20	-	+20	ppm
Crystal ESR	-	-	-	50	Ω
Load Capacitance (Note 1)	-	6	8	10	pF

Note 1 Not to exceed ±20 ppm. There is an internal adjustable shunt capacitor inside the chipset, which must be written to the OTP block after XTAL correction. There is a 0~12.7 pF tunable capacitor inside the DA16200. To use it without shunt capacitors outside, it must be selected an XTAL with a load capacitance of 6~10 pF.

6. Power Management

DA16200 has an RTC block which provides power management and function control for low power operation. In normal operation, the RTC block is always powered on when RTC_PWR_KEY is enabled. The RTC block also has a control function for DA16200's internal power supplying components such as LDOs, DC-DCs, and power switches.

6.1 Power on Sequence

Figure 11 shows the sequence after the initial switching from power-off to power-on.

The RTC_PWR_KEY of the DA16200 is a pin that enables the RTC block. When the RTC_PWR_KEY is enabled after VBAT power is supplied, all the internal regulators are turned on automatically in the sequence predefined by the RTC block.

When the RTC_PWR_KEY is turned on, LDOs for both XTAL and digital I/O are turned on shortly and then the DC-DC regulator is turned on according to the predefined interval. The enabling intervals can also be modified in the register settings after initial power-up.

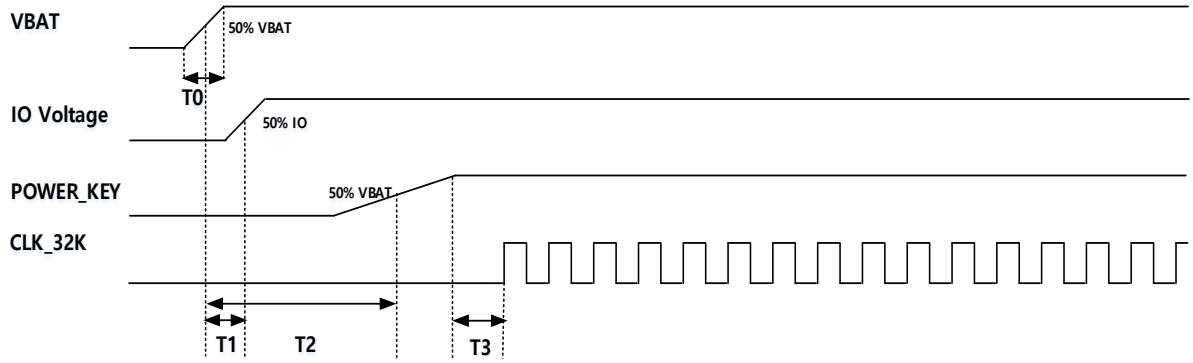

Figure 11. Power on sequence

Table 27. Power on sequence timing requirements

Name	Description	Min	Typ	Max	Unit
T0	VBAT power-on time from 10% to 90% of VBAT	-	-	-	ms
T1	I/O voltage and VCC supply	-	0	-	ms
T2	RTC_PWR_KEY turn-on time from 50% VBAT to 50% POWER_KEY * (Note 1)	-	5*T0	-	ms
T3	Internal RC oscillator wake-up time	-	217	-	µs

Note 1 If the T0 = 10 ms to turn on VBAT, the recommended T2 is 50 ms for the safe booting operation. It can be externally controlled by MCU or it can be implemented using RC filter at the input of RTC_PWR_KEY. The recommended C is 470 nF or 1 µF (not to exceed 1 µF) and R value is chosen to have T2 delay. For example, R and C values are 82 kΩ and 1 µF when T0 is 10 ms.

6.2 Power Management Unit

The DA16200 has one internal DC-DC converter and several LDOs to supply power to all internal sub-blocks. Power management does the on-off control of these regulators and is implemented through the register setting inside the RTC block.

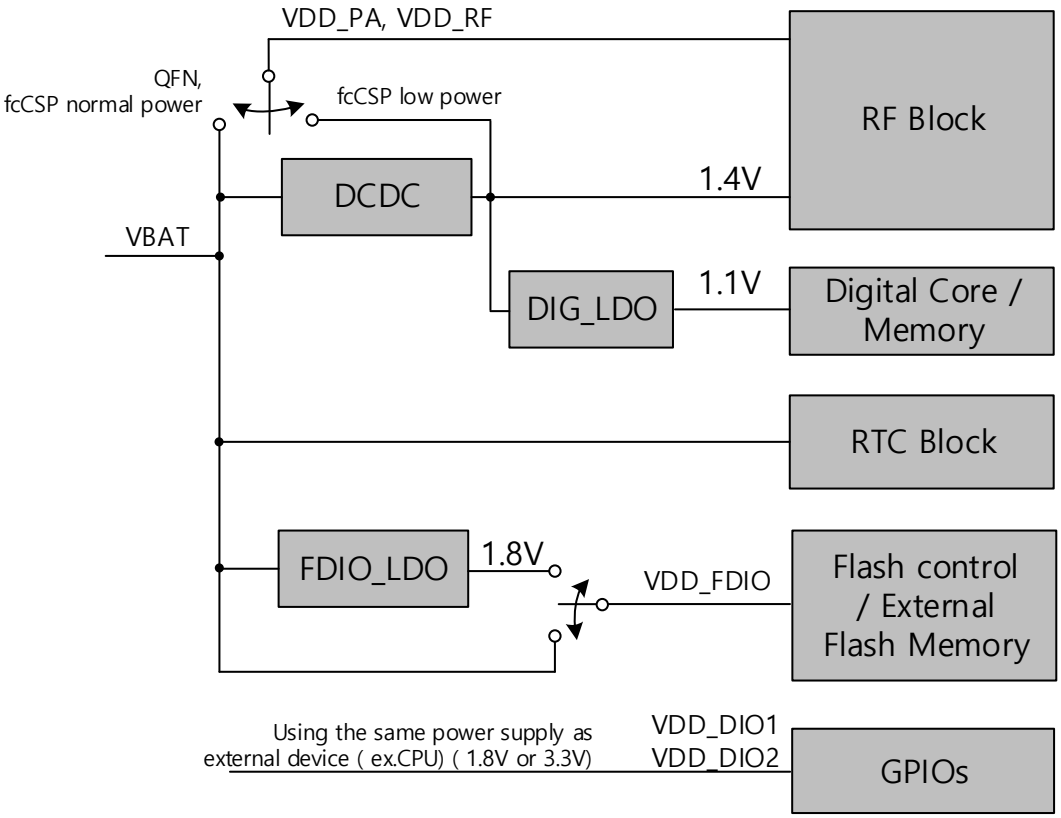

Figure 12. Power management block diagram

Details of the internal DC-DC converters and LDOs are explained:

- DC-DC converter: from the power supply of external VBAT input, it generates 1.4 V power for the digital LDO and RF block.
- LDO for digital blocks: from the DC-DC output, it generates 1.1 V power which is used for digital blocks.
- LDO for I/O and external flash memory:
  - This LDO output is used only for 1.8 V digital I/O applications.
  - From external VBAT power input, it generates 1.8 V output voltage which is used for digital I/O power domain in 1.8 V digital I/O applications.
  - It is also used for external flash memory.
  - For 3.3 V digital I/O applications, external power (3.3 V) is directly supplied for digital I/O power.
- FDIO_LDO_OUT supports only 1.8 V.

With the internal DC-DC converters and LDOs, all the power necessary for DA16200's internal sub-blocks are sufficiently generated.

6.3 Low Power Operation Mode

The DA16200 provides three Sleep modes as low power operation modes.

6.3.1 Sleep Mode 1

Sleep mode 1 is an operational mode in which the RTC_PWR_KEY is not turned to high yet. The RTC_PWR_KEY is in the LOW state and the DA16200 is only supplied with VBAT power. With all the internal blocks off in Sleep mode 1, only the leakage current from a minimal number of internal blocks connected to VBAT remains.

6.3.2 Sleep Mode 2

Sleep mode 2 is an operational mode in which the RTC_PWR_KEY is set to high and the RTC block is running. Sleep mode 2 is activated by setting RTC registers to control the power management unit through a command from the CPU.

To turn Sleep mode 2 back to Sleep mode 1, set RTC_PWR_KEY to low. Changing the state of the device from Sleep mode 2 to an ACTIVE state occurs in one of two ways:

- The counter value set by the CPU is reached before entering Sleep mode 2.
- An external wake-up event occurs through the RTC_WAKE_UP pin.

6.3.3 Sleep Mode 3

Sleep mode 3 is a low power mode which is the same as Sleep mode 2 but it maintains the retention memory during sleep. This allows for the software to keep information such as network connection state while in the Sleep mode. For more information on how to use Sleep mode 3, see Ref. [2].

7. Core System

7.1 Arm® Cortex-M4F Processor

The Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, low cost debug, and includes floating point arithmetic functionality. The processor is intended for deeply embedded applications that require fast interrupt response features.

The features of the Cortex-M4F processor in the DA16200 are summarized:

- Operation clock frequency is up to 160 MHz
- 32-bit Arm® Cortex-M4F architecture optimized for embedded applications
- Thumb-2 mixed 16/32-bit instruction set
- Hardware division and fast multiplication
- Include Nested Vectored Interrupt Controller (NVIC)
- SysTick timer provided by Cortex-M4F processor
- Support both standard JTAG (5-wire) and the low-pin-count ARM SWD (2-wire, TCLK/TMS) debug interfaces
- Cortex-M4F is binary compatible with Cortex-M3.

For more information on the ARM® Cortex-M4F, see Ref. [1].

7.2 Wi-Fi Processor

The DA16200 includes an internal MCU (ARM® Cortex-M4F) to completely offload the host MCU along with an 802.11 b/g/n radio, baseband, and MAC with a powerful crypto engine for a fast and secure WLAN and Internet connections with 256-bit encryption. It supports the station and Soft AP modes of operation. It also supports WPA/WPA2 personal and enterprise security, WPA2 SI, WPA3 SAE, OWE, and WPS 2.0. In addition, it has an embedded IPv4 and IPv6 TCP/IP stack.

7.3 Memory

7.3.1 Internal Memory

The DA16200 contains four types of internal memories and supports an external serial flash memory interface. The roles and functions of each memory are described in the following subsections.

7.3.1.1 ROM

This memory contains boot loader, system kernel, network stack, and various kinds of drivers for interfaces and peripherals.

7.3.1.2 SRAM

SRAM is used only as data space for the applications which run on the internal CPU. The applications execute directly from serial flash using an execute in place (XIP) process which loads the code into I-Cache as required. The SRAM is volatile memory, and its contents disappears when in the low-power Sleep mode.

The address range of the internal SRAM is from 0x0008_0000 to 0x000F_FFFF, and the controller of this memory supports the swap operation for the internal CPU. To perform a swap operation, add the offset value to the SRAM address for read operation only.

If the offset value is 0x2080_0000, the controller performs a swap to reverse the byte order for a scalar 32-bit value. If the offset value is 0x2040_0000, the controller performs a swap to reverse the halfword (16-bit) order for a scalar 32-bit value. For example, if the value of address 0x0000_8000 is 0x12345678, reading address 0x2080_8000 outputs value 0x78563412 and reading address 0x2040_8000 outputs value 0x56781234.

7.3.1.3 Retention Memory

This memory is a kind of non-volatile memory and is used to save and manage essential information that should be preserved even in the low-power Sleep mode of the DA16200.

7.3.1.4 OTP

The DA16200 includes a one-time field programmable (OTP) non-volatile CMOS memory. The OTP memory array supports write accesses of 1 bit and read accesses of 32 bits by executing read/write commands through the OTP controllers register interface.

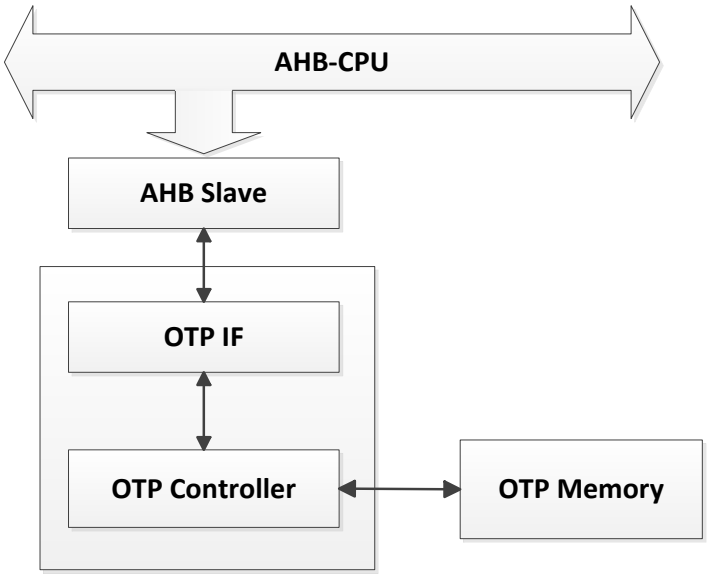

Figure 13. OTP block diagram

This memory is used to store and protect important information essential for mass production and the management of end products, such as boot information, MAC addresses, and serial numbers.

The OTP is also used for storing secret information which is used by the advanced security functions like secure boot, secure debug, and secure asset storage. This secret information is programmed during a secure manufacturing process and then locked so that it cannot be accessed directly by CPU read or write operations thus protecting it from external access.

Table 28. OTP map

Offset	Field	Size (Byte)
0x000	Reserved for internal use	1024
0x100	MAC Address #0 Low	4
0x101	MAC Address #0 High	4
0x102	MAC Address #1 Low	4
0x103	MAC Address #1 High	4
0x104	MAC Address #2 Low	4
0x105	MAC Address #2 High	4
0x106	MAC Address #3 Low	4
0x107	MAC Address #3 High	4
0x10A	XTAL Offset #0	4
0x10B	XTAL Offset #1	4
0x10C to 0x1FE	User Area	972

7.3.1.5 Serial Flash Interface

The DA16200 supports an external serial memory interface, QSPI (Section 9.1). This memory is used for storing DA16200's software code, including user application code, predefined data, and various configuration data in the form of NVRAM.

7.3.1.6 Memory Map

Figure 15 shows the various peripherals that are part of the DA16200 and how they are mapped to the processor memory.

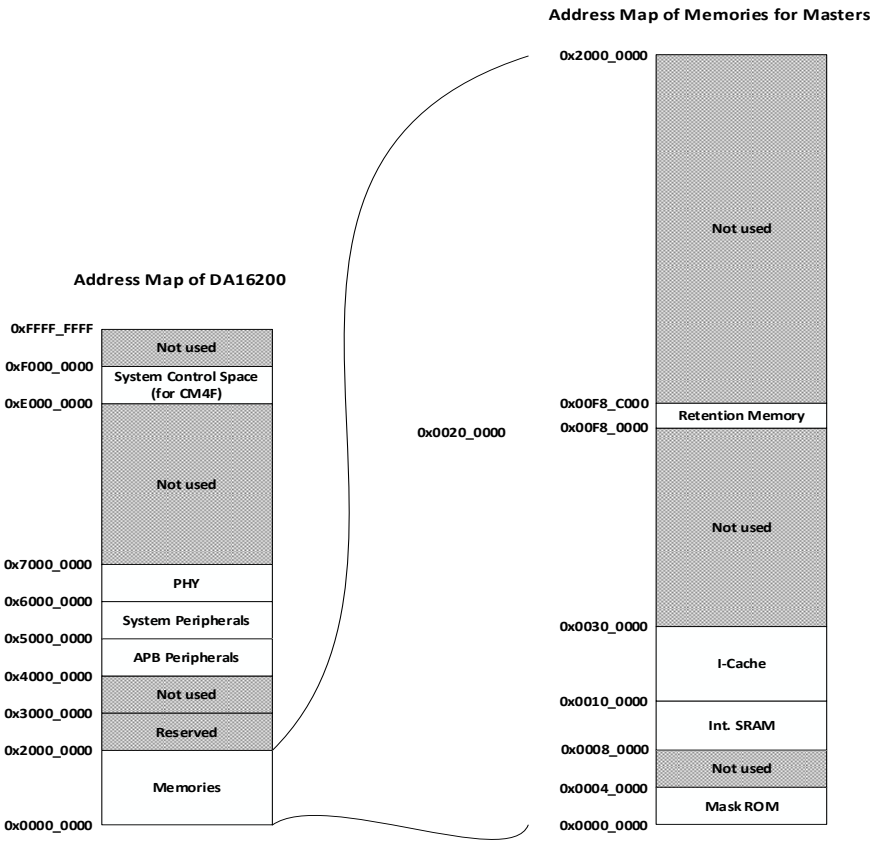

Figure 14. Memory map

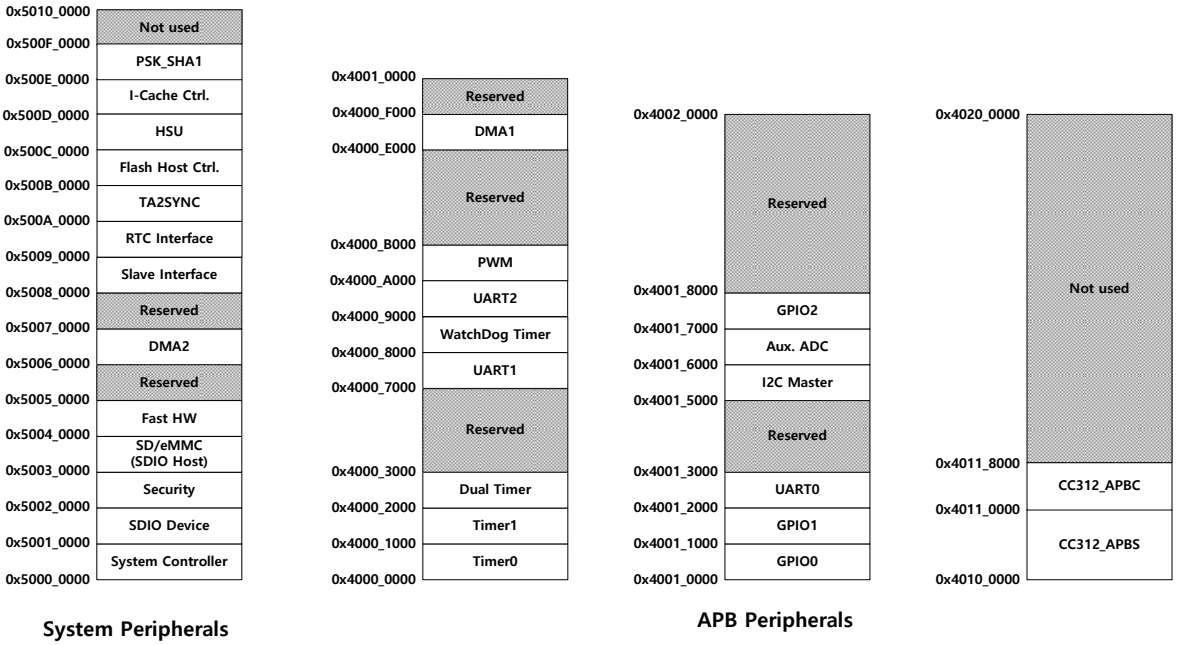

Figure 15. Memory map - Peripherals

7.4 RTC

Among the pins in the DA16200, four special pins are directly connected to the RTC block, which are RTC_PWR_KEY, RTC_GPO, RTC_WAKE_UP, and RTC_WAKE_UP2.

Table 29. RTC pin description

Pin name	Pin number		Description
	QFN	fcCSP	
RTC_PWR_KEY	42	A5	RTC_PWR_KEY represents a power key for the RTC block. When this pin is enabled, the RTC starts to work by following a predefined power-up sequence and eventually all the necessary power is supplied to all the sub-blocks including the main digital block in the DA16200. When disabled, all blocks are powered off and this mode is defined as Sleep mode 1. The DA16200 consumes minimum leakage current in Sleep mode 1.
RTC_GPO	44	E7	This pin is an output and high level is **VBAT**. It has three different functions: ● **GPO** function: its output value can be set as 1 or 0 through register setting. It can keep the value even in Sleep mode 2 and Sleep mode 3. ● **Flash control** function: when it is in Sleep mode, it becomes 0; when in Active mode, it is 1. ● **Sensor wake-up** function: when the sensor wake-up function is used (Section 9.8.4), a programmable periodic signal is provided for an external device. Inside the RTC, there are registers to set count values.
RTC_WAKE_UP	43	D6	This pin is an input pin for receiving an external event signal from an external device like a sensor. The RTC block detects an external event signal through this pin and wakes up the DA16200 from Sleep mode 2 or Sleep mode 3.
RTC_WAKE_UP2	23	H6	

The DA16200 contains not only an on-chip oscillator that uses a 32.768 kHz external crystal but also an internal 32.768 kHz RC oscillator for faster initialization, which leads to prompt clock generation after power-up and is used until the external crystal becomes stable. Afterwards, the input source can be switched to the external crystal through a register setting.

The RTC block has a 36-bit real time counter. Its resolution is equal to a one clock period of 32.768 kHz. The count value can be read with the register read command.

7.4.1 Wake-up Controller

The Wake-up Controller is designed to wake up the DA16200 from a Sleep mode by an external signal. It detects an edge trigger of the wake-up signal and selects either the rising edge or the falling edge. Also, the wake-up signal must be maintained for at least 200 µs upon occurrence of transition on one side.

For wake-up source, 11 digital I/Os in addition to the two pins directly connected to the RTC block can be used. Although up to 11 digital I/Os are available for use, the maximum number of digital I/Os that are simultaneously available is eight. Table 30 describes the digital I/Os that are available for simultaneous use.

Table 30. Wake-up sources

QFN and fcCSP package	
Input selection = 0	**Input selection = 1**
GPIOA4	X
GPIOA5	X
GPIOA6	X
GPIOA7	X
GPIOA8	X
GPIOA9	GPIOC6

QFN and fcCSP package	
Input selection = 0	**Input selection = 1**
GPIOA10	GPIOC7
GPIOA11	GPIOC8

For more information on the wake-up source selection, see the input selection register: 0x50091008[25:16].

The wake-up controller is in the RTC block. RTC registers can set several parameters and identify which pin is used to wake up the SoC by checking the status register after wake-up.

The DA16200 has another wake-up function using analog sources (Section 9.8.4). Using the Aux ADC, the DA16200 detects whether it exceeds the predefined threshold value. If it detects the wanted condition, it wakes up from a Sleep mode. Four ports (GPIOA[3:0]) are used for this function.

7.4.2 I/O Retention

The DA16200 I/O supports a retention mode where the I/O cells retain their previous values at the core side inputs when in Sleep mode 2 or Sleep mode 3.

Retention mode for the I/O cells is controlled by three bits in the retention enable register of the RTC block (0x5009_1018:BIT[27:24]).

To maintain a specific GPIO value when in Sleep mode 2 or Sleep mode 3, the specific bit controlling the I/O power for it must be enabled in the retention enable register.

For example, to maintain a HIGH value on GPIOA4 during Sleep mode 2 or Sleep mode 3, set the value of GPIOA4 to HIGH and also set the retention enable register BIT[25] to HIGH.

Table 31 shows the descriptions of the retention enable register and the I/O power domains.

Table 31. I/O power domain

[25] DIO1	[26] DIO2	[27] FDIO
GPIOA[11:4]	GPIOC[8:6]	F_CLK
-	TCLK/TMS	F_CSN
-	UART0_RXD/UART0_TXD	F_IO0 to F_IO3

7.5 Pulse Counter

7.5.1 Introduction

The pulse counter is a module that counts the number of rising or falling edges of input signals. And this counter module can run even in Sleep mode 2 and Sleep mode 3. It includes one 32-bit up-counter. The input channel can be set with a register setting among the 11 digital I/Os. It also has a glitch filter that is designed to remove the unwanted trigger of an input signal.

7.5.2 Functional Description

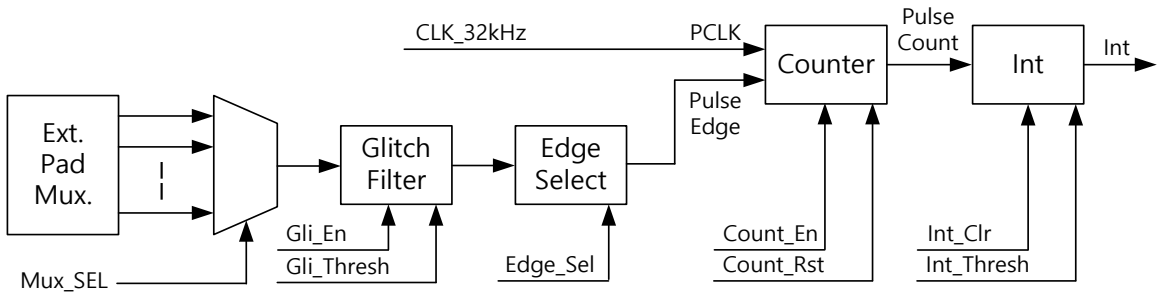

Figure 16. Pulse counter block diagram

7.5.2.1 Input

Available input channels are described in Table 30. It uses the same input sources with the wake-up controller. By register setting, input channels can be selected among 11 digital I/Os.

7.5.2.2 Clock

The operation clock of the pulse counter is 32 kHz.

7.5.2.3 Counter

The pulse counter is activated by several counter control signals (see Figure 16). With a register setting, input signals can be selected on either the rising edges or falling edges. To enable the glitch filter module, the Gli_En and Gli_Thresh register values need to be set. The pulses whose cycles are shorter than the Gli_Thresh value are removed. The counter is a 32-bit up counter and the counter value can be reset to zero by Count_Rst.

7.5.2.4 Interrupts

An interrupt occurs when the counter values reach the Interrupt Threshold value (Int_Thresh). In Sleep mode 2 and Sleep mode 3, this interrupt can be used as a wake-up source.

7.6 Hardware Accelerators

7.6.1 Zeroing of SRAM

The DA16200 provides a function to quickly set a constant value for the set SRAM area. This function is mainly used to initialize the set SRAM area to zero and can be used even when SRAM is used.

For example, if the entire 512 kB SRAM is being initialized, the processing time is 8192 cycles based on the CPU clock. That is, the maximum processing time is 8192 cycles irrespective of the SRAM size to be initialized. For more information about this function, see Ref. [2].

7.6.2 CRC Calculation

The CRC algorithm detects the corruption of data during transmission and detects a higher percentage of errors than a simple checksum. The CRC calculation consists of an iterative algorithm involving XOR and shifts operations that are executed much faster in hardware than in software. The CRC calculator is mainly used to check the flash image and the features of CRC calculator in the DA16200 are summarized:

- Operation clock frequency is up to 160 MHz, the same as CPU clock
- Supports 8-bit, 16-bit, and 32-bit data paths
- Performs CRC operation simultaneously in real time during data transfer on the selected AHB bus
- Operation type of CRC calculation
  - CRC-32: generator polynomial is G(x) = x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 +x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1
  - CRC-16 CCITT: generator polynomial is G(x) = x^16 + x^12 + x^5 +1
  - CRC-16 IBM: generator polynomial is G(x) = x^16 + x^15 + x^2 +1

For more information, see Ref. [2].

7.6.3 Pseudo Random Number Generator

The DA16200 provides a function, Pseudo Random Number Generator (PRNG), to generate a pseudo random number. The features of PRNG in the DA16200 are summarized as follows:

- Operation clock frequency is up to 160 MHz, the same as CPU clock.
- Supports partial parallel processing of 8-bit, 16-bit, and 32-bit units.

Generator polynomial is G(x) = x^31 + x^28 + 1 (see Ref. [3]).

7.7 DMA Operation

7.7.1 DMA1

The DA16200 includes a DMA controller of its own with a single AHB master. The DMA1 has sixteen channels for fast data transfers from/to I2S, I2C, UARTs, and ADC to/from any on-chip RAM. The DMA requests of each module are directly connected to the dedicated DMA channels. Each DMA channel has a priority level, a smaller channel number standing for a higher priority.

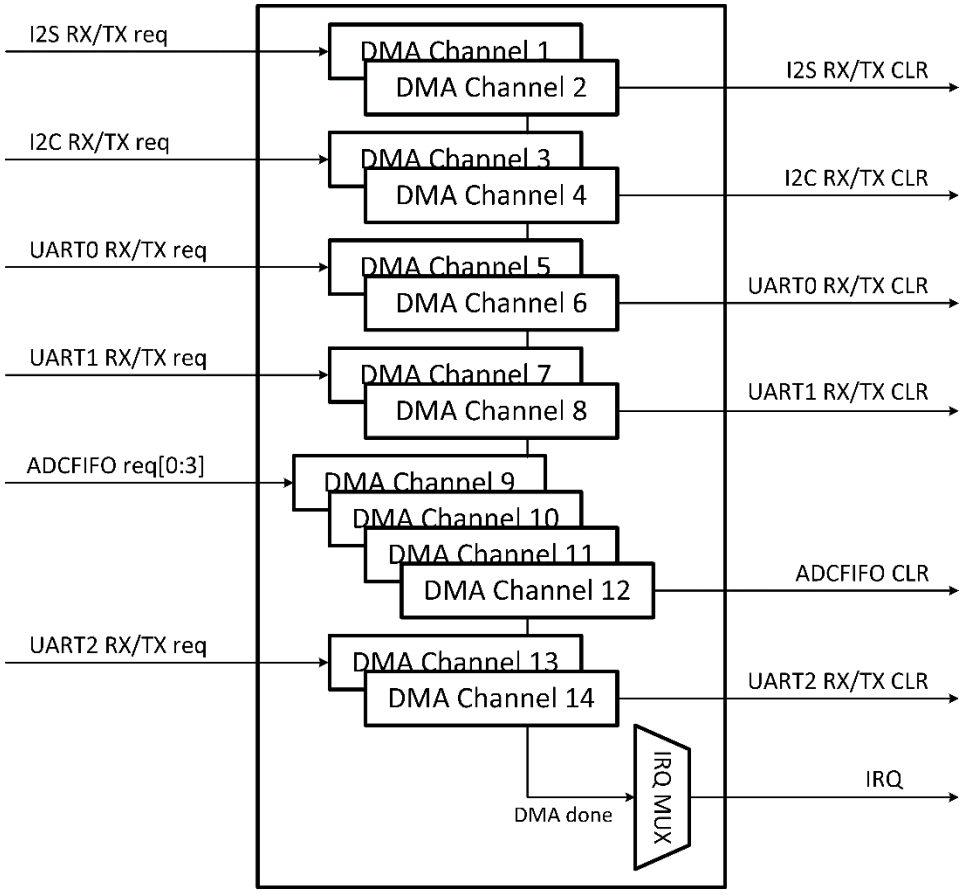

Figure 17. DMA1 controller block diagram

Table 32. DMA1 served peripherals

DMA channel	Module name	Direction	Transfer size
Channel 0	Mem-to-mem	TX/RX	Word
Channel 1	I2S	RX	Word
Channel 2	I2S	TX	Word
Channel 3	I2C	RX	Byte
Channel 4	I2C	TX	Byte
Channel 5	UART0	RX	Byte
Channel 6	UART0	TX	Byte
Channel 7	UART1	RX	Byte
Channel 8	UART1	TX	Byte
Channel 9	ADCFIFO[0]	READ	Halfword
Channel 10	ADCFIFO[1]	READ	Halfword
Channel 11	ADCFIFO[2]	READ	Halfword
Channel 12	ADCFIFO[3]	READ	Halfword
Channel 13	UART2	RX	Byte
Channel 14	UART2	TX	Byte
Channel 15	Mem-to-mem	TX/RX	Word

The DA16200's DMA1 controller supports the Linked-List Item (LLI) function that can sequentially operate multiple DMA tasks. It is possible to reduce the software burden and process delay with this function. Figure 18 shows the DMA1 state machine.

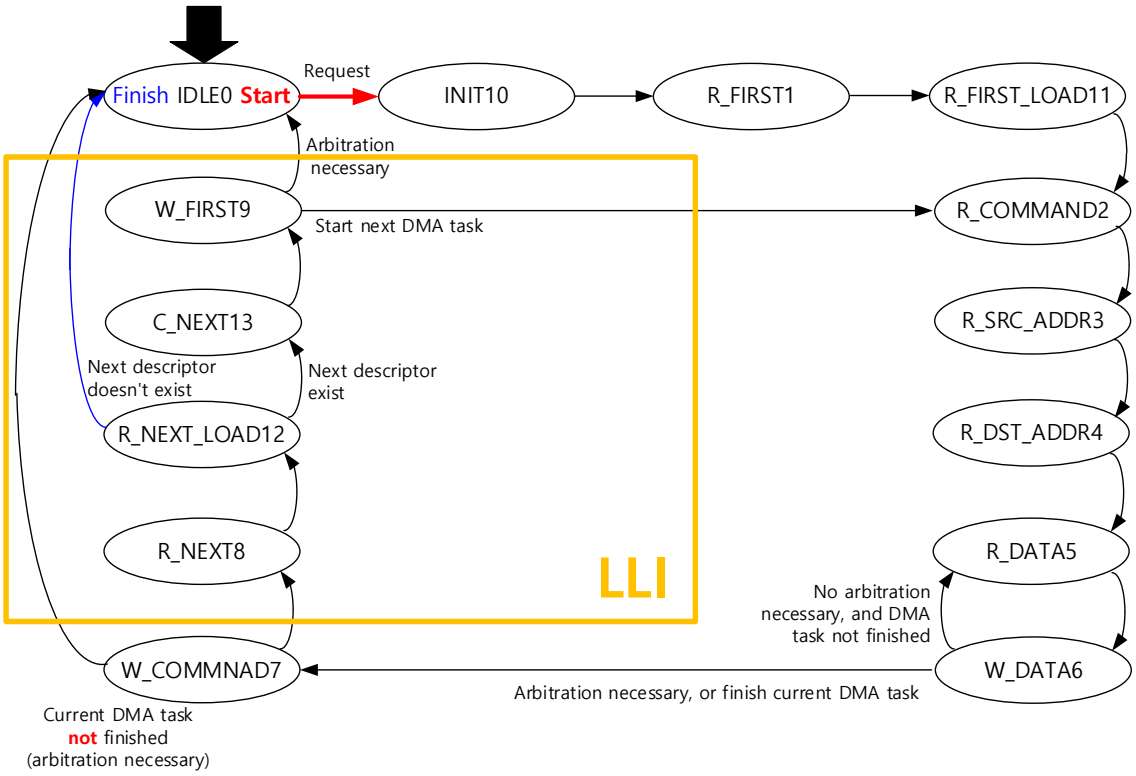

Figure 18. DMA1 state machine

- **IDLE**: waits for the DMA request. When the DMA request appears, the state moves to R_FIRST.
- **R_FIRST**: reads the address of the first DMA descriptor (head node of the linked list).
- **R_COMMAND**: reads the Command field of the DMA descriptor.
- **R_SRC_ADDR**: reads the Src_start_addr field of the DMA descriptor.
- **R_DST_ADDR**: reads the Dst_start_addr field of the DMA descriptor.
- **R_DATA**: reads the data from the source address.
- **W_DATA**: writes the data read in the R_DATA state to the destination address. According to the information written in the DMA descriptor, if data read/write is required, the state moves to R_DATA. If the DMA task is required to be suspended or stopped, the state moves to W_COMMAND.
- **R_NEXT**: reads the next_descriptor field to check whether the next DMA task exists or not, before stopping the current DMA task.
- **W_FIRST**: writes the address of the next DMA descriptor read in R_NEXT to the memory region where the first address of the DMA descriptor is stored. If arbitration is required, the state moves to IDLE state. If the current DMA channel is required to operate, the state moves to R_FIRST state.
- **INIT, R_FIRST_LOAD, R_NEXT_LOAD, and C_NEXT**: reduce the critical path delay in the DMA block. These states generate one clock delay.

7.7.2 DMA2

The DMA2 (Fast DMA) controller consists of a master read port, a master write port, and a slave port for configuration register setting. Fast DMA performs bulk data transfers, data reading from the source address range, and data writing to the destination address range. Fast DMA is mainly used for fast data transfer from memory to memory.

The features of Fast DMA in the DA16200 are summarized as follows:

- Transfer size is programmable from 1 byte to 1 MB
- Up to four channels can be set at the same time
- LLI function of ring type is supported by using configuration registers of four channels
- Interrupt enable can be set for each channel
- Provide a hold function to pause data transfer for each channel.

The basic unit of bus transmission is 32-bit and has a function to automatically correct address align, even if the source and destination addresses are not in word units.

For example, assuming that the transfer size is 23 bytes, the source base address is 0x001 for read access, and the destination base address is 0x102 for write access, the number of bytes per transaction is performed as follows:

- Source base address [1:0] = 0x1: the master read port of fast DMA performs read access with the following sequences:
  - 1 -> 2 -> 4 -> 4 -> 4 -> 4 -> 4 bytes
- Destination base address [1:0] = 0x2: the master write port of fast DMA performs write access with the following sequences:
  - 2 -> 4 -> 4 -> 4 -> 4 -> 4 -> 1 bytes

Figure 19 shows the DMA2 block diagram.

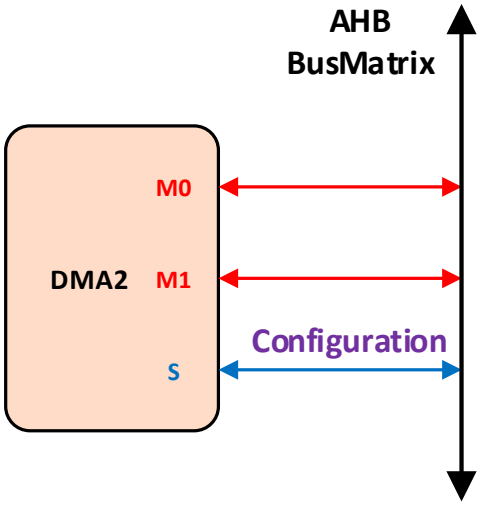

Figure 19. DMA2 block diagram

7.8 Simple Memory Protection

The DA16200 provides simple protection for internal SRAM, ROM, and Retention Memory. The memory controllers are AMBA AHB slaves and simple protection operates between the main AHB bus and the AHB slave port of the memory controllers.

The features of memory protection in the DA16200 are summarized as follows:

- Memory protection provides the function to set the security area of each memory that should be protected
- The setting unit to set the security area for each memory is different:
  - SRAM: 1 kB/unit
  - MROM: 16 bytes/unit
  - Retention Memory: 4 bytes/unit
- Provide the access protection for the security zone for each AHB master
- Provide the write protection function for each AHB master
- Provide the read protection function for each AHB master
- Latency is 0 cycle.

The index numbers to distinguish AHB masters are:

- 0x0: Cortex M4 – DCode bus
- 0x1: Cortex M4 – ICode bus

- 0x2: Cortex M4 – System bus
- 0x3: MAC DMA
- 0x4: DMA1
- 0x5: SD/eMMC (SD Host)
- 0x6: Serial Slave Interface (SPI, I2C, SDIO)
- 0x7: DMA2_M0 (read port)
- 0x8: DMA2_M1 (write port)
- 0x9: DMA of Crypto Engine
- 0xA: QSPI master – flash controller with XIP
- 0xB: Hardware Security Unit for Temporal Key Integrity Protocol (HSU for TKIP)
- 0xC: SPI master for another external SPI slaves.

For more information to use this function, see Ref. [2].

7.9 Bus Protection of Serial Slave Interfaces

The DA16200 supports a variety of serial slave interfaces, including SPI, I2C, and SDIO slaves. When the DA16200 interfaces with an external host, it is necessary to provide access to the authorized area. Therefore, the DA16200 provides bus protection for serial slave interfaces.

The features of bus protection in the DA16200 are summarized as follows:

- Up to two accessible areas can be set and the setting unit is 4-byte.
- The bus protection provides the write/read protection function outside the set area.

For more information to use this function, see Ref. [2].

7.10 Watchdog Timer

The watchdog timer in the DA16200 is based on a 32-bit down counter that is initialized from the reload register, WDOGLOAD. The watchdog timer generates a regular interrupt, WDOGINT, depending on the programmed value. The counter decrements by one on each positive clock edge of WDOGCLK when the clock enable, WDOGCLKEN, is HIGH.

The watchdog monitors the interrupt and asserts a reset request signal, WDOGRES, when the counter reaches 0, and the counter is stopped. On the next enabled WDOGCLK clock edge, the counter is reloaded from the WDOGLOAD register and the countdown sequence continues. If the interrupt is not cleared by the time the counter reaches 0 for a second time, the watchdog timer reasserts the reset signal.

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog unit can be enabled or disabled as required.

Figure 20 shows the watchdog timer block diagram.

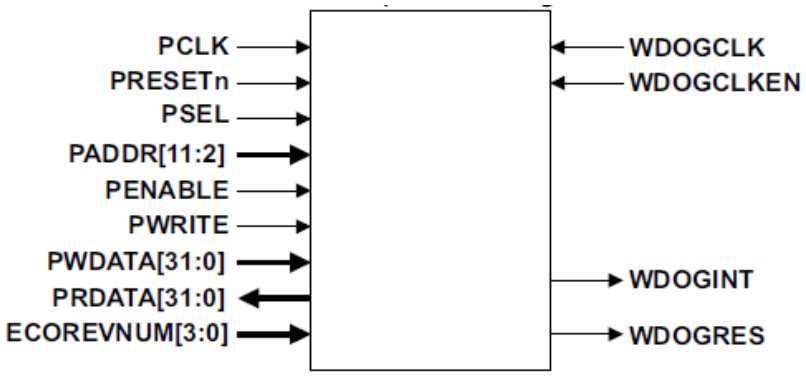

Figure 20. Watchdog timer block diagram

Figure 21 shows the flow diagram for the watchdog operation.

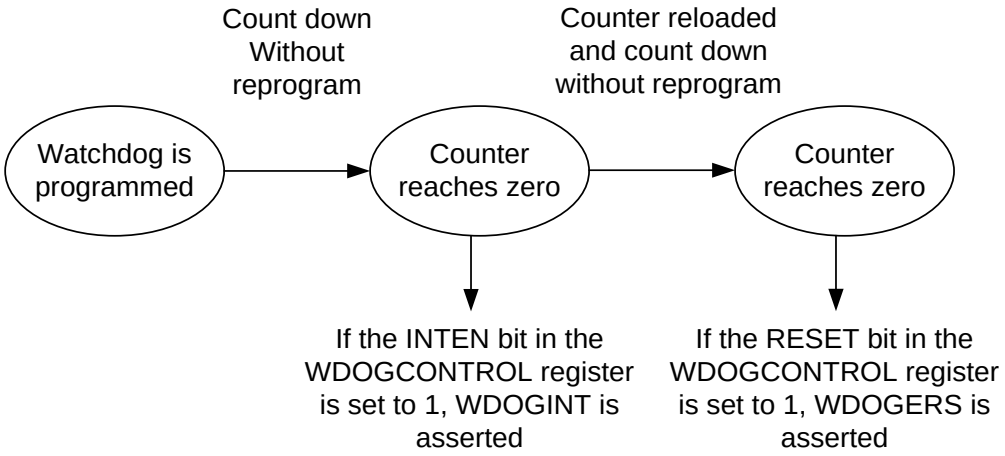

Figure 21. Watchdog operation flow diagram

7.11 Clock Generator

The generation of the system's clocks is described in detail in Figure 22.

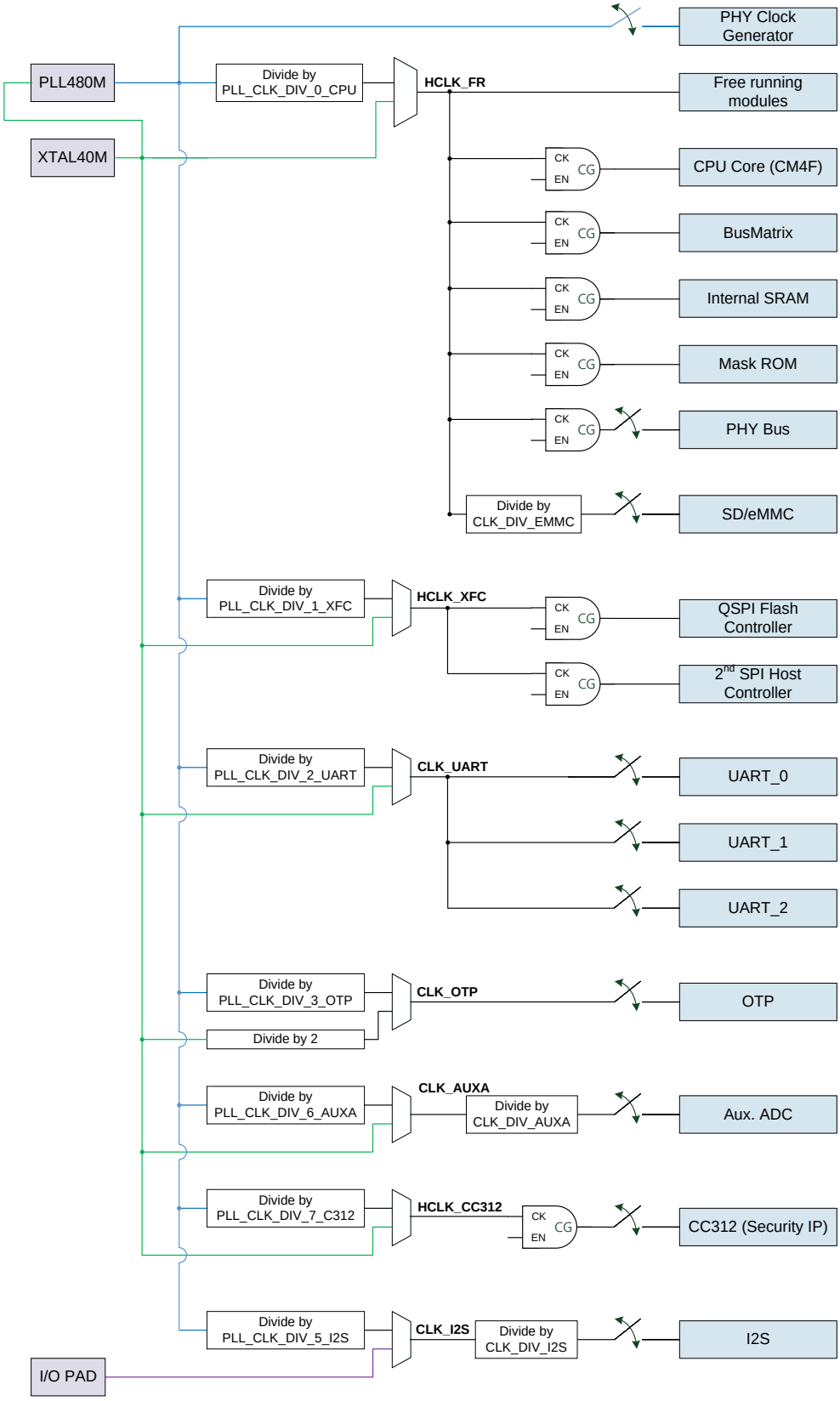

Figure 22. Clock tree diagram

8. Crypto Engine

The hardware crypto engine provides acceleration of many crypto algorithms such as hashing, secret key generation, encryption/decryption, and sign/verify operations.

Table 33 shows the hardware accelerated crypto algorithms supported by the DA16200. Examples on how to use these crypto algorithms, see Ref. [2] and Ref. [4].

Table 33. Hardware accelerated crypto algorithms in DA16200

Algorithm	Mode	Key Sizes
AES	ECB, CBC, CTR, OFB, CMAC, CBC-MAC, AESCCM, AES-CCM*, AES-GCM	128 bits, 192 bits, and 256 bits
AES key wrapping	N/A	All
Chacha20 and Poly1305	N/A	256 bits
Diffie-hellman ● ANSI X9.42-2003: Public Key Cryptography for the Financial Services Industry: Agreement of Symmetric Keys Using Discrete Logarithm Cryptography ● Public-Key Cryptography Standards (PKCS) #3: Diffie Hellman Key Agreement Standard	N/A	1024 bits, 2048 bits, and 3072 bits
ECC key generation	N/A	NIST curves and 25519 curves
ECIES	N/A	NIST curves and 25519 curves
ECDSA	N/A	NIST curves and ED25519
ECDH	N/A	NIST curves and 25519 curves
Hash	SHA1, SHA224 and SHA256	N/A
HKDF	N/A	N/A
HMAC	SHA1, SHA224 and SHA256	N/A
KDF NIST SP 800-108: Recommendation for Key Derivation Using Pseudorandom Functions	CMAC or HMAC	N/A
RSA PKCS#1 operations ● Public-Key Cryptography Standards (PKCS) #1 v2.1: RSA Cryptography Specifications ● Public-Key Cryptography Standards (PKCS) #1 v1.5: RSA Encryption	Encryption and signature schemes	2048 bits, 3072 bits, and 4096 bits
RSA key generation	N/A	2048 bits and 3072 bits

9. Peripherals

This section describes the peripherals that are supported by the DA16200 device.

9.1 QSPI Master with XIP Feature

QSPI master supports 4-line SPI communication with commercial flash memory devices and uses a Motorola SPI-compatible interface among SPI communication modes. The highest communication speed is the same as the AMBA bus clock, and the speed is adjustable in integer multiples. The designed QSPI supports 4-/2-/1-line types depending on the purpose. These types should be combined. Especially when the 1-line communication mode is used, it can be used as the SPI master.

QSPI master is an IP for communication between the flash memory and AMBA AHB bus and is designed to support XIP. The features of the QSPI master are summarized as follows:

Serial Flash Interface:

- SPI compatible serial bus interface
  - Configurable SPI I/O modes:
    - Single I/O mode
    - Dual I/O mode
    - Quad I/O mode
  - JEDEC Standard: JESD216B
  - 24-bit and 32-bit addressing
  - Support to access flash with XIP mode
    - Read access without command
    - Read access without address and command
  - Programmable SPI clock phase and polarity
  - Maximum number of SPI CS is four that can be operated
- Compatible with serial NOR flash devices, such as Macronix, Micron, Spansion, ESMT, and ISSI.

AMBA Slave Interface:

- Compliance to the AMBA AHB Bus Specification, Rev 3.0 Ref. [6]
- Direct code execution: directly addressable access without additional driver software
- Support single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Support byte, halfword, and word transaction
- AMBA slave interface is optional to access configuration and status registers
- Simple timer is used to check the completion time of flash operation
- XIP path of QSPI master supports hardware remapping function to execute selected boot image for over-the-air programming (OTA).

AMBA Master Interface:

- Compliance to the AMBA AHB Bus Specification, Rev 3.0 Ref. [6]
- Support DMA operation to access serial flash devices
  - Automatic copy of code image from serial flash to system RAM
  - Automatic programming of code image from system RAM to serial flash
- Perform a mem-to-mem copy in units of 32 bits, regardless of the address and length
- Support single and incrementing burst transfer (SINGLE, INCR, INCR4, INCR8, INCR16)
- Support byte, halfword, and word transaction.

Figure 23 shows the QSPI Master Block Diagram.

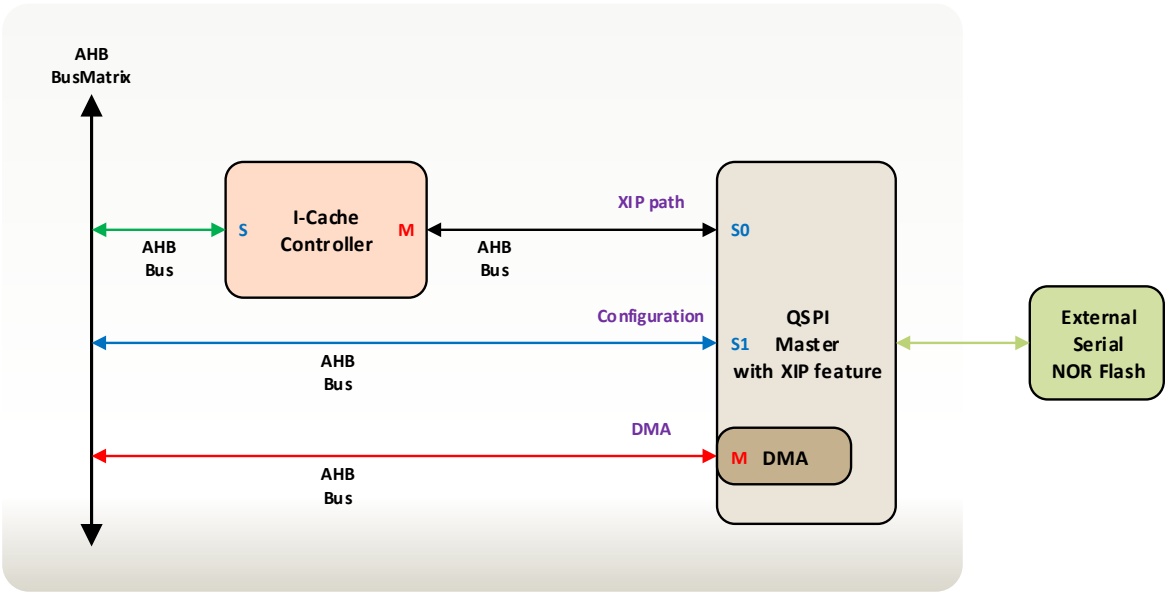

Figure 23. QSPI master block diagram

Figure 24 shows the timing diagram for the QSPI master.

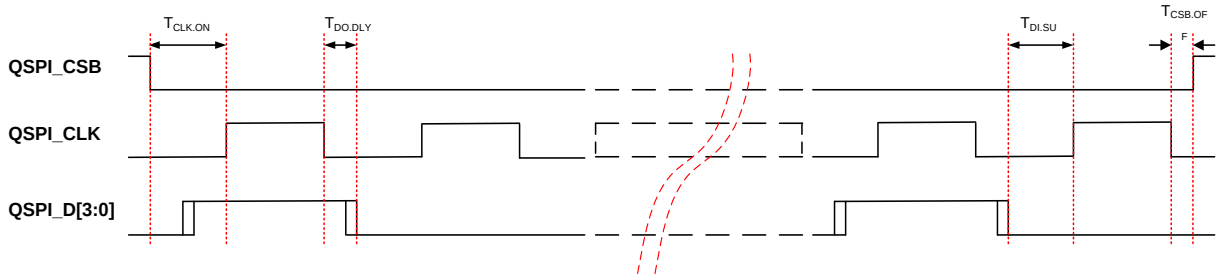

Figure 24. QSPI master timing diagram (Mode 0)

Table 34 lists the timing parameters for the QSPI master.

Table 34. QSPI master timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	10		120	MHz
QSPI_CLK clock duty	-	-	50	-	%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 ×T_{CLK}	-	T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0	-	TCLK	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6	-	-	ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$	-	-	2	ns

Note 1 TCLK = (FCLK× 106) -1 seconds.

9.2 SPI Master

QSPI can use the SPI master with the use of a single line interface. Table 35 shows the pin definition of the SPI master interface. SPI signal timing is the same as QSPI.

To use the DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from the GPIO special function by setting the registers in the GPIO.

Table 35. SPI master pin configuration

Parameter	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOx	-	-	O	E_SPI_CSB[3:1]
GPIOA6	32	E3	O	E_SPI_CSB[0]
GPIOA7	31	E1	O	E_SPI_CLK
GPIOA8	30	G3	I/O	E_SPI_MOSI or E_SPI_D[0]
GPIOA9	29	H2	I/O	E_SPI_MISO or E_SPI_D[1]
GPIOA10	28	F2	I/O	E_SPI_D[2]
GPIOA11	27	G1	I/O	E_SPI_D[3]

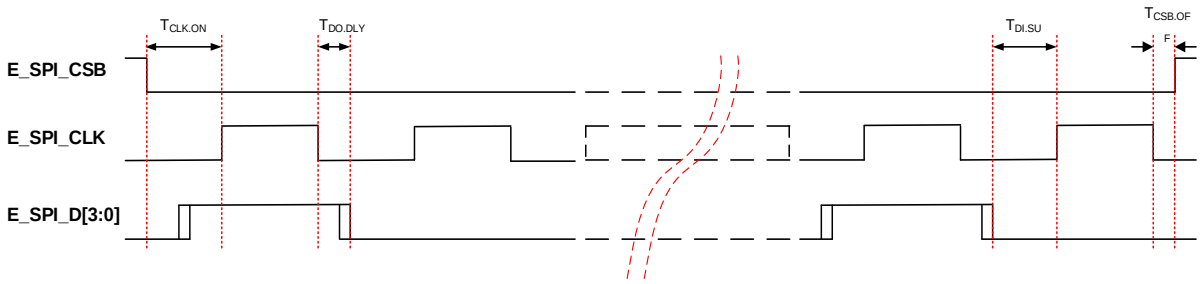

Figure 25. SPI master timing diagram (Mode 0)

Table 36. SPI master timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
QSPI_CLK frequency	F_{CLK}	5	-	60	MHz
QSPI_CLK clock duty	-	-	50	-	%
1st CLK active rising transition time	$T_{CLK.ON}$	0.5 × T_{CLK}	-	T_{CLK} (Note 1)	ns
QSPI_CSB non-active rising transition time	$T_{CSB.OFF}$	0	-	T_{CLK}	ns
QSPI_D[3:0] input setup time	$T_{DI.SU}$	6	-	-	ns
QSPI_D[3:0] output delay time	$T_{DO.DLY}$	-	-	2	ns

Note 1 TCLK = (FCLK× 106) -1 seconds.

9.3 SPI Slave

The SPI slave interface is a half-duplex connection for an external host to control the DA16200. The range of the SPI clock speed is based on the internal bus clock speed and can be calculated using:

spi clock = system clock/N

where N is an integer divider such as 1,2,3,4,5,6, ...

The SPI slave supports both the Burst mode and Non-Burst mode. In the Burst mode, SPI_CSB remains active from the start to the end of communication. In the Non-Burst mode, SPI_CSB remains active at every eight bits.

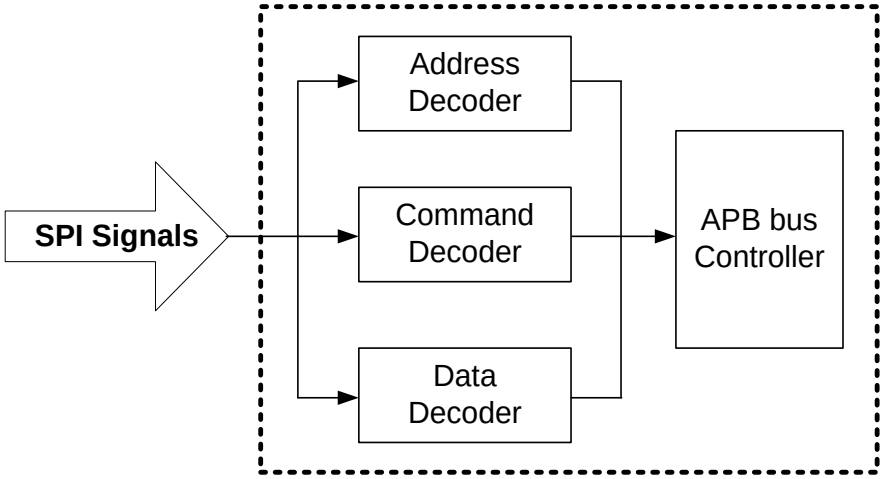

Figure 26. SPI slave block diagram

Communication protocols of the SPI slave interface use either 4-byte or 8-byte control signals. Between the two available communication protocols, the CPU chooses one before initiating the control.

Figure 27 and Figure 28 show the 8-byte and 4-byte control types.

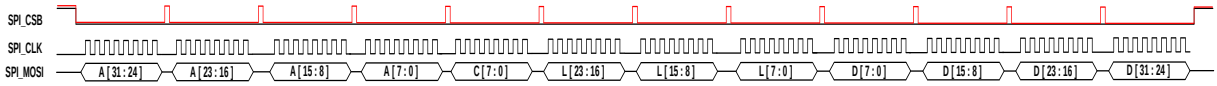

Figure 27. 8-byte control type

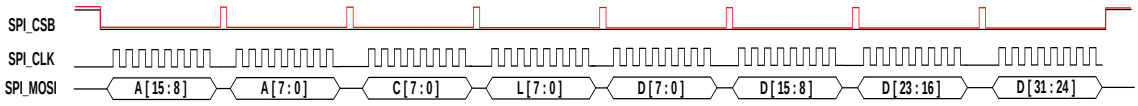

Figure 28. 4-byte control type

The 8-byte control type uses a 4-byte address, 1-byte control, and 3-byte length. The 4-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 3-byte length shows the length of data subject to continuous access in bytes. Thus, when the 8-byte control type is applied, the maximal length of data subject to continuous access is 16 MB.

The 4-byte control type uses a 2-byte address, 1-byte control, and 1-byte length. The 2-byte address displays the address of registers subject to internal access. The 1-byte control is for communication control and 1-byte length shows the length of data subject to continuous access in bytes. Since the 32-bit address map is used internally, the 2-byte address is not enough to express everything. Thus, the upper 2-byte base address is designated, and then the lower 2-byte address is used.

Table 37 and Table 38 show the meaning of each bit in the 1-byte control in the 8-byte control type and the 4-byte control type respectively.

Table 37. Control field of 8-byte control type

Bit	Name	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5:0	-	Not used. Set all bits to 0	

Table 38. Control field of 4-byte control type

Bit	Name	Description	
7	Auto Inc.	1 = Internal address auto-increment	0 = Address fixed
6	Read/Write	1 = Read	0 = Write
5	Common	1 = Refer base address as common area	0 = Refer base address

Bit	Name	Description	
4	Length section	1 = Refer to register value	0 = Refer to length field
3:0	Length[12:8]	Length field upper	

Table 39 shows the pin definition of the SPI slave interface.

Table 39. SPI slave pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA2	37	B2	I	SPI_CSB
GPIOA6	32	E3	I	
GPIOA3	36	D4	I	SPI_CLK
GPIOA7	31	E1	I	
GPIOA1	38	C3	I	SPI_MOSI
GPIOA9	29	H2	I	
GPIOA11	27	G1	I	
GPIOA0	39	A3	O	SPI_MISO
GPIOA8	30	G3	O	
GPIOA10	28	F2	O	

Figure 29 shows the timing diagram for the SPI slave.

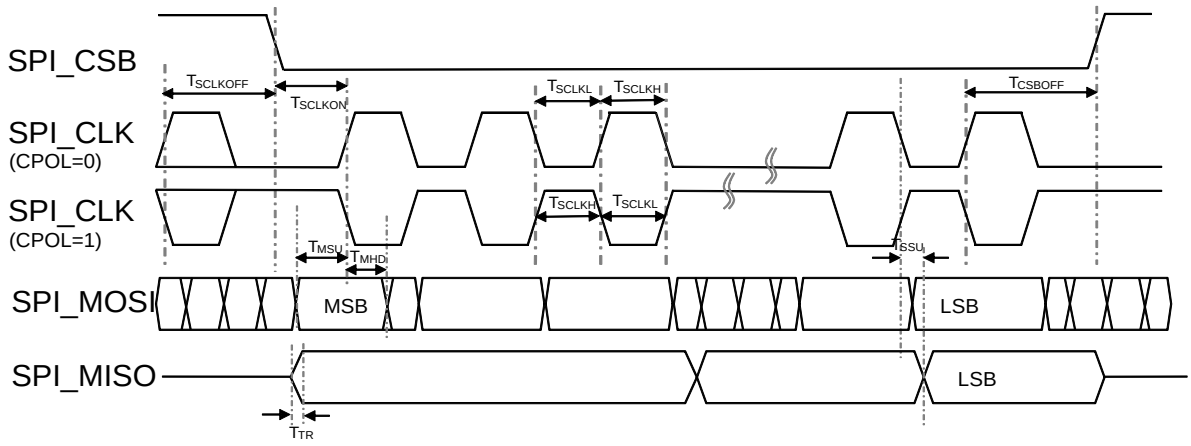

Figure 29. SPI slave timing diagram

Table 40 lists the timing parameters for the SPI slave.

Table 40. SPI slave timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}	-	-	50	MHz
SCLK clock duty		40	-	-	%
Non active duration	$T_{SCLKOFF}$	400	-	-	ns
1st CLK active rising transition time	T_{SCLKON}	T_{SCLKL} (CPOL = 0) T_{SCLKH} (CPOL = 1)	-	-	ns
CSB non active rising transition time	T_{CSBOFF}	T_{SCLKH} (CPOL = 0) T_{SCLKL} (CPOL = 1)	-	-	ns
MOSI setup time	T_{MSU}	8	-	T_{SCLK} (Note 1)	ns
MOSI hold time	T_{MHD}	8	-	T_{SCLK}	ns
MISO delay time	T_{SSU}	-	-	8	ns
MISO transition time (10% to 90% transition)	T_{TR}	-	4	5	ns

Note 1 TSCLK = 0.5 × (FSCLK x 106) -1 second.

9.4 SDIO

SDIO is a full/high speed card suitable for memory card and I/O card applications with low power consumption. The full/high speed card supports SPI, 1-bit SD, and 4-bit SD transfer modes at the full clock range of 0 to 50 MHz. To be compatible with the serviceable SDIO clock, the internal BUS clock needs to be set to a minimum of 50 MHz. The CIS and CSA areas are located inside the internal memory and the SDIO registers (CCCR and FBR) are programmed by the SD host.

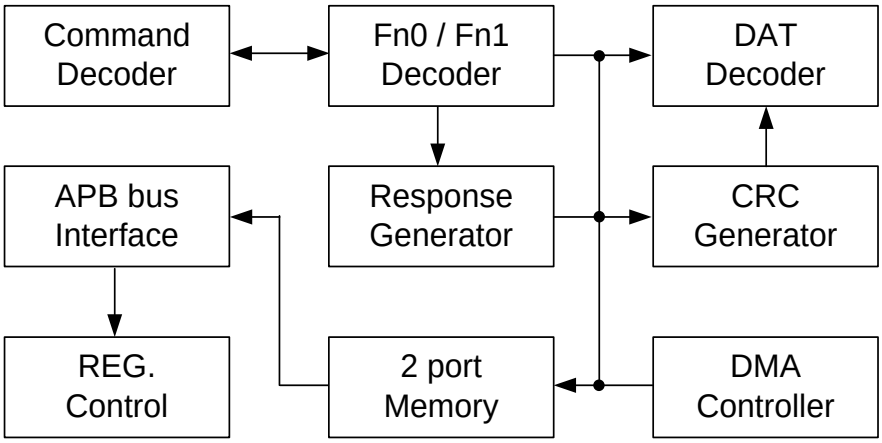

Figure 30. SDIO slave block diagram

Table 41 shows the pin definition of the SDIO interface.

The GPIOA4 and GPIOA5 pins are set to SDIO CMD and CLK by default. If SDIO initialization is completed and SDIO communication is enabled, then the SDIO data pin setting is done automatically. In other words, when the SDIO communication is detected, the pin used as the SDIO data among the GPIO pins is automatically activated in the SDIO use mode. However, the auto setting function is not supported for the F_xxx pin used as the Flash function.

Table 41. SDIO slave pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SDIO_CMD
GPIOA5	33	D2	I	SDIO_CLK
GPIOA9	29	H2	I/O	SDIO_D0
GPIOA8	30	G3	I/O	SDIO_D1
GPIOA7	31	E1	I/O	SDIO_D2
GPIOA6	32	E3	I/O	SDIO_D3

Figure 31 shows the timing diagram for the SDIO slave.

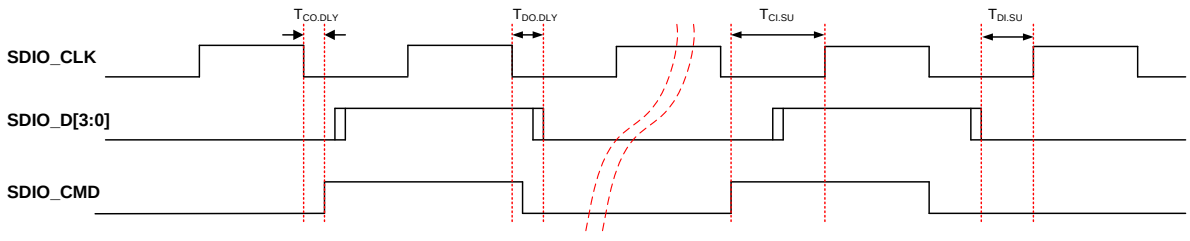

Figure 31. SDIO slave timing diagram

Table 42 lists the timing parameters for the SDIO slave.

Table 42. SDIO slave timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CLK frequency	F_{SCLK}	-	-	50	MHz
SDIO_CLK clock duty	-	-	50	-	%

Parameter	Symbol	Min	Typ	Max	Unit
SDIO_CMD input setup time	$T_{CI.SU}$	3	-	-	ns
SDIO_CMD output delay time	$T_{CO.DLY}$	-	-	11 (Note 1)	ns
SDIO_D[3:0] input setup time	$T_{DI.SU}$	3	-	-	ns
SDIO_D[3:0] output delay time	$T_{DO.DLY}$	-	-	11 (Note 1)	ns

Note 1 SDIO signals can set previous output from half cycle.

The SDIO interface requires pull-up resistors to be connected between the signal lines and the supply to enable communication.

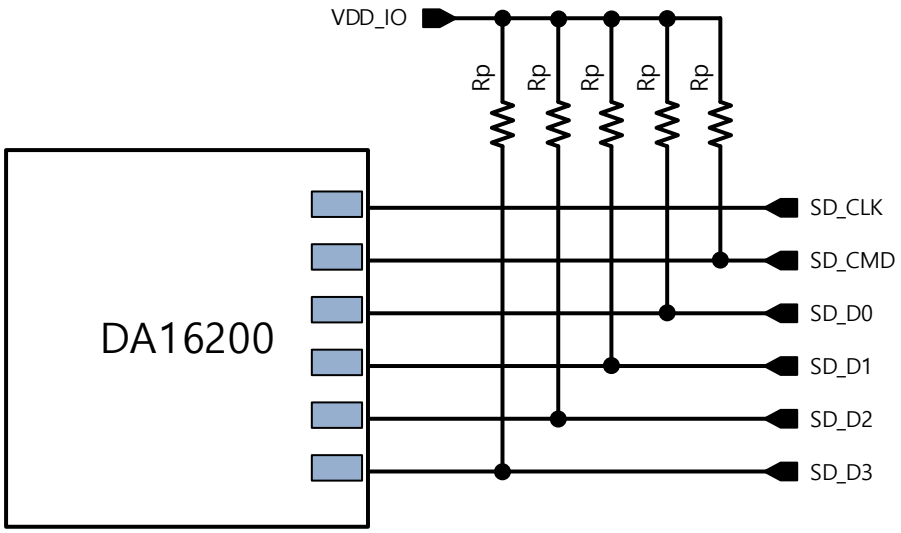

Figure 32. SDIO pull-up resistor

Pull-up resistor values may vary based on the board layout.

9.5 I2C Interface

9.5.1 I2C Master

The DA16200 includes an I2C master module. Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz), and High Speed (3.4 MHz) mode. Table 43 shows the pin definition of the I2C master interface.

Table 43. I2C master pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA1	38	C3	O	I2C_CLK
GPIOA5	33	D2	O	
GPIOA9	29	H2	O	
GPIOA0	39	A3	I/O	I2C_SDA
GPIOA4	34	F4	I/O	
GPIOA8	32	G3	I/O	

Figure 33 shows the I2C timing diagram. The timing diagram is the same as that of the I2C slave timing diagram.

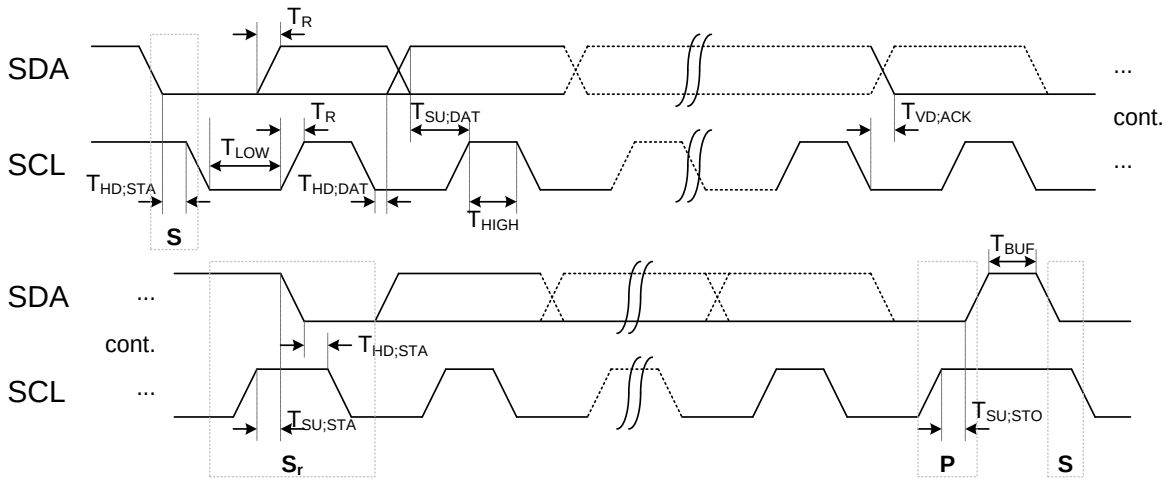

Figure 33. I2C master timing diagram

Table 44 lists the I2C master timing parameters.

Table 44. I2C master timing parameter

Parameter	Symbol	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
Operating bus clock frequency	F_{op_clk}	30	120	30	120	MHz
SCL clock frequency	F_{SCLK}	100	400	100	3400 (Note 2)	kHz
Clock duty (Note 1)	-	40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.2	-	0.2	-	µs
Low period of the SCL clock	T_{LOW}	1.27	-	0.55	-	µs
High period of the SCL clock	T_{HIGH}	1.23	-	0.45	-	µs
Setup time for START condition	$T_{SU;STA}$	1.1	-	0.37	-	µs
Data hold time	$T_{HD;DAT}$	3x T_{op_clk} (Note 3)	-	3x T_{op_clk} (Note 3)	-	µs
Data setup time	$T_{SU;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	-	T_{LOW} - $T_{HD;DAT}$	µs
Rise time of both SDA and SCL	T_R (Note 4)	0.02	0.3	0.05	0.05	µs
Setup time for STOP condition	$T_{SU;STO}$	0.36	-	0.45	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	3x T_{op_clk} (Note 3)	-	3x T_{op_clk} (Note 3)	-	µs
Buffer free time between START and STOP condition	T_{BUF}	0.5	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH/TSCLK) × 100[%], TSCLK = 1/FSCLK.

Note 2 Max. clock = 3.4 MHz (TSCLK = 294 ns) over 40 MHz of the Fop_clk.
Max. clock = 1.0 MHz (TSCLK = 1000 ns) under 40 MHz of the Fop_clk.

Note 3 Top_clk = (1/Fop_clk) x 106 µsec.

Note 4 TR depends on a pull-up resistor value.

9.5.2 I2C Slave

The I2C slave interface provides support for an external host to control the DA16200. The pin mux configuration is defined in Table 45. Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz) and High Speed (3.4 MHz).

Table 45. I2C slave pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA1	38	C3	I	I2C_CLK
GPIOA3	36	D4	I	
GPIOA5	33	D2	I	
GPIOA7	31	E1	I	
GPIOA0	39	A3	I/O	I2C_SDA
GPIOA2	37	B2	I/O	
GPIOA4	34	F4	I/O	
GPIOA6	32	E3	I/O	

Figure 34 shows the I2C slave timing diagram.

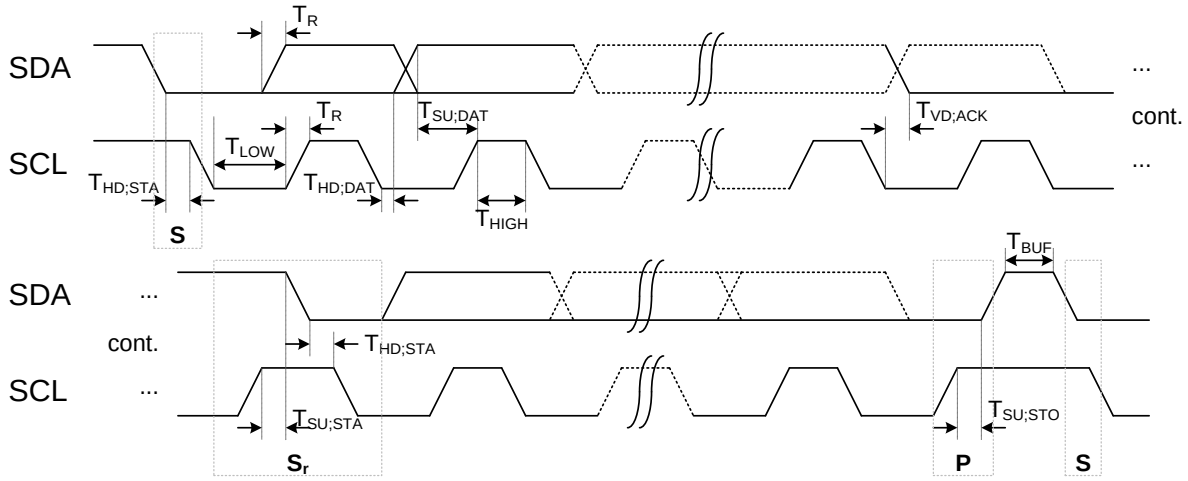

Figure 34. I2C slave timing diagram

Table 46 lists the I2C slave timing parameters.

Table 46. I2C slave timing parameters

Parameter	Description	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	F_{SCLK}	100	400	100	3400 (Note 2)	kHz
Clock duty (Note 1)	-	40	60	40	60	%
Hold time of START	$T_{HD;STA}$	0.6	-	0.26	-	µs
Low period of the SCL clock	T_{LOW}	1.3	-	0.15	-	µs
High period of the SCL clock	T_{HIGH}	1.2	-	0.14	-	µs
Setup time for START condition	$T_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$T_{HD;DAT}$	0	-	0	-	µs

Parameter	Description	Fast mode		High speed mode		Unit
		Min	Max	Min	Max	
Data setup time	$T_{SU;DAT}$	0.1	-	0.05	-	µs
Rise time of both SDA and SCL	T_R	0.02	0.3	-	0.12	µs
Setup time for STOP condition	$T_{SU;STO}$	0.6	-	0.26	-	µs
Data valid acknowledge time	$T_{VD;ACK}$	-	-	-	-	µs
Buffer free time between START and STOP condition	T_{BUF}	1.3	-	0.5	-	µs

Note 1 Clock duty ratio = (THIGH/TSCLK) × 100[%], TSCLK = 1/FSCLK.

Note 2 Max. clock = 3.4 MHz (TSCLK = 294 ns) over 40 MHz of the Fop_clk.
Max. clock = 1.0 MHz (TSCLK = 1000 ns) under 40 MHz of the Fop_clk.

9.5.3 Interface Pull-up

The I2C interface requires pull-up resistors to be connected between the signal lines and the supply to enable communication.

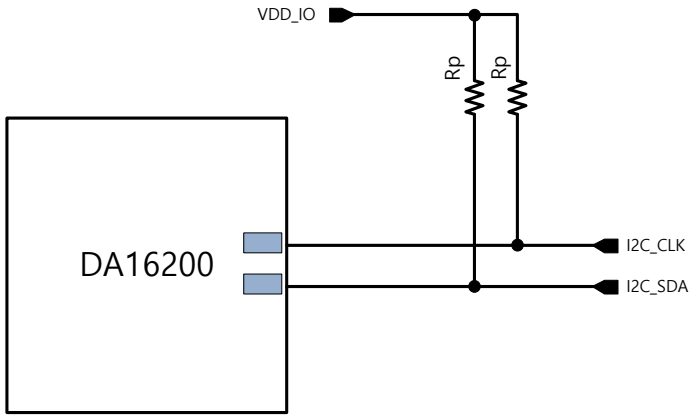

Figure 35. I2C pull-up resistor

Pull-up resistor values may vary based on the board layout.

9.6 SD/eMMC

The SD/eMMC host interface of the DA16200 provides access to SD or eMMC memory cards. The SD/eMMC host interface supports a 4-bit data bus with a maximum clock rate of 48 MHz giving a maximum data rate of 24 MB/s (192 Mbps). The SD/eMMC pin mux condition is defined in Table 47.

Table 47. SD/eMMC master pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA4	34	F4	I/O	SD/eMMC_CMD
GPIOA5	33	D2	O	SD/eMMC_CLK
GPIOA9	29	H2	I/O	SD/eMMC_D0
GPIOA8	30	G3	I/O	SD/eMMC_D1

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA7	31	E1	I/O	SD/eMMC_D2
GPIOA6	32	E3	I/O	SD/eMMC_D3
GPIOA10	28	F2	I	SD/eMMC_WRP
GPIOA1	38	C3	I	

9.6.1 Block Diagram

Figure 36 shows the block diagram of the SD/eMMC host interface including the control register, clock control, command/response pipe, data pipe, and AHB master interface blocks.

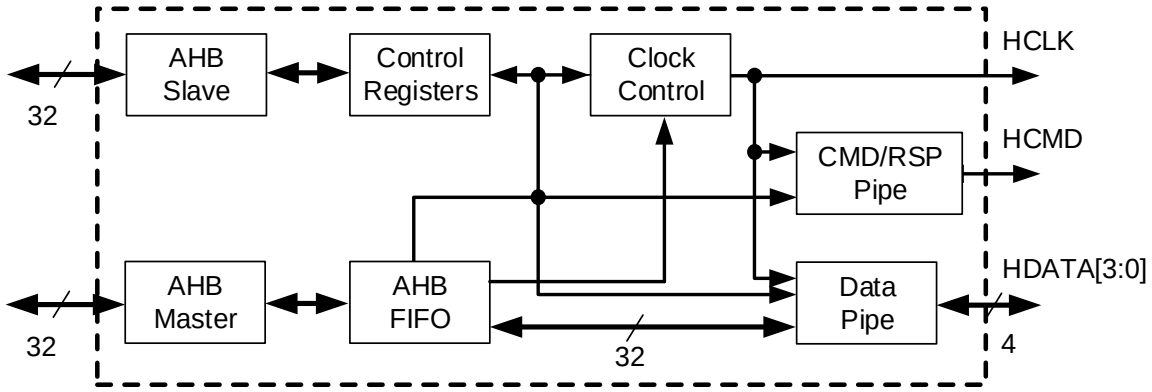

Figure 36. SD/eMMC block diagram

Figure 37 shows the timing diagram for the SD/eMMC master.

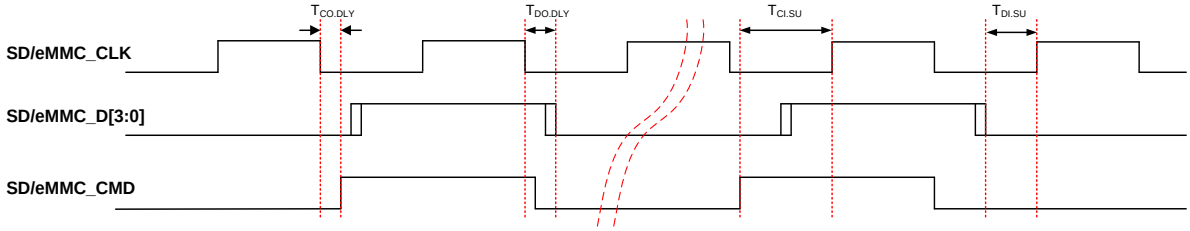

Figure 37. SD/eMMC master timing diagram

Table 48 lists the timing parameters for the SD/eMMC master.

Table 48. SD/eMMC master timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
SD/eMMC_CLK frequency	F_{SCLK}	-	-	50	MHz
SD/eMMC_CLK clock duty	-	-	50	-	%
SD/eMMC_CMD input setup time	$T_{CI.SU}$	8	-	-	ns
SD/eMMC_CMD output delay time	$T_{CO.DLY}$	-	-	3	ns
SD/eMMC_D[3:0] input setup time	$T_{DI.SU}$	8	-	-	ns
SD/eMMC_D[3:0] output delay time	$T_{DO.DLY}$	-	-	8	ns

9.7 I2S

The DA16200 provides an I2S interface. When an I2S block receives audio data through the DMA, that audio data is sent to the external port according to the I2S standard. To use the external DAC, output through the GPIO port is possible when a register setting is made according to the pin configuration (see Table 49).

The I2S also provides a receive function. However, I2S transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by register setting. If the I2S signal is input from outside after the reception function is set, the audio signal can be decoded, stored in the FIFO, and read

out through the DMA. The decodable reception function provides 8/16/24/32-bit modes and can receive either mono or stereo.

Using the I2S clock divider register, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24 MHz or 48 MHz. There is also a way to apply the I2S clock source directly from outside using the GPIO pin. For accurate I2S audio sampling, the I2S clock source can be input to external GPIO pins. It needs to select the GPIO pin setting as the I2S clock input and apply the appropriate clock source. The available I2S clock pins are shown in Table 49.

Table 49. I2S pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA1	38	C3	O	I2S_MCLK
GPIOA5	33	D2	O	
GPIOA9	29	H2	O	
GPIOA0	39	A3	O	I2S_BCLK
GPIOA4	34	F4	O	
GPIOA8	30	G3	O	
GPIOA3	36	D4	O	I2S_LRCK
GPIOA7	31	E1	O	
GPIOA2	37	B2	I/O	I2S_SDO
GPIOA6	32	E3	I/O	
GPIOA3	36	D4	I	I2S_CLK_IN
GPIOA10	28	F2	I	

9.7.1 Block Diagram

I2S has the following features:

- Master Clock Mode only
- I2S Data pin can work in either Input mode or Output mode
- Clock source can be "internal 480 MHz/N" (currently using 24 MHz) or "external clock source"
- Max Sampling Rate: 48 kHz
- Mono/Stereo Mode.

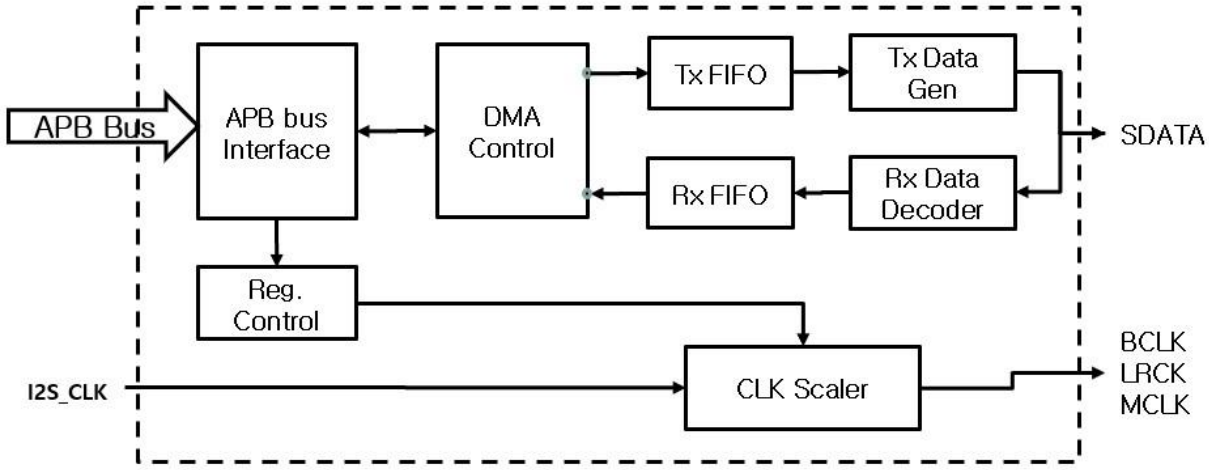

Figure 38. I2S block diagram

9.7.2 I2S Clock Scheme

The I2S uses a 24 MHz clock as default from the RF reference clock (40 MHz), so it can support 46.875 kHz of sampling rate. External clock sources are needed to support the standard sampling rate. See Table 50.

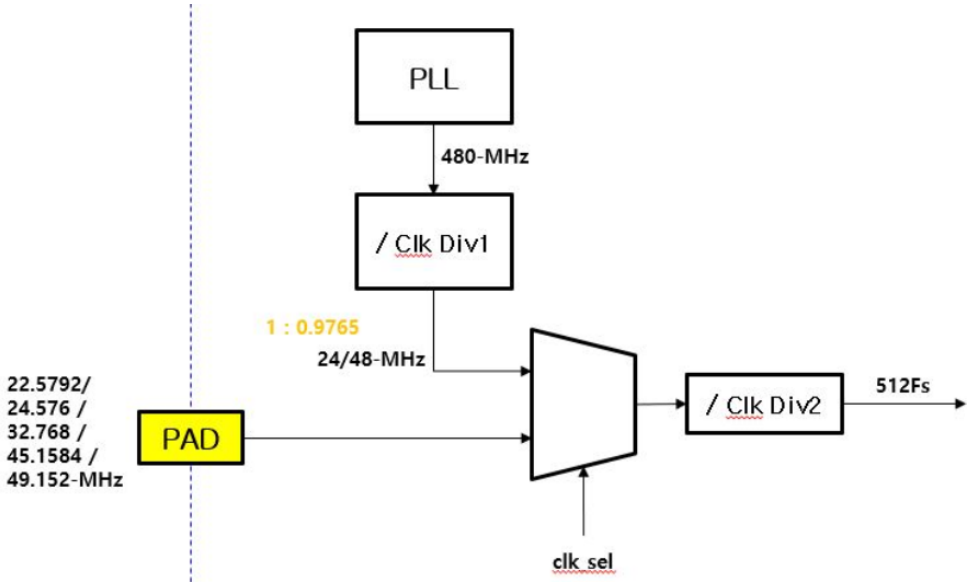

Figure 39. I2S clock scheme

Table 50. I2S clock selection guide

LRCK (kHz)	BCLK (MHz)	MCLK (MHz)	Clk Div2	Desired I2S_CLK (MHz) (Note 1)
8	0.512	4.096	6	24.576
12	0.768	6.144	4	24.576
16	1.024	8.192	3	24.576
24	1.536	12.288	2	24.576
32	2.048	16.384	2	32.768
44.1	2.8224	22.5792	1	22.5792
46.875	3	24	1	24 (Internal PLL)
48	3.072	24.576	1	24.576

Note 1 LRCK = Fs, BCLK = 64 × Fs, MCLK = 512 × Fs, Clk Div2 = N (1, 2, 3...).

NOTE
To confirm the exact LRCK operation, drive the Clock source from I2S_CLK.

9.7.3 I2S Transmit and Receive Timing Diagram

I2S output is available in the following three modes. The main clock (MCLK) always outputs 512×fs.

- I2S Mode

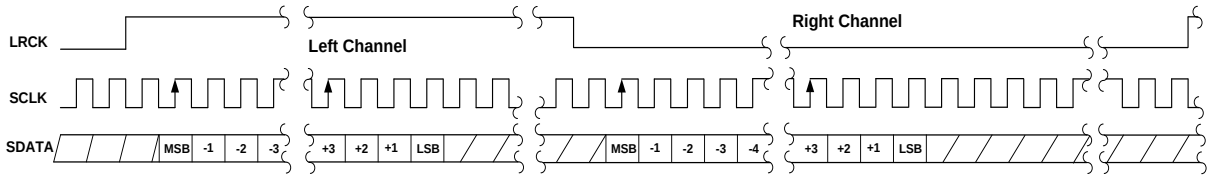

Figure 40. I2S timing diagram

- Left Justified Mode

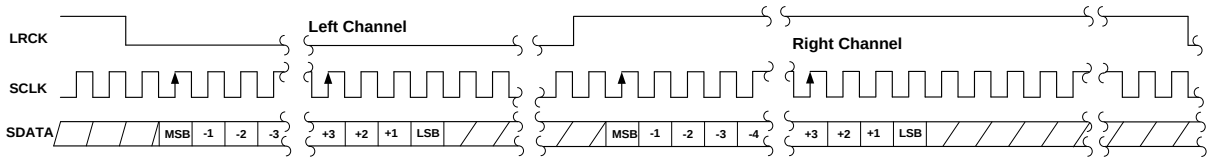

Figure 41. Left justified mode timing diagram

- Right Justified Mode

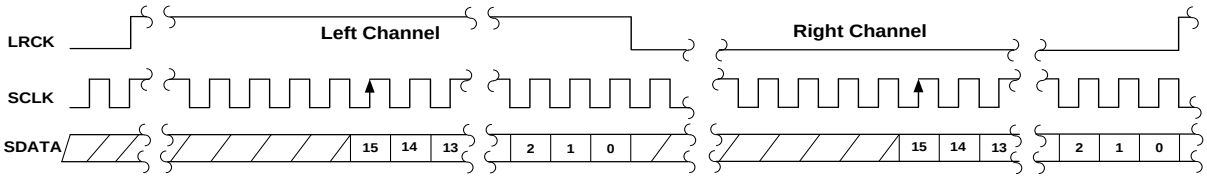

Figure 42. Right justified mode timing diagram

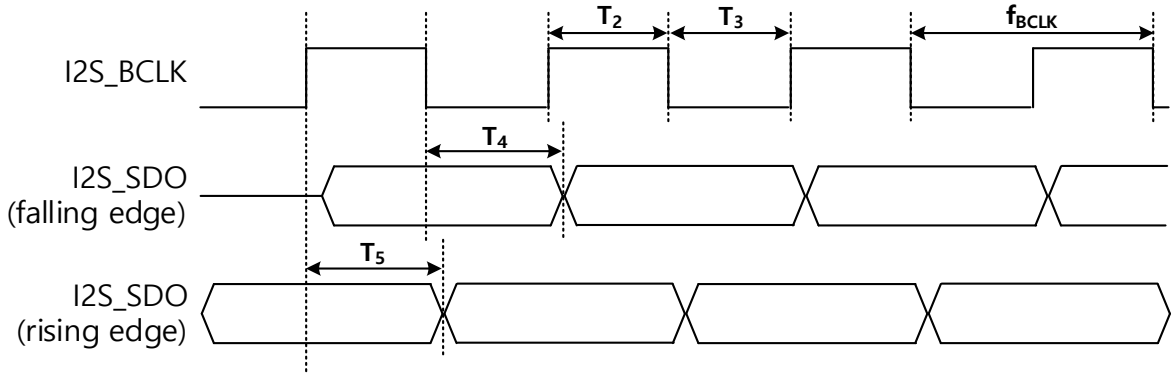

Figure 43. I2S transmit timing diagram

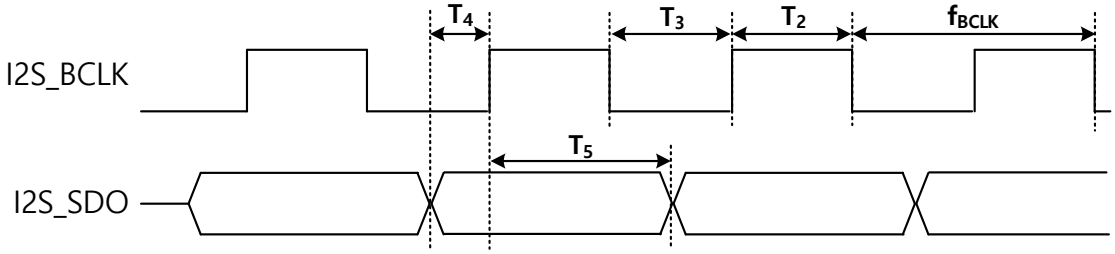

Figure 44. I3S receive timing diagram

Table 51. I2S transmit timing parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-	-	3.072	MHz
High period of the BCLK clock	T_2	-	-	½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-	-	½ f_{BCLK}	ns
I2S_SDO output hold (falling edge)	T_4	160	-	-	ns
I2S_SDO output hold (rising edge)	T_5	160	-	-	ns

Table 52. I2S receive timing parameters

Description	Timing	Min	Typ	Max	Unit
I2S_BCLK frequency	f_{BCLK}	-	-	3.072	MHz
High period of the BCLK clock	T_2	-	-	½ f_{BCLK}	ns
Low period of the BCLK clock	T_3	-	-	½ f_{BCLK}	ns
I2S_SDO input setup time	T_4	15	-	-	ns
I2S_SDO input hold time	T_5	60	-	-	ns

9.8 ADC (Aux 12-bit)

9.8.1 Overview

The DA16200 includes a high precision, ultra-low power, and wide dynamic range SAR ADC with a 12-bit resolution. It has a 4-channel single-end ADC. Analog input is measured by four pins from GPIOA0 to GPIOA3, and pin selection is changed through the register setting. Figure 45 shows the control block diagram.

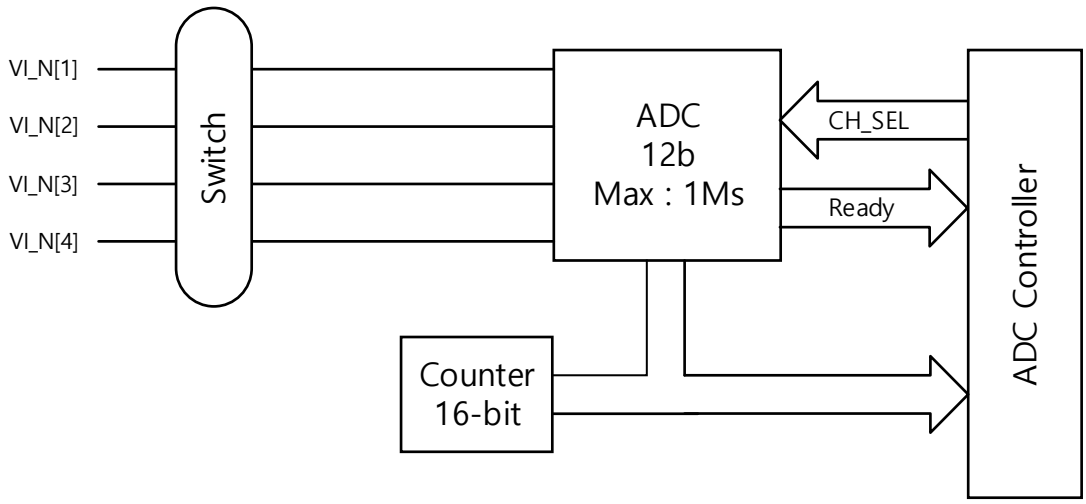

Figure 45. ADC control block diagram

9.8.2 Timing Diagram

The input is digitized at a maximum of 1.0 MSPS throughput rate. And the maximum input clock rate is 15 MHz. Figure 46 shows the conversion timing, and Table 53 describes the DC specifications.

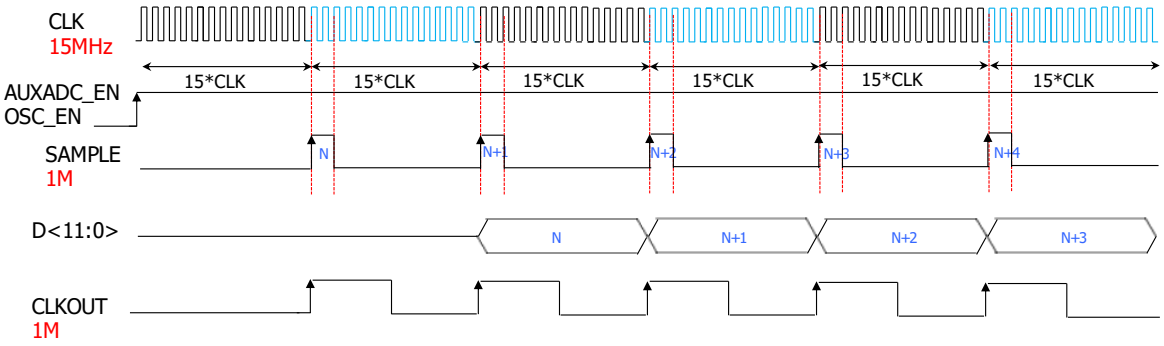

Figure 46. 12-bit ADC timing diagram

Table 53. DC specification

Description	Min	Typ	Max	Unit
Resolution	4	12	12	Bits
Max clock input	-	-	15	MHz
Conversion frequency	-	-	1	MHz
Accuracy: SNR SNDR	-	 67.2 61.7	-	dB
Analog input voltage	0	-	1.4	V
Reference voltage	-	0.7		V

9.8.3 DMA Transfer

There are four ADC channel settings available. When the input data of each channel reaches the FIFO level, it is possible to read the data through the DMA path.

9.8.4 Sensor Wake-up

The DA16200 has an external sensor wake-up function that uses the analog input signal through an Aux ADC. Even in Sleep mode 2 and 3, it detects the change of an external analog signal, wakes up from Sleep mode 2 and 3, and converts the DA16200 into a normal operation. This function can be used in up to four channels. Also, when multiple external sensors are used, analog signals are detected while the channel are automatically

changed. For example, if all four channels are set as input sources which have their threshold registers respectively, the channels are measured sequentially from 0 to 3.

If one of the four values exceeded the allowed range of values set by the threshold register, the DA16200 awakes from the Sleep mode 2 and 3. The value setting of the input change can be either over threshold or under threshold.

9.8.5 ADC Ports

Table 54 shows the pin definition of the ADC.

Table 54. ADC pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA3	36	D4	A	Analog signal
GPIOA2	37	B2	A	Analog signal
GPIOA1	38	C3	A	Analog signal
GPIOA0	39	A3	A	Analog signal

9.9 GPIO

All digital pads can be used as GPIO, and each GPIO port is mixed with a multi-functional interface. The GPIO features of the DA16200 are as follows:

- Programmable direction (input/output)
- Word and halfword read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- Maskable interrupt generation based on input value change
- Each GPIO output can be configured as either PWM[3:0], external interrupt, QSPI_CSB[3:1], RF_SW[1:0], or UART_TXDOE[2:0].

9.9.1 Antenna Switching Diversity

The DA16200 provides the antenna switching diversity function for performance improvement in a multi-path environment. A PHY block measures the RSSI of each antenna and selects the antenna with the largest RSSI. The selected antenna is also used for transmission. To use this function, an external switching element is required, and switching control is done through GPIOs. Two GPIOs can be used for switching control, and for this purpose any unused pins among the GPIO pins can be selected. The control signal can be changed by register setting to suit the external switching device.

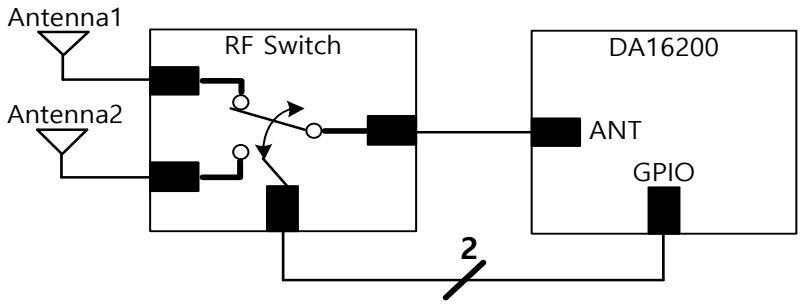

Figure 47. Antenna switching internal block diagram

If the Antenna Switching Diversity function is enabled, the function is automatically performed by PHY hardware block. The basic operation scheme is as follows:

- The antenna's RSSI decision is made for 11b PPDU, except for 11g/n PPDU.
- When PHY hardware detects the existence of 11b PPDU, it stores the RSSI.
- After the switch to another antenna, the RSSI is stored, and a decision is made about which antenna has better RSSI.

- This operation is done during 11b PPDU's preamble duration to protect corruption of 11b PPDU data reception.
- The decided antenna is not changed until there is a new 11b PPDU.

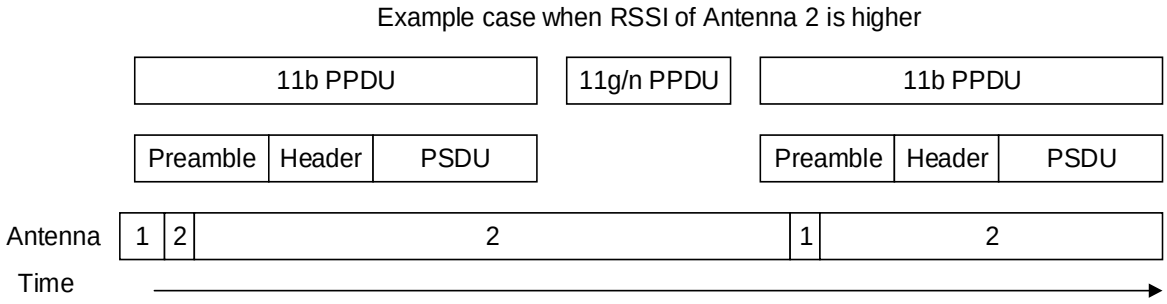

Figure 48. Antenna switching timing diagram

NOTE
This antenna switching diversity is different from Maximum Ratio Combining (MRC).

9.10 UART

The DA16200 provides three UARTs, features of which are described:

- Programmable use of UART (UART1 and UART2)
- Support both byte and word access for reduction of bus burden
- Support both RS-232 and RS-485
- Separate 32×8 bit transmit and 32×12 bit receive FIFO memory buffers to reduce CPU interrupts
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator
- Standard asynchronous communication bits (start, stop, and parity), which are added prior to transmission and removed on reception
- Independent masking of transmit FIFO, receive FIFO, and receive timeout
- Support for DMA
- False start bit detection
- Programmable flow control (CTS/RTS, UART1)
- Fully programmable serial interface characteristics:
  - Data can be of 5, 6, 7, or 8 bits
  - Even, odd, stick, or no-parity bit generation and detection
  - 1- or 2- stop bit generation
  - Baud rate generation.

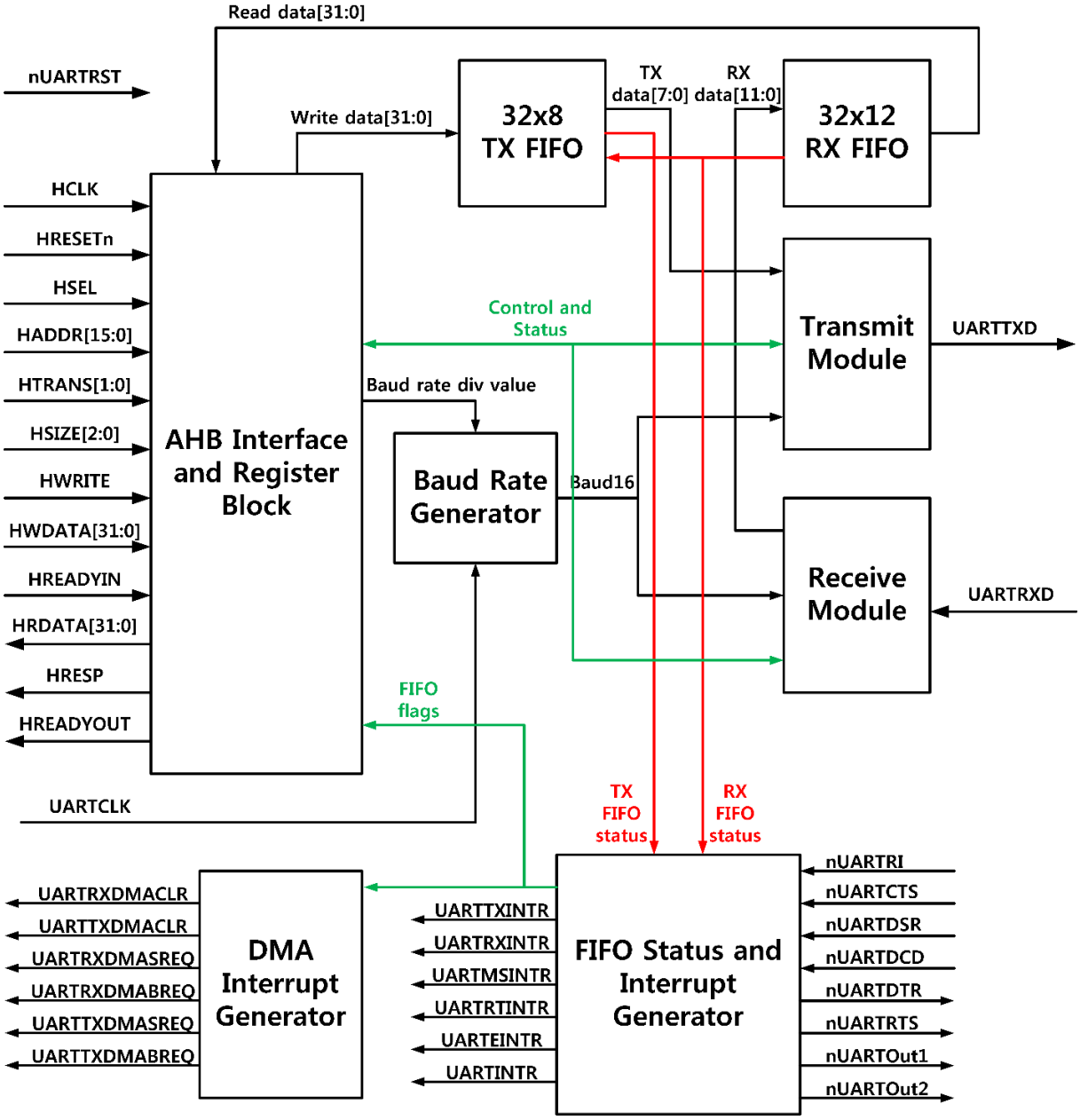

Figure 49. DA16200 UART block diagram

9.10.1 RS-232

As the serial communication between the UART and the selected device is asynchronous, additional bits (start and stop) are inserted into the data line to indicate the beginning and end. With these bits, two devices can be synchronized. This structure of serial data accompanied by start and stop bits is referred to as a character, see Figure 50.

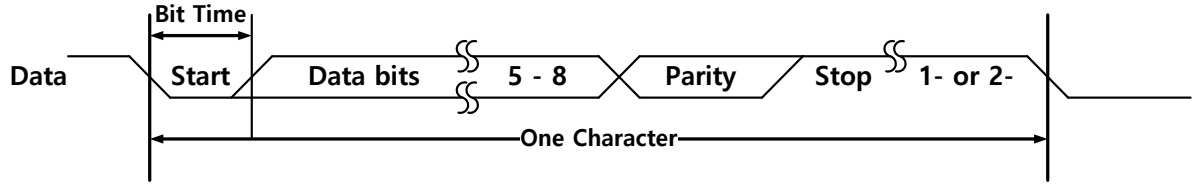

Figure 50. Serial data format

An additional parity bit may be added to the serial character. This bit appears between the last data bit and the stop bit(s) in the character structure. It provides the UART with the ability to do simple error checking on the received data.

The UART Line Control Register is used to control the serial character characteristics. The individual bits of the data word are sent after the start bit, starting with the least significant bit (LSB). These are followed by the optional parity bit, followed by the stop bit(s), which can be 1 or 2.

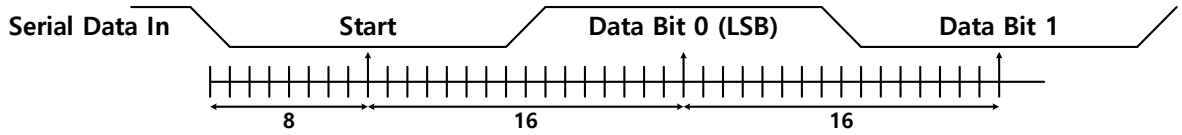

Figure 51. Serial input data sampling points

All the bits in the transmission are transmitted for the same time duration. This is referred to as a Bit Period or Bit Time. One Bit Time equals 16 baud clocks. To ensure stability on the line, the receiver samples the serial input data at approximately the mid-point of the Bit Time when the start bit is detected. As the exact number of baud clocks that each bit was transmitted for is known, calculating the mid-point for sampling is not difficult, that is every 16 baud clocks after the mid-point sample of the start bit. Figure 51 shows the sampling points of the first couple of bits in a serial character.

9.10.2 RS-485

DA16200 UART supports RS-485. A UART485EN register (0x054) is required to be assigned to enable the RS-485. To use RS-485, an additional signal (UARTTXDOE) is required to notice TXD intervals. This signal can be an output by selecting any of the unused GPIO pins.

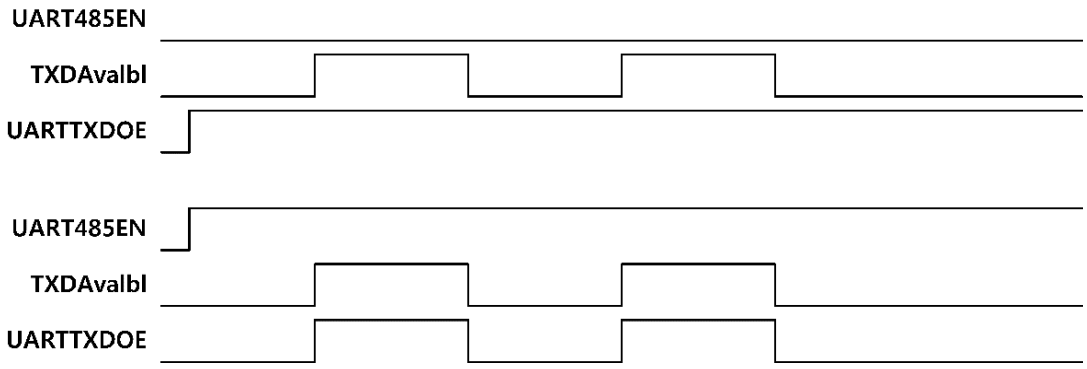

Figure 52. UARTTXDOE output signal for UART RS-485

9.10.3 Baud Rate

The UART clock frequency (FUARTCLK) is fixed at 80 MHz. The Baud Rate Divisor can be calculated as (FUARTCLK/(16 x Baud Rate)). The Baud Rate Divisor is comprised of the integer part (UART_INTBRDIV) and fractional part (UART_FRABRDIV). The maximum baud rate of DA16200 UART is 2.5 MBaud.

The following example shows how to calculate the divisor value.

If the required baud rate is 921600 with 80 MHz FUARTCLK, the Baud Rate Divisor becomes:

(8 x 107)/(16 x 921600) = 5.425

This means that the integer value is 5 and the fractional value is 0.425.

Then, the fraction part becomes an integer (0.425 x 64) + 0.5) = 27.

Then, the generated baud rate divider is 5 + 27/64 = 5.422.

Finally, the generated baud rate becomes (8 x 107)/(16 x 5.422) = 922169.

And the error between the required baud rate and the generated baud rate is:

(922169 – 921600)/921600 x100 = 0.062%.

9.10.4 Hardware Flow Control

The hardware flow control feature is fully selectable, and serial data flow is controlled by using nUARTRTS output and nUARTCTS input signals. Figure 53 shows how two different UARTs can communicate using hardware flow control.

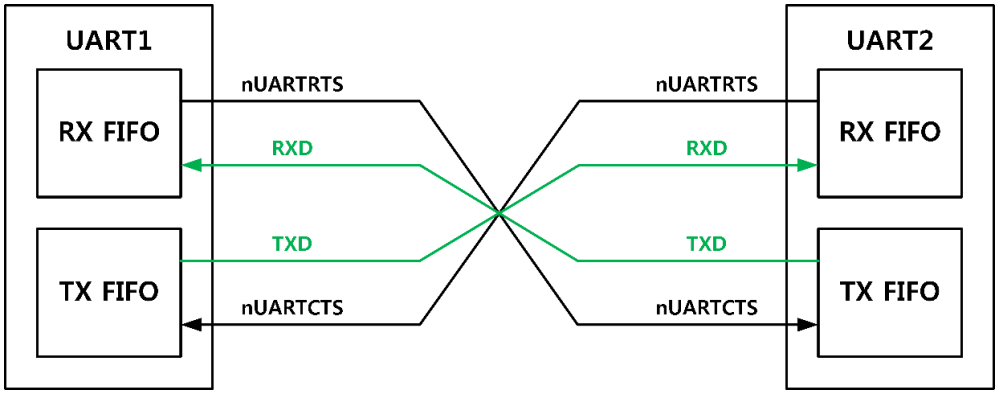

Figure 53. UART hardware flow control

When RTS flow control is enabled, nUARTRTS signal is asserted until the receive FIFO is filled up to programmed level. When CTS flow control is enabled, the transmitter can transmit the data when the nUARTCTS signal is asserted. CTSEn (CTS enable) and RTSEn (RTS enable) bits are determined by 14th (RTS) and 15th bit (CTS) of UARTCR register.

Table 55. Control bits to enable/disable hardware flow control

CTSEn	RTSEn	Description
1	1	Both RTS and CTS flow control are enabled.
1	0	Only CTS flow control is enabled.
0	1	Only RTS flow control is enabled.
0	0	Both RTS and CTS flow control are disabled.

9.10.5 Interrupts

DA16200 UART block provides five interrupt signals by separate interrupt lines. Conditions of each interrupt are Modem Status, Receive FIFO Request, Transmit FIFO Request, Receive Timeout, and Reception Error. These conditions are logically ORed to provide a single combined interrupt, UARTINTR. Table 56 shows the interrupt signals.

Table 56. UART interrupt signals

Signal name	Description
UARTMSINTR	UART Modem Status Interrupt.
UARTRXINTR	UART Receive FIFO Interrupt.
UARTTXINTR	UART Transmit FIFO Interrupt.
UARTRTINTR	UART Receive Timeout Interrupt.
UARTEINTR	UART Error Interrupt.
UARTINTR	UART Interrupt. Five Interrupt signals are combined by OR function.

9.10.6 DMA Interface

DA16200 UART block can generate DMA request signals with register settings by using a DMA interrupt generator module to connect to DA16200 DMA Controller (DMA1). The DMA operation of the UART is controlled with the DMA Control Register.

DA16200 UART provides four DMA signals and receives two DMA signals, two signals to transmit (TXDMASREQ, TXDMABREQ), which are cleared by a TX clear signal (TXDMACLR) and two signals to receive (RXDMASREQ, RXDMABREQ), which are cleared by a RX clear signal (RXDMACLR). When the DMA interface is not used, the TXDMACLR and RXDMACLR lines should be connected to a logic 0.

Table 57 shows the pin definition of the UART interface.

Table 57. UART pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOA3	36	D4	A	Analog signal

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
UART0_RXD	12	M10	I	UART0_RXD
UART0_TXD	11	L9	O	UART0_TXD
GPIOA7	31	E1	I	UART1_RXD
GPIOA5	33	D2	I	
GPIOA3	36	D4	I	
GPIOA1	38	C3	I	
GPIOA6	32	E3	O	UART1_TXD
GPIOA4	34	F4	O	
GPIOA2	37	B2	O	
GPIOA0	39	A3	O	
GPIOA5	33	D2	I	UART1_CTS
GPIOA4	34	F4	O	UART1_RTS
GPIOA11	27	G1	I	UART2_RXD
GPIOC7	9	K12	I	
GPIOA10	28	F2	O	UART2_TXD
GPIOC6	10	L11	O	

9.11 PWM

Pulse Width Modulation (PWM) is a modulation technique used to encode a message into a pulse signal. The blocks are designed to adjust output pulse duration by the CPU bus clock (HCLK). Figure 54 shows the structure of the PWM block.

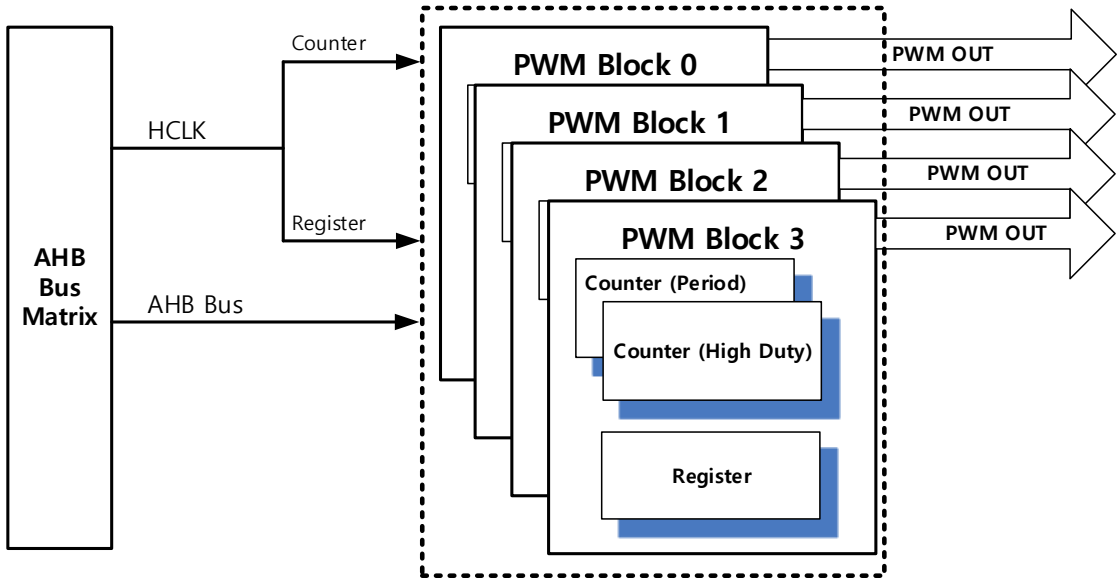

Figure 54. PWM block diagram

Table 58 shows the pin definition of the PWM interface. GPIOx means that PWM signals can go out through any GPIO pins through a register setting.

Table 58. PWM pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
GPIOx	-	-	-	PWM[3:0] output

9.11.1 Timing Diagram

Table 59 shows the relation between the internal bus clock and PWM output wave patterns. Figure 55 shows the conversion timing diagram. **a** and **b** can be adjusted through the register setting, and PWM wave patterns vary depending on the ratio. **a** controls the high width of pulses (nCycle High) while **b** controls the general cycle (nCycle Period).

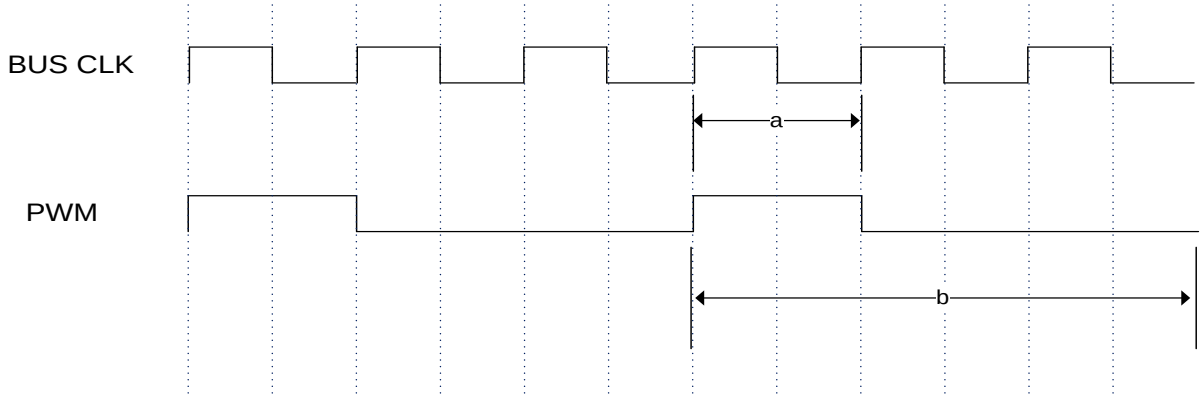

Figure 55. PWM timing diagram

Table 59. PWM timing diagram description

Time	Description
a	Bus Clock Period × (nCycle High + 1)
b	Bus Clock Period × (nCycle Period + 1)

9.12 Debug Interface

The DA16200 supports both IEEE Standard 1149.1 JTAG (5-wire) and the low-pin-count Arm SWD (2-wire, TCLK/TMS) debug interfaces. The SWD protocol provides the same debug features as JTAG.

The JTAG port is an IEEE standard that defines a test access port (TAP) and boundary scan architecture for digital integrated circuits and provides a standardized serial interface to control the associated test logic. For detailed information on the operation of the JTAG port and TAP controller, see Ref. [5].

Figure 56 shows the JTAG timing diagram.

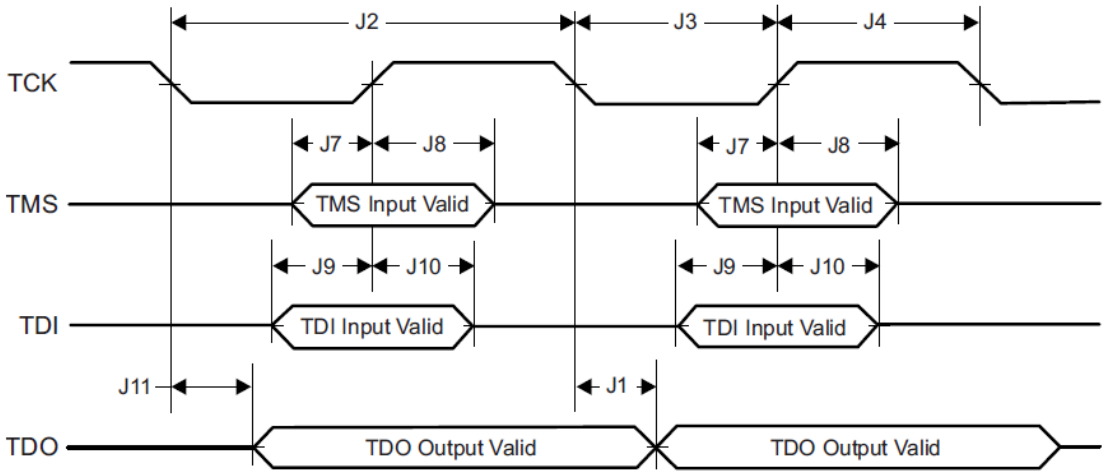

Figure 56. JTAG timing diagram

Table 60 shows the JTAG timing parameters.

Table 60. JTAG timing parameters

Parameter Number	Parameter	Parameter Name	Min	Max	Unit
J1	f_{TCK}	Clock Frequency	-	15	MHz
J2	t_{TCK}	Clock Period	-	$1/f_{TCK}$	ns
J3	t_{CL}	Clock Low Period	-	$t_{TCK}/2$	ns
J4	t_{CH}	Clock High Period	-	$t_{TCK}/2$	ns
J7	t_{TMS_SU}	TMS Setup Time	1	-	-
J8	t_{TMS_HO}	TMS Hold Time	16	-	-
J9	t_{TDI_SU}	TDI Setup Time	1	-	-
J10	t_{TDI_HO}	TDI Hold Time	16	-	-
J11	t_{TDO_HO}	TDO Hold Time	-	15	-

Table 61 shows the pin definition of the JTAG interface.

Table 61. JTAG pin configuration

Pin name	Pin number		I/O	Function name
	QFN	fcCSP		
TMS (Note 1)	6	J11	I/O	Data
TCLK (Note 2)	7	J9	I	Clock
GPIOC8	8	K10	I	TDI: Data Input
GPIOC7	9	K12	O	TDO: Data Output
GPIOC6	10	L11	I	nTRST: Reset

Note 1 For SWD, TMS = SWDIO, a bidirectional signal.

Note 2 For SWD, TCLK = SWCLK.

NOTE
The SWD protocol provides the same debug features as JTAG.

9.13 Bluetooth® Coexistence

The DA16200 provides a Bluetooth coexistence function to properly coordinate the use of the 2.4 GHz Wi-Fi radio with external devices that also use a 2.4 GHz radio such as Bluetooth.

9.13.1 Interface Configuration

The following three pins can be set in pin multiplexing:

- BT_sig0 (oWlanAct)
  - Output - indicates WLAN is currently active.
- BT_sig1 (iBtAct)
  - Input - indicates Bluetooth®/Bluetooth® LE is currently active.
- BT_sig2 (iBTPri)
  - Input (optional) - indicates Bluetooth®/Bluetooth® LE has higher priority than WLAN.

A variety of configuration settings are available, including active high/low, manual force mode, use status of the optional iBTPri function, and whether to switch oWlanAct to active in the event of TX/RX/TRX.

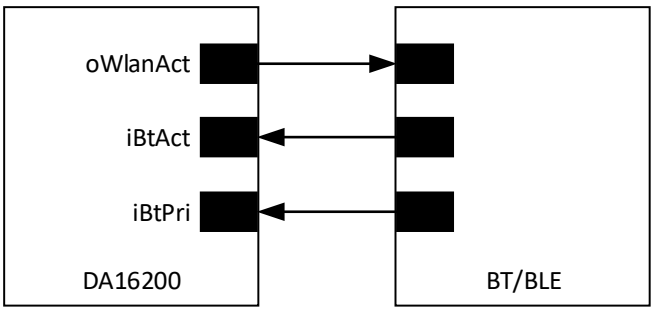

Figure 57. Bluetooth coexistence Interface

9.13.2 Operation Scenario

Bluetooth coexistence can be enabled/disabled through configuration registers. The activation scenarios based on the status of each pin are described:

- BT_sig0 (oWlanAct)
  - When asserted, the external Bluetooth®/Bluetooth LE device is expected to stop occupying RF.
- BT_sig1 (iBtAct)
  - When asserted, the DA16200 stops occupying RF.
- BT_sig2 (iBTPri)
  - Optional and thus may not be used.
  - When iBtPri is active, the DA16200 stops occupying the RF when iBtAct is active even if a Wi-Fi transmission is in progress.

10. Register Map

10.1 GPIO Register

Table 62. GPIO registers

Address	Register	Description
Common control for GPIO Pin status		
0x5000_1208	GPIO_FSEL_GPIO1_REG	Function Selection of the GPIOA Register
0x5000_120C	GPIO_FSEL_GPIO2_REG	Function Selection of the GPIOB and GPIOC Register
0x5000_1218	GPIO_UART_PAD_REG	Function Selection of the UART Pad Register
0x5000_121C	GPIO_JTAG_PAD_REG	Function Selection of the JTAG Pad Register
0x5000_1220	GPIOA_DS_REG	GPIOA Driving Strength Control Register
0x5000_1224	GPIOA_SR_REG	GPIOA Slew Rate Control Register
0x5000_1228	GPIOA_PE_PS_REG	GPIOA Pull-up/Pull-down Control Register
0x5000_122C	GPIOA_IE_IS_REG	GPIOA Input enable/CMOS Control Register
0x5000_1234	GPIO_FLASH_PAD_REG	External Flash PAD Control Register
0x5000_1238	GPIOB_DS_REG	GPIOB Driving Strength Control Register
0x5000_123C	GPIOB_SR_REG	GPIOB Slew Rate Control Register
0x5000_1240	GPIOB_PE_PS_REG	GPIOB Pull-up/Pull-down Control Register
0x5000_1244	GPIOB_IE_IS_REG	GPIOB Input Enable/CMOS Control Register
0x5000_1248	GPIOC_DS_REG	GPIOC Driving Strength Control Register
0x5000_124C	GPIOC_SR_REG	GPIOC Slew Rate Control Register
0x5000_1250	GPIOC_PE_PS_REG	GPIOC Pull-up/Pull-down Control Register
GPIO In/Out control		
0x4001_0000	GPIOA_DIN_REG	GPIOA Input Value Register
0x4001_0004	GPIOA_DOUT_REG	GPIOA Output Value Register
0x4001_0008	Reserved	-
0x4001_000C	Reserved	-
0x4001_0010	GPIOA_DOUT_SET_REG	GPIOA Data Output Enable Set Register
0x4001_0014	GPIOA_DOUT_CLR_REG	GPIOA Data Output Clear Register
0x4001_0018	GPIOA_FUNC_SET_REG	GPIOA Alternate Function Output Enable Set Register
0x4001_001C	GPIOA_FUNC_CLR_REG	GPIOA Alternate Function Output Clear Register
0x4001_0020	GPIOA_INTR_SET_REG	GPIOA Interrupt Enable Set Register
0x4001_0024	GPIOA_INTR_CLR_REG	GPIOA Interrupt Enable Clear Register
0x4001_0028	GPIOA_INTR_TYPE_SET_REG	GPIOA Interrupt Type Set Register
0x4001_002C	GPIOA_INTR_TYPE_CLR_REG	GPIOA Interrupt Type Clear Register
0x4001_0030	GPIOA_INTR_POL_SET_REG	GPIOA Interrupt Polarity Set Register
0x4001_0034	GPIOA_INTR_POL_CLR_REG	GPIOA Interrupt Polarity Clear Register
0x4001_0038	GPIOA_INTR_STS_REG	GPIOA Interrupt Status Register
0x4001_003C	GPIOA_FUNC_OUT_EN_REG	GPIOA Alternate Function Output Enable Register
0x4001_0FC0	GPIOA_PWM_OUT_SEL_REG	GPIOA PWM_OUT[3:0] Port Selection Register
0x4001_0FC4	GPIOA_mSPI_CS_SEL_REG	GPIOA mSPI_CSB[3:1] and Ext_Intr Port Selection Register
0x4001_0FC8	GPIOA_RF_SW_SEL_REG	GPIOA RF_SW[2:1] Port Selection Register
0x4001_0FCC	GPIOA_UART_SEL_REG	GPIOA UART_TXDOE[3:0] Port Selection Register
0x4001_1000	GPIOB_DIN_REG	GPIOB Input Value Register
0x4001_1004	GPIOB_DOUT_REG	GPIOB Output Value Register
0x4001_1008	Reserved	-
0x4001_100C	Reserved	-
0x4001_1010	GPIOB_DOUT_SET_REG	GPIOB Data Output Enable Set Register
0x4001_1014	GPIOB_DOUT_CLR_REG	GPIOB Data Output Clear Register

Address	Register	Description
0x4001_1018	GPIOB_FUNC_SET_REG	GPIOB Alternate Function Output Enable Set Register
0x4001_101C	GPIOB_FUNC_CLR_REG	GPIOB Alternate Function Output Clear Register
0x4001_1020	GPIOB_INTR_SET_REG	GPIOB Interrupt Enable Set Register
0x4001_1024	GPIOB_INTR_CLR_REG	GPIOB Interrupt Enable Clear Register
0x4001_1028	GPIOB_INTR_TYPE_SET_REG	GPIOB Interrupt Type Set Register
0x4001_102C	GPIOB_INTR_TYPE_CLR_REG	GPIOB Interrupt Type Clear Register
0x4001_1030	GPIOB_INTR_POL_SET_REG	GPIOB Interrupt Polarity Set Register
0x4001_1034	GPIOB_INTR_POL_CLR_REG	GPIOB Interrupt Polarity Clear Register
0x4001_1038	GPIOB_INTR_STS_REG	GPIOB Interrupt Status Register
0x4001_103C	GPIOB_FUNC_OUT_EN_REG	GPIOB Alternate Function Output Enable Register
0x4001_1FC0	GPIOB_PWM_OUT_SEL_REG	GPIOB PWM_OUT[3:0] Port Selection Register
0x4001_1FC4	GPIOB_mSPI_CS_SEL_REG	GPIOB mSPI_CSB[3:1] and Ext_Intr Port Selection Register
0x4001_1FC8	GPIOB_RF_SW_SEL_REG	GPIOB RF_SW[2:1] Port Selection Register
0x4001_1FCC	GPIOB_UART_SEL_REG	GPIOB UART_TXDOE[3:0] Port Selection Register
0x4001_7000	GPIOC_DIN_REG	GPIOC Input Value Register
0x4001_7004	GPIOC_DOUT_REG	GPIOC Output Value Register
0x4001_7008	Reserved	-
0x4001_700C	Reserved	-
0x4001_7010	GPIOC_DOUT_SET_REG	GPIOC Data Output Enable Set Register
0x4001_7014	GPIOC_DOUT_CLR_REG	GPIOC Data Output Clear Register
0x4001_7018	GPIOC_FUNC_SET_REG	GPIOC Alternate Function Output Enable Set Register
0x4001_701C	GPIOC_FUNC_CLR_REG	GPIOC Alternate Function Output Clear Register
0x4001_7020	GPIOC_INTR_SET_REG	GPIOC Interrupt Enable Set Register
0x4001_7024	GPIOC_INTR_CLR_REG	GPIOC Interrupt Enable Clear Register
0x4001_7028	GPIOC_INTR_TYPE_SET_REG	GPIOC Interrupt Type Set Register
0x4001_702C	GPIOC_INTR_TYPE_CLR_REG	GPIOC Interrupt Type Clear Register
0x4001_7030	GPIOC_INTR_POL_SET_REG	GPIOC Interrupt Polarity Set Register
0x4001_7034	GPIOC_INTR_POL_CLR_REG	GPIOC Interrupt Polarity Clear Register
0x4001_7038	GPIOC_INTR_STS_REG	GPIOC Interrupt Status Register
0x4001_703C	GPIOC_FUNC_OUT_EN_REG	GPIOC Alternate Function Output Enable Register
0x4001_7FC0	GPIOC_PWM_OUT_SEL_REG	GPIOC PWM_OUT[3:0] Port Selection Register
0x4001_7FC4	GPIOC_mSPI_CS_SEL_REG	GPIOC mSPI_CSB[3:1] and Ext_Intr Port Selection Register
0x4001_7FC8	GPIOC_RF_SW_SEL_REG	GPIOC RF_SW[2:1] Port Selection Register
0x4001_7FCC	GPIOC_UART_SEL_REG	GPIOC UART_TXDOE[3:0] Port Selection Register

Table 63. GPIO_FSEL_GPIO1_REG (0x5000_1208)

Bit	Mode	Symbol	Description	Reset
31:30	R/W	FSEL_GPIO1	Pin function selection for GPIOA[15]	0x0
29:28	R/W	FSEL_GPIO1	Pin function selection for GPIOA[14]	0x3
27:26	R/W	FSEL_GPIO1	Pin function selection for GPIOA[13]	0x3
25:24	R/W	FSEL_GPIO1	Pin function selection for GPIOA[12]	0x3
22:20	R/W	FSEL_GPIO1	Pin function selection for GPIOA[11:10]	0x6
19:16	R/W	FSEL_GPIO1	Pin function selection for GPIOA[9:8]	0x1
15:12	R/W	FSEL_GPIO1	Pin function selection for GPIOA[7:6]	0x1
11:8	R/W	FSEL_GPIO1	Pin function selection for GPIOA[5:4]	0x3
7:4	R/W	FSEL_GPIO1	Pin function selection for GPIOA[3:2]	0x8
3:0	R/W	FSEL_GPIO1	Pin function selection for GPIOA[1:0]	0x9

See Table 133 for GPIO1 pin muxing.

Table 64. GPIO_FSEL_GPIO2_REG (0x5000_120C)

Bit	Mode	Symbol	Description	Reset
21:20	R/W	FSEL_GPIO2	Pin function selection for GPIOC[8:6]	0x2
19:7	R/W	-	Reserved	-
6:4	R/W	FSEL_GPIO2	Pin function selection for GPIOC[14:13]	0x0
3:0	R/W	FSEL_GPIO2	Pin function selection for GPIOC[12:9]	0x0

See Table 134 for GPIO2 pin muxing.

Table 65. GPIO_UART_PAD_REG (0x5000_1218)

Bit	Mode	Symbol	Description	Reset
4	R/W	TXD_PE	Enable pull-up/pull-down (active high) for UART0_TXD 0: Pull disable 1: Pull enable	0x0
3	R/W	RXD_PE	Enable pull-up/pull-down (active high) for UART0_RXD 0: Pull disable 1: Pull enable	0x0
2	R/W	PS	Pull selection for UART0_TXD and UART0_RXD 0: Pull-down 1: Pull-up	0x0
1:0	R/W	DS	Driving strength 00: 2 mA 01: 8 mA (default) 10: 4 mA 11: 12 mA	0x1

Table 66. GPIO_JTAG_PAD_REG (0x5000_121C)

Bit	Mode	Symbol	Description	Reset
7	R/W	TMS_PE	Enable pull-up/pull-down (active high) for TMS 0: Pull disable 1: Pull enable	0x1
6	RW	TMS_PS	Pull selection for TMS 0: Pull-down 1: Pull-up	0x1
5	R/W	TCLK_PE	Enable pull-up/pull-down (active high) for TCLK (GPIOA15) 1: Pull enable 0: Pull disable	0x1
4	RW	TCLK_PS	Pull selection for TCLK (GPIOA15) 0: Pull-down 1: Pull-up	0x0
3	R/W	SR	Slew rate control for TMS and TCLK 0: Fast slew (default) 1: Slow slew	0x0
2	R/W	IS	Input selection TMS and TCLK 0: CMOS 1: Schmitt (default)	0x1
1:0	R/W	DS	Driving strength 00: 2 mA 01: 8 mA (default) 10: 4 mA 11: 12 mA	0x1

Table 67. GPIOA_DS_REG (0x5000_1220)

Bit	Mode	Symbol	Description	Reset
29:0	R/W	-	Driving strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11: 12 mA [29:28] GPIOA14 [27:26] GPIOA13 [25:24] GPIOA12 [23:22] GPIOA11 [21:20] GPIOA10 [19:18] GPIOA9 [17:16] GPIOA8 [15:14] GPIOA7 [13:12] GPIOA6 [11:10] GPIOA5 [9:8] GPIOA4 [7:6] GPIOA3 [5:4] GPIOA2 [3:2] GPIOA1 [1:0] GPIOA0	0x5555_5555

Table 68. GPIOA_SR_REG (0x5000_1224)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	-	Slew rate control, default = 0 (fast slew) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x0000

Table 69. GPIOA_PE_PS_REG (0x5000_1228)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Pull-up/pull-down enable (active high) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0xFFFF
15:0	R/W	-	Pull selection Pull-up = 1 Pull-down = 0 [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x0000

Table 70. GPIOA_IE_IS_REG (0x5000_122C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Input enable (active high, default = 1) [30] GPIOA14 [29] GPIOA13 … [17] GPIOA1 [16] GPIOA0	0x7FFF
15:0	R/W	-	Input selection 0: CMOS 1: Schmitt (default = 1) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x7FFF

Table 71. GPIOB_DS_REG (0x5000_1234)

Bit	Mode	Symbol	Description	Reset
23:0	R/W	-	Driving strength 00: 2 mA 01: 8 mA (default) 10: 4 mA 11: 12 mA [23:22] GPIOB11 [21:20] GPIOB10 [19:18] GPIOB9 [17:16] GPIOB8 [15:14] GPIOB7 [13:12] GPIOB6 [11:10] GPIOB5 [9:8] GPIOB4 [7:6] GPIOB3 [5:4] GPIOB2 [3:2] GPIOB1 [1:0] GPIOB0	0x0055_5555

Table 72. GPIOB_SR_REG (0x5000_1238)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	Slew rate control, default = 0 (fast slew) [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0000

Table 73. GPIOB_PE_PS_REG (0x5000_123C)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Pull-up/pull-down enable (active high) [27] GPIOB11 [26] GPIOB10 …	0x0FFF

Bit	Mode	Symbol	Description	Reset
			[17] GPIOB1 [16] GPIOB0	
11:0	R/W	-	Pull selection, pull-up = 1, pull-down = 0 [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0000

Table 74. GPIOB_IE_IS_REG (0x5000_1240)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Input enable (active high, default = 1) [27] GPIOB11 [26] GPIOB10 … [17] GPIOB1 [16] GPIOB0	0x0FFF
11:0	R/W	-	Input selection 0: CMOS 1: Schmitt (default = 1) [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0FFF

Table 75. GPIOC_DS_REG (0x5000_1244)

Bit	Mode	Symbol	Description	Reset
17:0	R/W	-	Driving strength 00: 2 mA 01: 8 mA (default) 10: 4 mA 11: 12 mA [17:16] GPIOC8 [15:14] GPIOC7 [13:12] GPIOC6 [11:10] GPIOC5 [9:8] GPIOC4 [7:6] GPIOC3 [5:4] GPIOC2 [3:2] GPIOC1 [1:0] GPIOC0	0x0001_5555

Table 76. GPIOC_SR_REG (0x5000_1248)

Bit	Mode	Symbol	Description	Reset
8:0	R/W	-	Slew rate control, default = 0 (fast slew) [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1	0x0000

Bit	Mode	Symbol	Description	Reset
			[0] GPIOC0	

Table 77. GPIOC_PE_PS_REG (0x5000_124C)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Pull-up/pull-down enable (active high) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Pull selection, pull-up = 1, pull-down = 0 [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1 [0] GPIOC0	0x0000

Table 78. GPIOC_IE_IS_REG (0x5000_1250)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Input enable (active high, default = 1) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Input selection: 0: CMOS 1: Schmitt (default = 1) [8] GPIOC8 [7] GPIOC7 … [1] GPIOB1 [0] GPIOB0	0x01FF

Table 79. GPIOA_DIN_REG (0x4001_0000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOA input data	0x0000

Table 80. GPIOA_DOUT_REG (0x4001_0004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA output data	0x0000

Table 81. GPIOA_DOUT_SET_REG (0x4001_0010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA data output enable set. 1 = Output enable 0 = Input enable	0x0000

Table 82. GPIOA_DOUT_CLR_REG (0x4001_0014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA data output clear. 1 = Output clear	0x0000

Table 83. GPIOA_FUNC_SET_REG (0x4001_0018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA alternate function output enable set. 1 = Output enable 0 = Disable	0x0000

Table 84. GPIOA_FUNC_CLR_REG (0x4001_001C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA alternate function output clear. 1 = Output clear	0x0000

Table 85. GPIOA_INTR_SET_REG (0x4001_0020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt set. 1 = Interrupt enable 0 = Disable	0x0000

Table 86. GPIOA_INTR_CLR_REG (0x4001_0024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt clear. 1 = Interrupt clear	0x0000

Table 87. GPIOA_INTR_TYPE_SET_REG (0x4001_0028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt type set. 1: Edge 0: Level	0x0000

Table 88. GPIOA_INTR_TYPE_CLR_REG (0x4001_002C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt type clear.	0x0000

Table 89. GPIOA_INTR_POL_SET_REG (0x4001_0030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt polarity set. 1: Active high 0: Active low	0x0000

Table 90. GPIOA_INTR_POL_CLR_REG (0x4001_0034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt polarity clear.	0x0000

Table 91. GPIOA_INTR_STS_REG (0x4001_0038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA interrupt status.	0x0000

Table 92. GPIOA_FUNC_OUT_EN_REG (0x4001_003C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate function output enable for GPIOA. 1 = Enable 0 = Disable [12]: UART2_TXDOE enable	0x0000

Bit	Mode	Symbol	Description	Reset
			[11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	

Table 93. GPIOA_PWM_OUT_SEL_REG (0x4001_0FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOA. [15:12]: Port selection of the PWM_OUT[3] [11: 8]: Port selection of the PWM_OUT[2] [7: 4]: Port selection of the PWM_OUT[1] [3: 0]: Port selection of the PWM_OUT[0]	0x0000

Table 94. GPIOA_mSPI_CS_SEL_REG (0x4001_0FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOA. [15:12]: Port selection of the mSPI_CSB[3] [11: 8]: Port selection of the mSPI_CSB[2] [7: 4]: Port selection of the mSPI_CSB[1] [3: 0]: Port selection of the Ext_Intr	0x0000

Table 95. GPIOA_RF_SW_SEL_REG (0x4001_0FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOA. [7: 4]: Port selection of the RF_SW2 [3: 0]: Port selection of the RF_SW1	0x0000

Table 96. GPIOA_UART_SEL_REG (0x4001_0FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOA. [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE [3: 0]: Port selection of the UART0_TXDOE	0x0000

Table 97. GPIOB_DIN_REG (0x4001_1000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOB input data.	0x0000

Table 98. GPIOB_DOUT_REG (0x4001_1004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB output data.	0x0000

Table 99. GPIOB_DOUT_SET_REG (0x4001_1010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB data output enable set. 1 = Output enable 0 = Input enable	0x0000

Table 100. GPIOB_DOUT_CLR_REG (0x4001_1014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB data output clear. 1 = Output clear	0x0000

Table 101. GPIOB_FUNC_SET_REG (0x4001_1018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB alternate function output enable set. 1 = Output enable 0 = Disable	0x0000

Table 102. GPIOB_FUNC_CLR_REG (0x4001_101C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB alternate function output clear. 1 = Output clear	0x0000

Table 103. GPIOB_INTR_SET_REG (0x4001_1020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt set. 1 = Interrupt enable 0 = Disable	0x0000

Table 104. GPIOB_INTR_CLR_REG (0x4001_1024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt clear. 1 = Interrupt clear	0x0000

Table 105. GPIOB_INTR_TYPE_SET_REG (0x4001_1028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt type set. 1: Edge 0: Level	0x0000

Table 106. GPIOB_INTR_TYPE_CLR_REG (0x4001_102C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt type clear.	0x0000

Table 107. GPIOB_INTR_POL_SET_REG (0x4001_1030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt polarity set. 1: Active high 0: Active low	0x0000

Table 108. GPIOB_INTR_POL_CLR_REG (0x4001_1034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt polarity clear.	0x0000

Table 109. GPIOB_INTR_STS_REG (0x4001_1038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB interrupt status.	0x0000

Table 110. GPIOB_FUNC_OUT_EN_REG (0x4001_103C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate function output enable for GPIOB. 1 = Enable 0 = Disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 111. GPIOB_PWM_OUT_SEL_REG (0x4001_1FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOB. [15:12]: Port selection of the PWM_OUT[3] [11: 8]: Port selection of the PWM_OUT[2] [7: 4]: Port selection of the PWM_OUT[1] [3: 0]: Port selection of the PWM_OUT[0]	0x0000

Table 112. GPIOB_mSPI_CS_SEL_REG (0x4001_1FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOB. [15:12]: Port selection of the mSPI_CSB[3] [11: 8]: Port selection of the mSPI_CSB[2] [7: 4]: Port selection of the mSPI_CSB[1] [3: 0]: Port selection of the Ext_Intr	0x0000

Table 113. GPIOB_RF_SW_SEL_REG (0x4001_1FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOB. [7: 4]: Port selection of the RF_SW2 [3: 0]: Port selection of the RF_SW1	0x0000

Table 114. GPIOB_UART_SEL_REG (0x4001_1FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOB. [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE [3: 0]: Port selection of the UART0_TXDOE	0x0000

Table 115. GPIOC_DIN_REG (0x4001_7000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOC input data.	0x0000

Table 116. GPIOC_DOUT_REG (0x4001_7004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC output data.	0x0000

Table 117. GPIOC_DOUT_SET_REG (0x4001_7010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC data output enable set. 1 = Output enable 0 = Input enable	0x0000

Table 118. GPIOC_DOUT_CLR_REG (0x4001_7014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC data output clear. 1 = Output clear	0x0000

Table 119. GPIOC_FUNC_SET_REG (0x4001_7018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC alternate function output enable set. 1 = Output enable 0 = Disable	0x0000

Table 120. GPIOC_FUNC_CLR_REG (0x4001_701C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC alternate function output clear. 1 = Output clear	0x0000

Table 121. GPIOC_INTR_SET_REG (0x4001_7020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt set. 1 = Interrupt enable 0 = Disable	0x0000

Table 122. GPIOC_INTR_CLR_REG (0x4001_7024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt clear. 1 = Interrupt clear	0x0000

Table 123. GPIOC_INTR_TYPE_SET_REG (0x4001_7028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt type set. 1: Edge 0: Level	0x0000

Table 124. GPIOC_INTR_TYPE_CLR_REG (0x4001_702C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt type clear.	0x0000

Table 125. GPIOC_INTR_POL_SET_REG (0x4001_7030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt polarity set. 1: Active high 0: Active low	0x0000

Table 126. GPIOC_INTR_POL_CLR_REG (0x4001_7034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt polarity clear	0x0000

Table 127. GPIOC_INTR_STS_REG (0x4001_7038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC interrupt status	0x0000

Table 128. GPIOC_FUNC_OUT_EN_REG (0x4001_703C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate function output enable for GPIOC. 1 = Enable 0 = Disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 129. GPIOC_PWM_OUT_SEL_REG (0x4001_7FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOC. [15:12]: Port selection of the PWM_OUT[3] [11: 8]: Port selection of the PWM_OUT[2] [7: 4]: Port selection of the PWM_OUT[1] [3: 0]: Port selection of the PWM_OUT[0]	0x0000

Table 130. GPIOC_mSPI_CS_SEL_REG (0x4001_7FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOC. [15:12]: Port selection of the mSPI_CSB[3] [11: 8]: Port selection of the mSPI_CSB[2] [7: 4]: Port selection of the mSPI_CSB[1] [3: 0]: Port selection of the Ext_Intr	0x0000

Table 131. GPIOC_RF_SW_SEL_REG (0x4001_7FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOC. [7: 4]: Port selection of the RF_SW2 [3: 0]: Port selection of the RF_SW1	0x0000

Table 132. GPIOC_UART_SEL_REG (0x4001_7FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOC. [11: 8]: Port selection of the UART2_TXDOE [7: 4]: Port selection of the UART1_TXDOE [3: 0]: Port selection of the UART0_TXDOE	0x0000

Table 133. GPIO pin mux

Bit Sel	Value										
	0	1	2	3	4	5	6	7	8	9	10
FSEL_GPIO1[31:30]	Semi-fixed pin: JTAG_01 TMS TCLK	D_SYS D_SYS_OUT[0] D_SYS_OUT[1]	GPIO(2) x GPIOA[15]	GPIO(2) x GPIOA[15]	-	-	-	-	-	-	-
FSEL_GPIO[29:28] FSEL_GPIO[27:26] FSEL_GPIO[25:24]	UART2_01 I2S_CLK_In UART2_RXD UART2_TXD	BT(0:2) BT_sig2 (iBTPri) BT_sig1 (iBtAct) BT_sig0 (oWlanAct)	D_SYS D_SYS_CLK D_SYS_OUT[3] D_SYS_OUT[2]	GPIO(2) GPIOA[14] GPIOA[13] GPIOA[12]	-	-	-	-	-	-	-
FSEL_GPIO[22:20]	G(1) + BT GPIOA[11] BT_sig2 (iBTPri)	G(1) + I2S GPIOA[11] I2S_CLK_In	G(1) + eMMC(6) GPIOA[11] mSDeMMC_WRP	sSPI (2:3) sSPI_MOSI sSPI_MISO	UART2 (0:1) UART2_RXD UART2_TXD	mSPI (4:5) E_SPI_IO3 E_SPI_IO2	GPIO(2) GPIOA[11] GPIOA[10]	GPIO(2) GPIOA[11] GPIOA[10]	-	-	-
FSEL_GPIO[19:16]	5G control(45) 5GC_Sig[5] 5GC_Sig[4]	sSPI (2:3) sSPI_MOSI sSPI_MISO	eMMC (0:1) mSDeMMC_D0 mSDeMMC_D1	sSDIO (0:1) sSDIO_D0 sSDIO_D1	I2C_master mI2C_CLK mI2C_SDA	BT (0:1) BT_sig1(iBtAct) BT_sig0(oWlanAct)	mSPI (2:3) E_SPI_IO1 E_SPI_IO0	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[9] GPIOA[8]	GPIO(2) GPIOA[9] GPIOA[8]	-
FSEL_GPIO[15:12]	-	sSPI (0:1) sSPI_CLK sSPI_CSB	eMMC (2:3) mSDeMMCIO_D2 mSDeMMCIO_D3	sSDIO (2:3) sSDIO_D2 sSDIO_D3	UART1 (0:1) UART1_RXD UART1_TXD	I2C slave sI2C_CLK sI2C_SDA	mSPI (0:1) E_SPI_CLK E_SPI_CSB	I2S(2:3) I2S_LRCK I2S_SDO	GPIO(2) GPIOA[7] GPIOA[6]	GPIO(2) GPIOA[7] GPIOA[6]	-
FSEL_GPIO[11:8]	5G control(01) 5GC_Sig[3] 5GC_Sig[2]	I2C slave sI2C_CLK sI2C_SDA	eMMC (4:5) mSDeMMC_CLK mSDeMMC_CMD	sSDIO (4:5) sSDIO_CLK sSDIO_CMD	UART1 (2:3) UART1_CTS UART1_RTS	I2C master mI2C_CLK mI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[5] GPIOA[4]	GPIO(2) GPIOA[5] GPIOA[4]	-
FSEL_GPIO[7:4]	AD12 (2) X (Analog In) X (Analog In)	sSPI (0:1) sSPI_CLK sSPI_CSB	I2S (2:3) I2S_LRCK I2S_SDO	I2C slave sI2C_CLK sI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	-	AD12(1) + GPIO(1) GPIO[3] X (Analog In)	AD12(1) + I2S_CLK I2S_CLK_In X (Analog In)	GPIO(2) GPIOA[3] GPIOA[2]	GPIO(2) GPIOA[3] GPIOA[2]	-
FSEL_GPIO[3:0]	AD12 (2) X (Analog In) X (Analog In)	sSPI (2:3) sSPI_MOSI sSPI_MISO	I2S (0:1) I2S_MCLK I2S_BCLK	I2C slave sI2C_CLK sI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	I2C master mI2C_CLK mI2C_SDA	5G control(01) 5GC_Sig[1] 5GC_Sig[0]	AD12(1) + GPIO(1) GPIO[1] X (Analog In)	AD12(1) + WRP mSDeMMC_WRP X (Analog In)	GPIO(2) GPIOA[1] GPIOA[0]	GPIO(2) GPIO[1] GPIO[0]

Table 134. GPIO2 pin mux

Bit Sel	Value					
	0	1	2	3	4	5
FSEL_GPIO2[21:20]	JTAG(2:3) TDI TDO nTRST	G(1) + UART2 (0:1) GPIO[8] UART2_RXD UART2_TXD	GPIO(2) GPIOC[8] GPIOC[7] GPIOC[6]	-	-	-
FSEL_GPIO2[6:4]	QSPI (4:5) F_IO3 (F_HOLD) F_IO2 (F_WP)	UART2 (0:1) UART2_TXD UART2_RXD	-	sSDIO(4:5) sSDIO_D3 sSDIO_D2	GPIO(2) GPIOC[14] GPIOC[13]	GPIO(2) GPIOC[14] GPIOC[13]
FSEL_GPIO2[3:0]	QSPI (3:0) F_IO1 (F_SI) F_IO0 (F_SO) F_CLK F_CSB[1]	sSPI (3:0) sSPI_MISO sSPI_MOSI sSPI_CLK sSPI_CSB	I2S(0:3) I2S_SDO I2S_LRCK I2S_MCLK I2S_BCLK	sSDIO(0:3) sSDIO_D1 sSDIO_D0 sSDIO_CLK sSDIO_CMD	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]

10.2 UART Register

Table 135. UART feature specification

Specification	RS-232	RS-485
Differential	No	Yes
Operation Mode	Full duplex	Half duplex
Maximum Baud Rate	921600 Baud	5M Baud
Flow Control	Support	Support

Note 1 See Ref. [2] for the pin configurations of the UARTs.

Table 136. UART registers

Address	Register	Description
0x4001_2000	UART0_DATA	UART0 Data Register

Address	Register	Description
0x4001_2004	UART0_RXSTS UART0_ERRCLR	UART0 Receive Status Register (Read) Error Clear Register (Write)
0x4001_2018	UART0_FLAG	UART0 Flag Register
0x4001_2024	UART0_INTBRDIV	UART0 Integer Baud Rate Divisor Register
0x4001_2028	UART0_FRABRDIV	UART0 Fractional Baud Rate Divisor Register
0x4001_202C	UART0_LCNTRL	UART0 Line Control Register
0x4001_2030	UART0_CNTRL	UART0 Control Register
0x4001_2034	UART0_INTFLS	UART0 Interrupt FIFO Level Select Register
0x4001_2038	UART0_INTMSKSC	UART0 Interrupt Mask Set/Clear Register
0x4001_2040	UART0_INTMSKSTS	UART0 Masked Interrupt Status Register
0x4001_2044	UART0_INTCLR	UART0 Interrupt Clear Register
0x4001_2048	UART0_DMACNTRL	UART0 DMA Control Register
0x4001_204C	UART0_WAEN	UART0 Word Access Enable Register
0x4001_2054	UART0_485EN	UART0 RS-485 Mode Enable Register
0x4000_7000	UART1_DATA	UART1 Data Register
0x4000_7004	UART1_RXSTS UART1_ERRCLR	UART1 Receive Status Register (Read) Error Clear Register (Write)
0x4000_7018	UART1_FLAG	UART1 Flag Register
0x4000_7024	UART1_INTBRDIV	UART1 Integer Baud Rate Divisor Register
0x4000_7028	UART1_FRABRDIV	UART1 Fractional Baud Rate Divisor Register
0x4000_702C	UART1_LCNTRL	UART1 Line Control Register
0x4000_7030	UART1_CNTRL	UART1 Control Register
0x4000_7034	UART1_INTFLS	UART1 Interrupt FIFO Level Select Register
0x4000_7038	UART1_INTMSKSC	UART1 Interrupt Mask Set/Clear Register
0x4000_7040	UART1_INTMSKSTS	UART1 Masked Interrupt Status Register
0x4000_7044	UART1_INTCLR	UART1 Interrupt Clear Register
0x4000_7048	UART1_DMACNTRL	UART1 DMA Control Register
0x4000_704C	UART1_WAEN	UART1 Word Access Enable Register
0x4000_7054	UART1_485EN	UART1 RS-485 Mode Enable Register
0x4000_9000	UART2_DATA	UART2 Data Register
0x4000_9004	UART2_RXSTS UART2_ERRCLR	UART2 Receive Status Register (Read) Error Clear Register (Write)
0x4000_9018	UART2_FLAG	UART2 Flag Register
0x4000_9024	UART2_INTBRDIV	UART2 Integer Baud Rate Divisor Register
0x4000_9028	UART2_FRABRDIV	UART2 Fractional Baud Rate Divisor Register
0x4000_902C	UART2_LCNTRL	UART2 Line Control Register
0x4000_9030	UART2_CNTRL	UART2 Control Register
0x4000_9034	UART2_INTFLS	UART2 Interrupt FIFO Level Select Register
0x4000_9038	UART2_INTMSKSC	UART2 Interrupt Mask Set/Clear Register
0x4000_9040	UART2_INTMSKSTS	UART2 Masked Interrupt Status Register
0x4000_9044	UART2_INTCLR	UART2 Interrupt Clear Register
0x4000_9048	UART2_DMACNTRL	UART2 DMA Control Register
0x4000_904C	UART2_WAEN	UART2 Word Access Enable Register
0x4000_9054	UART2_485EN	UART2 RS-485 Mode Enable Register

Table 137. UART0_DATA (0x4001_2000)

Bit	Mode	Symbol	Description	Reset
15:12	-	-	Reserved	0x0
11:8	RO	-	Error status for data read. These bits cannot be read when UART_WAEN is enabled. [11] Overrun Error	0x0

Bit	Mode	Symbol	Description	Reset
			[10] Break Error [9] Parity Error [8] Framing Error	
7:0	R/W	DATA	Receive data bits for data read. Transmit data bits for data write.	0x00

Table 138. UART0_RXSTS/UART0_ERRCLR (0x4001_2004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:0	WO	-	UART0_ERRCLR, writing to this register clears every error.	0x00
7:4	RO	-	UART0_RXSTS, Reserved	0x0
3:0	RO	-	UART0_RXSTS, UART0 error status. [3] Overrun error [2] Break error [1] Parity error [0] Framing error	0x0

Table 139. UART0_FLAG (0x4001_2018)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:4	RO	-	The status of FIFOs. [7] TXFE, Transmit FIFO empty [6] RXFF, Receive FIFO full [5] TXFF, Transmit FIFO full [4] RXFE, Receive FIFO empty	0x9
3	RO	BUSY	UART0 busy. This bit is set to 1 as soon as the transmit FIFO becomes non-empty.	0x0
2:0	-	-	Reserved	0x0

Table 140. UART0_INTBRDIV (0x4001_2024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IBRD	Integer baud rate divisor.	0x0000

Table 141. UART0_FRABRDIV (0x4001_2028)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:0	R/W	FBRD	Fractional baud rate divisor.	0x00

Table 142. UART0_LCNTRL (0x4001_202C)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7	R/W	SPS	Stick parity select. 0 = Stick parity disabled 1 = Either ● If PARSEL bit is 0, the parity bit is transmitted and checked as a 1. ● If PARSEL bit is 1, the parity bit is transmitted and checked as a 0.	0x0
6:5	R/W	DTLEN	The number of data bits transmitted or received in a frame. b'11 = 8 bits b'10 = 7 bits	0x0

Bit	Mode	Symbol	Description	Reset
			b'01 = 6 bits b'00 = 5 bits	
4	R/W	FIFOEn	FIFO enable. 0 = UART0 FIFO disabled 1 = UART0 transmit and receive FIFO enabled	0x0
3	R/W	TSTP	Two stop bits select. 0 = Two bits are transmitted as stop bit 1 = One bit is transmitted as stop bit	0x0
2	R/W	PARSEL	Parity select. 0 = Odd parity 1 = Even parity	0x0
1	R/W	PAREn	Parity enable. 0 = Parity is disabled 1 = Parity is enabled	0x0
0	-	-	Reserved	0x0

Table 143. UART0_CNTRL (0x4001_2030)

Bit	Mode	Symbol	Description	Reset
15	R/W	CTSEn	UART0 CTS hardware flow control enable. 0 = CTS hardware flow control disabled 1 = CTS hardware flow control enabled	0x0
14	R/W	RTSEn	UART0 RTS hardware flow control enable. 0 = RTS hardware flow control disabled 1 = RTS hardware flow control enabled	0x0
13:10	-	-	Reserved	0x0
9	R/W	RXEn	Receive enable. 0 = Receive section of the UART0 disabled 1 = Receive section of the UART0 enabled	0x1
8	R/W	TXEn	Transmit enable. 0 = Transmit section of the UART0 disabled 1 = Transmit section of the UART0 enabled	0x1
7:1	-	-	Reserved	0x00
0	R/W	UARTEn	UART0 enable. 0 = UART0 is disabled 1 = UART0 is enabled	0x0

Table 144. UART0_INTFLS (0x4001_2034)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:3	R/W	RXIFLS	UART0 receive interrupt FIFO level select. The receive interrupt occurs as follows: b'000 = Receive FIFO ≥ 1/8 full b'001 = Receive FIFO ≥ 1/4 full b'010 = Receive FIFO ≥ 1/2 full b'011 = Receive FIFO ≥ 3/4 full b'100 = Receive FIFO ≥ 7/8 full b'101 b'111 = Reserved	3'b010
2:0	R/W	TXIFLS	UART0 transmit interrupt FIFO level select. The transmit interrupt occurs as follows: b'000 = Transmit FIFO ≤ 1/8 full b'001 = Transmit FIFO ≤ 1/4 full b'010 = Transmit FIFO ≤ 1/2 full	3'b010

Bit	Mode	Symbol	Description	Reset
			b'011 = Transmit FIFO ≤ 3/4 full b'100 = Transmit FIFO ≤ 7/8 full b'101 b'111 = Reserved	

Table 145. UART0_INTMSKSC (0x4001_2038)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask. [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	R/W	RXTIM	Receive timeout interrupt mask.	0x0
5	R/W	TXIM	Transmit interrupt mask.	0x0
4	R/W	RXIM	Receive interrupt mask.	0x0
3:0	-	-	Reserved	0x0

Table 146. UART0_INTMSKSTS (0x4001_2040)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask. [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	R/W	RXTIM	Receive timeout interrupt mask.	0x0
5	R/W	TXIM	Transmit interrupt mask.	0x0
4	R/W	RXIM	Receive interrupt mask.	0x0
3:0	-	-	Reserved	0x0

Table 147. UART0_INTCLR (0x4001_2044)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	WO	-	Error interrupt mask. [10] = Overrun error interrupt clear [9] = Break error interrupt clear [8] = Parity error interrupt clear [7] = Framing error interrupt clear	0x0
6	WO	RXTICLR	Receive timeout interrupt clear.	0x0
5	WO	TXICLR	Transmit interrupt clear.	0x0
4	WO	RXICLR	Receive interrupt clear.	0x0
3:0	-	-	Reserved	0x0

Table 148. UART0_DMACNTRL (0x4001_2048)

Bit	Mode	Symbol	Description	Reset
15:2	-	-	Reserved	0x0000
1	R/W	TXDMAEn	Transmit DMA enable. 0 = Transmit DMA is disabled 1 = Transmit DMA is enabled	0x0
0	R/W	RXDMAEn	Receive DMA enable. 0 = Receive DMA is disabled	0x0

Bit	Mode	Symbol	Description	Reset
			1 = Receive DMA is enabled	

Table 149. UART0_WAEN (0x4001_204C)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	WA	UART0 word access enable register. 0 = UART0 Word Access is disabled 1 = UART0 Word Access is enabled	0x1

Table 150. UART0_485EN (0x4001_2054)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	RS485En	UART0 RS-485 mode enable register. 0 = UART0 RS-485 mode is disabled 1 = UART0 RS-485 mode is enabled	0x0

Table 151. UART1_DATA (0x4000_7000)

Bit	Mode	Symbol	Description	Reset
15:12	-	-	Reserved	0x0
11:8	RO	-	Error status for data read. These bits cannot be read when UART1_WAEN is enabled. [11] Overrun Error [10] Break Error [9] Parity Error [8] Framing Error	0x0
7:0	R/W	DATA	Receive data bits for data read. Transmit data bits for data write.	0x00

Table 152. UART1_RXSTS/UART1_ERRCLR (0x4000_7004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:0	WO	-	UART1_ERRCLR, writing to this register clears every error. The value is not important.	0x00
7:4	RO	-	UART1_RXSTS, Reserved	0x0
3:0	RO	-	UART1_RXSTS, UART1 error status. [3] Overrun error [2] Break error [1] Parity error [0] Framing error	0x0

Table 153. UART1_FLAG (0x4000_7018)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:4	RO	-	The status of FIFOs. [7] TXFE, Transmit FIFO empty [6] RXFF, Receive FIFO full [5] TXFF, Transmit FIFO full [4] RXFE, Receive FIFO empty	0x9
3	RO	BUSY	UART1 busy. This bit is set to 1 as soon as the transmit FIFO becomes non-empty.	0x0
2:0	-	-	Reserved	0x0

Table 154. UART1_INTBRDIV (0x4000_7024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IBRD	Integer baud rate divisor.	0x0000

Table 155. UART1_FRABRDIV (0x4000_7028)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:0	R/W	FBRD	Fractional baud rate divisor.	0x00

Table 156. UART1_LCNTRL (0x4000_702C)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7	R/W	SPS	Stick parity select. 0 = Stick parity disabled 1 = Either ● If PARSEL bit is 0, the parity bit is transmitted and checked as a 1. ● If PARSEL bit is 1, the parity bit is transmitted and checked as a 0.	0x0
6:5	R/W	DTLEN	The number of data bits transmitted or received in a frame. b'11 = 8 bits b'10 = 7 bits b'01 = 6 bits b'00 = 5 bits	0x0
4	R/W	FIFOEn	FIFO enable. 0 = UART1 FIFO disabled 1 = UART1 Transmit and Receive FIFO enabled	0x0
3	R/W	TSTP	Two stop bits select. 0 = Two bits are transmitted as stop bit 1 = One bit is transmitted as stop bit	0x0
2	R/W	PARSEL	Parity select. 0 = Odd parity 1 = Even parity	0x0
1	R/W	PAREn	Parity enable. 0 = Parity is disabled 1 = Parity is enabled	0x0
0	-	-	Reserved	0x0

Table 157. UART1_CNTRL (0x4000_7030)

Bit	Mode	Symbol	Description	Reset
15	R/W	CTSEn	UART1 CTS hardware flow control enable. 0 = CTS hardware flow control disabled 1 = CTS hardware flow control enabled	0x0
14	R/W	RTSEn	UART1 RTS hardware flow control enable. 0 = RTS hardware flow control disabled 1 = RTS hardware flow control enabled	0x0
13:10	-	-	Reserved	0x0
9	R/W	RXEn	Receive enable. 0 = Receive section of the UART1 disabled 1 = Receive section of the UART1 enabled	0x1
8	R/W	TXEn	Transmit enable. 0 = Transmit section of the UART1 disabled	0x1

Bit	Mode	Symbol	Description	Reset
			1 = Transmit section of the UART1 enabled	
7:1	-	-	Reserved	0x00
0	R/W	UARTEn	UART1 enable. 0 = UART1 is disabled 1 = UART1 is enabled	0x0

Table 158. UART1_INTFLS (0x4000_7034)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:3	R/W	RXIFLS	UART1 receive interrupt FIFO level select. The receive interrupt occurs as follows: b'000 = Receive FIFO ≥ 1/8 full b'001 = Receive FIFO ≥ 1/4 full b'010 = Receive FIFO ≥ 1/2 full b'011 = Receive FIFO ≥ 3/4 full b'100 = Receive FIFO ≥ 7/8 full b'101 b'111 = Reserved	3'b010
2:0	R/W	TXIFLS	UART1 transmit interrupt FIFO level select. The transmit interrupt occurs as follows: b'000 = Transmit FIFO ≤ 1/8 full b'001 = Transmit FIFO ≤ 1/4 full b'010 = Transmit FIFO ≤ 1/2 full b'011 = Transmit FIFO ≤ 3/4 full b'100 = Transmit FIFO ≤ 7/8 full b'101 b'111 = Reserved	3'b010

Table 159. UART1_INTMSKSC (0x4000_7038)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask. [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	R/W	RXTIM	Receive timeout interrupt mask.	0x0
5	R/W	TXIM	Transmit interrupt mask.	0x0
4	R/W	RXIM	Receive interrupt mask.	0x0
3:0	-	-	Reserved	0x0

Table 160. UART1_INTMSKSTS (0x4000_7040)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	RO	-	Error interrupt mask. [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	RO	RXTIMS	Receive timeout masked interrupt status.	0x0
5	RO	TXIMS	Transmit masked interrupt status.	0x0
4	RO	RXIMS	Receive masked interrupt status.	0x0
3:0	-	-	Reserved	0x0

Table 161. UART1_INTCLR (0x4000_7044)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	WO	-	Error interrupt mask. [10] = Overrun error interrupt clear [9] = Break error interrupt clear [8] = Parity error interrupt clear [7] = Framing error interrupt clear	0x0
6	WO	RXTICLR	Receive timeout interrupt clear.	0x0
5	WO	TXICLR	Transmit interrupt clear.	0x0
4	WO	RXICLR	Receive interrupt clear.	0x0
3:0	-	-	Reserved	0x0

Table 162. UART1_DMACNTRL (0x4000_7048)

Bit	Mode	Symbol	Description	Reset
15:2	-	-	Reserved	0x0000
1	R/W	TXDMAEn	Transmit DMA enable. 0 = Transmit DMA is disabled 1 = Transmit DMA is enabled	0x0
0	R/W	RXDMAEn	Receive DMA enable. 0 = Receive DMA is disabled 1 = Receive DMA is enabled	0x0

Table 163. UART1_WAEN (0x4000_704C)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	WA	UART1 word access enable register. 0 = UART1 Word Access is disabled 1 = UART1 Word Access is enabled	0x1

Table 164. UART1_485EN (0x4000_7054)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	RS485En	UART1 RS-485 mode enable register. 0 = UART1 RS-485 mode is disabled 1 = UART1 RS-485 mode is enabled	0x0

Table 165. UART2_DATA (0x4000_9000)

Bit	Mode	Symbol	Description	Reset
15:12	-	-	Reserved	0x0
11:8	RO	-	Error status for data read. These bits cannot be read when UART2_WAEN is enabled. [11] Overrun Error [10] Break Error [9] Parity Error [8] Framing Error	0x0
7:0	R/W	DATA	Receive data bits for data read. Transmit data bits for data write.	0x00

Table 166. UART2_RXSTS/UART2_ERRCLR (0x4000_9004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00

Bit	Mode	Symbol	Description	Reset
7:0	WO	-	UART2_ERRCLR, write to this register clears every error. The value is not important.	0x00
7:4	RO	-	UART2_RXSTS, Reserved	0x0
3:0	RO	-	UART2_RXSTS, UART2 error status. [3] Overrun error [2] Break error [1] Parity error [0] Framing error	0x0

Table 167. UART2_FLAG (0x4000_9018)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:4	RO	-	The status of FIFOs. [7] TXFE, Transmit FIFO empty [6] RXFF, Receive FIFO full [5] TXFF, Transmit FIFO full [4] RXFE, Receive FIFO empty	0x9
3	RO	BUSY	UART2 busy. This bit is set to 1 as soon as the transmit FIFO becomes non-empty.	0x0
2:0	-	-	Reserved	0x0

Table 168. UART2_INTBRDIV (0x4000_9024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IBRD	Integer baud rate divisor.	0x0000

Table 169. UART2_FRABRDIV (0x4000_9028)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:0	R/W	FBRD	Fractional baud rate divisor.	0x00

Table 170. UART2_LCNTRL (0x4000_902C)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7	R/W	SPS	Stick parity select. 0 = Stick parity disabled 1 = Either ● If PARSEL bit is 0, the parity bit is transmitted and checked as a 1. ● If PARSEL bit is 1, the parity bit is transmitted and checked as a 0.	0x0
6:5	R/W	DTLEN	The number of data bits transmitted or received in a frame. b'11 = 8 bits b'10 = 7 bits b'01 = 6 bits b'00 = 5 bits	0x0
4	R/W	FIFOEn	FIFO Enable. 0 = UART2 FIFO disabled 1 = UART2 Transmit and Receive FIFO enabled	0x0
3	R/W	TSTP	Two stop bits select. 0 = Two bits are transmitted as stop bit 1 = One bit is transmitted as stop bit	0x0

Bit	Mode	Symbol	Description	Reset
2	R/W	PARSEL	Parity select. 0 = Odd parity 1 = Even parity	0x0
1	R/W	PAREn	Parity enable. 0 = Parity is disabled 1 = Parity is enabled	0x0
0	-	-	Reserved	0x0

Table 171. UART2_CNTRL (0x4000_9030)

Bit	Mode	Symbol	Description	Reset
15	R/W	CTSEn	UART2 CTS hardware flow control enable. 0 = CTS hardware flow control disabled 1 = CTS hardware flow control enabled	0x0
14	R/W	RTSEn	UART2 RTS hardware flow control enable. 0 = RTS hardware flow control disabled 1 = RTS hardware flow control enabled	0x0
13:10	-	-	Reserved	0x0
9	R/W	RXEn	Receive enable. 0 = Receive section of the UART2 disabled 1 = Receive section of the UART2 enabled	0x1
8	R/W	TXEn	Transmit enable. 0 = Transmit section of the UART2 disabled 1 = Transmit section of the UART2 enabled	0x1
7:1	-	-	Reserved	0x00
0	R/W	UARTEn	UART2 enable. 0 = UART2 is disabled 1 = UART2 is enabled	0x0

Table 172. UART2_INTFLS (0x4000_9034)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:3	R/W	RXIFLS	UART2 receive interrupt FIFO level select. The receive interrupt occurs as follows: b'000 = Receive FIFO ≥ 1/8 full b'001 = Receive FIFO ≥ 1/4 full b'010 = Receive FIFO ≥ 1/2 full b'011 = Receive FIFO ≥ 3/4 full b'100 = Receive FIFO ≥ 7/8 full b'101 b'111 = Reserved	3'b010
2:0	R/W	TXIFLS	UART2 transmit interrupt FIFO level select. The transmit interrupt occurs as follows: b'000 = Transmit FIFO ≤ 1/8 full b'001 = Transmit FIFO ≤ 1/4 full b'010 = Transmit FIFO ≤ 1/2 full b'011 = Transmit FIFO ≤ 3/4 full b'100 = Transmit FIFO ≤ 7/8 full b'101 b'111 = Reserved	3'b010

Table 173. UART2_INTMSKSC (0x4000_9038)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask.	0x0

Bit	Mode	Symbol	Description	Reset
			[10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	
6	R/W	RXTIM	Receive timeout interrupt mask.	0x0
5	R/W	TXIM	Transmit interrupt mask.	0x0
4	R/W	RXIM	Receive interrupt mask.	0x0
3:0	-	-	Reserved	0x0

Table 174. UART2_INTMSKSTS (0x4000_9040)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	RO	-	Error interrupt mask. [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	RO	RXTIMS	Receive timeout masked interrupt status.	0x0
5	RO	TXIMS	Transmit masked interrupt status.	0x0
4	RO	RXIMS	Receive masked interrupt status.	0x0
3:0	-	-	Reserved	0x0

Table 175. UART2_INTCLR (0x4000_9044)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	WO	-	Error interrupt mask. [10] = Overrun error interrupt clear [9] = Break error interrupt clear [8] = Parity error interrupt clear [7] = Framing error interrupt clear	0x0
6	WO	RXTICLR	Receive timeout interrupt clear.	0x0
5	WO	TXICLR	Transmit interrupt clear.	0x0
4	WO	RXICLR	Receive interrupt clear.	0x0
3:0	-	-	Reserved	0x0

Table 176. UART2_DMACNTRL (0x4000_9048)

Bit	Mode	Symbol	Description	Reset
15:2	-	-	Reserved	0x0000
1	R/W	TXDMAEn	Transmit DMA enable. 0 = Transmit DMA is disabled 1 = Transmit DMA is enabled	0x0
0	R/W	RXDMAEn	Receive DMA enable. 0 = Receive DMA is disabled 1 = Receive DMA is enabled	0x0

Table 177. UART2_WAEN (0x4000_904C)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	WA	UART2 word access enable register. 0 = UART2 Word Access is disabled 1 = UART2 Word Access is enabled	0x1

Table 178. UART2_485EN (0x4000_9054)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	RS485En	UART2 RS-485 mode enable register. 0 = UART2 RS-485 mode is disabled 1 = UART2 RS-485 mode is enabled	0x0

10.3 I2S Register

Table 179. I2S registers

Address	Register	Description
Common control for I2S Pin Status		
0x4001_4000	I2S_CTRL0_REG	I2S Control 0 Register
0x4001_4004	I2S_CTRL1_REG	I2S Control 1 Register
0x4001_4008	I2S_DATA_REG	I2S Data Register
0x4001_400C	I2S_STATUS_REG	I2S Status Register
0x4001_4010	Reserved	-
0x4001_4014	I2S_IMASK_REG	I2S Interrupt Mask Register
0x4001_4018	Reserved	-
0x4001_401C	Reserved	-
0x4001_4020	I2S_ICR_REG	I2S Rx Overrun Interrupt Clear Register
0x4001_4024	I2S_DMACR_REG	I2S DMA Enable Register
0x5000_1314	I2S_CLK_SEL_REG	I2S Clock Divider Register

Table 180. I2S_CTRL0_REG (0x4001_4000)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	CLK_DIV	I2S_SCLK control factor. 4'h0: I2SCLK/2 4'h1: I2SCLK/4 4'h3: I2SCLK/8 4'h7: I2SCLK/16	4'b0011
11	R/W	STEREO	1 = Stereo 0 = Mono	1'b0
10:9	R/W	PCM_BW	PCM bus width for TX/RX. TX RX 2'b11: PCM_24 PCM_32 2'b10: PCM_20 PCM_24/PCM_20 2'b01: PCM_16 PCM_16 2'b00: PCM_8 PCM_8	2'b00
8	R/W	MUTE	If set, SDATA output assert 0.	1'b0
7	R/W	HALF_DELAY	Relationship between FS and SCLK. 1: Falling edge	1'b0
6	R/W	PCMM	If set, PCM mode is enabled.	1'b1
5	R/W	Right_Align	If set, PCM data output right is enabled.	1'b0
4	R/W	ENDIAN	SDATA output mode. 1 = Big endian 0 = Little endian	1'b0
3	R/W	MCLK_INV	If set, MCLK inversion.	1'b1
2	R/W	LRCK_INV	If set, LRCK inversion.	1'b0
1	R/W	I2S_Enalbe	If set, I2S block is enabled.	1'b0
0	R/W	CLK_DOWN	If set, output clock signals, LRCK/BCLK/SCLK, assert 0.	1'b0

Table 181. I2S_CTRL1_REG (0x4001_4004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	-
7	R/W	RxFIFO_Rst	Master RX FIFO reset. 0: Reset 1: Normal	1'b0
6	-	-	Reserved	
5	R/W	Left_Justify	RX decoding left justified.	1'b0
4	R/W	Rx_Mode	RX decoding edge. 0: Rising edge @ SCLK 1: Falling edge	1'b0
3	R/W	Mst_RxEn	Master RX load enable signal. 0: TX enable 1: RX enable	1'b0
2	-	-	Reserved	
1	R/W	Rx_ChSel	RX data channel selection. 0: RX decoding only Right channel 1: RX decoding only Left channel	1'b0
0	R/W	LR_ChSel	Left/Right Channel selection. 1: First data comes out LRCK high 0: First data comes out LRCK low duration	1'b0

Table 182. I2S_DATA_REG (0x4001_4008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	I2S_DATA	I2S_DATA. Write data @ TX Read data @ RX	32'b0000

Table 183. I2S_STATUS_REG (0x4001_400C)

Bit	Mode	Symbol	Description	Reset
5:0	R	Status	[5]: RX FIFO not empty [4]: RX FIFO full [2]: Busy [1]: TX FIFO not full [0]: TX FIFO empty	-

Table 184. I2S_IMASK_REG (0x4001_4014)

Bit	Mode	Symbol	Description	Reset
3	R/W	TXIM	TX FIFO DMA interrupt request mask. An interrupt is triggered when the TX FIFO becomes half full. 1 = Enable 0 = Disable	1'b0
2	R/W	RXIM	RX FIFO DMA interrupt request mask. An interrupt is triggered when RX FIFO becomes half full. 1 = Enable 0 = Disable	1'b0
1	R/W	RTIM	RX receive timeout interrupt mask. 1 = Enable 0 = Disable Reserved. Not used.	1'b0
0	R/W	RORIM	RX FIFO over run interrupt request mask.	1'b0

Bit	Mode	Symbol	Description	Reset
			An interrupt is triggered when RX FIFO becomes full. 1 = Enable 0 = Disable	

Table 185. I2S_ICR_REG (0x4001_4020)

Bit	Mode	Symbol	Description	Reset
0	R/W	RORIC	RX FIFO over run interrupt request clear.	1'b0

Table 186. I2S_DMACR_REG (0x4001_4024)

Bit	Mode	Symbol	Description	Reset
1	R/W	TXDMAE	TX DMA Enable. 1 = Enable 0 = Disable	1'b0
0	R/W	RXDMAE	RX DMA Enable. 1 = Enable 0 = Disable	1'b0

Table 187. I2S_CLK_SEL_REG (0x5000_1314)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	-	FNPLL frequency divider factor register. 3'h0: No clock 3'h1: FNPLL 1/2 3'h2: FNPLL 1/4 3'h3: FNPLL 1/8	3'b000

10.4 SDeMMC Register

Table 188. SDeMMC register

Address	Register	Description
Common control for SDeMMC Pin Status		
0x5003_0000	MMC_CTRL0_REG	Host Interface Control Register
0x5003_0004	MMC_EVNT_CTRL_REG	Event Control and Status Register
0x5003_0008	MMC_INT_CTRL_REG	Interrupt Control and Status Register
0x5003_000C	MMC_CLK_CNT_CTRL_REG	Host Clock Control Count Register
0x5003_0010	MMC_CMD_ARG_REG	Command Arguments Register
0x5003_0014	MMC_CMD_IDX_REG	Command Index Register
0x5003_0018	MMC_CMD_ARGQ_REG	Command Arguments Queue Register
0x5003_001C	MMC_CND_IDXQ_REG	Command Index Queue Register
0x5003_0020	MMC_PAD_CTRL_REG	Pad Control Register
0x5003_0024	MMC_BLK_LG_REG	Block Length Register
0x5003_0028	MMC_BLK_CNT_REG	Transfer Block Count Register
0x5003_002C	-	Reserved
0x5003_0030	MMC_RSP_TMO_CNT_REG	Response Time-Out Count Register
0x5003_0034	MMC_RD_TMO_CNT_REG	Read Data Time-Out Count Register
0x5003_0038	MMC_WB_TMO_CNT_REG	Write Busy Time-Out Count Register
0x5003_003C	MMC_RSP_CIX_ST_REG	Response Command Index Status Register
0x5003_0040	MMC_RSP_ARG_0_REG	Response Argument Status0 Register
0x5003_0044	MMC_RSP_ARG_1_REG	Response Argument Status1 Register
0x5003_0048	MMC_RSP_ARG_2_REG	Response Argument Status2 Register
0x5003_004C	MMC_RSP_ARG_3_REG	Response Argument Status3 Register
0x5003_0050	MMC_AHB_SA_REG	AHB Starting Address Register

Address	Register	Description
0x5003_0054	MMC_AHB_EA_REG	AHB End Address Register
0x5003_0058	-	Reserved
0x5003_005C	-	Reserved
0x5003_0060	MMC_BUS_ST_REG	Bus Status Register
0x5003_0064	MMC_SM_ST_REG	CMD/RSP and Data State Machine Status Register
0x5003_0068	MMC_XTR_CNT_REG	Transferred Data Block Count Status Register
0x5003_006C	MMC_ERR_CNT_REG	Error Data Block Count Status Register

Table 189. MMC_CTRL0_REG (0x5003_0000)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	ALL_RST	Reset all hardware circuit control. 0: Normal operation 1: Reset	1'b0
14	R/W	HIF_RST	Control register and hardware circuit control. 0: Normal operation 1: Reset	1'b0
13	R/W	CSM_RST	Command state machine reset control. 0: Normal operation 1: Reset	1'b0
12	R/W	DSM_RST	Data state machine reset control. 0: Normal operation 1: Reset	1'b0
11	R/W	STOP_XTR	Immediately stop the ongoing data transfer. 0: Normal operation 1: Immediately stop the ongoing data transfer	1'b0
9:8	R/W	WR_STR_CTL[1:0]	Data transfer start control for write operation. 2'b0x: The starting of write data is triggered by TRIG bit of HIF_CMD_IDX register. 2'b10: Not trigger the starting for write data operation. 2'b11: Trigger the starting for write data operation.	2'b00
7	R/W	HIF_PWR_CTL	Host interface power control. 0: Turn-off host interface power 1: Turn-on host interface power	1'b0
6	-	-	Reserved	
5	R/W	CDI_POL_CTL	Card detect input polarity control. 0: Active low 1: Active high	1'b0
4	R/W	RD_CRC_CHK	Read data CRC check control. 0: Disable 1: Enable	1'b1
3	R/W	RSP_CRC_CK	Response CRC check control. 0: Disable 1: Enable	1'b1
2	R/W	BUS_4BIT	4 Bit data bus mode. 0: 1-bit mode 1: 4-bit mode	1'b0
1	R/W	HIGH_SPD	High speed timing mode. 0: Default speed timing mode (SDC and SDATA[3:0] signals output at clock falling edge) 1: High speed timing mode (SDC and SDATA[3:0] signals output at clock rising edge)	1'b0
0	R/W	CDO_MODE	Command/data output mode. 0: Open drain mode 1: Push-pull mode	1'b0

Table 190. MMC_EVNT_CTRL_REG (0x5003_0004)

Bit	Mode	Symbol	Description	Reset
31	R	P_CD_IN_ST	Card detect pad status	1'b0
30	R	P_WP_IN_ST	Write protect pad status	1'b0
29	R/W	CD_IN_EST	Card detect event status. 0: No event generation 1: Event generation	1'b0
28	R/W	WP_IN_EST	Write protect event status. 0: No event generation 1: Event generation	1'b0
27	R/W	XTR_END_EST	Read/write data transfer end event status. 0: No event generation 1: Event generation	1'b0
26	R/W	BLK_END_EST	Read/write one block data event status. 0: No event generation 1: Event generation	1'b0
25	R/W	NG_CRCS_EST	Negative write CRC status token event status. 0: No event generation 1: Event generation	1'b0
24	R/W	WDB_TMO_EST	Write data busy time-out event status. 0: No event generation 1: Event generation	1'b0
23	R/W	RXT_END_EST	Read data transfer end event status. 0: No event generation 1: Event generation	1'b0
22	R/W	SRD_END_EST	Complete to read single block data event status. 0: No event generation 1: Event generation	1'b0
21	R/W	RD_CRCE_EST	Read data CRC error event status. 0: No event generation 1: Event generation	1'b0
20	R/W	RD_TMO_EST	Read data time-out event status. 0: No event generation 1: Event generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_EST	Command/response end event status. 0: No event generation 1: Event generation	1'b0
17	R/W	RP_CRCE_EST	Response CRC error event status. 0: No event generation 1: Event generation	1'b0
16	R/W	RSP_TMO_EST	Response time-out event status. 0: No event generation 1: Event generation	1'b0
15:14	-	-	Reserved	
13	R/W	CD_IN_ETE	Card detect event control. 0: Disable 1: Enable	1'b0
12	R/W	WP_IN_ETE	Write protect event control. 0: Disable 1: Enable	1'b1
11	R/W	XTR_END_ETE	Read/write data transfer end event control.	1'b1

Bit	Mode	Symbol	Description	Reset
			0: Disable 1: Enable	
10	R/W	BLK_END_ETE	Read/write one block data event control. 0: Disable 1: Enable	1'b0
9	R/W	NG_CRCS_ETE	Negative write CRC status token event control. 0: Disable 1: Enable	1'b1
8	R/W	WDB_TMO_ETE	Write data busy time-out event control. 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_ETE	Read data CRC error event control. 0: Disable 1: Enable	1'b1
4	R/W	RD_TMO_ETE	Read data time-out event control. 0: Disable 1: Enable	1'b1
3	-	-	Reserved	1'b1
2	R/W	RSP_END_ETE	Response end event control. 0: Disable 1: Enable	1'b1
1	R/W	RP_CRCE_ETE	Response CRC error event control. 0: Disable 1: Enable	1'b1
0	R/W	RSP_TMO_ETE	Response time-out event control. 0: Disable 1: Enable	1'b1

Table 191. MMC_INT_CTRL_REG (0x5003_0008)

Bit	Mode	Symbol	Description	Reset
31	R	HST_INT_ST	SD/eMMC host interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
30	-	-	Reserved	1'b0
29	R/W	CD_INT_ST	Card detect interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
28	R/W	WP_INT_ST	Write protect interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
27	R/W	XTR_END_IST	Read/write data transfer end interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
26	R/W	BLK_END_IST	Read/write one block data interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
25	R/W	NG_CRCS_IST	Negative write CRC token interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
24	R/W	WDB_TMO_IST	Write data busy time-out interrupt status.	1'b0

Bit	Mode	Symbol	Description	Reset
			0: No interrupt generation 1: Interrupt generation	
23:22	-	-	Reserved	1'b0
21	R/W	RD_CRCE_IST	Read data CRC error interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
20	R/W	RD_TMO_IST	Read data time-out interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_IST	Command/response end interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
17	R/W	RD_CRCE_IST	Read data CRC error interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
16	R/W	RSP_TMO_IST	Response time-out interrupt status. 0: No interrupt generation 1: Interrupt generation	1'b0
15	R/W	HST_ENT_EN	SD/eMMC host interrupt function enable control. 0: Disable 1: Enable	1'b0
14	-	-	Reserved	
13	R/W	CD_INT_EN	Card detect interrupt control. 0: Disable 1: Enable	1'b0
12	R/W	WP_INT_EN	Write protect interrupt control. 0: Disable 1: Enable	1'b0
11	R/W	XTR_INT_EN	Read/write data transfer end interrupt control. 0: Disable 1: Enable	1'b0
10	R/W	BLK_INT_EN	Read/write one block data interrupt control. 0: Disable 1: Enable	1'b0
9	R/W	NG_CRCS_INT	Negative write CRC status token interrupt control. 0: Disable 1: Enable	1'b0
8	R/W	WDB_TMO_INT	Write data busy time-out interrupt control. 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_INT	Read data CRC error interrupt control. 0: Disable 1: Enable	1'b0
4	R/W	RD_TMO_INT	Read data time-out interrupt control. 0: Disable 1: Enable	1'b0
3	-	-	Reserved	1'b0
2	R/W	RP_DIRE_INT	Response direction bit error interrupt control. 0: Disable	1'b0

Bit	Mode	Symbol	Description	Reset
			1: Enable	
1	R/W	RP_CRCE_INT	Response CRC error interrupt control. 0: Disable 1: Enable	1'b0
0	R/W	RSP_TMO_INT	Response time-out interrupt control. 0: Disable 1: Enable	1'b0

Table 192. MMC_CLK_CNT_CTRL_REG (0x5003_000C)

Bit	Mode	Symbol	Description	Reset
31:23	-	-	Reserved	-
22	R/W	STOP_HCLK	Enable to stop SD/eMMC interface clock. 0: Disable 1: Enable	1'b0
21	R/W	SYNC_STCTL	Synchronous circuit stage control. 0: 3-stage synchronizer (Low clock ratio) 1: 2-stage synchronizer (High clock ratio)	1'b0
20	R/W	HCLK_OE	HCLK output enable control. 0: Disable 1: Enable (Normal operation)	1'b1
19	-	-	Reserved	
18:17	R/W	HCLK_CTL	Internal host clock control 00: Turn off the internal host clock 01: Turn off the internal host clock immediately 10: Turn on the internal host clock immediately 11: Always turn on internal host clock	2'b11
16	R	HCLK_SW	Software host clock control. Note: Software can program this bit to high/low to toggle the internal host clock when HCLK_CTL[1:0] = 2'b00.	1'b0
15:0	R/W	HCLK_CT_CNT	Host Clock Control Count Register. This control register specifies the number of host clock to enable or stop the host clock signal.	16'h0

Table 193. MMC_CMD_ARG_REG (0x5003_0010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	HCLK_CMD_ARG	This register specifies the value of SD/eMMC command argument.	32'h0

Table 194. MMC_CMD_IDX_REG (0x5003_0014)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	CMDQ_TRIG	Trigger to transfer the value of Command Index and Argument registers into Command Index Queue and Command Argument Queue registers. The trigger (transfer) operation is only active when the value of this bit is high, and the status of command queue is not busy (QBUSY_ST).	1'b0
14	R/W	CMD_TCTL	Command trigger control. 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set. 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result was read.	1'b0

Bit	Mode	Symbol	Description	Reset
13	R/W	STB_CTL	Command start bit and transmission bit control. 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by hardware circuit. 1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register.	1'b0
12:11	R/W	RSP_TYPE	Response type control. 00: No response 01: R3 response 10: Short response (Total: 48 bits) 11: Long response (Total: 136 bits)	2'b00
10:9	R/W	DATA_TYPE	Data type control. 0x: Command only (without data transfer) 10: Command with single/multiple read data 11: Command with single/multiple write data	2'b00
8	-	-	Reserved	
7	R/W	STR_NIT	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used.	1'b0
6	R/W	TRM_BIT	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used.	1'b1
5:0	R/W	HIF_CMD_IDX	This register specifies the value of the SD/eMMC command index.	6'h0

Table 195. MMC_CMD_ARGQ_REG (0x5003_0018)

Bit	Mode	Symbol	Description	Reset
31:0	R	HCLK_CMD_ARG	This register is a queue to receive the value of the SD/eMMC command argument register when the trigger (transfer) operation is active.	32'h0

Table 196. MMC_CMD_IDXQ_REG (0x5003_001C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R	QBUSY_ST	Status of command queue. 0: Empty 1: Queued	1'b0
14	R	CMD_TCTLQ	Command trigger control queue. 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set. 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result was read.	1'b0
13:12	R	RSP_TYPEQ	Response type control queue. 0x: No response 10: Short response (Total: 48 bits) 11: Long response (Total: 136 bits)	2'b00
11	R	STB_CTL	Command start bit and transmission bit control queue. 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by hardware circuit.	1'b0

Bit	Mode	Symbol	Description	Reset
			1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register.	
10:8	R	DATA_TYPEQ	Data type control queue. 0xx: Command only (without data transfer) 100: Command with single read data 101: Command with multiple read data 110: Command with single write data 111: Command with multiple write data	3'b000
7	R	STR_NITQ	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used.	1'b0
6	R	TRM_BITQ	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used.	1'b1
5:0	R	HIF_CMD_IDXQ	This register specifies the value of the SD/eMMC command index.	6'h0

Table 197. MMC_PAD_CTRL_REG (0x5003_0020)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	-
29:28	R/W	HCOE_DLY	Output enable delay control for host command signal. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
27:26	R/W	HCO_DLY	Output delay control for host command signal. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
25:24	R/W	HCI_DLY	Input delay control for host command signal. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
23:22	R/W	HDATI_ST	Input Schmitt trigger level control for host data signals	2'b00
21:20	R/W	HDAT_PUD	Host data signals pull-up/pull-down control. 00: No Pull-up/Pull-down 01: Pull-down 10: Pull-up 11: Keeper	2'b00
19:16	R/W	HDATO_DS	Output drive strength control for host data signals	2'b00
15:14	R/W	HCMDI_ST	Input Schmitt trigger level control for host data signals	2'b00
13:12	R/W	HDAT_PUD	Host command signals pull-up/pull-down control. 00: No Pull-up/Pull-down 01: Pull-down 10: Pull-up 11: Keeper	2'b00
11:8	R/W	HCMDO_DS	Output drive strength control for host command signals	4'h0
7:6	-	-	Reserved	
5:4	R/W	HCLK_PUDC	Host clock signals pull-up/pull-down control.	2'b00

Bit	Mode	Symbol	Description	Reset
			00: No Pull-up/Pull-down 01: Pull-down 10: Pull-up 11: Keeper	
3:0	R/W	HCLK_DS	Host clock control count register. Output drive strength control for host clock signals.	4'h0

Table 198. MMC_BLK_LG_REG (0x5003_0024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	
27:16	R/W	HIF_BLK_LG	Block length register. This register specifies the length (unit: byte) of each block for read/write data transfer.	8'h0
15:6	-	-	Reserved	
5:4	R/W	HDOE_DLY	Output enable delay control for host data signals. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
3:2	R/W	HDO_DLY	Output delay control for host data signals. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
1:0	R/W	HDI_DLY	Input delay control for host data signals. 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00

Table 199. MMC_BLK_CNT_REG (0x5003_0028)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:0	R/W	HIF_BLK_CNT	Block Count Register	24'h0

Table 200. MMC_RSP_TMO_CNT_REG (0x5003_0030)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	RSP_TMO_CNT	This register specifies the number of host clock cycles for the response time-out interrupt. If the host cannot receive the response, it does not return to the host before the specified clock cycles.	8'h40

Table 201. MMC_RD_TMO_CNT_REG (0x5003_0034)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RD_TMO_CNT	Read Data Time-Out Count Register. This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles.	8'h0040_0000

Table 202. MMC_WB_TMO_CNT_REG (0x5003_0038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WB_TMO_CNT	Read Data Time-Out Count Register. This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles.	32'h0A00_0000

Table 203. MMC_RSP_CIX_ST_REG (0x5003_003C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7	R	RSP_STR_B	Status of the start bit of the received response. R2 response: RSP[135] Other responses: RSP[47]	1'b0
6	R	RSP_DIR_B	Status of the direction (Transmission) bit of the received response. R2 response: RSP[134] Other responses: RSP[46]	1'b0
5:0	R	RSP_CMD_IDX	Status of the command Index of the received response. R2 response: RSP[133:128] Other responses: RSP[45:40]	6'h0

Table 204. MMC_RSP_ARG0_REG (0x5003_0040)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG0	Status of the received response argument 0. R2 response: RSP[127:96] Other responses: RSP[39:8]	32'h00

Table 205. MMC_HIF_RSP_ARG1_REG (0x5003_0044)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG1	Status of the received response argument 1. R2 response: RSP[95:64] Other responses: Reserved	32'h00

Table 206. MMC_RSP_ARG2_REG (0x5003_0048)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG2	Status of the received response argument 2. R2 response: RSP[63:32] Other responses: Reserved	32'h00

Table 207. MMC_RSP_ARG3_REG (0x5003_004C)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG3	Status of the received response argument 3. R2 response: RSP[31:0] Other responses: Reserved	32'h00

Table 208. MMC_AHB_SA_REG (0x5003_0050)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_SA	This register specifies the start address of AHB bus for data transfer.	32'h00

Table 209. MMC_AHB_EA_REG (0x5003_0054)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_EA	This register specifies the end address of AHB bus for data transfer.	32'h00

Table 210. MMC_BUS_ST_REG (0x5003_0060)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7	R/W	RSP_RET_ST	Receive the response from the device. 0: Not receive 1: Receive	1'b0
6	R	CMD_BUSY	CMD/RSP status machine busy status. 0: Not ongoing command/response (Idle) 1: Have ongoing command/response (Busy)	1'b0
5	R	DAT_BUSY	Data status machine busy status. 0: Not ongoing data transfer (Idle) 1: Have ongoing data transfer (Busy)	1'b0
4	R	HCMD_ST	Status of host interface CMD signal	1'b0
3:0	R	RSP_CMD_IDX	Status of host interface Data signals	4'h0

Table 211. MMC_SM_ST_REG (0x5003_0064)

Bit	Mode	Symbol	Description	Reset
31:16	R	HIF_DAT_CNT	Data count status	16'h0
15:13	-	-	Reserved	-
12:8	R	HIF_DAT_SM	Data state machine status	5'h0
7:5	-	-	Reserved	-
4:0	R	HIF_CMD_SM	CMD/RSP state machine status	5'h0

Table 212. MMC_XTR_CNT_REG (0x5003_0068)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:0	R	RSP_TMO_CNT	Transferred data block count status. This register reports the number of the transferred data blocks. The value of this counter is cleared after a new read/write command was sent.	24'h00

Table 213. MMC_ERR_CNT_REG (0x5003_006C)

Bit	Mode	Symbol	Description	Reset
31:25	-	-	Reserved	-
24	R/W	ERR_CNT_FG	Error count flag. **Read**: 0: No data CRC error. 1: Data CRC error (Read CRC error or Non-positive Write CRC status token). **Write**: Clear the error count flag for allowing to record the data error block count. 0: No effect. 1: Clear the error count flag for allowing to record the data error block count when the data CRC error occurred.	1'b0
23:0	R	HIF_ERR_CNT	ERR data block count status. This register recorded the number of error data blocks. When the first data error occurs (Read CRC error or received the non-positive write CRC status token) during the read/write data transfer, the value of the transferred data block count is recorded into this register. The software needs to write 1 into the CLE_ERR_CNT bit to clear the internal flag that it controls, to record the error block count or not when the data error occurred.	24'h00

10.5 SPI and I2C Register

Table 214. SPI slave and I2C master/slave registers

Address	Register	Description
Common control for SPI slave and I2C slave pin status		
0x5008_023C	SPI_INTR_STATUS_REG	SPI Interrupt Status Register
0x5008_0240	SPI_CTRL_REG	SPI Control Register
0x5008_0244	I2C_CTRL_REG	I2C Control Register
0x5008_0248	SPI_LENGTH_REG	SPI Length Register
0x5008_024C	I2C_BUFFER_ADDR_REG	I2C Buffer Address Register
0x5008_0250	SPI_BASE_ADDR_REG	SPI Base Address Register
0x5008_0254	CMD_ADDR_REG	Command Address Register
0x5008_0258	RESP_ADDR1_REG	Response Address1 Register
0x5008_025C	RESP_ADDR2_REG	Response Address2 Register
0x5008_0260	AT_CMD_BASE_REG	AT Command Base Address Register
0x5008_0264	AT_CMD_REF_REG	AT Command Base Address Register
0x5008_0268	SPI_TIMER_REG	SPI Timer Register
0x5008_02C0	CLK_GATE_REG	Clock Gating Register
0x5008_02D0	PERI_MAN_RST_REG	Peripheral Manual Reset Register
Common control for I2C master pin status		
0x4001_5000	I2C_CR0_REG	I2C Control0 Register
0x4001_5004	I2C_CR1_REG	I2C Control1 Register
0x4001_5008	I2C_DR_REG	I2C Data Register
0x4001_500C	I2C_SR_REG	I2C Status Register
0x4001_5010	I2C_CPSR_REG	I2C Clock Pre-scale Register
0x4001_5014	I2C_IMSC_REG	I2C Interrupt Mask Register
0x4001_5018	I2C_RIS_REG	I2C Interrupt Status Register
0x4001_501C	I2C_MIS_REG	I2C Masked Interrupt Status Register
0x4001_5020	I2C_ICR_REG	I2C Interrupt Clear Register
0x4001_5024	I2C_DMACR_REG	I2C DMA Control Register
0x4001_5028	I2C_BUSCR_REG	I2C Bus Control Register
0x4001_502C	I2C_RDLEN_REG	I2C Read Length Register
0x4001_5030	I2C_DRVID_REG	I2C Device ID Register
0x4001_5034	I2C_SWRST_REG	I2C Soft Reset Register
0x4001_5038	I2C_OE_SEL_REG	I2C Output Delay Selection Register

Table 215. SPI_INTR_STATUS_REG (0x5008_023C)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	INTR	SPI slave interrupt status register. bit[15]: Command interrupt status/clear bit[14]: AT Command interrupt status/clear bit[13]: Processing end interrupt status/clear	0x0
12:0	R/W	-	Reserved	0x000

Table 216. SPI_CTRL_REG (0x5008_0240)

Bit	Mode	Symbol	Description	Reset
15	R/W	CmdIntr	Command interrupt enable. 1: Enable 0: Disable	1'b0
14	R/W	ATIntr	AT Command interrupt enable. 1: Enable 0: Disable	1'b0

Bit	Mode	Symbol	Description	Reset
13	R/W	PEIntr	Processing end interrupt enable. 1: Enable 0: Disable	1'b0
12	R/W	Prot	Protocol mode. 1: 8-byte 0: 4-byte (default)	1'b0
11	R/W	SW_Rst	SPI block software reset. 1: Normal 0: Reset state	1'b1
10	R/W	-	MISO Output mode selection. 1: Normal 0: Half Pre output	1'b1
9	R/W	-	Reserved	1'b0
8	R/W	Endian	Endian mode for Data	1'b1
7:6	R/W	MODE	Define the SPI mode (CPOL/CPHA). 0: New data on falling, capture on rising, CLK low in idle state 1: New data on rising, capture on falling, CLK low in idle state 2: New data on rising, capture on falling, CLK high in idle state 3: New data on falling, capture on rising, CLK high in idle state	2'b00
5:4	R/W	ChipID	Valid when 8-byte protocol mode. Effective when matching ChipID field is the same as command[1:0] on the SPI protocol function.	2'b00
3:2	R/W	DBusW	Data bus width. 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = Not used	2'b10
1:0	R/W	ABusW	Address bus width. 00 = 8-bit 01 = 16-bit 10 = 24-bit 11 = 32-bit (default)	2'b11

Table 217. I2C_CTRL_REG (0x5008_0244)

Bit	Mode	Symbol	Description	Reset
7	R/W	SW_Rst	I2C block software reset. 1: Normal 0: Reset state	1'b0
6	R/W	Endian	Endian mode for Data	1'b1
5:4	R/W	ChipID	Device ID for lower 2-bit	2'b00
3:2	R/W	DBusW	Data bus width. 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = Not used	2'b10
1:0	R/W	ABusW	Address bus width. 00 = 8-bit 01 = 16-bit 10 = 24-bit	2'b11

Bit	Mode	Symbol	Description	Reset
			11 = 32-bit (default)	

Table 218. SPI_LENGTH_REG (0x5008_0248)

Bit	Mode	Symbol	Description	Reset
23:0	R/W	Length	SPI reference length at read access	0x0100

Table 219. I2C_BUFFER_ADDR_REG (0x5008_024C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Length	I2C buffer address	0x0000

Table 220. SPI_BASE_ADDR_REG (0x5008_0250)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	BaseAddr	When the 4-byte control type is used, this register contains the upper 2 bytes of the address field.	0x0000

Table 221. CMD_ADDR_REG (0x5008_0254)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CmdAddr	Write/Read request. If accessed, internal interrupt should be generated.	0x0000

Table 222. RESP_ADDR1_REG (0x5008_0258)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #1	0x0000

Table 223. RESP_ADDR2_REG (0x5008_025C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #2	0x0000

Table 224. AT_CMD_BASE_REG (0x5008_0260)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command base address. Indicate the AT command reference register.	0x0000

Table 225. AT_CMD_REF_REG (0x5008_0264)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command reference register. Indicate the SRAM address that external AP accesses.	0x0000

Table 226. SPI_TIMER_REG (0x5008_0268)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Timer	Optional	0x1000

Table 227. CLK_GATE_REG (0x5008_02C0)

Bit	Mode	Symbol	Description	Reset
2	R/W	eMMC_EN	SDeMMC clock gating on/off. 1: Clock gating enable 0: Disable	0x0
1	R/W	SDIO_EN	SDIO clock gating on/off. 1: Clock gating enable 0: Disable	0x0
0	R/W	SPI_EN	SPI Slave clock gating on/off. 1: Clock gating enable	0x0

Bit	Mode	Symbol	Description	Reset
			0: Disable	

Table 228. PERI_MAN_RST_REG (0x5008_02D0)

Bit	Mode	Symbol	Description	Reset
7	R/W	eMMC_RST	Manual reset for SDeMMC (active low). 1: Normal operation 0: Reset	0x1
6	R/W	SDIO_RST	Manual reset for SDIO (active low). 1: Normal operation 0: Reset	0x1
5	R/W	AuxADC_RST	Manual reset for AuxADC (active low). 1: Normal operation 0: Reset	0x1
4	R/W	I2S_RST	Manual reset for I2S (active low). 1: Normal operation 0: Reset	0x1
3	R/W	UART1_RST	Manual reset for UART1 (active low). 1: Normal operation 0: Reset	0x1
2	R/W	UART0_RST	Manual reset for UART0 (active low). 1: Normal operation 0: Reset	0x1
1	R/W	I2C_MST_RST	Manual reset for I2C Master (active low). 1: Normal operation 0: Reset	0x1
0	R/W	I2C_SLV_RST	Manual reset for I2C Slave (active low). 1: Normal operation 0: Reset	0x1

Table 229. I2C_CR0_REG (0x4001_5000)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	SCR	Serial clock rate. Bit rate = FSSPCLK/(CPSDVR x (1+SCR)) CPSDVR: Even number among 2~254 SCR: 0~255	0x00
7:4	R/W	FRF	Reserved	0x0
3:0	R/W	DSS	Data size select. 0111: 8-bit data Others: Not used	0x0

Table 230. I2C_CR1_REG (0x4001_5004)

Bit	Mode	Symbol	Description	Reset
15:5	R/W	-	Reserved	0x00
4	R/W	STEP2	Read/Write step 2-phase enable. 1: Enable 0: Disable	0x0
3	R/W	-	Reserved	0x0
2	R/W	MS	Master or Slave mode select. 0: Master (default) 1: Slave	0x0
1	R/W	SSE	I2C Port enable (soft reset in NACK detected)	0x0
0	R/W	LBM	Loop back mode (only test mode).	0x0

Bit	Mode	Symbol	Description	Reset
			If the LBM input is asserted, RXD is connected to TXD to implement loopback, and otherwise it connected to IICRXD pad input. 1: Enable 0: Disable	

Table 231. I2C_DR_REG (0x4001_5008)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	DATA	Transmit/Receive FIFO data. Read: Receive FIFO data Write: Transmit FIFO data	0x00

Table 232. I2C_SR_REG (0x4001_500C)

Bit	Mode	Symbol	Description	Reset
15	R	BSY	Busy flag. 0: Idle 1: Currently transmitting and/or receiving a frame or the transmit FIFO is not empty	0x00
14:6	R	-	Reserved	0x0
5	R	WrDone	Write Access done. 0: Processing 1: Write done	0x0
4	R	RdDone	Read Access done. 0: Processing 1: Read done	0x0
3	R	RFF	Receive FIFO full. 0: Not full 1: Full	0x0
2	R	RNE	Receive FIFO not empty. 0: Empty 1: Not empty	0x0
1	R	TNF	Transmit FIFO not full. 0: Full 1: Not full	0x0
0	R	TFE	Transmit FIFO empty. 0: Not empty 1: Empty	0x0

Table 233. I2C_CPSR_REG (0x4001_5010)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	-	Reserved	0x00
7:0	R/W	CPSDVSR	Clock pre-scale divisor, even number from 2 to 254.	0x0

Table 234. I2C_IMSC_REG (0x4001_5014)

Bit	Mode	Symbol	Description	Reset
15:7	R/W	-	Reserved	0x00
6	R/W	WrDone	Write done interrupt mask. 1: Enable 0: Disable	0x0
5	R/W	RdDone	Read done interrupt mask. 1: Enable 0: Disable	0x0
4	R/W	NACKIM	NACK interrupt mask.	0x0

Bit	Mode	Symbol	Description	Reset
			1: Enable 0: Disable	
3	R/W	TXIM	Transmit FIFO interrupt mask. 1: Enable 0: Disable	0x0
2	R/W	RXIM	Received FIFO interrupt mask. 1: Enable 0: Disable	0x0
1	R/W	RTIM	Receive timeout interrupt mask. 1: Enable 0: Disable	0x0
0	R/W	RORIM	Receive overrun interrupt mask. 1: Enable 0: Disable	0x0

Table 235. I2C_RIS_REG (0x4001_5018)

Bit	Mode	Symbol	Description	Reset
15:7	R	-	Reserved	0x00
6	R	WrDoneRIS	Write done raw interrupt status. 1: Write done 0: No interrupt	0x0
5	R	RdDoneRIS	Read done raw interrupt status. 1: Read done 0: No interrupt	0x0
4	R	NACKRIS	NACK interrupt status. 1: NACK state 0: Not	0x0
3	R	TXRIS	Transmit FIFO raw interrupt source. Unmasked state of the I2CTXINTR interrupt. Asserted when the Transmit FIFO contains four or fewer valid entries. 1: Interrupt due to the TX FIFO becoming half full 0: No interrupt	0x0
2	R	RXRIS	Receive FIFO raw interrupt status. Unmasked state of the I2CRXINTR interrupt. Asserted when the Receive FIFO contains four or more valid entries. 1: Interrupt due to the RX FIFO becoming half empty 0: No interrupt	0x0
1	R	RTRIS	RX time out raw interrupt status. Unmasked state of the I2CRTINTR interrupt. 1: Interrupt due to time out 0: No interrupt	0x0
0	R	RORRIS	Receive over run raw interrupt status. Unmasked state of the I2CRORINTR interrupt. The RORRIS signal is set when the Receive FIFO is Full. 1: Interrupt due to the RX FIFO becoming full 0: No interrupt	0x0

Table 236. I2C_MIS_REG (0x4001_501C)

Bit	Mode	Symbol	Description	Reset
15:7	R	-	Reserved	0x00

Bit	Mode	Symbol	Description	Reset
6	R	WrDoneMIS	Write done masked interrupt status. 1: Write done 0: No interrupt	0x0
5	R	RdDoneMIS	Read done masked interrupt status. 1: Read done 0: No interrupt	0x0
4	R	NACKMIS	NACK masked interrupt status. 1: NACK state 0: No interrupt	0x0
3	R	TXMIS	TX FIFO masked interrupt status. Masked status of the I2CTXINTR interrupt. 1: Interrupt due to the TX FIFO becoming half full 0: No interrupt	0x0
2	R	RXMIS	RX FIFO masked interrupt status. Masked status of the I2CRXINTR interrupt. 1: Interrupt due to the RX FIFO becoming half empty 0: No interrupt	0x0
1	R	RTMIS	RX time out masked interrupt status. Masked status of the I2CRTINTR interrupt. 1: Interrupt due to time out 0: No interrupt	0x0
0	R	RORMIS	RX FIFO over run masked interrupt status. Masked status of the I2CRORINTR interrupt. 1: Interrupt due to the RX FIFO becoming full 0: No interrupt	0x0

Table 237. I2C_ICR_REG (0x4001_5020)

Bit	Mode	Symbol	Description	Reset
15:2	W	-	Reserved	0x00
1	W	RTIC	RX time out interrupt clear. Clear the I2CRTINTR interrupt. 1: Interrupt clear	0x0
0	W	RORIC	RX over run interrupt clear. Clear the I2CRORINTR interrupt. 1: Interrupt clear	0x0

Table 238. I2C_DMACR_REG (0x4001_5024)

Bit	Mode	Symbol	Description	Reset
15:2	R/W	-	Reserved	0x00
1	R/W	TXDMAE	Transmit DMA enable. If set to 1, DMA for the transmit FIFO is enabled.	0x0
0	R/W	RXDMAE	Receive DMA enable. If set to 1, DMA for the receive FIFO is enabled.	0x0

Table 239. I2C_BUSCR_REG (0x4001_5028)

Bit	Mode	Symbol	Description	Reset
15:5	R/W	-	Reserved	0x00
4	R/W	STOP_EN	Stop bit control. 1: Enable 0: Disable	0x0
3	R/W	RdAcc	Read access enable. 1: Read access	0x0

Bit	Mode	Symbol	Description	Reset
			0: Write access	
2:0	R/W	AdrSize	Address size. Range: 0 ~ 7	0x0

Table 240. I2C_RDLEN_REG (0x4001_502C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	RdLEN	Data read length. Range: 1 ~ 65535	0x00

Table 241. I2C_DRVID_REG (0x4001_5030)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	-	Reserved	0x00
7:1	R/W	DEVID	Slave device ID 7-bit. The last bit is read or write control bit. It is auto inserted with RDACC flag.	--
0	R/W	-	Reserved	

Table 242. I2C_SWRST_REG (0x4001_5034)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Reserved	0x00
0	R/W	SW_RST	TX/RX FIFO soft reset (active low)	0x0

Table 243. I2C_OE_SEL_REG (0x4001_5038)

Bit	Mode	Symbol	Description	Reset
15:4	R/W	-	Reserved	0x00
3:0	R/W	OE_SEL	Data output delay selection. Range: 0 ~ 15	0x0

10.6 RTC Register

Table 244. RTC registers

Address	Register	Description
0x5009_1000	wakeup_counter0	Wake-up Counter [31:0]
0x5009_1004	wakeup_counter1	Wake-up Counter [35:32]
0x5009_1008	gpio_wakeup_config	Wake Up by GPIO Config Register
0x5009_100C	gpio_wakeup_control	Wake Up by GPIO Control Register
0x5009_1010	rtc_control	RTC Control Register
0x5009_1014	xtal_control	32 kHz XTAL Control Register
0x5009_1018	retention_control	Retention Memory Power Control Register
0x5009_101C	dc_power_control	DC-DC Control Register
0x5009_1020	ldo_control	Control LDOs
0x5009_1024	-	Reserved
0x5009_1028	wakeup_source	Wake Up Source
0x5009_102C	-	Reserved
0x5009_1030	-	Reserved
0x5009_1034	-	Reserved
0x5009_1038	counter0	Real Time Counter [31:0]
0x5009_103C	counter1	Real Time Counter [35:32]
0x5009_1040	ldo_status	LDO Status Register
0x5009_1044	ldo_pwr_control	uLDO Control Register
0x5009_1048	-	Reserved

Address	Register	Description
0x5009_104C	bor_circuit	Brownout/Blackout Control Register
0x5009_1050	-	Reserved
0x5009_1054	-	Reserved
0x5009_1058	-	Reserved
0x5009_105C	watchdog_cnt	RTC Watchdog Counter
0x5009_1060	AuxADC12_CTRL	ADC Control Register
0x5009_1064	AuxADC12_TLevel10	ADC Threshold Level Register for channel 1/0
0x5009_1068	AuxADC12_TLevel32	ADC Threshold Level Register for channel 3/2
0x5009_106C	AuxADC12_SP_NUM	ADC Sample Number Register
0x5009_1070	AuxADC12_TIMER_SET	ADC Sensor Control Register
0x5009_1074	PulseCnt_CTRL	PulseCnt Control Register
0x5009_1078	PulseCnt_TLevel	PulseCnt Threshold Level Register
0x5009_107C	PulseCnt_CNT	PulseCnt Count Value Register

Table 245. wakeup_counter0 (0x5009_1000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	-	RTC timer value to wake up the chip. Bits [31:0] of the 36 bits wake-up counter.	0x00000000

Table 246. wakeup_counter1 (0x5009_1004)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	-	RTC timer value to wake up the chip. Bits [35:32] of the 36 bits wake-up counter.	0x0

Table 247. gpio_wakeup_config (0x5009_1008)

Bit	Mode	Symbol	Description	Reset
25:16	R/W	-	Wake-up source selection (Note 1). [16] 0: GPIOA4 1: GPIOC0 [17] 0: GPIOA5 1: GPIOC1 [18] 0: GPIOA6 1: GPIOC2 [19] 0: GPIOA7 1: GPIOC3 [20] 0: GPIOA8 1: GPIOC4 [21] 0: GPIOA9 1: GPIOC6 [22] 0: GPIOA10 1: GPIOC7 [23] 0: GPIOA11 1: GPIOC8 [24] 0: GPIOC5 1: GPIOA12 [25] 0: GPIOA13 1: GPIOA14	0x000
12:10	R/W	-	Edge selection of RTC_WAKE_UP2/3/4 (Note 2). [12] RTC_WKAE_UP4 [11] RTC_WAKE_UP3 [10] RTC_WAKE_UP2 0: Rising edge 1: Falling edge	0x0
9:0	R/W	-	Edge selection: selected signal by [25:16]. 0: Rising edge 1: Falling edge	0x000

Note 1 GPIOA[11:0] and GPIOC[8:6] can be used in 6x6.

Note 2 RTC_WAKE_UP and RTC_WAKE_UP2 can be used in 6x6.

Table 248. gpio_wakeup_control (0x5009_100C)

Bit	Mode	Symbol	Description	Reset
28:26	R/W	-	Wake-up enable (Note 1). [28] RTC_WAKE_UP4 [27] RTC_WAKE_UP3 [26] RTC_WAKE_UP2 0: Wake-up disable 1: Wake-up enable	0x0
25:16	R/W	-	Wake-up enable of selected signal by gpio_wakeup_config[25:16]. 0: Wake-up disable 1: Wake-up enable	0x000
13:10	R	-	Indicate wake up source. [13] RTC_WAKE_UP4 [12] RTC_WAKE_UP3 [11] RTC_WAKE_UP2 [10] RTC_WAKE_UP 1: Indicate wake up from the port	0x0
9:0	R	-	Indicate GPIO wakeup source 9:0. 1: Indicate wake up from the port	0x000

Note 1 RTC_WAKE_UP and RTC_WAKE_UP2 can be used in 6x6.

Table 249. rtc_control (0x5009_1010)

Bit	Mode	Symbol	Description	Reset
6	R/W	-	Wake-up enable for RTC_WAKE_UP. 0: Wake-up disable 1: Wake-up enable	1'b0
5	R/W	-	Brownout interrupt enable field. 0: Interrupts are not enabled 1: When an event occurs, IRQ is generated	1'b0
4	R/W	-	Blackout interrupt enable field. 0: Interrupts are not enabled 1: When an event occurs, IRQ is generated	1'b0
3	R/W	-	RTC Watchdog count. 0: Count disable 1: Count enable	1'b0
2	R/W	-	RTC_WAKE_UP input polarity selection. 0: Rising edge 1: Falling edge	1'b0
1	R/W	-	RTC_WAKE_UP interrupt enable (Normal mode). 0: Interrupts are not enabled 1: When an event occurs, IRQ is generated	1'b0
0	R/W	-	Power down enable. 0: No effect 1: Go to power down mode	1'b0

Table 250. xtal_control (0x5009_1014)

Bit	Mode	Symbol	Description	Reset
10	R/W	-	VBAT BIAS current control. 0: Max current 1: Min current	1'b0
9:8	R/W	-	XTAL LDO current control. 0: Max current	2'b00

Bit	Mode	Symbol	Description	Reset
			3: Min current	
7:5	R/W	-	40M XTAL LDO output voltage control	3'b100
4	R/W	EN_XR_BAT	External resistor enable. 0: Internal resistor used 1: External resistor used	1'b0
3:2	R/W	CLK_SEL	Select clock source (default 32 kHz OSC). 0: 32 kHz OSC 1: 32 kHz Crystal 2: For test	2'b00
1	R/W	EN_XTAL_BAT	32 kHz crystal power on/off (default:1). 0: Off 1: On	1'b1
0	R/W	EN_OSC	32 kHz oscillator power on/off (default:1). 0: Off 1: On	1'b1

Table 251. retention_control (0x5009_1018)

Bit	Mode	Symbol	Description	Reset
27:24	R/W	-	GPIO retention control bit. [27] FDIO region [26] GPIOC [25] GPIOA [24] Reserved 0: Disable 1: Enable	4'b0000
22:16	R/W	RET_RET	Retention memory Retention mode enable. 0: Disable 1: Enable	7'b0000000
14:8	R/W	RET_SLR]	Retention memory Sleep mode enable (when memory goes to sleep, it lost the content of the memory). 0: Disable 1: Enable	7'b0000000
7:4	R/W	-	Power down information	4'b0000
2	R/W	-	PDB_ISO_shared_io (GPIOA0~3) 0: Isolation enable, cannot access to GPIOA0~3 1: Isolation disable, access to GPIOA0~3	1'b1
1	R/W	RTM_INFORM	-	1'b0
0	R/W	-	PDB_ISO default 0. 1: Isolation disable, access to Retention Memory 0: Isolation enable, cannot access to Retention Memory	1'b0

Table 252: dc_power_control (0x5009_101C)

Bit	Mode	Symbol	Description	Reset
1	R/W	-	Auto power on enable. 0: No effect 1: When set to 1, go to sleep and wake up automatically, all register values are reset	1'b0
0	R/W	-	DCDC1.2 power off. 0: No effect 1: When set to 1, DC-DC1.2 Off	1'b0

Table 253. ldo_control (0x5009_1020)

Bit	Mode	Symbol	Description	Reset
9	R/W	EN_IP1_LDO	0: IP1 LDO power off 1: IP1 LDO power on	1'b0
8	R/W	PDB_RF_LDO	0: RF LDO power off 1: RF LDO power on	1'b0
7	R/W	EN_DIG_LDO_CNTL	0: DIG LDO power off 1: DIG LDO power on	1'b1
6	R/W	EN_DCDC_CNTL_XTAL	0: DIG LDO power off 1: DIG LDO power on	1'b1
5	R/W	PDB_uLDO	PDB_uLDO for retention memory power supply LDO control. 0: LDO off 1: LDO on	1'b0
4	R/W	EN_IP3_OTP_PWR	OTP power switch. 0: OTP block power off 1: OTP block power on	1'b1
3	R/W	OTP_PWRRDY	OTP power stable. 0: OTP block power is not ready 1: OTP block power is stable	1'b1
2	R/W	EN_LDO_PLL1	EN_LDO_PLL1: for PLL power. 0: PLL LDO off 1: PLL LDO on	1'b0
1	-	-	Reserved	
0	R/W	EN_XTAL_NOISE_REDU	XTAL noise reduction circuit. 0: No effect 1: Noise reduction circuit on	1'b0

Table 254. wakeup_source (0x5009_1028)

Bit	Mode	Symbol	Description	Reset
11:8	R	-	ADC sensor wakeup status: indicates ADC wakeup source pin. [11]: Sensor Wakeup GPIOA3 [10]: Sensor Wakeup GPIOA2 [9]: Sensor Wakeup GPIOA1 [8]: Sensor Wakeup GPIOA0	4'h0
6	R/W	-	DWAKE source detect. Read case: 1: Indicate wakeup source from GPIOs Write cases: 0: Wait for event 1: Source clear	1'b0
5	R/W	-	Pulse CNT detect. Read case: 1: Indicate wakeup source from pulse CNT function Write cases: 0: Wait for event 1: Source clear	1'b0
4	R/W	-	Sensor (ADC) detect. Read case: 1: Indicate wakeup source from ADC sensor function Write case: 0: Wait for event	1'b0

Bit	Mode	Symbol	Description	Reset
			1: Source clear	
3	R/W	-	Watchdog detect. Read case: 1: Indicate wakeup source from RTC watchdog Write case: 0: Wait for event 1: Source clear	1'b0
2	R/W	-	POR indicator. Read case: 1: Indicate wakeup source from POR port Write case: 0: Wait for event 1: Source clear	1'b0
1	R/W	-	FRC compare detect. Read case: 1: Indicate wakeup from RTC count meet the wanted value Write case: 0: Wait for event 1: Source clear	1'b0
0	R/W	-	Ext wakeup signal detect. Read case: 1: Indicate wakeup source from RTC_WAKE_UPx pins Write case: 0: Wait for event 1: Source clear	1'b0

Table 255. counter0 (0x5009_1038)

Bit	Mode	Symbol	Description	Reset
31:0	R	-	RTC free running counter read value [31:0]	0x00

Table 256. counter1 (0x5009_103C)

Bit	Mode	Symbol	Description	Reset
3:0	R	-	RTC free running counter read value [35:32]	0x00

Table 257. ldo_status (0x5009_1040)

Bit	Mode	Symbol	Description	Reset
13	R	IP1_LDO_RDY	1: IP1_LDO is ready	1'b0
12	R	DCDC_RDY	1: DCDC is ready	1'b0
11	R	F_LDO_RDY	1: Flash LDO is ready	1'b0
10	R	DIG_LDO_RDY	1: DIG LDO is ready	1'b0
9	R	RF_LDO_RDY	1: RF LDO is ready	1'b0
8	R	XTAL40M_RDY	1: XTAL 40 MHz clock is ready	1'b0
7	R	-	Reserved	-
6	R	-	Reserved	-
5	R	-	Reserved	-
4	R	-	Reserved	-
3	R	XTAL32K_RDY	1: XTAL 32 kHz is ready	1'b0
2	R	-	Reserved	-
1	R	-	Reserved	-
0	R	-	Represent pin status of RTC_WAKE_UP	-

Table 258. ldo_pwr_control (0x5009_1044)

Bit	Mode	Symbol	Description	Reset
29	R/W	DCDC_ST-BYP	0: Soft start bypass disable 1: Soft start bypass enable	1'b0
28:24	R/W	DCDC_ST_CTRL	DCDC soft start timing control delay time.	5'b01011
21	R/W	IP2_MON_PATH_CTRL	0: LDO and low frequency path 1: RF clock path	1'b0
20:18	R/W	IP2_MON_CTRL	For testing purpose	3'b0
17:16	R/W	RTC_XTAL32K_GM	XTAL 32 kHz gain control	2'b11
15:14	R/W	RTC_OSC32K_ICTRL	Osc32K sleep current control, 00: min ~ 11: max	2'h0
13:12	R/W	RTC_TAL32K_ICTRL	XTAL32K sleep current control, 00: min ~ 11: max	2'b01
11:10	R/W	RTC_uLDO_LICTRL	uLDO sleep current control, 00: min~ 11: max	2'b01
9:8	R/W	RTC_uLDO_HICTRL	uLDO speed up control 00: Low speed 11: High speed	2'b11
7:4	R/W	RTC_uLDO_VCTRL	uLDO output voltage control. 4'b0001 (1.12 V) ~ 4'b1111 (0.8 V)	4'b0001
1	R/W	RPDB_TEST_BUF	PDB_TEST_BUF: IP2 test buffer enable	1'b0
0	R/W	-	RTC clock inversion: for test purpose. 0: Bypass 1: Inversion	1'b0

Table 259. bor_circuit (0x5009_104C)

Bit	Mode	Symbol	Description	Reset
14	R	-	BR status read. 1: Brownout event occurred	-
13	R	-	BL status read. 1: Blackout event occurred	-
12	R/W	BR_HYS_CTRL	0: Hysteresis 100 mV (Default) 1: Hysteresis 150 mV	1'b0
11	R/W	BL_HYS_CTRL	0: Hysteresis 100 mV (Default) 1: Hysteresis 150 mV	1'b0
10	R/W	-	Reserved	1'b0
9	R/W	BR_OUT_EN	BR_OUT_EN (brownout) 0: Disable BR logic 1: Enable BR logic	1'b0
8	R/W	BL_OUT_EN	BL_OUT_EN (blackout) 0: Disable BL logic 1: Enable BL logic	1'b0
7:4	R/W	BR_OUT_CTRL	Voltage threshold for the brownout detector.	4'b0111
3:0	R/W	BL_OUT_CTRL	Voltage threshold for the blackout detector.	4'b0101

Table 260. watchdog_cnt (0x5009_105C)

Bit	Mode	Symbol	Description	Reset
6:5	R	-	Watchdog count read value.	-
4:0	R/W	-	Free running counter[35:14] bit selection.	0x00

Table 261. AuxADC12_CTRL (0x5009_1060)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:14	R/W	BITNUM	ADC sample bit number. 3 = 12-bit	0x0

Bit	Mode	Symbol	Description	Reset
			2 = 10-bit 1 = 6-bit 0 = 4-bit	
13:12	R/W	IVREF	-	0x0
11:10	R/W	ICOMPS	Free running counter[35:14] bit selection	0x0
9:8	R/W	ICOMP	-	0x0
7	R/W	SS_EN	-	0x0
6:4	R/W	TRIM	-	0x0
3:2	R/W	CS	ADC channel selection. 0 = ADC channel 0 1 = ADC channel 1 2 = ADC channel 2 3 = ADC channel 3	0x0
1	R/W	PDB	-	0x0
0	R/W	RESET	-	0x1

Table 262. AuxADC12_TLevel10 (0x5009_1064)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	
29:28	R/W	-	Threshold level condition for channel-1. 0 = Over threshold 1 = Under threshold 2 = Difference threshold 3 = Reserved	0x0
27:16	R/W	-	Threshold level0[11:0] for channel-1	0x0
15:14	R/W	-	Reserved	0x0
13:12	R/W	-	Threshold level condition for channel-0. 0 = Over threshold 1 = Under threshold 2 = Difference threshold 3 = Reserved	0x0
11:0	R/W	-	Threshold level0[11:0] for channel-0	0x0

Table 263. AuxADC12_TLevel32 (0x5009_1068)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	-
29:28	R/W	-	Threshold level condition for channel-3. 0 = Over threshold 1 = Under threshold 2 = Difference threshold 3 = Reserved	0x0
27:16	R/W	-	Threshold level0[11:0] for channel-3	0x0
15:14	R/W	-	Reserved	0x0
13:12	R/W	-	Threshold level condition for channel-2. 0 = Over threshold 1 = Under threshold 2 = Difference threshold 3 = Reserved	0x0
11:0	R/W	-	Threshold level0[11:0] for channel-2	0x0

Table 264. AuxADC12_SP_NUM (0x5009_106C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:3	R/W	-	ADC sample select range	0x0
2:0	R/W	-	Sample number for average (sample count = 2^{n+2}). 0 = 4-sample processing 1 = 8-sample processing 7 = 512-sample processing	0x0

Table 265. AuxADC12_TIMER_SET (0x5009_1070)

Bit	Mode	Symbol	Description	Reset
31:29	-	-	Reserved	-
28:24	R/W	ASWCH	Auto switch control. [28] = Auto-switch activate [27] = Selection enable with Ch-3 [26] = Selection enable with Ch-2 [25] = Selection enable with Ch-1 [24] = Selection enable with Ch-0 For example, if set b'10111, auto switch enables with channel-2, 1, and 0.	0x0
23:14	R/W	-	Reserved	-
13:8	R/W	SUB_CNT	Timer value (sub_cnt). Delta T = 8/32.768 kHz x sub_cnt Valid range = 0x00 ~ 0x3B Max. = 0x3B	0x1
7	R/W	SEN_ACT	Sensor detect activate. 1 = Sensor mode enable 0 = Normal mode	0x0
6:4	R/W	X12_CLK	Timer count clock source (base = 32.768 kHz). 3'b000 = 7.81-msec period 3'b001 = 15.6-msec period 3'b010 = 62.5-msec period 3'b011 = 250-msec period 3'b100 = 1000-msec period 3'b101 = 4000-msec period 3'b110 = 16000-msec period 3'b111 = 64,000-msec period	0x0
3:0	R/W	MAIN_CNT	Timer value (main_cnt). Periodic cycle = X12_CLK x (MAIN_CNT+1) Valid range = 0x0 ~ 0xE Max value = 0xE	0xF

Table 266. PulseCnt_CTRL (0x5009_1074)

Bit	Mode	Symbol	Description	Reset
23	-	-	Reserved	-
22:21	R	CompINT	Interrupt threshold and counter compare value	0x0
20	R/W		Reserved	0x0
19:16	R/W	CLK_SEL	Pulse counter operation clock select. 0: 32 kHz 1: 15 MHz	0x0
15	R/W	PSEL	Input pulse selection.	0xF

Bit	Mode	Symbol	Description	Reset
			4'd0: GPIO_IN0 4'd1: GPIO_IN1 4'd2: GPIO_IN2 4'd3: GPIO_IN3 4'd4: GPIO_IN4 4'd5: GPIO_IN5 4'd6: GPIO_IN6 4'd7: GPIO_IN7 4'd8: GPIO_IN8 4'd9: GPIO_IN9 4'd10: Wakeup	
14	R/W	INT_CLR	Interrupt clear. 1: Clear	0x0
13:4	R/W	INT_EN	Interrupt enable. 1: Enable 0: Disable	0x0
3	R/W	-	Reserved	0x0
2	R/W	EDGE	Counter clock edge selection. 1: Falling edge 0: Rising edge	0x0
1	R/W	RST	Pulse counter reset (active low)	0x0
0	R/W	EN	Pulse counter enable. 1: Enable 0: Disable	0x0
	R/W	15M_EN	OSC_15 MHz enable. 1: 15 MHz clock enable 0: Disable	0x0

Table 267. PulseCnt_TLevel (0x5009_1078)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	INT_THR	Threshold level for counter value	0x0

Table 268. PulseCnt_CNT (0x5009_107C)

Bit	Mode	Symbol	Description	Reset
31:0	R	CNT	Counter value of edge	0x0

10.7 External Interrupt Control Register

Table 269. External interrupt control registers

Address	Register	Description
0x5000_1200	EXT_INTB_CTRL_REG	External Interrupt Control Register
0x5000_1204	EXT_INTB_SET_REG	External Interrupt Set Register

Table 270. EXT_INTB_CTRL_REG (0x5000_1200)

Bit	Mode	Symbol	Description	Reset
7:2	R/W	-	Pulse duration. (unit: 256 CPU clocks) Valid when edge mode.	6’b100000
1	R/W	-	Interrupt mode. 0: Level mode 1: Edge mode	1’b0
0	R/W	-	Interrupt polarity.	1’b0

Bit	Mode	Symbol	Description	Reset
			0: Active low 1: Active high	

Table 271. EXT_INTB_SET_REG (0x5000_1204)

Bit	Mode	Symbol	Description	Reset
0	R/W	-	External interrupt set register. When level mode, set 1 for trigger and 0 for clear. When edge mode, set 1 and it clears automatically after pulse width.	1'b0

10.8 ADC Register

Table 272. ADC registers

Address	Register	Description
0x4001_6000	XADC12B_CTRL_REG	Aux ADC 12-bit Control Register
0x4001_6008	SWITCHING_MODE_REG	Aux ADC 12-bit Channel Enable Register
0x4001_600C	XADC12B_THR_INTR_MASK_REG	Interrupt Enable Register from Threshold Level Register
0x4001_6010	XADC12B_THR_INTR_CLR_REG	Interrupt Clear Register from Threshold Level Register
0x4001_6014	XADC12B_FIFO_INTR_MASK_REG	Interrupt Mask Set Register
0x4001_6018	XADC12B_INTR_STATUS_REG	Interrupt Status Set Register
0x4001_601C	XADC12B_DMA_EN_REG	FIFO 3 ~ FIFO 0 DMA Enable Register
0x4001_6020	FIFO0_DMA_DATA_REG	FIFO0 DMA Data for Channel 0 Register
0x4001_6024	FIFO1_DMA_DATA_REG	FIFO1 DMA Data for Channel 1 Register
0x4001_6028	FIFO2_DMA_DATA_REG	FIFO2 DMA Data for Channel 2 Register
0x4001_602C	FIFO3_DMA_DATA_REG	FIFO3 DMA Data for Channel 3 Register
0x4001_6030	XADC12B_RM_SAMPLE_REG	The Number of Removing Initial Samples Register
0x4001_6034	XADC12B_ST_SAMPLE_REG	The Number of Sampling Interval Register
0x4001_6038	XADC12B_INTR_THR_OVER_REG	Over Threshold Value of Interrupt Register
0x4001_6040	ADC12B_INTR_THR_UNDER_REG	Under Threshold Value of Interrupt
0x4001_6048	ADC12B_INTR_THR_DIFF_REG	Difference Threshold Value of Interrupt
0x4001_6050	FIFO0_DATA_CURR_REG	Aux ADC12-bit Current Data for Channel 0 Register
0x4001_6054	FIFO1_DATA_CURR_REG	Aux ADC12-bit Current Data for Channel 1 Register
0x4001_6058	FIFO2_DATA_CURR_REG	Aux ADC12-bit Current Data for Channel 2 Register
0x4001_605C	FIFO3_DATA_CURR_REG	Aux ADC12-bit Current Data for Channel 3 Register
0x4001_6060	TIME_STAMP_CTRL_REG	Time Stamp Base Count Level Register
0x4001_6064~ 6C	-	Reserved
0x4001_7048	DA_R3	Bandgap Reference Voltage Selection
0x4001_705C	DA_R8	DAC Left Channel PGA Gain Select
0x4001_7060	DA_R9	DAC Right Channel PGA Gain Select
0x4001_7100	R40	AD Reset, Activate, and Select
0x4001_710C	R43	MCLK_ADC Divisor
0x4001_7110	R44	SINC Reset and Decimation Rate
0x4001_712C	AD_R0	VH Voltage Reference Level Selection

Table 273. XADC12B_CTRL_REG (0x4001_6000)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	0x0
8	R/W	DF	Aux ADC12-bit data format. 0: 2's complement 1: Offset binary	0x0

Bit	Mode	Symbol	Description	Reset
7:5	R/W	TRIM	Trim VREF voltage for Aux ADC12-bit control	0x0
3:2	R/W	CS	Channel select input for Aux ADC12-bit control signal. 0: VIN1 1: VIN2 2,3: Reserved	0x0
1	R/W	POWDN	Power down for Aux ADC12-bit control signal. 0: No power down 1: Power down	0x1
0	R/W	RSTB	Reset for Aux ADC12-bit control signal. 0: No reset 1: Reset	0x1

Table 274. SWITCHING_MODE_REG (0x4001_6008)

Bit	Mode	Symbol	Description	Reset
8	R/W	AUTO_SCH_EN	Auto switching enable for using multi-channel. When setting the register, must set to 0x000->01x0. 0: Disable 1: Enable	0x0
7:4	R/W	CH_EN	Aux ADC 12-bit enable for each channel. [7]: 12-bit 4th channel enable [6]: 12-bit 3rd channel enable [5]: 12-bit 2nd channel enable [4]: 12-bit 1st channel enable	0x1
3:0	-	-	Reserved	0x1

Table 275. XADC12B_THR_INTR_MASK_REG (0x4001_600C)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	INT_LVL	Interrupt when exceeds a threshold level. [11]: Threshold difference interrupt mask of FIFO3 [10]: Threshold difference interrupt mask of FIFO2 [9]: Threshold difference interrupt mask of FIFO1 [8]: Threshold difference interrupt mask of FIFO0 [7]: Under threshold interrupt mask of FIFO3 [6]: Under threshold interrupt mask of FIFO2 [5]: Under threshold interrupt mask of FIFO1 [4]: Under threshold interrupt mask of FIFO0 [3]: Over threshold interrupt mask of FIFO3 [2]: Over threshold interrupt mask of FIFO2 [1]: Over threshold interrupt mask of FIFO1 [0]: Over threshold interrupt mask of FIFO0	0x00

Table 276. XADC12B_THR_INTR_CLR_REG (0x4001_6010)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	INT_CLR	Interrupt when exceeds a threshold level. [11]: Threshold difference interrupt clear of FIFO3 [10]: Threshold difference interrupt clear of FIFO2 [9]: Threshold difference interrupt clear of FIFO1 [8]: Threshold difference interrupt clear of FIFO0 [7]: Under level interrupt clear of FIFO3 [6]: Under level interrupt clear of FIFO2 [5]: Under level interrupt clear of FIFO1 [4]: Under level interrupt clear of FIFO0 [3]: Over level interrupt clear of FIFO3 [2]: Over level interrupt clear of FIFO2	0x00

Bit	Mode	Symbol	Description	Reset
			[1]: Over level interrupt clear of FIFO1 [0]: Over level interrupt clear of FIFO0	

Table 277. XADC12B_FIFO_INTR_MASK_REG (0x4001_6014)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	INT_MASK	Interrupt mask set. bit[7]: Interrupt mask for full level of FIFO 3 bit[6]: Interrupt mask for full level of FIFO 2 bit[5]: Interrupt mask for full level of FIFO 1 bit[4]: Interrupt mask for full level of FIFO 0 bit[3]: Interrupt mask for half level of FIFO 3 bit[2]: Interrupt mask for half level of FIFO 2 bit[1]: Interrupt mask for half level of FIFO 1 bit[0]: Interrupt mask for half level of FIFO 0	0x00

Table 278. XADC12B_INTR_STATUS_REG (0x4001_6018)

Bit	Mode	Symbol	Description	Reset
19:0	RO	INT_STS	Interrupt status set. bit[19]: Interrupt status for threshold difference of FIFO 3 bit[18]: Interrupt status for threshold difference of FIFO 2 bit[17]: Interrupt status for threshold difference of FIFO 1 bit[16]: Interrupt status for threshold difference of FIFO 0 bit[15]: Interrupt status for threshold under level of FIFO 3 bit[14]: Interrupt status for threshold under level of FIFO 2 bit[13]: Interrupt status for threshold under level of FIFO 1 bit[12]: Interrupt status for threshold under level of FIFO 0 bit[11]: Interrupt status for threshold over level of FIFO 3 bit[10]: Interrupt status for threshold over level of FIFO 2 bit[9]: Interrupt status for threshold over level of FIFO 1 bit[8]: Interrupt status for threshold over level of FIFO 0 bit[7]: Interrupt status for full level of FIFO 3 bit[6]: Interrupt status for full level of FIFO 2 bit[5]: Interrupt status for full level of FIFO 1 bit[4]: Interrupt status for full level of FIFO 0 bit[3]: Interrupt status for half level of FIFO 3 bit[2]: Interrupt status for half level of FIFO 2 bit[1]: Interrupt status for half level of FIFO 1 bit[0]: Interrupt status for half level of FIFO 0	0x00

Table 279. XADC12B_DMA_EN_REG (0x4001_601C)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	DMA_EN	FIFO 3 ~ FIFO 0 DMA enable. [3]: FIFO 3 0: Disable 1: Enable [2]: FIFO 2 0: Disable 1: Enable [1]: FIFO 1 0: Disable 1: Enable [0]: FIFO 0	0x0

Bit	Mode	Symbol	Description	Reset
			0: Disable 1: Enable	

Table 280. FIFO0_DMA_DATA_REG (0x4001_6020)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO0 DMA data for Aux ADC12-bit channel 0 sampled data. Interrupt indicates to read 4 consecutive sampled data with half-level FIFO or 8 consecutive sampled data with full-level FIFO. Sampled data is constructed: [15:4] 12-bit sampled data from Aux ADC12-bit [3:0] 4 bits are filled with zero	0x00

Table 281. FIFO1_DMA_DATA_REG (0x4001_6024)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO1 DMA data for Aux ADC12-bit channel 1 sampled data. Interrupt indicates to read 4 consecutive sampled data with half-level FIFO or 8 consecutive sampled data with full-level FIFO. Sampled data is constructed: [15:4] 12-bit sampled data from Aux ADC12-bit [3:0] 4 bits are filled with zero	0x00

Table 282. FIFO2_DMA_DATA_REG (0x4001_6028)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO2 DMA data for Aux ADC12-bit channel 2 sampled data. Interrupt indicates to read 4 consecutive sampled data with half-level FIFO or 8 consecutive sampled data with full-level FIFO. Sampled data is constructed: [15:4] 12-bit sampled data from Aux ADC12-bit [3:0] 4 bits are filled with zero	0x00

Table 283. FIFO3_DMA_DATA_REG (0x4001_602C)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	FIFO3 DMA data for Aux ADC12-bit channel 3 sampled data. Interrupt indicates to read 4 consecutive sampled data with half-level FIFO or 8 consecutive sampled data with full-level FIFO. Sampled data is constructed: [15:4] 12-bit sampled data from Aux ADC12-bit [3:0] 4 bits are filled with zero	0x00

Table 284. XADC12B_RM_SAMPLE_REG (0x4001_6030)

Bit	Mode	Symbol	Description	Reset
15:8	R/W	-	The number of removing initial samples of Aux ADC12-bit.	0x10
7:0	-	-	Reserved	0x00

Table 285. XADC12B_ST_SAMPLE_REG (0x4001_6034)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	-	The number of sampling interval of Aux ADC12-bit in Auto switching mode. 0, 1 = Internal none 2~15 = N-1 interval sampling	0x2
3:0	-	-	Reserved	0x0

Table 286. XADC12B_INTR_THR_OVER_REG (0x4001_6038)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Over threshold value of interrupt	0x00
0	R/W	-	Over threshold enable. 0: Disable 1: Enable	0x1

Table 287. XADC12B_INTR_THR_UNDER_REG (0x4001_6040)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Over threshold value of interrupt	0x00
0	R/W	-	Under threshold enable. 0: Disable 1: Enable	0x1

Table 288. XADC12B_INTR_THR_DIFF_REG (0x4001_6048)

Bit	Mode	Symbol	Description	Reset
15:1	R/W	-	Difference threshold value of interrupt	0x00
0	R/W	-	Difference threshold enable. 0: Disable 1: Enable	0x1

Table 289. FIFO0_DATA_CURR_REG (0x4001_6050)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO0 data of Aux ADC12-bit	0x00

Table 290. FIFO1_DATA_CURR_REG (0x4001_6054)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO1 data of Aux ADC12-bit	0x00

Table 291. FIFO2_DATA_CURR_REG (0x4001_6058)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO2 data of Aux ADC12-bit	0x00

Table 292. FIFO3_DATA_CURR_REG (0x4001_605C)

Bit	Mode	Symbol	Description	Reset
15:0	RO	-	Current FIFO3 data of Aux ADC12-bit	0x00

Table 293. TIME_STAMP_CTRL_REG (0x4001_6060)

Bit	Mode	Symbol	Description	Reset
11:8	R/W	-	Time Stamp base count level 12-bit ADC (default = 'd5)	0x5
7:0	-	-	Reserved	0x0

10.9 CRC Register

Table 294. CRC32 registers

Address	Register	Description
0x5004_0200	CRC_REQ_CTRL_REG	Stop Request of CRC Calculation, active high with auto clear function
0x5004_0204	CRC_OP_EN_REG	Operation Enable of CRC Calculation
0x5004_0208	CRC_CONFIG_REG	Configuration of CRC Calculation Input Data
0x5004_020C	CRC_SEED_VAL_REG	CRC seed value
0x5004_0210	CRC_ADDR_MIN_REG	Minimum address to check the bus address range

Address	Register	Description
0x5004_0214	CRC_ADDR_MAX_REG	Maximum address to check the bus address range
0x5004_0218	CRC_PSEUDO_VAL_REG	CRC pseudo value to accumulate manually
0x5004_0220	CRC_CAL_VAL_REG	CRC calculation value
0x5004_0224	CRC_STA_REG	Status of CRC Calculation
0x5004_0228	CRC_CAL_VAL_REV_REG	CRC calculation reversed value

Table 295. CRC_REQ_CTRL_REG (0x5004_0200)

Bit	Mode	Symbol	Description	Reset
2	WO	CRC_REQ_STOP	Stop request of CRC calculation, active high with auto clear function	0x0
1	WO	CRC_REQ_START	Start request of CRC calculation, active high with auto clear function	0x0
0	WO	CRC_REQ_CLR	Clear request of CRC calculation, active high with auto clear function	0x0

Table 296. CRC_OP_EN_REG (0x5004_0204)

Bit	Mode	Symbol	Description	Reset
0	R/W	CRC_OP_EN	Operation enable of CRC calculation	0x1

Table 297. CRC_CONFIG_REG (0x5004_0208)

Bit	Mode	Symbol	Description	Reset
27:26	R/W	CRC_OP_TYPE	Operation type of CRC calculation. 0: CRC-32 1: CRC-16 CCITT 2: CRC-16 IBM	0x0
25	R/W	CRC_CHK_MST	Master checking enable of CRC calculation for **slave path selection**	0x1
24	R/W	CRC_CHK_ADDR	Address checking enable of CRC calculation	0x1
20:16	R/W	CRC_MST_TYPE	Master type of CRC calculation for slave path selection in master checking enable. 0x00: Slave 0 (unused) 0x05: Slave 5 (unused) 0x14: Master 4 (uDMA or kDMA) 0x16: Master 6 (SSI) 0x17: Master 7 (fDMA-M0) 0x18: Master 8 (fDMA-M1) 0x19: Master 9 (CC-312) 0x1A: Master A (Flash controller)	0x16
13	R/W	CRC_SWAP_EN	Input data swap enable. 0: Normal 1: Byte swap	0x0
12	R/W	CRC_ENDIAN_TYPE	Input endian type. 0: Big endian (if 8 bits access: 0->1->2->3->4->5->6->7) 1: Little endian (if 8 bits access: 7->6->5->4->3->2->1->0)	0x0
11	R/W	CRC_DAT_TYPE	Data type of CRC calculation. 0: Normal data 1: Header data (Header bytes are all zero during CRC Calculation)	0x0
10:9	R/W	CRC_PAR_TYPE	Parallel type of CRC calculation. 00: 8 bits 01: 16 bits 10: 32 bits	0x2
8	R/W	CRC_ACC_TYPE	Access type of CRC calculation. 0: Read access 1: Write access	0x1

Bit	Mode	Symbol	Description	Reset
4:0	R/W	CRC_PATH_SEL	Path selection of CRC calculation. 0x00: Slave 0 0x05: Slave 5 0x14: Master 4 (uDMA or kDMA) 0x16: Master 6 (SSI) 0x17: Master 7 (fDMA-M0) 0x18: Master 8 (fDMA-M1) 0x19: Master 9 (CC-312) 0x1A: Master A (Flash Controller)	0x17

Table 298. CRC_SEED_VAL_REG (0x5004_020C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_SEED_VAL	CRC seed value	0xFFFF_FFFF

Table 299. CRC_ADDR_MIN_REG (0x5004_0210)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_ADDR_MIN	Minimum address to check the bus address range	0x0

Table 300. CRC_ADDR_MAX_REG (0x5004_0214)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_ADDR_MAX	Maximum address to check the bus address range	0xFFFF_FFFF

Table 301. CRC_PSEUDO_VAL_REG (0x5004_0218)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CRC_PSEUDO_VAL	CRC pseudo value to accumulate manually	0x0

Table 302. CRC_CAL_VAL_REG (0x5004_0220)

Bit	Mode	Symbol	Description	Reset
31:0	RO	CRC_CAL_VAL	CRC calculation value	0x0

Table 303. CRC_STA_REG (0x5004_0224)

Bit	Mode	Symbol	Description	Reset
25:24	RO	CRC_CAL_STA	Status of CRC calculation. 0: Idle 1: Busy 2: Stop 3: Error	0x0
19:0	RO	CRC_CAL_NUM	Number of CRC calculation bytes (Max. 1M bytes)	0x0

Table 304. CRC_CAL_VAL_REV_REG (0x5004_0228)

Bit	Mode	Symbol	Description	Reset
31:0	RO	CRC_CAL_VAL_REV	CRC calculation reversed value	0x0

10.10 PWM Register

Table 305. PWM registers

Address	Register	Description
0x4000_A000	PWM_EN0	PWM #0 signal enable
0x4000_A004	PWM_EN1	PWM #1 signal enable
0x4000_A008	PWM_EN2	PWM #2 signal enable
0x4000_A00C	PWM_EN3	PWM #3 signal enable
0x4000_A010	PWM_MAXCY0	PWM #0 CNT0's max value

Address	Register	Description
0x4000_A014	PWM_MAXCY1	PWM #1 CNT1's max value
0x4000_A018	PWM_MAXCY2	PWM #2 CNT2's max value
0x4000_A01C	PWM_MAXCY3	PWM #3 CNT3's max value
0x4000_A020	PWM_HDUTY0	PWM #0 high signal's threshold value
0x4000_A024	PWM_HDUTY1	PWM #1 high signal's threshold value
0x4000_A028	PWM_HDUTY2	PWM #2 high signal's threshold value
0x4000_A02C	PWM_HDUTY3	PWM #3 high signal's threshold value
0x4000_A030	PWM_MC_OFFS0	PWM #0 setting offset
0x4000_A034	PWM_MC_OFFS1	PWM #1 setting offset
0x4000_A038	PWM_MC_OFFS2	PWM #2 setting offset
0x4000_A03C	PWM_MC_OFFS3	PWM #3 setting offset
0x4000_A040	MC_MODE	0: (HDUTYx >= CNTx) ? 1'b1 : 1'b0; 1: (HDUTYx >= CNTx - MC_OFFSx) ? 1'b1 : 1'b0;

Table 306. PWM_EN0 (0x4000_A000)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN0	PWM #0 signal enable	0x00

Table 307. PWM_EN1 (0x4000_A004)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN1	PWM #1 signal enable	0x00

Table 308. PWM_EN2 (0x4000_A008)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN2	PWM #2 signal enable	0x00

Table 309. PWM_EN3 (0x4000_A00C)

Bit	Mode	Symbol	Description	Reset
0	R/W	PWM_EN3	PWM #3 signal enable	0x00

Table 310. PWM_MAXCY0 (0x4000_A010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY0	PWM #0 CNT0's max value	0x00

Table 311. PWM_MAXCY1 (0x4000_A014)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY1	PWM #1 CNT1's max value	0x00

Table 312. PWM_MAXCY2 (0x4000_A018)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY2	PWM #2 CNT2's max value	0x00

Table 313. PWM_MAXCY3 (0x4000_A01C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MAXCY3	PWM #3 CNT3's max value	0x00

Table 314. PWM_HDUTY0 (0x4000_A020)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY0	PWM #0 high signal's threshold value	0x00

Table 315. PWM_HDUTY1 (0x4000_A024)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY1	PWM #1 high signal's threshold value	0x00

Table 316. PWM_HDUTY2 (0x4000_A028)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY2	PWM #2 high signal's threshold value	0x00

Table 317. PWM_HDUTY3 (0x4000_A02C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_HDUTY3	PWM #3 high signal's threshold value	0x00

Table 318. PWM_MC_OFFS0 (0x4000_A030)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS0	PWM #0 setting offset	0x00

Table 319. PWM_MC_OFFS1 (0x4000_A034)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS1	PWM #1 setting offset	0x00

Table 320. PWM_MC_OFFS2 (0x4000_A038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS2	PWM #2 setting offset	0x00

Table 321. PWM_MC_OFFS3 (0x4000_A03C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	PWM_MC_OFFS3	PWM #3 setting offset	0x00

Table 322. MC_MODE (0x4000_A040)

Bit	Mode	Symbol	Description	Reset
0	R/W	MC_MODE	0: (HDUTYx >= CNTx) ? 1'b1 : 1'b0; 1: (HDUTYx >= CNTx - MC_OFFSx) ? 1'b1 : 1'b0;	0x00

10.11 kDMA Register

Table 323. kDMA registers

Address	Register	Description
0x4000_E000	dma_enable	Enable DMA. 1: Enable DMA 0: Disable DMA
0x4000_E004	dma_reset	Software reset. (Write 1 resets DMA and automatically returns to 0)
0x4000_E008	cfg_descriptor_addr	Base address of first task descriptor memory area
0x4000_E00C	cfg_channel_enable	Enable a DMA channel. 1: Enable channel 0: Disable channel
0x4000_E010	cfg_irq_done_type	dma_done interrupt type. 0: dma_done interrupt occurs when DMA chain is done 1: dma_done interrupt occurs when DMA task is done 2: dma_done interrupt occurs when REQ_MODE is 0 and arbitration period is done 3: Reserved

Address	Register	Description
0x4000_E014	sw_request	Software DMA request. (Write 1 sends request signal and automatically returns to 0)
0x4000_E018	irq_done_chs	Indicator of which channel invokes dma_done.
0x4000_E01C	irq_done_clr	Clear irq_done_chs. (Write 1 clears irq_done_chs, and automatically returns to 0)
0x4000_E020	irq_err_chs	Indicator of which channel invokes dma_err.
0x4000_E024	irq_err_clr	Clear irq_err_chs. (Write 1 clears irq_done_chs, and automatically returns to 0)
0x4000_E028	status_dma	Current status of DMA. Pending channel bitmap: Pending channel's bitmap. Current active channel: Current operating DMA channel number. Current state on FSM: Current state of FSM.
0x4000_E02C	status_desc_addr	Address of current task descriptor.
0x4000_E030	status_counter	Counters of current DMA task. arb_last flag: The flag to check whether the operating arbitration period is the last one of current task. arb_done counter: The number of operated arbitration period in current task. tf_last flag: The flag to check whether the operating transfer is the last one of current arbitration period. tf_done counter: The number of operated transfers in current arbitration period.
0x4000_E034	status_descriptor	Current task descriptor.
0x4000_E038	status_desc_addr_pre	Address of previous task descriptor.
0x4000_E03C	ahb_hprot_3_to_0	HPROT signal of AHB bus. [3]: Modifiable (1: Cacheable, 0: Non-cacheable) [2]: Bufferable (1: Bufferable, 0: Non-bufferable) [1]: Privileged (1: Privileged, 0: User access) [0]: Data/Opcode (1: Data access, 0: Opcode fetch)
0x4000_E040	ahb_hprot_7_to_4	
0x4000_E044	ahb_hprot_11_to_8	
0x4000_E048	ahb_hprot_15_to_12	

Table 324. DMA_ENABLE (0x4000_E000)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	dma_enable	Enable DMA. 0: Disable DMA 1: Enable DMA	1'b0

Table 325. DMA_RESET (0x4000_E004)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	WO	dma_reset	Software reset. (Write 1 resets DMA, and automatically returns to 0)	1'b0

Table 326. CFG_DESCRIPTOR_ADDR (0x4000_E008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	cfg_descriptor_addr	Base address of first task descriptor memory area	32'd0

Table 327. CFG_CHANNEL_ENABLE (0x4000_E00C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-

Bit	Mode	Symbol	Description	Reset
15:0	R/W	cfg_channel_enable	[15:0] Channel number	16'd0

Table 328. CFG_IRQ_DONE_TYPE (0x4000_E010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	cfg_irq_done_type	[31:30] Channel 15 done type [29:28] Channel 14 done type ... [1:0] Channel 0 done type	32'd0

Table 329. SW_REQUEST (0x4000_E014)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	WO	sw_request	[15:0] Channel number	16'd0

Table 330. IRQ_DONE_CHS (0x4000_E018)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	RO	Irq_done_chs	[15:0] Channel number	16'd0

Table 331. IRQ_DONE_CLR (0x4000_E01C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	WO	Irq_done_clr	[15:0] Channel number	16'd0

Table 332. IRQ_ERR_CHS (0x4000_E020)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	RO	Irq_err_chs	[15:0] Channel number	16'd0

Table 333. IRQ_ERR_CLR (0x4000_E024)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	WO	Irq_err_clr	[15:0] Channel number	16'd0

Table 334. STATUS_DMA (0x4000_E028)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:20	RO	state_on_fsm	Current state on FSM	4'd0
19:16	RO	act_channel	Current active channel	4'd0
15:0	RO	pending_ch	Pending channel number	16'd0

Table 335. STATUS_DESC_ADDR (0x4000_E02C)

Bit	Mode	Symbol	Description	Reset
31:0	RO	status_desc_addr	Address of current task descriptor	32'd0

Table 336. STATUS_COUNTER (0x4000_E030)

Bit	Mode	Symbol	Description	Reset
31	RO	arb_last_flag	The flag to check whether the operating arbitration period is the last one of current task.	1'b0
30:16	RO	arb_done_counter	The number of operated arbitration period in current task.	15'd0

Bit	Mode	Symbol	Description	Reset
15	RO	tf_last_flag	The flag to check whether the operating transfer is the last one of current arbitration period.	1'b0
14:0	RO	tf_done_counter	The number of operated transfers in current arbitration period.	15'd0

Table 337. STATUS_DESCRIPTOR (0x4000_E034)

Bit	Mode	Symbol	Description	Reset
31:0	RO	dma_task_descriptor	Current task descriptor	32'd0

Table 338. STATUS_DESC_ADDR_PRE (0x4000_E038)

Bit	Mode	Symbol	Description	Reset
31:0	RO	address	Address of previous task descriptor	32'd0

Table 339. AHB_HPROT_3_TO_0 (0x4000_E03C)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch3_src_hprot	HPROT signal of AHB bus. [3]: Modifiable (1: Cacheable, 0: Non-cacheable) [2]: Bufferable (1: Bufferable, 0: Non-bufferable) [1]: Privileged (1: Privileged, 0: User access) [0]: Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch3_dst_hprot		4'd1
23:20	R/W	ch2_src_hprot		4'd1
19:16	R/W	ch2_dst_hprot		4'd1
15:12	R/W	ch1_src_hprot		4'd1
11:8	R/W	ch1_dst_hprot		4'd1
7:4	R/W	ch0_src_hprot		4'd1
3:0	R/W	ch0_dst_hprot		4'd1

Table 340. AHB_HPROT_7_TO_4 (0x4000_E040)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch7_src_hprot	HPROT signal of AHB bus. [3]: Modifiable (1: Cacheable, 0: Non-cacheable) [2]: Bufferable (1: Bufferable, 0: Non-bufferable) [1]: Privileged (1: Privileged, 0: User access) [0]: Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch7_dst_hprot		4'd1
23:20	R/W	ch6_src_hprot		4'd1
19:16	R/W	ch6_dst_hprot		4'd1
15:12	R/W	ch5_src_hprot		4'd1
11:8	R/W	ch5_dst_hprot		4'd1
7:4	R/W	ch4_src_hprot		4'd1
3:0	R/W	ch4_dst_hprot		4'd1

Table 341. AHB_HPROT_11_TO_8 (0x4000_E044)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch11_src_hprot	HPROT signal of AHB bus. [3]: Modifiable (1: Cacheable, 0: Non-cacheable) [2]: Bufferable (1: Bufferable, 0: Non-bufferable) [1]: Privileged (1: Privileged, 0: User access) [0]: Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
27:24	R/W	ch11_dst_hprot		4'd1
23:20	R/W	ch10_src_hprot		4'd1
19:16	R/W	ch10_dst_hprot		4'd1
15:12	R/W	ch9_src_hprot		4'd1
11:8	R/W	ch9_dst_hprot		4'd1
7:4	R/W	ch8_src_hprot		4'd1
3:0	R/W	ch8_dst_hprot		4'd1

Table 342. AHB_HPROT_15_TO_12 (0x4000_E048)

Bit	Mode	Symbol	Description	Reset
31:28	R/W	ch15_src_hprot	HPROT signal of AHB bus. [3]: Modifiable (1: Cacheable, 0: Non-cacheable) [2]: Bufferable (1: Bufferable, 0: Non-bufferable) [1]: Privileged (1: Privileged, 0: User access)	4'd1
27:24	R/W	ch15_dst_hprot		4'd1
23:20	R/W	ch14_src_hprot		4'd1
19:16	R/W	ch14_dst_hprot		4'd1

Bit	Mode	Symbol	Description	Reset
15:12	R/W	ch13_src_hprot	[0]: Data/Opcode (1: Data access, 0: Opcode fetch)	4'd1
11:8	R/W	ch13_dst_hprot		4'd1
7:4	R/W	ch12_src_hprot		4'd1
3:0	R/W	ch12_dst_hprot		4'd1

10.12 SYS_CLOCK Register

Table 343. SYS_CLOCK registers

Address	Register	Description
0x5000_3000	PLL_CLK_DIV_0_CPU	#0 Divider parameter to generate CPU Clock from PLL output 480 MHz (for CPU and Bus Clock). 00: Reserved 01: 240.000 MHz (=480/2) 02: 160.000 MHz (=480/3) 03: 120.000 MHz (=480/4) 04: 96.000 MHz (=480/5) 05: 80.000 MHz (=480/6) 06: 68.571 MHz (=480/7) 07: 60.000 MHz (=480/8) 08: 53.333 MHz (=480/9) 09: 48.000 MHz (=480/10) 0A: 43.636 MHz (=480/11) 0B: 40.000 MHz (=480/12) 0C: 36.923 MHz (=480/13) 0D: 34.286 MHz (=480/14) 0E: 32.000 MHz (=480/15) 0F: 30.000 MHz (=480/16) 10: 28.235 MHz (=480/17) 11: 26.667 MHz (=480/18) 12: 25.263 MHz (=480/19) 13: 24.000 MHz (=480/20) 14: 22.857 MHz (=480/21) 15: 21.818 MHz (=480/22) 16: 20.870 MHz (=480/23) 17: 20.000 MHz (=480/24) 18: 19.200 MHz (=480/25) 19: 18.462 MHz (=480/26) 1A: 17.778 MHz (=480/27) 1B: 17.143 MHz (=480/28) 1C: 16.552 MHz (=480/29) 1D: 16.000 MHz (=480/30) 1E: 15.484 MHz (=480/31) 1F: 15.000 MHz (=480/32)
0x5000_3001	PLL_CLK_DIV_1_XFC	#1 Divider parameter to generate XFC core clock from PLL output 480 MHz (for XFC core clock). XFC core clock frequency must be n multiplication of CPU clock frequency (8 >= n >= 1).
0x5000_3002	PLL_CLK_DIV_2_UART	#2 Divider parameter to generate UART core clock from PLL output 480 MHz (for UART core clock 80 MHz).
0x5000_3003	PLL_CLK_DIV_3_OTP	#3 Divider parameter to generate OTP core clock from PLL output 480 MHz (for OTP core clock 20 MHz).
0x5000_3004	PLL_CLK_DIV_4_PHY	#4 Divider parameter to generate PHY top clock from PLL output 480 MHz (for PHY top clock 480 MHz)
0x5000_3005	PLL_CLK_DIV_5_I2S	#5 Divider parameter to generate I2S master clock from PLL output 480 MHz (for I2S master clock) = 480/(PLL_CLK_DIV_5_I2S+1) MHz maximum 240 MHz ~ minimum 15.0 MHz

Address	Register	Description
0x5000_3006	PLL_CLK_DIV_6_AUXA	#6 Divider parameter to generate Aux ADC clock from PLL output 480 MHz (for Aux ADC clock) = 480/(PLL_CLK_DIV_6_AUXA+1) MHz maximum 240 MHz ~ minimum 15.0 MHz
0x5000_3007	PLL_CLK_DIV_7_CC312	#2 Divider parameter to generate CC-312 core clock from PLL output 480 MHz. CC-312 core clock frequency must be n multiplication of CPU clock freq. (8 >= n >= 1).
0x5000_3010	PLL_CLK_EN_0_CPU	PLL Counter Enable of #0 Divider
0x5000_3011	PLL_CLK_EN_1_XFC	PLL Counter Enable of #1 Divider
0x5000_3012	PLL_CLK_EN_2_UART	PLL Counter Enable of #2 Divider
0x5000_3013	PLL_CLK_EN_3_OTP	PLL Counter Enable of #3 Divider
0x5000_3014	PLL_CLK_EN_4_PHY	PLL Counter Enable of #4 Divider
0x5000_3015	PLL_CLK_EN_5_I2S	PLL Counter Enable of #5 Divider
0x5000_3016	PLL_CLK_EN_6_AUXA	PLL Counter Enable of #6 Divider
0x5000_3017	PLL_CLK_EN_7_CC312	PLL Counter Enable of #7 Divider
0x5000_3030	SRC_CLK_SEL_0_CPU	Selection signal of clock source #0 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_0)
0x5000_3031	SRC_CLK_SEL_1_XFC	Selection signal of clock source #1 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_1)
0x5000_3032	SRC_CLK_SEL_2_UART	Selection signal of clock source #2 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_2)
0x5000_3033	SRC_CLK_SEL_3_OTP	Selection signal of clock source #3 in the clock generator. 0: XTAL/2 (20 MHz) 1: PLL path (PLL_CLK_DIV_3)
0x5000_3035	SRC_CLK_SEL_5_I2S	Selection signal of clock source #5 in the clock generator. 0: External Clock from GPIO PADs 1: PLL path (PLL_CLK_DIV_5)
0x5000_3036	SRC_CLK_SEL_6_AUXA	Selection signal of clock source #6 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_6)
0x5000_3037	SRC_CLK_SEL_7_CC312	Selection signal of clock source #7 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_7)
0x5000_3070	SRC_CLK_STA_0	Status of current clock source #0 in the clock generator. 0: XTAL 1: XTAL to PLL 2: PLL 3: PLL to XTAL
0x5000_3074	IRQ_CLK_STA_0	Status of current interrupt in the clock generator. 0: XTAL 1: XTAL to PLL 2: PLL 3: PLL to XTAL
0x5000_3085	CLK_DIV_I2S	Last divider parameter to generate I2S core clock (MCLK). 0: 1/1

Address	Register	Description
		1: 1/2 2: 1/3 n: 1/(n+1)
0x5000_3090	CLK_EN_CPU	Clock enable of CPU clock.
0x5000_3091	CLK_EN_XFC	Clock enable of XFC core clock.
0x5000_3092	CLK_EN_UART	Clock enable of UART core clock.
0x5000_3093	CLK_EN_OTP	Clock enable of OTP core clock.
0x5000_3095	CLK_EN_I2S	Clock enable of I2S core clock
0x5000_3096	CLK_EN_AUXA	Clock enable of Aux ADC core clock.
0x5000_3097	CLK_EN_CC312	Clock enable of CC-312 core clock.
0x5000_30A0	CLK_DIV_PHYBUS	Divider parameter to generate PHY bus clock from CPU clock.
0x5000_30A1	CLK_DIV_EMMC	Divider parameter to generate SDeMMC controller's core clock from CPU clock. 0: 1/(2^0) 1: 1/(2^1) 2: 1/(2^2) n: 1/(2^n)
0x5000_30A4	CLK_DIV_AUXA	Last divider parameter to generate Aux ADC input clock from Aux ADC reference PLL clock. 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)
0x5000_30B0	CLK_EN_PHYBUS	Clock enable of PHY bus
0x5000_30B1	CLK_EN_SDeMMC	Clock enable of SDeMMC
0x5000_30F0	DIFF_CPU_XFC	Ratio difference between CPU clock and flash controller's core clock. 00_0000: CPU:XFC=1:2^0 00_0001: CPU:XFC=1:2^1 00_0010: CPU:XFC=1:2^2 ….. 00_1011: CPU:XFC=1:2^7 10_0001: CPU:XFC=1:2^-1 10_0010: CPU:XFC=1:2^-2 ….. 10_0111: CPU:XFC=1:2^-15
0x5000_3100	c_pipe_mst2ints	Enable registers to use pipelined paths from AHB bus masters to internal SRAM. [00]: AHB Bus Master #0 (CPU DCode) [01]: AHB Bus Master #1 (CPU ICode) [02]: AHB Bus Master #2 (CPU System) [03]: AHB Bus Master #3 (MAC DMA) [04]: AHB Bus Master #4 (uDMA/kDMA) [05]: AHB Bus Master #5 (SDeMMC) [06]: AHB Bus Master #6 (SPI/I2C Slave) [07]: AHB Bus Master #7 (Fast DMA M0) [08]: AHB Bus Master #8 (Fast DMA M1) [09]: AHB Bus Master #9 (CC-312 DMA) [10]: AHB Bus Master #A (XFC DMA) [11]: AHB Bus master #B (RW HSU) [12]: AHB Bus master #C (SDIO Slave) [13]: AHB Bus master #D (DBGT) [14]: AHB Bus master #E (Secure DMA) [15]: Reserved
0x5000_3104	c_pipe_ints2mst	Enable registers to use pipelined paths from Internal SRAM to AHB bus masters.

Address	Register	Description
0x5000_3108	c_pipe_mst2mskr	Enable registers to use pipelined paths from AHB bus masters to MaskROM.
0x5000_310C	c_pipe_mskr2mst	Enable registers to use pipelined paths from MaskROM to AHB bus masters.
0x5000_3110	c_pipe_mst2retm	Enable registers to use pipelined paths from AHB bus masters to RetentionMem.
0x5000_3114	c_pipe_retm2mst	Enable registers to use pipelined paths from RetentionMem to AHB bus masters.
0x5000_3120	c_pipe_mst2cfgs	Enable registers to use pipelined paths to configuration registers. [00]: CC-312 Env. CFGs [01]: Sys_Common CFGs (Common & Analog IPs) [02]: Sys_CPU CFGs [03]: Sys_ClkRst CFGs (Clock & Reset) [04]: Sys_ProtC CFGs (Protection controller) [05]: Sys_AM2D CFGs (AHB master to DMA) [06]: Sys_ClkGating [07]: Reserved
0x5000_3130	CLK_SET_WAIT_CPU	[0] Waiting control signal of CPU (or XFC) clock setting. 0: Non-waiting 1: Waiting until XFC idle [1] Force XFC clock to CPU clock. [2] Force CC-312 clock to CPU clock.

Table 344. PLL_CLK_DIV_0_CPU (0x5000_3000)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_0_CPU	#0 Divider parameter to generate CPU clock from PLL output 480 MHz (for CPU and Bus Clock). 00: Reserved 01: 240.000 MHz (= 480/2) 02: 160.000 MHz (= 480/3) 03: 120.000 MHz (= 480/4) 04: 96.000 MHz (= 480/5) 05: 80.000 MHz (= 480/6) 06: 68.571 MHz (= 480/7) 07: 60.000 MHz (= 480/8) 08: 53.333 MHz (= 480/9) 09: 48.000 MHz (= 480/10) 0A: 43.636 MHz (= 480/11) 0B: 40.000 MHz (= 480/12) 0C: 36.923 MHz (= 480/13) 0D: 34.286 MHz (= 480/14) 0E: 32.000 MHz (= 480/15) 0F: 30.000 MHz (= 480/16) 10: 28.235 MHz (= 480/17) 11: 26.667 MHz (= 480/18) 12: 25.263 MHz (= 480/19) 13: 24.000 MHz (= 480/20) 14: 22.857 MHz (= 480/21) 15: 21.818 MHz (= 480/22) 16: 20.870 MHz (= 480/23) 17: 20.000 MHz (= 480/24) 18: 19.200 MHz (= 480/25)	5'h05

Bit	Mode	Symbol	Description	Reset
			19: 18.462 MHz (= 480/26) 1A: 17.778 MHz (= 480/27) 1B: 17.143 MHz (= 480/28) 1C: 16.552 MHz (= 480/29) 1D: 16.000 MHz (= 480/30) 1E: 15.484 MHz (= 480/31) 1F: 15.000 MHz (= 480/32)	

Table 345. PLL_CLK_DIV_1_XFC (0x5000_3001)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_1_XFC	#1 Divider parameter to generate XFC core clock from PLL output 480 MHz (for XFC core clock). XFC core clock frequency must be n multiplication of CPU clock frequency (8 >= n >= 1).	5'h02

Table 346. PLL_CLK_DIV_2_UART (0x5000_3002)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_2_UART	#2 Divider parameter to generate UART clock from PLL output 480 MHz (for UART clock).	5'h05

Table 347. PLL_CLK_DIV_3_OTP (0x5000_3003)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R	PLL_CLK_DIV_3_OTP	#3 Divider parameter to generate OTP Clock from PLL output 480 MHz (for OTP clock).	5'h17

Table 348. PLL_CLK_DIV_4_PHY (0x5000_3004)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R	PLL_CLK_DIV_4_PHY	#4 Divider parameter to generate PHY Clock from PLL output 480 MHz (for PHY clock).	5'h00

Table 349. PLL_CLK_DIV_5_I2S (0x5000_3005)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_5_I2S	#5 Divider parameter to generate I2S Clock from PLL output 480 MHz (for I2S clock).	5'h09

Table 350. PLL_CLK_DIV_6_AUXA (0x5000_3006)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_6_AUXA	#6 Divider parameter to generate Aux ADC Clock from PLL output 480 MHz (for Aux ADC clock). = 480/(PLL_CLK_DIV_6_AUXA+1) MHz maximum 240 MHz ~ minimum 15.0 MHz	5'h1F

Table 351. PLL_CLK_DIV_7_CC312 (0x5000_3007)

Bit	Mode	Symbol	Description	Reset
7:5	-	-	Reserved	-
4:0	R/W	PLL_CLK_DIV_7_CC312	#7 Divider parameter to generate CC-312 Core Clock from PLL output 480 MHz.	5'h05

Bit	Mode	Symbol	Description	Reset
			CC-312 core clock frequency must be n multiplication of CPU clock freq. (8 >= n >= 1).	

Table 352. PLL_CLK_EN_0_CPU (0x5000_3010)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_0_CPU	PLL counter enable of #0 divider	1'b0

Table 353. PLL_CLK_EN_1_XFC (0x5000_3011)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_1_XFC	PLL counter enable of #1 divider	1'b0

Table 354. PLL_CLK_EN_2_UART (0x5000_3012)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_2_UART	PLL counter enable of #2 divider	1'b0

Table 355. PLL_CLK_EN_3_OTP (0x5000_3013)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_3_OTP	PLL counter enable of #3 divider	1'b0

Table 356. PLL_CLK_EN_4_PHY (0x5000_3014)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_4_PHY	PLL counter enable of #4 divider	1'b0

Table 357. PLL_CLK_EN_5_I2S (0x5000_3015)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_5_I2S	PLL counter enable of #5 divider	1'b0

Table 358. PLL_CLK_EN_6_AUXA (0x5000_3016)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_6_AUXA	PLL counter enable of #6 divider	1'b0

Table 359. PLL_CLK_EN_7_CC312 (0x5000_3017)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	PLL_CLK_EN_7_CC312	PLL counter enable of #7 divider	1'b0

Table 360. SRC_CLK_SEL_0_CPU (0x5000_3030)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_0_CPU	Selection signal of clock source #0 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_0)	1'b0

Table 361. SRC_CLK_SEL_1_XFC (0x5000_3031)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_1_XFC	Selection signal of clock source #1 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_1)	1'b1

Table 362. SRC_CLK_SEL_2_UART (0x5000_3032)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_2_UART	Selection signal of clock source #2 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_2)	1'b1

Table 363. SRC_CLK_SEL_3_OTP (0x5000_3033)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_3_OTP	Selection signal of clock source #3 in the clock generator. 0: XTAL/2 (20 MHz) 1: PLL path (PLL_CLK_DIV_3)	1'b0

Table 364. SRC_CLK_SEL_5_I2S (0x5000_3035)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_5_I2S	Selection signal of clock source #5 in the clock generator. 0: External Clock from GPIO PADs 1: PLL path (PLL_CLK_DIV_5)	1'b0

Table 365. SRC_CLK_SEL_6_AUXA (0x5000_3036)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_6_AUXA	Selection signal of clock source #6 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_6)	1'b1

Table 366. SRC_CLK_SEL_7_CC312 (0x5000_3037)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	SRC_CLK_SEL_7_CC312	Selection signal of clock source #7 in the clock generator. 0: XTAL (40 MHz) 1: PLL path (PLL_CLK_DIV_7)	1'b0

Table 367. SRC_CLK_STA_0 (0x5000_3070)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R	SRC_CLK_STA_0	Status of current clock source #0 in the clock generator. 0: XTAL 1: XTAL to PLL	2'h0

Bit	Mode	Symbol	Description	Reset
			2: PLL 3: PLL to XTAL	

Table 368. IRQ_CLK_STA_0 (0x5000_3074)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R	IRQ_CLK_STA_0	Status of current interrupt in the clock generator. 0: XTAL 1: XTAL to PLL 2: PLL 3: PLL to XTAL	2'h0

Table 369. CLK_DIV_I2S (0x5000_3085)

Bit	Mode	Symbol	Description	Reset
7:3	-	-	Reserved	-
2:0	R/W	CLK_DIV_I2S	Last divider parameter to generate I2S core clock (MCLK). 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)	3'h0

Table 370. CLK_EN_CPU (0x5000_3090)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_CPU	Clock enable of CPU clock	1’b1

Table 371. CLK_EN_XFC (0x5000_3091)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_XFC	Clock enable of XFC core clock	1’b0

Table 372. CLK_EN_UART (0x5000_3092)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_UART	Clock enable of UART core clock	1’b0

Table 373. CLK_EN_OTP (0x5000_3093)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_OTP	Clock enable of OTP core clock	1’b1

Table 374. CLK_EN_I2S (0x5000_3095)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_I2S	Clock enable of I2S core clock	1’b0

Table 375. CLK_EN_AUXA (0x5000_3096)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_AUXA	Clock enable of Aux ADC core clock	1’b0

Table 376. CLK_EN_CC312 (0x5000_3097)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_CC312	Clock enable of CC-312 core clock	1'b1

Table 377. CLK_DIV_PHYBUS (0x5000_30A0)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	-
3:0	R	CLK_DIV_PHYBUS	Divider parameter to generate PHY bus clock from CPU clock.	4'h0

Table 378. CLK_DIV_EMMC (0x5000_30A1)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	-
3:0	R/W	CLK_DIV_EMMC	Divider parameter to generate SDeMMC controller's core clock from CPU clock. 0: 1/(2^0) 1: 1/(2^1) 2: 1/(2^2) n: 1/(2^n)	4'h0

Table 379. CLK_DIV_AUXA (0x5000_30A4)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:0	R/W	CLK_DIV_AUXA	Last divider parameter to generate Aux ADC input clock from Aux ADC reference PLL clock. 0: 1/1 1: 1/2 2: 1/3 n: 1/(n+1)	10'h3E7

Table 380. CLK_EN_PHYBUS (0x5000_30B0)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_PHYBUS	Clock enable of PHY bus	1'b0

Table 381. CLK_EN_SDeMMC (0x5000_30B1)

Bit	Mode	Symbol	Description	Reset
7:1	-	-	Reserved	-
0	R/W	CLK_EN_SDeMMC	Clock enable of SDeMMC	1'b0

Table 382. DIFF_CPU_XFC (0x5000_30F0)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	
5:0	R	DIFF_CPU_XFC	Ratio difference between CPU clock and Flash controller's core clock. 00_0000: CPU:XFC=1:2^0 00_0001: CPU:XFC=1:2^1 00_0010: CPU:XFC=1:2^2 ..... 00_1011: CPU:XFC=1:2^7 10_0001: CPU:XFC=1:2^-1 10_0010: CPU:XFC=1:2^-2	6'h00

Bit	Mode	Symbol	Description	Reset
			..... 10_0111: CPU:XFC=1:2^-15	

Table 383. c_pipe_mst2ints (0x5000_3100)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_mst2ints	Enable registers to use pipelined paths from AHB bus masters to internal SRAM. [00]: AHB bus master #0 (CPU DCode) [01]: AHB bus master #1 (CPU ICode) [02]: AHB bus master #2 (CPU System) [03]: AHB bus master #3 (MAC DMA) [04]: AHB bus master #4 (uDMA/kDMA) [05]: AHB bus master #5 (SDeMMC) [06]: AHB bus master #6 (SPI/I2C Slave) [07]: AHB bus master #7 (Fast DMA M0) [08]: AHB bus master #8 (Fast DMA M1) [09]: AHB bus master #9 (CC-312 DMA) [10]: AHB bus master #A (XFC DMA) [11]: AHB bus master #B (RW HSU) [12]: AHB bus master #C (SDIO Slave) [13]: AHB bus master #D (DBGT) [14]: AHB bus master #E (Secure DMA) [15]: Reserved	16'h0000

Table 384. c_pipe_ints2mst (0x5000_3104)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_ints2mst	Enable registers to use pipelined paths from internal SRAM to AHB bus masters.	16'h0000

Table 385. c_pipe_mst2mskr (0x5000_3108)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_mst2mskr	Enable registers to use pipelined paths from AHB bus masters to MaskROM.	16'h0000

Table 386. c_pipe_mskr2mst (0x5000_310C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_mst2retm	Enable Registers to use pipelined paths from AHB Bus Masters to RetentionMem.	16'h0000

Table 387. c_pipe_mst2retm (0x5000_3110)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_mst2retm	Enable registers to use pipelined paths from AHB bus masters to RetentionMem.	16'h0000

Table 388. c_pipe_retm2mst (0x5000_3114)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-

Bit	Mode	Symbol	Description	Reset
15:0	R/W	c_pipe_retm2mst	Enable registers to use pipelined paths from RetentionMem to AHB bus masters.	16'h0000

Table 389. c_pipe_mst2cfgs (0x5000_3120)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:0	R/W	c_pipe_mst2cfgs	Enable registers to use pipelined paths to configuration registers. [00]: CC-312 Env. CFGs [01]: Sys_Common CFGs (Common and Analog IPs) [02]: Sys_CPU CFGs [03]: Sys_ClkRst CFGs (Clock and Reset) [04]: Sys_ProtC CFGs (Protection Controller) [05]: Sys_AM2D CFGs (AHB Master to DMA) [06]: Sys_ClkGating [07]: Reserved	16'h0000

Table 390. CLK_SET_WAIT_CPU (0x5000_3130)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2	R/W	CLK_SET_WAIT_CPU [2]	Force CC-312 clock to CPU clock	1'b0
1	R/W	CLK_SET_WAIT_CPU [1]	Force XFC clock to CPU clock	1'b0
0	R/W	CLK_SET_WAIT_CPU [0]	Waiting control signal of CPU (or XFC) clock setting. 0: Non-waiting 1: Waiting until XFC idle	1'b1

10.13 Watchdog Register

Table 391. Watchdog registers

Address	Register	Description
0x4000_8000	WDOGLOAD	Watchdog Load Register
0x4000_8004	WDOGVALUE	Watchdog Value Register
0x4000_8008	WDOGCONTROL	Watchdog Control Register
0x4000_800C	WDOGINTCLR	Watchdog Clear Interrupt Register
0x4000_8010	WDOGRIS	Watchdog Raw Interrupt Status Register
0x4000_8014	WDOGMIS	Watchdog Interrupt Status Register
0x4000_8C00	WDOGLOCK	Watchdog Lock Register
0x4000_8F00	WDOGITCR	Watchdog Integration Test Control Register
0x4000_8F04	WDOGITOP	Watchdog Integration Test Output Set Register

Table 392. WDOGLOAD (0x4000_8000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WDOGLOAD	The WDOGLOAD register contains the value where the counter starts decrementing. When this register is written, the count is immediately restarted from the new value. The minimum valid value for WDOGLOAD is 1.	32'hFFFF FFFF

Table 393. WDOGVALUE (0x4000_8004)

Bit	Mode	Symbol	Description	Reset
31:0	RO	WDOGVALUE	The WDOGVALUE register gives the current value of the decrementing counter.	32'hFFFF FFFF

Table 394. WDOGCONTROL (0x4000_8008)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved, read UNDEFINED, must read as 0s.	-
1	R/W	RESEN	Enable watchdog reset output, WDOGRES. Acts as a mask for the reset output. Set to 1 to enable the reset, or to 0 to disable the reset.	1'b0
0	R/W	INTEN	Enable the interrupt event, WDOGINT. Set to 1 to enable the counter and the interrupt, or to 0 to disable the counter and interrupt. Reloads the counter from the value in WDOGLOAD when the interrupt is enabled, after previously being disabled.	1'b0

Table 395. WDOGINTCLR (0x4000_800C)

Bit	Mode	Symbol	Description	Reset
-	WO	WDOGINTCLR	A write of any value to the WDOGINTCLR register clears the watchdog interrupt and reloads the counter from the value in WDOGLOAD.	-

Table 396. WDOGRIS (0x4000_8010)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s.	-
0	RO	Raw Watchdog Interrupt	Raw interrupt status from the counter.	1'b0

Table 397. WDOGMIS (0x4000_8014)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s.	-
0	RO	Watchdog Interrupt	Enabled interrupt status from the counter.	1'b0

Table 398. WDOGLOCK (0x4000_8C00)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Enable register writes	Enable write access to all other registers by writing 0x1ACCE551. Disable write access by writing any other value. A read returns the lock status: 0x00000000 = Write access to all other registers is enabled. 0x00000001 = Write access to all other registers is disabled	32'h0000 0000

Table 399. WDOGITCR (0x4000_8F00)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved, read UNDEFINED, must read as 0s.	-
0	RW	Integration Test Mode Enable	When set to 1, places the watchdog into integration test mode.	1'b0

Table 400. WDOGITOP (0x4000_8F04)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1	WO	Integration Test WDOGINT value	Value output on WDOGINT when in integration test mode.	1'b0
0	WO	Integration Test WDOGRES value	Value output on WDOGRES when in integration test mode.	1'b0

10.14 Timer Register

Table 401. Timer registers

Address	Register	Description
0x4000_0000	TIMER0_CTRL_REG	Timer0 Control Register
0x4000_0004	TIMER0_VALUE_REG	Timer0 Value Register
0x4000_0008	TIMER0_RELOAD_REG	Timer0 Reload Value Register
0x4000_000C	TIMER0_INTSTATUS_REG TIMER0_INTCLEAR_REG	Timer0 Interrupt Register. Write one to clear.
0x4000_1000	TIMER1_CTRL_REG	Timer1 Control Register
0x4000_1004	TIMER1_VALUE_REG	Timer1 Value Register
0x4000_1008	TIMER1_RELOAD_REG	Timer1 Reload Value Register
0x4000_100C	TIMER1_INTSTATUS_REG TIMER1_INTCLEAR_REG	Timer1 Interrupt Register. Write one to clear.

Table 402. TIMER0_CTRL_REG (0x4000_0000)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3	R/W	CTRL[3]	Timer interrupt enable	1'b0
2	R/W	CTRL[2]	Select external input as clock	1'b0
1	R/W	CTRL[1]	Select external input as enable	1'b0
0	R/W	CTRL[0]	Enable	1'b0

Table 403. TIMER0_VALUE_REG (0x4000_0004)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	VALUE	Current Value	32'h0000 0000

Table 404. TIMER0_RELOAD_REG (0x4000_0008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RELOAD	Reload value. A write to this register sets the current value after it reaches 0.	32'h0000 0000

Table 405. TIMER0_INTSTATUS_REG/TIMER0_INTCLEAR_REG (0x4000_000C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
-	R/W	INTSTATUS INTCLEAR	Timer interrupt. Write one to clear.	1'b0

Table 406. TIMER1_CTRL_REG (0x4000_1000)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3	R/W	CTRL[3]	Timer interrupt enable	1'b0
2	R/W	CTRL[2]	Select external input as clock	1'b0
1	R/W	CTRL[1]	Select external input as enable	1'b0
0	R/W	CTRL[0]	Enable	1'b0

Table 407. TIMER1_VALUE_REG (0x4000_1004)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	VALUE	Current value	32'h0000 0000

Table 408. TIMER1_RELOAD_REG (0x4000_1008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RELOAD	Reload value. A write to this register sets the current value after it reaches 0.	32'h0000 0000

Table 409. TIMER1_INTSTATUS_REG/TIMER1_INTCLEAR_REG (0x4000_100C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
-	R/W	INTSTATUS INTCLEAR	Timer interrupt. Write one to clear.	1'b0

10.15 QSPI Register

Table 410. QSPI registers

Address	Register	Description
0x500B_0000	QSPI_IRQ_MSK_REG	Interrupt Mask Register
0x500B_0004	QSPI_REQ_START_REG	Operation Starting Request Register
0x500B_0008	QSPI_REQ_CLR_REG	Request and Interrupt Clear Register
0x500B_000C	QSPI_REQ_CLR_OP_REG	Operation Clear Request Register
0x500B_0010	QSPI_IRQ_STATUS_REG	Main IRQ Status Register
0x500B_0014	QSPI_IRQ_STATUS_DMA_REG	IRQ Status of the DMA Controller Register
0x500B_0018	QSPI_IRQ_STATUS_SPI_REG	IRQ Status of the SPI Controller Register
0x500B_001C	QSPI_IRQ_STATUS_XIP_REG	IRQ Status of the XIP Controller Register
0x500B_0020	QSPI_CORE_CLK_REG	XFC Core Clock Ratio Register
0x500B_0024	QSPI_CORE_FREQ_REG	XFC Core Clock Frequency Register
0x500B_0030	QSPI_TIMEOUT_REG	Time Out Register
0x500B_0034	QSPI_TIMEOUT_COUNT_REG	Time Out Counter Register
0x500B_0040	QSPI_CE_SEL_CYC_REG	CE Select Cycles Register
0x500B_0044	QSPI_CE_DES_CYC_REG	CE De-select Cycles Register
0x500B_0050	QSPI_DBG_REG	TX/RX Debug Features Register
0x500B_0054	QSPI_RX_POS_REG	Reference Position of RX Sampling Register
0x500B_0058	QSPI_CLK_POS_REG	Clock Ratio Register
0x500B_0060	QSPI_TX_DLY0_REG	TX CMD~TXD Clock Delay Parameter 0 Register
0x500B_0064	QSPI_RX_DLY0_REG	RX RXD Clock Delay Parameter 0 Register
0x500B_0070	QSPI_TX_DLY1_REG	TX CMD~TXD Clock Delay Parameter 1 Register
0x500B_0074	QSPI_RX_DLY1_REG	RX RXD Clock Delay Parameter 1 Register
0x500B_0080	QSPI_TX_DLY2_REG	TX CMD~TXD Clock Delay Parameter 2 Register
0x500B_0084	QSPI_RX_DLY2_REG	RX RXD Clock Delay Parameter 2 Register
0x500B_0090	QSPI_TX_DLY3_REG	TX CMD~TXD Clock Delay Parameter 3 Register
0x500B_0094	QSPI_RX_DLY3_REG	RX RXD Clock Delay Parameter 3 Register
0x500B_0100	SPI_CLK_FREQ_S_REG	Setting Value of SPI Clock Frequency Register
0x500B_0104	SPI_CLK_FREQ_R_REG	Division Parameter of SPI Clock Frequency Register
0x500B_0108	SPI_DMY_CYC_REG	Number of SPI Dummy Cycles Register
0x500B_010C	SPI_WAIT_CYC_REG	Wait cycles between Consecutive Transfers Register
0x500B_0110	SPI_CLK_MODE_REG	SPI Interface Clock Mode Register
0x500B_0114	SPI_CTRL_MODE_REG	SPI Interface Control Mode Register
0x500B_0118	SPI_BYTE_SWAP_REG	Swap Type of SPI Data Bytes in AHB Bus Register
0x500B_011C	SPI_WRAP_EN_REG	Wrap Enable to Access the First Critical Address Register
0x500B_0120	SPI_BUS_TYPE_REG	SPI Bus Type Register

Address	Register	Description
0x500B_0124	SPI_IO_TX_TYPE_REG	SPI DIOx Type Register
0x500B_0128	SPI_IO_CK_TYPE_REG	SPI Clock Pin Register
0x500B_012C	SPI_IO_CS_TYPE_REG	Output Polarity of SPI CSx if Operation Type Register
0x500B_0130	SPI_CS_SEL_REG	Selecting CS Port Register
0x500B_0134	SPI_IO_1_TYPE_REG	I/O Operation Type when SPI is Single I/O mode
0x500B_0138	SPI_TWIN_QSPI_EN_REG	Enable of Twin QSPI Flash Register
0x500B_0140	SPI_RW_REG	SPI Data Type Register
0x500B_0144	SPI_CMD_REG	SPI Command Register
0x500B_0148	SPI_ADDR_REG	SPI Address Register
0x500B_014C	SPI_MODE_REG	SPI Mode Register
0x500B_0150	SPI_TTL_REG	Total Transfer Length for the SPI Domain Register
0x500B_0154	SPI_DLY_INDEX_REG	SPI Delay Index in the Non-DMA Mode Register
0x500B_0160	SPI_ACC_DIN_REG	SPI 1st Write Data to Debug Register
0x500B_0164	SPI_ACC_DOUT_REG	SPI 1st Read Data to Debug Register
0x500B_0170	SPI_OP_STATUS_REG	Current Operation Status of the SPI Domain Register
0x500B_0180	SPI_LEGACY_EN_REG	Enable of SPI Legacy Mode Register
0x500B_0184	SPI_LEGACY_TX_SIZE_REG	Address Size of SPI Legacy Mode Register
0x500B_0190	SPI_LEGACY_TX_DAT00_REG	TX Data 0 to 3 Register
0x500B_0194	SPI_LEGACY_TX_DAT04_REG	TX Data 4 to 7 Register
0x500B_0198	SPI_LEGACY_TX_DAT08_REG	TX Data 8 to 11 Register
0x500B_019C	SPI_LEGACY_TX_DAT12_REG	TX Data 12 to 15 Register
0x500B_01A0	SPI_LEGACY_TX_DAT16_REG	TX Data 16 to 19 Register
0x500B_01A4	SPI_LEGACY_TX_DAT20_REG	TX Data 20 to 23 Register
0x500B_01A8	SPI_LEGACY_TX_DAT24_REG	TX Data 24 to 27 Register
0x500B_01AC	SPI_LEGACY_TX_DAT28_REG	TX Data 28 to 31 Register
0x500B_0200	DMA_MP0_CTRL_REG	DMA Control of Master Port 0 Register
0x500B_0204	DMA_MP0_TASK_REG	Operation Channel Task Size of the DMA Master Port 0 Register
0x500B_0208	DMA_IRQ_MASK_REG	IRQ Mask Enable of the DMA Task Operation Register
0x500B_020C	DMA_FIFO_THR_REG	DMA FIFO Threshold Register
0x500B_0210	DMA_TSK_0_ADR_REG	Base Address for the DMA Task 0 Register
0x500B_0214	DMA_TSK_0_TTL_REG	Total Transfer Length for the DMA Task 0 Register
0x500B_0260	DMA_OP_STATUS_REG	Current Operation Status of the DMA Domain Register
0x500B_0264	DMA_OP_TASK_REG	Operation Task of the DMA Register
0x500B_0268	DMA_CURR_TSK_ADR_REG	Base Address for the Current DMA Task Register
0x500B_026C	DMA_CURR_TSK_TTL_REG	Total Transfer Length for the Current DMA Task Register
0x500B_0270	DMA_FIFO_ADDR_REG	Address of the DMA FIFO Register
0x500B_0280	DMA_CLK_FREQ_S_REG	Setting value of DMA SPI Clock Frequency Register
0x500B_0284	DMA_CLK_FREQ_R_REG	Division parameter of DMA SPI Clock Frequency Register
0x500B_0288	DMA_DLY_INDEX_REG	SPI Delay Index in the DMA Mode Register
0x500B_0300	QSPI_CLK_FREQ_S_REG	Setting Value of XIP SPI Clock Frequency Register
0x500B_0304	QSPI_CLK_FREQ_R_REG	Division Parameter of XIP SPI Clock Frequency Register
0x500B_0308	QSPI_DMY_CYC_REG	Number of XIP SPI Dummy Cycles Register
0x500B_030C	QSPI_WAIT_CYC_REG	Wait Cycles between Consecutive Transfers Register
0x500B_0310	QSPI_IF_MODE_REG	XIP SPI Interface Register
0x500B_0314	QSPI_CTRL_REG	XIP SPI Control Register
0x500B_0318	QSPI_BYTE_SWAP_REG	Swap Type of XIP SPI Data Register

Address	Register	Description
0x500B_031C	QSPI_WRAP_EN_REG	Wrap Enable to Access the First Critical Address Register
0x500B_0320	QSPI_BUS_TYPE_REG	XIP SPI Bus Type Register
0x500B_0324	QSPI_IO_DX_TYPE_REG	XIP SPI DIOx Type Register
0x500B_0328	QSPI_IO_CK_TYPE_REG	XIP SPI Clock Pin Register
0x500B_032C	QSPI_IO_CS_TYPE_REG	Output polarity of XIP SPI CSx Register
0x500B_0330	QSPI_CS_SEL_REG	Selecting XIP CS Port Register
0x500B_0334	QSPI_IO_1_TYPE_REG	I/O Operation Type if SPI is Single I/O Register
0x500B_033C	QSPI_TWIN_EN_REG	Enable of Twin QSPI Flash Register
0x500B_0340	QSPI_RW_REG	XIP SPI Data Type Register
0x500B_0344	QSPI_CMD_REG	XIP SPI Command Register
0x500B_034C	QSPI_MODE_REG	XIP SPI Mode Register
0x500B_0350	QSPI_BURST_REG	XIP SPI Burst Access Size Register
0x500B_0354	QSPI_DLY_INDEX_REG	XIP SPI Delay Index Register
0x500B_0360	QSPI_OFFSET_ADDR_REG	Flash Offset Address to Remap Cache Address in XIP Mode Register
0x500B_0364	QSPI_CURR_DOUT_REG	XIP Current Read Data to Debug Register
0x500B_0368	QSPI_CURR_ADDR_REG	XIP Current Address to Debug Register
0x500B_0370	QSPI_OP_STATUS_REG	Current Operation Status of the XIP Domain Register
0x500B_0400	QSPI_DEC_SEED_VAL_REG	Seed Value of XIP Decryption Register
0x500B_0404	QSPI_DEC_SEL_REG	Address Position to Select Inversion Operation Register

Table 411. QSPI_IRQ_MSK_REG (0x500B_0000)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	-
11:8	R/W	IRQ_MSK_EN	IRQ mask enable of the QSPI Flash controller. [11]: Time out interrupt [10]: QSPI access (Directly access without the DMA operation) [9]: Non-DMA access (QSPI single access) [8]: DMA access	4'hF
7:3	-	-	Reserved	
2:0	R/W	OP_EN	Operation enable of the QSPI Flash controller. Deactivating the controller reduces power consumption. [2]: QSPI access (Directly access without the DMA operation) [1]: Non-DMA access (QSPI single access) [0]: DMA access	3'h0

Table 412. QSPI_REQ_START_REG (0x500B_0004)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	W	REQ_START	Operation starting request of the QSPI Flash controller, active high with auto clear function. [2]: QSPI access (Directly access without the DMA operation) [1]: Non-DMA access (QSPI single access) [0]: DMA access	3'h0

Table 413. QSPI_REQ_CLR_REG (0x500B_0008)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	-

Bit	Mode	Symbol	Description	Reset
10:8	W	REQ_CLR_STA	Status clear request of the QSPI Flash controller, active high with auto clear function. [10]: IRQ_STATUS_QSPI [9]: IRQ_STATUS_SPI (single bit mode) [8]: IRQ_STATUS_DMA	3'h0
7:4	-	-	Reserved	
3:0	W	REQ_CLR_IRQ	IRQ clear request of the QSPI Flash controller, active high with auto clear function. [3]: Time out interrupt [2]: QSPI access (Directly access without the DMA operation) [1]: Non-DMA access (QSPI single access) [0]: DMA access	3'h0

Table 414. QSPI_REQ_CLR_OP_REG (0x500B_000C)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	W	REQ_CLR_OP	Operation clear request of the QSPI Flash controller, active high with auto clear function. [2]: QSPI access (Directly access without the DMA operation) [1]: Non-DMA access (QSPI single access) [0]: DMA access	3'h0

Table 415. QSPI_IRQ_STATUS_REG (0x500B_0010)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R	IRQ_STS	Main IRQ status of the QSPI Flash controller. [3]: Time out interrupt [2]: QSPI [1]: Non-DMA (QSPI single access) [0]: DMA	4'h0

Table 416. QSPI_IRQ_STATUS_DMA_REG (0x500B_0014)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R	IRQ_STS_DMA	IRQ Status of the DMA controller. [7]: TX FIFO underflow [6]: TX FIFO overflow [5]: RX FIFO underflow [4]: RX FIFO overflow [3]: AHB bus error in the DMA AHB master port #0 [2]: Access count error [1]: Setting error [0]: Access done	8'h00

Table 417. QSPI_IRQ_STATUS_SPI_REG (0x500B_0018)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R	IRQ_STS_SPI	IRQ status of the QSPI single bit mode (non-DMA). [7]: TX FIFO underflow [6]: TX FIFO overflow [5]: RX FIFO underflow	8'h00

Bit	Mode	Symbol	Description	Reset
			[4]: RX FIFO overflow [3]: AHB bus error in the SPI AHB slave port [2]: Access count error [1]: Setting error [0]: Access done	

Table 418. QSPI_IRQ_STATUS_XIP_REG (0x500B_001C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R	IRQ_STS_QSPI	IRQ status of the QSPI controller (Directly access). [7]: TX FIFO underflow [6]: TX FIFO overflow [5]: RX FIFO underflow [4]: RX FIFO overflow [3]: AHB bus error in the SPI AHB slave port [2]: Access count error [1]: Setting error [0]: Access done	8'h00

Table 419. QSPI_CORE_CLK_REG (0x500B_0020)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	CORE_RATIO	QSPI core clock ratio per CPU clock. 0: 1x1 1: 2x1 2: 3x1 (reserved) 3: 4x1 4: 5x1 (reserved) 5: 6x1 (reserved) 6: 7x1 (reserved) 7: 8x1 . . . F: 16x1	4'h0

Table 420. QSPI_CORE_FREQ_REG (0x500B_0024)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	CORE_FREQ	QSPI core clock frequency (1 ~ 512 MHz). 0: 1 MHz N: N+1 MHz	9'h04F

Table 421. QSPI_TIMEOUT_REG (0x500B_0030)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R/W	TO_UNIT	Time Out, Unit K. Timeout = 8^K µs (1 µs ~ 8^7 µs)	3'h0

Table 422. QSPI_TIMEOUT_COUNT_REG (0x500B_0034)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4:0	R/W	TO_CNT	Time out counter, Unit C. Timeout total latency = (C+1) x 8^K µs	5'h00

Table 423. QSPI_CE_SEL_CYC_REG (0x500B_0040)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	CE_SEL_CYC	CE select cycles (Reference clock is core clock). Delay cycles between the activation of chip select and the 1st QSPI clock rising or delay cycles between the last QSPI clock edge and de-activation of the chip select in the SPI interface mode 0. 0: 0 cycle 1: 1 cycle F: 15 cycles	4'h1

Table 424. QSPI_CE_DES_CYC_REG (0x500B_0044)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	CE_DES_CYC	CE de-select cycles (Reference clock is core clock). Delay cycles between deactivation and activation of chip select. 0: 0 cycle 1: 1 cycle N: N cycles	8'h02

Table 425. QSPI_DBG_REG (0x500B_0050)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:8	R/W	TX_SHIFT	TX debug features. [9]: tx shift enable [8]: TX shift value	2'h0
7:3	-	-	Reserved	-
2:0	R/W	RX_SHIFT	RX debug features. [2]: RX shift enable [1:0]: RX shift value	3'h4

Table 426. QSPI_RX_POS_REG (0x500B_0054)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	RX_SHIFT_EN	Reference position of RX sampling. 0: QSPI_CLK falling edge 1: QSPI_CLK rising edge	1'b1

Table 427. QSPI_CLK_POS_REG (0x500B_0058)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R/W	SPI_CLK_1x1_EN	[2]: Operation enable to force 1:1:1/3 to 1:1:1 (debug) [1]: Operation enable to force 1:1:1/2 to 1:1:1 (debug) [0]: Operation enable of 1:1:1 clock mode	3'h1

Table 428. QSPI_TX_DLY0_REG (0x500B_0060)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	DLY_0_TXC	TX CMD~TXD clock delay parameter #0. [8]: TX clock polarity [7:0]: TX clock delay parameter	9'h000

Table 429. QSPI_RX_DLY0_REG (0x500B_0064)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:0	R/W	DLY_0_RXC	RX RXD clock delay parameter #0. [9:8]: RX clock polarity 0 = Ideal sampling position 1 = Ideal sampling position + 0.5 cycle 2 = Ideal sampling position + 1.0 cycle 3 = Ideal sampling position + 1.5 cycle [7:0]: RX clock delay parameter	10'h000

Table 430. QSPI_TX_DLY1_REG (0x500B_0070)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	DLY_1_TXC	TX CMD~TXD clock delay parameter #1. [8]: TX clock polarity [7:0]: TX clock delay parameter	9'h000

Table 431. QSPI_RX_DLY1_REG (0x500B_0074)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:0	R/W	DLY_1_RXC	RX RXD clock delay parameter #1. [9:8]: RX clock polarity 0 = Ideal sampling position 1 = Ideal sampling position + 0.5 cycle 2 = Ideal sampling position + 1.0 cycle 3 = Ideal sampling position + 1.5 cycle [7:0]: RX clock delay parameter	10'h000

Table 432. QSPI_TX_DLY2_REG (0x500B_0080)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	DLY_2_TXC	TX CMD~TXD clock delay parameter #2. [8]: TX clock polarity [7:0]: TX clock delay parameter	9'h000

Table 433. QSPI_RX_DLY2_REG (0x500B_0084)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:0	R/W	DLY_2_RXC	RX RXD clock delay parameter #2 [9:8]: RX clock polarity 0 = Ideal sampling position 1 = Ideal sampling position + 0.5 cycle 2 = Ideal sampling position + 1.0 cycle 3 = Ideal sampling position + 1.5 cycle [7:0]: RX clock delay parameter	10'h000

Table 434. QSPI_TX_DLY3_REG (0x500B_0090)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	DLY_3_TXC	TX CMD~TXD clock delay parameter #3. [8]: TX clock polarity [7:0]: TX clock delay parameter	9'h000

Table 435. QSPI_RX_DLY3_REG (0x500B_0094)

Bit	Mode	Symbol	Description	Reset
31:10	-	-	Reserved	-
9:0	R/W	DLY_3_RXC	RX RXD clock delay parameter #3. [9:8]: RX clock polarity 0 = Ideal sampling position 1 = Ideal sampling position + 0.5 cycle 2 = Ideal sampling position + 1.0 cycle 3 = Ideal sampling position + 1.5 cycle [7:0]: RX clock delay parameter	10'h000

Table 436. SPI_CLK_FREQ_S_REG (0x500B_0100)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	FREQ_S	Setting value of SPI interface clock frequency (0 ~ 511 MHz). This value should be less than or equal to 1/2 of QSPI core clock frequency.	9'h028

Table 437. SPI_CLK_FREQ_R_REG (0x500B_0104)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R	FREQ_R	Division parameter for the real value of SPI interface clock frequency. 0: Not used value 1: QSPI core clock frequency/2 N: QSPI core clock frequency/(N+1)	9'h028

Table 438. SPI_DMY_CYC_REG (0x500B_0108)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4:0	R/W	DMY_CYC	Number of SPI dummy cycles (Interface clock). N: N dummy cycles	5'h00

Table 439. SPI_WAIT_CYC_REG (0x500B_010C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	WAIT_CYC	Wait cycles between consecutive transfers for other SPI slaves (Interface clock). N: N wait cycles	8'h00

Table 440. SPI_CLK_MODE_REG (0x500B_0110)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	MODE	SPI Interface mode, {CPOL, CPHASE}. 0: Mode 0 (0,0) 3: Mode 3 (1,1)	2'h0

Table 441. SPI_CTRL_MODE_REG (0x500B_0114)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4	R/W	TO_EN	Enable of time out operation	1'b0
3:2	R/W	MODE_SZ	Number of SPI mode (or Option code) bits.	2'h1

Bit	Mode	Symbol	Description	Reset
			0: 8 bits (for example, 0xA5) 1: 4 bits (for example, 0xAX) 2: 2 bits (reserved) 3: 1 bit (reserved)	
1	R/W	CMD_SZ	Number of SPI command bytes. 0: 1 byte 1: 2 bytes	1'b0
0	R/W	ADDR_SZ	Number of SPI address bytes. 0: 3 bytes 1: 4 bytes	1'b0

Table 442. SPI_BYTE_SWAP_REG (0x500B_0118)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	SWAP	Swap type of SPI data bytes in AHB bus. 0: Normal (little endian) {3, 2, 1, 0} 1: 4-byte swap (big endian per 4 bytes) {3, 2, 1, 0} -> {0, 1, 2, 3} 2: 2-byte swap (big endian per 2 bytes) {3, 2, 1, 0} -> {2, 3, 0, 1} 3: 16-bit swap {3, 2, 1, 0} -> {1, 0, 3, 2}	2'h0

Table 443. SPI_WRAP_EN_REG (0x500B_011C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	WRAP_EN	Wrap enable to access the first critical address.	1'b0

Table 444. SPI_BUS_TYPE_REG (0x500B_0120)

Bit	Mode	Symbol	Description	Reset
31	R/W		1: Off 0: On	1'b0
30	R/W		1: DTR 0: STR	1'b0
29:28	R/W		I/O bits N: 2^N bit, should be used only 0	2'h0
27:24	R/W	TRX_DAT	SPI TX/RX Data	4'h0
23:20	-	-	Reserved	-
19:16	R/W	MODE	SPI mode	4'h0
15:12	-	-	Reserved	-
11:8	R/W	ADR	SPI address	4'h0
7:4	-	-	Reserved	-
3:0	R/W	CMD	SPI command	4'h0

Table 445. SPI_IO_TX_TYPE_REG (0x500B_0124)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:16	R/W		Output value of SPI DIOx if operation type is manual. 0: Logic 0 1: Logic 1	8'h00
15:8	R/W		Direction type of SPI DIOx if operation type is manual.	8'h00

Bit	Mode	Symbol	Description	Reset
			0: Input 1: Output	
7:0	R/W		Operation type of SPI DIOx. 0: Auto (by the Flash controller) 1: Manual	8'h00

Table 446. SPI_IO_CK_TYPE_REG (0x500B_0128)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R/W	TYPE	SPI clock pin. [2]: Output value of SPI CLK if operation type is manual [1]: Direction type of SPI CLK if operation type is manual [0]: Operation type of SPI CLK	3'h0

Table 447. SPI_IO_CS_TYPE_REG (0x500B_012C)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	-
27:24	R/W	CS_TYPE	Output polarity of SPI CS_x if operation type is auto. 0: Active low 1: Active high [27]: CS_3 [26]: CS_2 [25]: CS_1 [24]: CS_0	4'h0
23:20	-	-	Reserved	-
19:16	R/W	CS_OUT	Output value of SPI CS_x if operation type is manual.	4'h0
15:12	-	-	Reserved	-
11:8	R/W	CS_DIR	Direction type of SPI CS_x if operation type is manual.	4'h0
7:4	-	-	Reserved	-
3:0	R/W	CS_OP	Operation type of SPI CS_x.	4'h0

Table 448. SPI_CS_SEL_REG (0x500B_0130)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	CS_SEL	Selecting CS port to be used. [3]: SPI_CS_3 [2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	4'h1

Table 449. SPI_IO_1_TYPE_REG (0x500B_0134)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	IO_1	I/O Operation type if SPI is single I/O. 0: 3-wire SPI Bus (single I/O SPI Bus) 1: 4-wire SPI Bus (standard I/O SPI Bus) [3]: SPI_CS_3 [2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	4'h0

Table 450. SPI_TWIN_QSPI_EN_REG (0x500B_0138)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	TWIN_EN	Enable of twin QSPI Flash. [3]: SPI_CS_3 [2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	4'h0

Table 451. SPI_RW_REG (0x500B_0140)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	REG_RW	SPI data type. 0: Read 1: Write	1'b0

Table 452. SPI_CMD_REG (0x500B_0144)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
15:0	R/W	REG_CMD	SPI command field. [15:0]: Command (instruction code)	16'h0000

Table 453. SPI_ADDR_REG (0x500B_0148)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	REG_ADR	SPI address field	32'h0000

Table 454. SPI_MODE_REG (0x500B_014C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	REG_MODE	SPI mode (or Option control). Optional control bits that follow the address bits.	8'h00

Table 455. SPI_TTL_REG (0x500B_0150)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R/W	TTL	Total transfer length for the SPI domain. 0: 0 byte 1: 1 byte Max transfer length = 2M-1 bytes	21'h0000

Table 456. SPI_DLY_INDEX_REG (0x500B_0154)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	DLY_INDEX	SPI delay index in the non-DMA mode. 0: Use XFC_SPI_DLY_0_TXC and XFC_SPI_DLY_0_RXC 1: Use XFC_SPI_DLY_1_TXC and XFC_SPI_DLY_1_RXC 2: Use XFC_SPI_DLY_2_TXC and XFC_SPI_DLY_2_RXC 3: Use XFC_SPI_DLY_3_TXC and XFC_SPI_DLY_3_RXC	2'h0

Table 457. SPI_ACC_DIN_REG (0x500B_0160)

Bit	Mode	Symbol	Description	Reset
31:0	R/W		SPI 1st write data to debug	32'h0000

Table 458. SPI_ACC_DOUT_REG (0x500B_0164)

Bit	Mode	Symbol	Description	Reset
31:0	R		SPI 1st read data to debug	32'h0000

Table 459. SPI_OP_STATUS_REG (0x500B_0170)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R	OP_STS	Current operation status of the SPI domain. 0: S_IDLE 1: S_CE_I 2: S_CMD 3: S_ADDR 4: S_MODE 5: S_DUMM 6: S_D_WR 7: S_D_WH 8: S_D_RD 9: S_D_RH A: S_CE_D B: S_CE_C C: S_CE_W D: S_WAIT E: S_ERR	4'h0

Table 460. SPI_LEGACY_EN_REG (0x500B_0180)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W		Enable of SPI legacy mode	1'b0

Table 461. SPI_LEGACY_TX_SIZE_REG (0x500B_0184)

Bit	Mode	Symbol	Description	Reset
31:6	-	-	Reserved	-
5:0	R/W	-	Address size of SPI legacy mode. N: N bytes	6'h00

Table 462. SPI_LEGACY_TX_DAT00_REG (0x500B_0190)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 4th data	8'h00
23:16	R/W	-	TX value: 3rd data	8'h00
15:8	R/W	-	TX value: 2nd data	8'h00
7:0	R/W	-	TX value: 1st data	8'h00

Table 463. SPI_LEGACY_TX_DAT04_REG (0x500B_0194)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 8th data	8'h00
23:16	R/W	-	TX value: 7th data	8'h00
15:8	R/W	-	TX value: 6th data	8'h00
7:0	R/W	-	TX value: 5th data	8'h00

Table 464. SPI_LEGACY_TX_DAT08_REG (0x500B_0198)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 12th data	8'h00
23:16	R/W	-	TX value: 11th data	8'h00
15:8	R/W	-	TX value: 10th data	8'h00
7:0	R/W	-	TX value: 9th data	8'h00

Table 465. SPI_LEGACY_TX_DAT12_REG (0x500B_019C)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 16th data	8'h00
23:16	R/W	-	TX value: 15th data	8'h00
15:8	R/W	-	TX value: 14th data	8'h00
7:0	R/W	-	TX value: 13th data	8'h00

Table 466. SPI_LEGACY_TX_DAT16_REG (0x500B_01A0)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 20th data	8'h00
23:16	R/W	-	TX value: 19th data	8'h00
15:8	R/W	-	TX value: 18th data	8'h00
7:0	R/W	-	TX value: 17th data	8'h00

Table 467. SPI_LEGACY_TX_DAT20_REG (0x500B_01A4)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 24th data	8'h00
23:16	R/W	-	TX value: 23rd data	8'h00
15:8	R/W	-	TX value: 22nd data	8'h00
7:0	R/W	-	TX value: 21st data	8'h00

Table 468. SPI_LEGACY_TX_DAT24_REG (0x500B_01A8)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 28th data	8'h00
23:16	R/W	-	TX value: 27th data	8'h00
15:8	R/W	-	TX value: 26th data	8'h00
7:0	R/W	-	TX value: 25th data	8'h00

Table 469. SPI_LEGACY_TX_DAT28_REG (0x500B_01AC)

Bit	Mode	Symbol	Description	Reset
31:24	R/W	-	TX value: 32nd data	8'h00
23:16	R/W	-	TX value: 31st data	8'h00
15:8	R/W	-	TX value: 30th data	8'h00
7:0	R/W	-	TX value: 29th data	8'h00

Table 470. DMA_MP0_CTRL_REG (0x500B_0200)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	-
15:12	R/W	MP0_BURST	Burst access size per block for the DMA. 0: 2^0 1: 2^1 2: 2^2 F: 2^15 (32K access)	4'h0
11:8	R/W	MP0_IDLE	Idle size per block for the DMA. 0: 0	4'h0

Bit	Mode	Symbol	Description	Reset
			1: 2^0 2: 2^1 F: 2^14 (16K idle cycles)	
7:6	-	-	Reserved	-
5:4	R/W	MP0_HSIZE	Data width for the DMA AHB master port #0. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	2'h2
3	R/W	MP0_AI	Address incremental enable for the DMA AHB master port #0.	1'b1
2:0	R/W	MP0_PORT	AHB bus protection for the DMA (Reserved) HPROT[0] = Data access [21]: HPROT[1] = 0 User access, 1 Privileged access [22]: HPROT[2] = 0 Non-bufferable, 1 Bufferable [23]: HPROT[3] = 0 Non-cacheable, 1 Cacheable	3'h0

Table 471. DMA_MP0_TASK_REG (0x500B_0204)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	-
10:8	R/W	MP0_TASK_SZ	Operation channel task size of the DMA master port #0. N: N+1 task	3'h0
7:0	-	-	Reserved	-

Table 472. DMA_IRQ_MASK_REG (0x500B_0208)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	IRQ_MASK_EN	IRQ mask enable of the DMA task operation. [8]: Last Task [7]: Task #7 [6]: Task #6 [5]: Task #5 [4]: Task #4 [3]: Task #3 [2]: Task #2 [1]: Task #1 [0]: Task #0	9'h100

Table 473. DMA_FIFO_THR_REG (0x500B_020C)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	MP0_FIFO_TH	Write operation threshold of the DMA FIFO to check almost full.	6'h39
6:0	R/W	MP1_FIFO_TH	Read operation threshold of the DMA FIFO to check almost full.	6'h40

Table 474. DMA_TSK_0_ADR_REG (0x500B_0210)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	TSK_0_ADR	Base address for the DMA task #0 of the AHB bus domain.	32'h0000

Table 475. DMA_TSK_0_TTL_REG (0x500B_0214)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R/W	TSK_0_TTL	Total transfer length for the DMA task #0 of the AHB bus domain. 0: 0 byte 1: 1 byte Max transfer length = 2M-1 bytes	21'h0000

Table 476. DMA_OP_STATUS_REG (0x500B_0260)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R	OP_STATUS	Current operation status of the DMA domain. 0: S_IDLE 1: S_DONE 4: S_FRST 5: S_DRUN 6: S_LAST 2, 3, 7: Reserved	3'h0

Table 477. DMA_OP_TASK_REG (0x500B_0264)

Bit	Mode	Symbol	Description	Reset
31:12	-	-	Reserved	-
11:8	R	NEXT_OP_TASK	Next operation task of the DMA	4'h0
7:4	-	-	Reserved	-
3:0	R	CURR_OP_TASK	Current operation task of the DMA. 0: Idle 1: DMA Task #0 k: DMA Task #(k-1) 8: DMA Task #7 9: Error	4'h0

Table 478. DMA_CURR_TASK_ADR_REG (0x500B_0268)

Bit	Mode	Symbol	Description	Reset
31:0	R	CURR_TASK_ADR	Base address for the current DMA task	32'h0000

Table 479: DMA_CURR_TASK_TTL_REG (0x500B_026C)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R	CURR_TASK_TTL	Total transfer length for the current DMA task	21'h0000

Table 480: DMA_FIFO_ADDR_REG (0x500B_0270)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
11:8	R	FIFO_WADDR	Write address of the DMA FIFO	4'h0
7:4	-	-	Reserved	-
3:0	R	FIFO_RADDR	Read address of the DMA FIFO	4'h0

Table 481. DMA_CLK_FREQ_S_REG (0x500B_0280)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	FREQ_S	Setting value of DMA SPI interface clock frequency (0 ~ 511 MHz). This value should be less than or equal to 1/2 of XFC core clock frequency.	9'h028

Table 482. DMA_CLK_FREQ_R_REG (0x500B_0284)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R	FREQ_R	Division parameter for the real value of DMA SPI interface clock frequency. 0: Not used 1: XFC core clock frequency/2 N: XFC core clock frequency/(N+1)	9'h028

Table 483. DMA_DLY_INDEX_REG (0x500B_0288)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	DLY_INDEX	SPI delay index in the DMA mode. 0: Use XFC_SPI_DLY_0_TXC and XFC_SPI_DLY_0_RXC 1: Use XFC_SPI_DLY_1_TXC and XFC_SPI_DLY_1_RXC 2: Use XFC_SPI_DLY_2_TXC and XFC_SPI_DLY_2_RXC 3: Use XFC_SPI_DLY_3_TXC and XFC_SPI_DLY_3_RXC	2'h0

Table 484. QSPI_CLK_FREQ_S_REG (0x500B_0300)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R/W	FREQ_S	Setting value of XIP SPI interface clock frequency (0 ~ 511 MHz). This value should be less than or equal to 1/2 of XFC core clock frequency.	9'h028

Table 485. QSPI_CLK_FREQ_R_REG (0x500B_0304)

Bit	Mode	Symbol	Description	Reset
31:9	-	-	Reserved	-
8:0	R	FREQ_R	Division parameter for the real value of XIP interface clock frequency. 0: Not used 1: XFC core clock frequency/2 N: XFC core clock frequency/(N+1)	9'h028

Table 486: QSPI_DMY_CYC_REG (0x500B_0308)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4:0	R/W	DMY_CYC	Number of XIP SPI dummy cycles (Interface clock). N: N dummy cycles	5'h00

Table 487. QSPI_WAIT_CYC_REG (0x500B_030C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	WAIT_CYC	Wait cycles between consecutive transfers for other SPI slaves (Interface Clock). N: N wait cycles	8'h00

Table 488. QSPI_IF_MODE_REG (0x500B_0310)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	IF_MODE	XIP SPI Interface mode: {CPOL, CPHASE}. 0: Mode 0 (0,0) 3: Mode 3 (1,1)	2'h0

Table 489. QSPI_CTRL_REG (0x500B_0314)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4	R/W	TO_EN	Enable register of XIP time out operation.	1'b0
3:2	R/W	MODE_SIZE	Number of XIP SPI mode (or Option code) bits. 0: 8 bits (example: 0xA5) 1: 4 bits (example: 0xAX) 2: 2 bits 3: 1 bit	2'h1
1	R/W	CMD_SIZE	Number of XIP SPI command bytes. 0: 1 byte 1: 2 bytes	1'b0
0	R/W	ADR_SIZE	Number of XIP SPI address bytes. 0: 3 bytes 1: 4 bytes	1'b0

Table 490. QSPI_BYTE_SWAP_REG (0x500B_0318)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	BYTE_SWAP	Swap type of XIP SPI data in AHB bus. 0: Normal (little endian) {3, 2, 1, 0} 1: 4-byte swap (big endian per 4 bytes) {3, 2, 1, 0} -> {0, 1, 2, 3} 2: 2-byte swap (big endian per 2 bytes) {3, 2, 1, 0} -> {2, 3, 0, 1} 3: 16-bit swap {3, 2, 1, 0} -> {1, 0, 3, 2}	1'b0

Table 491. QSPI_WRAP_EN_REG (0x500B_031C)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	WRAP_EN	Wrap enable to access first the critical address.	1'b0

Table 492. QSPI_BUS_TYPE_REG (0x500B_0320)

Bit	Mode	Symbol	Description	Reset
31	R/W		1: Off 0: On	1'b0
30	R/W		1: DTR 0: STR	1'b0
29:28	R/W		I/O bits N: 2^N bit, should be used only 0	2'h0
27:24	R/W	TRX_DAT	XIP SPI TX/RX data	4'h0
23:20	-	-	Reserved	-
19:16	R/W	MODE	XIP SPI mode	4'h0
15:12	-	-	Reserved	-
11:8	R/W	ADR	XIP SPI address	4'h0
7:4	-	-	Reserved	-
3:0	R/W	CMD	XIP SPI command	4'h0

Table 493. QSPI_IO_DX_TYPE_REG (0x500B_0324)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:16	R/W		Output value of XIP SPI DIOx if operation type is manual.	8'h00

Bit	Mode	Symbol	Description	Reset
			0: Logic 0 1: Logic 1	
15:8	R/W		Direction type of XIP SPI DIOx if operation type is manual. 0: Input 1: Output	8'h00
7:0	R/W		Operation type of XIP SPI DIOx. 0: Auto 1: Manual	8'h00

Table 494. QSPI_IO_CK_TYPE_REG (0x500B_0128)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R/W	CK_TYPE	XIP SPI clock pin. [2]: Output value of SPI CLK if operation type is manual [1]: Direction type of SPI CLK if operation type is manual [0]: Operation type of SPI CLK	3'h0

Table 495. QSPI_IO_CS_TYPE_REG (0x500B_032C)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	-
27:24	R/W	CS_TYPE	Output polarity of XIP SPI CS_x if operation type is auto. 0: Active low 1: Active high [27]: CS_3 [26]: CS_2 [25]: CS_1 [24]: CS_0	4'h0
23:20	-	-	-	-
19:16	R/W	CS_OUT	Output value of XIP SPI CS_x if operation type is manual.	4'h0
15:12	-	-	-	-
11:8	R/W	CS_DIR	Direction type of XIP SPI CS_x if operation type is manual.	4'h0
7:4	-	-	-	-
3:0	R/W	CS_OP	Operation type of XIP SPI CS_x.	4'h0

Table 496. QSPI_CS_SEL_REG (0x500B_0330)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	CS_SEL	Selecting XIP CS port to be actually used. [3]: SPI_CS_3 [2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	4'h1

Table 497. QSPI_IO_1_TYPE_REG (0x500B_0334)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	IO_1	I/O Operation Type when SPI is Single I/O mode. 0: 4-wire SPI Bus (standard I/O SPI Bus) 1: 3-wire SPI Bus (single I/O SPI Bus) [3]: SPI_CS_3	4'h0

Bit	Mode	Symbol	Description	Reset
			[2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	

Table 498. QSPI_TWIN_EN_REG (0x500B_033C)

Bit	Mode	Symbol	Description	Reset
31:4	-	-	Reserved	-
3:0	R/W	TWIN_EN	Enable of twin QSPI Flash. [3]: SPI_CS_3 [2]: SPI_CS_2 [1]: SPI_CS_1 [0]: SPI_CS_0	4'h0

Table 499. QSPI_RW_REG (0x500B_0340)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	REG_RW	XIP SPI data type 0: Read 1: Write	1'b0

Table 500. QSPI_CMD_REG (0x500B_0344)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
15:0	R/W	REG_CMD	XIP SPI command field. [15:0]: Command (instruction code)	16'h0000

Table 501. QSPI_MODE_REG (0x500B_034C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	REG_MODE	XIP SPI mode (or Option control). Optional control bits that follow the address bits.	8'h00

Table 502. QSPI_BURST_REG (0x500B_0350)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R/W	BURST	XIP SPI burst access size for the cache controller. 0: 0 byte 1: 1 byte Max transfer length = 2M-1 bytes	21'h0004

Table 503. QSPI_DLY_INDEX_REG (0x500B_0354)

Bit	Mode	Symbol	Description	Reset
31:2	-	-	Reserved	-
1:0	R/W	DLY_INDEX	XIP SPI delay index. 0: Use XFC_SPI_DLY_0_TXC and XFC_SPI_DLY_0_RXC 1: Use XFC_SPI_DLY_1_TXC and XFC_SPI_DLY_1_RXC 2: Use XFC_SPI_DLY_2_TXC and XFC_SPI_DLY_2_RXC 3: Use XFC_SPI_DLY_3_TXC and XFC_SPI_DLY_3_RXC	2'h0

Table 504. QSPI_OFFSET_ADDR_REG (0x500B_0360)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:0	R/W	OFFSET	Flash offset address to remap cache address in XIP mode. [3:0] is all low (16 bytes/unit)	24'h0000

Table 505. QSPI_CURR_DOUT_REG (0x500B_0364)

Bit	Mode	Symbol	Description	Reset
31:0	R	OFFSET	XIP current read data to debug.	32'h0000

Table 506. QSPI_CURR_ADDR_REG (0x500B_0368)

Bit	Mode	Symbol	Description	Reset
31:0	R	OFFSET	XIP current address to debug.	32'h0000

Table 507. QSPI_OP_STATUS_REG (0x500B_0370)

Bit	Mode	Symbol	Description	Reset
31:3	-	-	Reserved	-
2:0	R		Current operation status of the XIP domain. 0: Normal 1: Running 2 ~ 6: Reserved 7: Error	3'h0

Table 508. QSPI_DEC_SEED_VAL_REG (0x500B_0400)

Bit	Mode	Symbol	Description	Reset
31	-	-	Reserved	-
30:0	R/W		Seed value of XIP decryption	31'h7FFF_FFFF

Table 509. QSPI_DEC_SEL_REG (0x500B_0404)

Bit	Mode	Symbol	Description	Reset
31	-	-	Reserved	-
27:24	R/W	SUMA	Address position to select inversion operation of SumA. 0x0: HADDR[[4] 0x1: HADDR[5] ... 0xF: HADDR[19]	4'h0
19:16	R/W	SUMK	Address position to select inversion operation of SumK. 0x0: HADDR[[4] 0x1: HADDR[5] ... 0xF: HADDR[19]	4'h0
11:8	R/W	SHIFT	Address position to select shift operation from calculated sum. 0x0: HADDR[[7:4] 0x1: HADDR[8:5] ... 0xF: HADDR[22:19]	4'h0
4:0	R/W	OP_EN	Operation enable of XIP decryption. [4]: Reverse operation [3]: Shift operation [2]: Inversion operation of SumK [1]: Inversion operation of SumA [0]: Operation enable of XIP decryption	5'h00

10.16 Fast DMA Register

Table 510. Fast DMA registers

Address	Register	Description
0x5006_0000	FDMA_REQ_HOLD	Hold request of the fast DMA, active high.
	FDMA_REQ_CLR_OP	Operation clear request of the fast DMA, active high with auto clear function.
0x5006_0004	FDMA_REQ_CLR_STA	Status clear request of the fast DMA, active high with auto clear function: History status of channel and LLI tasks.
	FDMA_REQ_CLR_IRQ	IRQ clear request of the fast DMA, active high with auto clear function.
0x5006_0008	FDMA_IRQ_MSK_EN	IRQ mask enable of the fast DMA.
	FDMA_OP_EN	Operation enable of the fast DMA.
0x5006_000C	FDMA_ST_CH_EN	DMA starting channel enable of the fast DMA, active high with auto clear function.
0x5006_0010	FDMA_ERR_TYPE	1st error type.
	FDMA_OP_STATUS	Current operation status of the fast DMA controller.
	FDMA_IRQ_STATUS	IRQ status of the fast DMA.
	FDMA_NEXT_CH	Next operation channel of the fast DMA.
	FDMA_CURR_CH	Current operation channel of the fast DMA.
0x5006_0014	FDMA_CH_LLI_SIZE	LLI size
0x5006_0020	FDMA_CH_HIST_0	Channel history of the DMA operation
0x5006_0024	FDMA_CH_HIST_1	Channel history of the DMA operation
0x5006_0028	FDMA_CH_HIST_2	Channel history of the DMA operation
0x5006_002C	FDMA_CH_HIST_3	Channel history of the DMA operation
0x5006_0100	FDMA_CH1_D_AI	Destination address incremental enable for channel #1.
	FDMA_CH1_D_PORT	Destination AHB master port select for channel #1.
	FDMA_CH1_D_HSIZE	Destination data width for channel #1.
	FDMA_CH1_S_AI	Source address incremental enable for channel #1.
	FDMA_CH1_S_PORT	Source AHB master port select for channel #1.
	FDMA_CH1_S_HSIZE	Source data width for channel #1.
	FDMA_CH1_BST	Burst access size per block for channel #1.
	FDMA_CH1_TTL	Total transfer length for channel #1.
0x5006_0104	FDMA_CH1_LLI_EN	Next LLI enable for channel #1 (Reserved).
	FDMA_CH1_NEXT_CH	Indicator for the next channel for channel #1.
	FDMA_CH1_PROT	AHB bus protection for channel #1 (Reserved).
	FDMA_CH1_IRQ_EN	Interrupt enable for channel #1.
	FDMA_CH1_IDLE	Idle size per block for channel #1.
	FDMA_CH1_Callback	Callback index for channel #1.
0x5006_0108	FDMA_CH1_SRC_A	Source address for channel #1
0x5006_010C	FDMA_CH1_DST_A	Destination address for channel #1
0x5006_0110	FDMA_CH1_LLI_BA	Base address of LLI for channel #1
0x5006_0114	FDMA_CH1_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #1.
	FDMA_CH1_LLI_TN	Total number of LLI tasks for channel #1.
0x5006_0118	FDMA_CH1_LLI_SI	Starting index of LLI tasks for channel #1
0x5006_0120	FDMA_CH1_LLI_ST	Status of current LLI task for channel #1.
	FDMA_CH1_LLI_CT	Current LLI task for Channel #1.
0x5006_0200	FDMA_CH2_D_AI	Destination address incremental enable for channel #2.
	FDMA_CH2_D_PORT	Destination AHB master port select for channel #2.
	FDMA_CH2_D_HSIZE	Destination data width for channel #2.
	FDMA_CH2_S_AI	Source address incremental enable for channel #2.

Address	Register	Description
	FDMA_CH2_S_PORT	Source AHB master port select for channel #2.
	FDMA_CH2_S_HSIZE	Source data width for channel #2.
	FDMA_CH2_BST	Burst size per block for channel #2.
	FDMA_CH2_TTL	Total transfer length for channel #2.
0x5006_0204	FDMA_CH2_LLI_EN	Next LLI enable for channel #2 (Reserved).
	FDMA_CH2_NEXT_CH	Indicator for the next channel for channel #2.
	FDMA_CH2_PROT	AHB bus protection for channel #2 (Reserved).
	FDMA_CH2_IRQ_EN	Interrupt enable for channel #2.
	FDMA_CH2_IDLE	Idle size per block for channel #2.
	FDMA_CH2_Callback	Callback index for channel #2.
0x5006_0208	FDMA_CH2_SRC_A	Source address for channel #2
0x5006_020C	FDMA_CH2_DST_A	Destination address for channel #2
0x5006_0210	FDMA_CH2_LLI_BA	Base address of LLI for channel #2
0x5006_0214	FDMA_CH2_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #2.
	FDMA_CH2_LLI_TN	Total number of LLI tasks for channel #2.
0x5006_0218	FDMA_CH2_LLI_SI	Starting index of LLI tasks for channel #2
0x5006_0220	FDMA_CH2_LLI_ST	Status of current LLI task for channel #2.
	FDMA_CH2_LLI_CT	Current LLI task for channel #2.
0x5006_0300	FDMA_CH3_D_AI	Destination address incremental enable for channel #3.
	FDMA_CH3_D_PORT	Destination AHB master port select for channel #3.
	FDMA_CH3_D_HSIZE	Destination data width for channel #3.
	FDMA_CH3_S_AI	Source address incremental enable for channel #3.
	FDMA_CH3_S_PORT	Source AHB master port select for channel #3.
	FDMA_CH3_S_HSIZE	Source data width for channel #3.
	FDMA_CH3_BST	Burst size per block for channel #3.
	FDMA_CH3_TTL	Total transfer length for channel #3.
0x5006_0304	FDMA_CH3_LLI_EN	Next LLI enable for channel #3 (Reserved).
	FDMA_CH3_NEXT_CH	Indicator for the next channel for Channel #3.
	FDMA_CH3_PROT	AHB bus protection for channel #3 (Reserved).
	FDMA_CH3_IRQ_EN	Interrupt enable for channel #3.
	FDMA_CH3_IDLE	Idle size per block for channel #3.
	FDMA_CH3_Callback	Callback index for channel #3.
0x5006_0308	FDMA_CH3_SRC_A	Source address for channel #3
0x5006_030C	FDMA_CH3_DST_A	Destination address for channel #3
0x5006_0310	FDMA_CH3_LLI_BA	Base address of LLI for channel #3
0x5006_0314	FDMA_CH3_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #3.
	FDMA_CH3_LLI_TN	Total number of LLI tasks for channel #3.
0x5006_0318	FDMA_CH3_LLI_SI	Starting index of LLI tasks for channel #3
0x5006_0320	FDMA_CH3_LLI_ST	Status of current LLI task for channel #3.
	FDMA_CH3_LLI_CT	Current LLI task for channel #3.
0x5006_0400	FDMA_CH4_D_AI	Destination address incremental enable for channel #4.
	FDMA_CH4_D_PORT	Destination AHB master port select for channel #4.
	FDMA_CH4_D_HSIZE	Destination data width for channel #4.
	FDMA_CH4_S_AI	Source address incremental enable for channel #4.
	FDMA_CH4_S_PORT	Source AHB master port select for channel #4.
	FDMA_CH4_S_HSIZE	Source data width for channel #4.
	FDMA_CH4_BST	Burst size per block for channel #4.
	FDMA_CH4_TTL	Total transfer length for channel #4.
0x5006_0404	FDMA_CH4_LLI_EN	Next LLI enable for channel #4 (Reserved)
	FDMA_CH4_NEXT_CH	Indicator for the next channel for channel #4.

Address	Register	Description
	FDMA_CH4_PROT FDMA_CH4_IRQ_EN FDMA_CH4_IDLE FDMA_CH4_Callback	AHB bus protection for channel #4 (Reserved). Interrupt enable for channel #4. Idle size per block for channel #4. Callback index for channel #4.
0x5006_0408	FDMA_CH4_SRC_A	Source address for channel #4
0x5006_040C	FDMA_CH4_DST_A	Destination address for channel #4
0x5006_0410	FDMA_CH4_LLI_BA	Base address of LLI for channel #4
0x5006_0414	FDMA_CH4_LLI_CN FDMA_CH4_LLI_TN	Number of LLI tasks to be processed in a continuous operation for Channel #4. Total number of LLI tasks for channel #4.
0x5006_0418	FDMA_CH4_LLI_SI	Starting index of LLI tasks for channel #4
0x5006_0420	FDMA_CH4_LLI_ST FDMA_CH4_LLI_CT	Status of current LLI task for channel #4. Current LLI task for channel #4.

Table 511. FDMA_REQ_REG (0x5006_0000)

Bit	Mode	Symbol	Description	Reset
11:8	R/W	FDMA_REQ_HOLD	Hold request of the fast DMA, active high. Bit[8+i]: for channel #i+1	0x0
3:0	W	FDMA_REQ_CLK_OP	Operation clear request of the fast DMA, active high with auto clear function. Bit[i]: for Channel #i+1	0x0

Table 512. FDMA_REQ_CLR_REG (0x5006_0004)

Bit	Mode	Symbol	Description	Reset
8	W	FDMA_REQ_CLR_STA	Status clear request of the fast DMA, active high with auto clear function: History status of channel and LLI tasks.	0x0
5:0	W	FDMA_REQ_CLR_IRQ	IRQ clear request of the fast DMA, active high with auto clear function. [5]: Operation error [4]: Operation hold [3]: Channel #4 done [2]: Channel #3 done [1]: Channel #2 done [0]: Channel #1 done	0x00

Table 513. FDMA_ENABLE_REG (0x5006_0008)

Bit	Mode	Symbol	Description	Reset
21:16	R/W	FDMA_IRQ_MSK_EN	IRQ mask enable of the fast DMA. [16+5]: Occurrence of error [16+4]: Occurrence of hold [16+3]: Channel #4 done [16+2]: Channel #3 done [16+1]: Channel #2 done [16+0]: Channel #1 done	0x3F
0	RW	FDMA_OP_EN	Operation enable of the fast DMA. Disabling the fast DMA reduces power consumption.	0x1

Table 514. FDMA_ST_CH_EN_REG (0x5006_000C)

Bit	Mode	Symbol	Description	Reset
3:0	W	FDMA_ST_CH_EN	DMA starting channel enable of the fast DMA, active high with auto clear function. Bit[i]: for channel #i+1	0x0

Table 515. FDMA_STATUS_REG (0x5006_0010)

Bit	Mode	Symbol	Description	Reset
31:28	R	FDMA_ERR_TYPE	1st error type. 0: Normal 1: AHB bus error in AHB master 0 port 2: AHB bus error in AHB master 1 port 3: FIFO overflow 4: FIFO underflow	0x0
25:24	R	FDMA_OP_STATUS	Current operation status of the fast DMA controller. 0: Idle 1: Running 2: Holding 3: Error	0x0
21:16	R	FMDA_IRQ_STATUS	IRQ status of the fast DMA. [16+5]: Occurrence of error [16+4]: Occurrence of hold [16+3]: Channel #4 done [16+2]: Channel #3 done [16+1]: Channel #2 done [16+0]: Channel #1 done	0x00
10:8	R	FDMA_NEXT_CH	Next operation channel of the fast DMA. 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4 5: Error	0x0
2:0	R	FDMA_CURR_CH	Current operation channel of the fast DMA. 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4 5: Error	0x0

Table 516. FDMA_CH_LLI_SIZE_REG (0x5006_0014)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	FDMA_CH_LLI_SIZE	LLI size. 0: 4 words 1: 5 words 2: 6 words 3: 7 words 4: 8 words	0x0

Table 517. FDMA_CH_HIST_0_REG (0x5006_0020)

Bit	Mode	Symbol	Description	Reset
31:0	R	FDMA_CH_HIST_0	Channel history of the DMA operation. [07:00]: Current channel [2:0] 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3	0x0000

Bit	Mode	Symbol	Description	Reset
			4: Channel #4 [7:3] Reserved [15:08]: Current channel - 1, past channel before current channel [23:16]: Current channel - 2 [31:24]: Current channel - 3	

Table 518. FDMA_CH_HIST_1_REG (0x5006_0024)

Bit	Mode	Symbol	Description	Reset
31:0	R	FDMA_CH_HIST_1	Channel history of the DMA operation. [07:00]: Current channel - 4 [15:08]: Current channel - 5 [23:16]: Current channel - 6 [31:24]: Current channel - 7	0x0000

Table 519. FDMA_CH_HIST_2_REG (0x5006_0028)

Bit	Mode	Symbol	Description	Reset
31:0	R	FDMA_CH_HIST_2	Channel history of the DMA operation. [07:00]: Current channel - 8 [15:08]: Current channel - 9 [23:16]: Current channel - 10 [31:24]: Current channel - 11	0x0000

Table 520. FDMA_CH_HIST_3_REG (0x5006_002C)

Bit	Mode	Symbol	Description	Reset
31:0	R	FDMA_CH_HIST_3	Channel history of the DMA operation. [07:00]: Current channel - 12 [15:08]: Current channel - 13 [23:16]: Current channel - 14 [31:24]: Current channel - 15	0x0000

Table 521. FDMA_CH1_CTRL_REG (0x5006_0100)

Bit	Mode	Symbol	Description	Reset
31	R/W	FDMA_CH1_D_AI	Destination address incremental enable for channel #1.	0x1
30	R/W	FDMA_CH1_D_PORT	Destination AHB master port select for channel #1. 0: AHB master 0 selected for destination transfer 1: AHB master 1 selected for destination transfer	0x1
29:28	R/W	FDMA_CH1_D_HSIZE	Destination data width for channel #1. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
27	R/W	FDMA_CH1_S_AI	Source address incremental enable for channel #1.	0x1
26	R/W	FDMA_CH1_S_PORT	Source AHB master port select for channel #1. 0: AHB master 0 selected for source transfer 1: AHB master 1 selected for source transfer	0x0
25:24	R/W	FDMA_CH1_S_HSIZE	Source data width for channel #1. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
23:20	R/W	FDMA_CH1_BST	Burst access size per block for channel #1.	0x0

Bit	Mode	Symbol	Description	Reset
			0: 2^0 1: 2^1 2: 2^2 F: 2^15 (32K access)	
19:0	R/W	FDMA_CH1_TTL	Total transfer length for channel #1. 0~6: Not supported 7: 8 bytes 8: 9 bytes Max transfer length = 1M bytes	0x00000

Table 522. FDMA_CH1_CTRL2_REG (0x5006_0104)

Bit	Mode	Symbol	Description	Reset
27	R/W	FDMA_CH1_LLI_EN	Next LLI enable for channel #1 (Reserved).	0x0
26:24	R/W	FDMA_CH1_NEXT_CH	Indicator for the next channel for channel #1. 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4	0x0
23:21	R/W	FDMA_CH1_PROT	AHB bus protection for channel #1 (Reserved). HPROT[0] = Data access [21]: HPROT[1] = 0 User access, 1 Privileged access [22]: HPROT[2] = 0 Non-bufferable, 1 Bufferable [23]: HPROT[3] = 0 Non-cacheable, 1 Cacheable	0x0
20	R/W	FDMA_CH1_IRQ_EN	Interrupt enable for channel #1	0x0
19:16	R/W	FDMA_CH1_IDLE	Idle size per block for channel #1. 0: 0 1: 2^0 2: 2^1 F: 2^14 (16K idle cycles)	0x0
15:0	R/W	FDMA_CH1_CALLBACK	Callback index for channel #1.	0x0000

Table 523. FDMA_CH1_SRC_A_REG (0x5006_0108)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH1_SRC_A	Source address for channel #1	32’d0

Table 524. FDMA_CH1_DST_A_REG (0x5006_010C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH1_DST_A	Destination address for channel #1	32’d0

Table 525. FDMA_CH1_LLI_BA_REG (0x5006_0110)

Bit	Mode	Symbol	Description	Reset
31:2	R/W	FDMA_CH1_LLI_BA	Base address of LLI for channel #1	30’d0
1:0	-	-	Reserved	0x0

Table 526. FDMA_CH1_LLI_TASK_NUM_REG (0x5006_0114)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FDMA_CH1_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #1	0x0000
15:0	R/W	FDMA_CH1_LLI_TN	Total number of LLI tasks for channel #1	0x0000

Table 527. FDMA_CH1_LLI_SI_REG (0x5006_0118)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	FDMA_CH1_LLI_SI	Starting index of LLI tasks for channel #1	0x0000

Table 528. FDMA_CH1_LLI_STS_REG (0x5006_0120)

Bit	Mode	Symbol	Description	Reset
19:16	R	FDMA_CH1_LLI_ST	Status of current LLI task for channel #1. [3]: 0 Reg, 1 Mem [2:0]: 0 Idle, 1 Set, 2 Run, 3 Done, 4 Wait	0x0
15:0	R	FDMA_CH1_LLI_CT	Current LLI task for channel #1	0x0000

Table 529. FDMA_CH2_CTRL_REG (0x5006_0200)

Bit	Mode	Symbol	Description	Reset
31	R/W	FDMA_CH2_D_AI	Destination address incremental enable for channel #2.	0x1
30	R/W	FDMA_CH2_D_PORT	Destination AHB master port select for Channel #2. 0: AHB master 0 selected for destination transfer 1: AHB master 1 selected for destination transfer	0x1
29:28	R/W	FDMA_CH2_D_HSIZE	Destination data width for channel #2. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
27	R/W	FDMA_CH2_S_AI	Source address incremental enable for channel #2.	0x1
26	R/W	FDMA_CH2_S_PORT	Source AHB master port select for channel #2. 0: AHB master 0 selected for source transfer 1: AHB master 1 selected for source transfer	0x0
25:24	R/W	FDMA_CH2_S_HSIZE	Source data width for channel #2. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
23:20	R/W	FDMA_CH2_BST	Burst access size per block for channel #2. 0: 2^0 1: 2^1 2: 2^2 F: 2^15 (32K access)	0x0
19:0	R/W	FDMA_CH2_TTL	Total transfer length for channel #2. 0~6: Not supported 7: 8 bytes 8: 9 bytes Max transfer length = 1M bytes	0x00000

Table 530. FDMA_CH2_CTRL2_REG (0x5006_0204)

Bit	Mode	Symbol	Description	Reset
27	R/W	FDMA_CH2_LLI_EN	Next LLI enable for channel #2 (Reserved).	0x0
26:24	R/W	FDMA_CH2_NEXT_CH	Indicator for the next channel for channel #2. 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4	0x0
23:21	R/W	FDMA_CH2_PROT	AHB bus protection for channel #2 (Reserved).	0x0

Bit	Mode	Symbol	Description	Reset
20	R/W	FDMA_CH2_IRQ_EN	Interrupt enable for channel #2.	0x0
19:16	R/W	FDMA_CH2_IDLE	Idle size per block for channel #2. 0: 0 1: 2^0 2: 2^1 F: 2^14 (16K idle cycles)	0x0
15:0	R/W	FDMA_CH2_CALLBACK	Callback index for channel #2	0x0000

Table 531. FDMA_CH2_SRC_A_REG (0x5006_0208)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH2_SRC_A	Source address for channel #2	32'd0

Table 532. FDMA_CH2_DST_A_REG (0x5006_020C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH2_DST_A	Destination address for channel #2	32'd0

Table 533. FDMA_CH2_LLI_BA_REG (0x5006_0210)

Bit	Mode	Symbol	Description	Reset
31:2	R/W	FDMA_CH2_LLI_BA	Base address of LLI for channel #2	30'd0
1:0	-	-	Reserved	0x0

Table 534. FDMA_CH2_LLI_TASK_NUM_REG (0x5006_0214)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FDMA_CH2_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #2	0x0000
15:0	R/W	FDMA_CH2_LLI_TN	Total number of LLI tasks for channel #2	0x0000

Table 535. FDMA_CH2_LLI_SI_REG (0x5006_0218)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	FDMA_CH2_LLI_SI	Starting index of LLI tasks for channel #2	0x0000

Table 536. FDMA_CH2_LLI_STS_REG (0x5006_0220)

Bit	Mode	Symbol	Description	Reset
19:16	R	FDMA_CH2_LLI_ST	Status of current LLI task for channel #2. [3]: 0 Reg, 1 Mem [2:0]: 0 Idle, 1 Set, 2 Run, 3 Done, 4 Wait	0x0
15:0	R	FDMA_CH2_LLI_CT	Current LLI task for channel #2	0x0000

Table 537. FDMA_CH3_CTRL_REG (0x5006_0300)

Bit	Mode	Symbol	Description	Reset
31	R/W	FDMA_CH3_D_AI	Destination address incremental enable for channel #3	0x1
30	R/W	FDMA_CH3_D_PORT	Destination AHB master port select for channel #3. 0: AHB master 0 selected for destination transfer 1: AHB master 1 selected for destination transfer	0x1
29:28	R/W	FDMA_CH3_D_HSIZE	Destination data width for channel #3. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
27	R/W	FDMA_CH3_S_AI	Source address incremental enable for channel #3.	0x1
26	R/W	FDMA_CH3_S_PORT	Source AHB master port select for channel #3.	0x0

Bit	Mode	Symbol	Description	Reset
			0: AHB master 0 selected for source transfer 1: AHB master 1 selected for source transfer	
25:24	R/W	FDMA_CH3_S_HSIZE	Source data width for channel #3. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
23:20	R/W	FDMA_CH3_BST	Burst access size per block for channel #3. 0: 2^0 1: 2^1 2: 2^2 F: 2^15 (32K access)	0x0
19:0	R/W	FDMA_CH3_TTL	Total transfer length for channel #3. 0~6: Not supported 7: 8 bytes 8: 9 bytes Max transfer length = 1M bytes	0x00000

Table 538. FDMA_CH3_CTRL2_REG (0x5006_0304)

Bit	Mode	Symbol	Description	Reset
27	R/W	FDMA_CH3_LLI_EN	Next LLI enable for channel #3 (Reserved).	0x0
26:24	R/W	FDMA_CH3_NEXT_CH	Indicator for the next channel for channel #3. 0: Idle 1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4	0x0
23:21	R/W	FDMA_CH3_PROT	AHB bus protection for channel #3 (Reserved).	0x0
20	R/W	FDMA_CH3_IRQ_EN	Interrupt enable for channel #3.	0x0
19:16	R/W	FDMA_CH3_IDLE	Idle size per block for channel #3. 0: 0 1: 2^0 2: 2^1 F: 2^14 (16K idle cycles)	0x0
15:0	R/W	FDMA_CH3_CALLBACK	Callback index for channel #3.	0x0000

Table 539. FDMA_CH3_SRC_A_REG (0x5006_0308)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH3_SRC_A	Source address for channel #3	32’d0

Table 540. FDMA_CH3_DST_A_REG (0x5006_030C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH3_DST_A	Destination address for channel #3	32’d0

Table 541. FDMA_CH3_LLI_BA_REG (0x5006_0310)

Bit	Mode	Symbol	Description	Reset
31:2	R/W	FDMA_CH3_LLI_BA	Base address of LLI for channel #3	30’d0
1:0	-	-	Reserved	0x0

Table 542. FDMA_CH3_LLI_TASK_NUM_REG (0x5006_0314)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FDMA_CH3_LLI_CN	Number of LLI tasks to be processed in a continuous operation for Channel #3	0x0000
15:0	R/W	FDMA_CH3_LLI_TN	Total number of LLI tasks for channel #3	0x0000

Table 543. FDMA_CH3_LLI_SI_REG (0x5006_0318)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	FDMA_CH3_LLI_SI	Starting index of LLI tasks for channel #3	0x0000

Table 544. FDMA_CH3_LLI_STS_REG (0x5006_0320)

Bit	Mode	Symbol	Description	Reset
19:16	R	FDMA_CH3_LLI_ST	Status of current LLI task for channel #3. [3]: 0 Reg, 1 Mem [2:0]: 0 Idle, 1 Set, 2 Run, 3 Done, 4 Wait	0x0
15:0	R	FDMA_CH3_LLI_CT	Current LLI task for channel #3	0x0000

Table 545. FDMA_CH4_CTRL_REG (0x5006_0400)

Bit	Mode	Symbol	Description	Reset
31	R/W	FDMA_CH4_D_AI	Destination address incremental enable for channel #4.	0x1
30	R/W	FDMA_CH4_D_PORT	Destination AHB master port select for channel #4. 0: AHB master 0 selected for destination transfer 1: AHB master 1 selected for destination transfer	0x1
29:28	R/W	FDMA_CH4_D_HSIZE	Destination data width for channel #4. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
27	R/W	FDMA_CH4_S_AI	Source address incremental enable for channel #4.	0x1
26	R/W	FDMA_CH4_S_PORT	Source AHB master port select for channel #4. 0: AHB master 0 selected for source transfer 1: AHB master 1 selected for source transfer	0x0
25:24	R/W	FDMA_CH4_S_HSIZE	Source data width for channel #4. 0: Byte (8 bits) 1: Halfword (16 bits) 2: Word (32 bits) 3: Reserved	0x2
23:20	R/W	FDMA_CH4_BST	Burst access size per block for channel #4. 0: 2^0 1: 2^1 2: 2^2 F: 2^15 (32K access)	0x0
19:0	R/W	FDMA_CH4_TTL	Total transfer length for channel #4. 0~6: Not supported 7: 8 bytes 8: 9 bytes Max transfer length = 1M bytes	0x00000

Table 546. FDMA_CH4_CTRL2_REG (0x5006_0404)

Bit	Mode	Symbol	Description	Reset
27	R/W	FDMA_CH4_LLI_EN	Next LLI enable for channel #4 (Reserved).	0x0
26:24	R/W	FDMA_CH4_NEXT_CH	Indicator for the next channel for channel #4. 0: Idle	0x0

Bit	Mode	Symbol	Description	Reset
			1: Channel #1 2: Channel #2 3: Channel #3 4: Channel #4	
23:21	R/W	FDMA_CH4_PROT	AHB bus protection for channel #4 (Reserved).	0x0
20	R/W	FDMA_CH4_IRQ_EN	Interrupt enable for channel #4.	0x0
19:16	R/W	FDMA_CH4_IDLE	Idle size per block for channel #4. 0: 0 1: 2^0 2: 2^1 F: 2^14 (16K idle cycles)	0x0
15:0	R/W	FDMA_CH4_CALLBACK	Callback index for channel #4	0x0000

Table 547. FDMA_CH4_SRC_A_REG (0x5006_0408)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH4_SRC_A	Source address for channel #4	32'd0

Table 548. FDMA_CH4_DST_A_REG (0x5006_040C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	FDMA_CH4_DST_A	Destination address for channel #4	32'd0

Table 549. FDMA_CH4_LLI_BA_REG (0x5006_0410)

Bit	Mode	Symbol	Description	Reset
31:2	R/W	FDMA_CH4_LLI_BA	Base address of lli for channel #4	30'd0
1:0	-	-	Reserved	0x0

Table 550. FDMA_CH4_LLI_TASK_NUM_REG (0x5006_0414)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	FDMA_CH4_LLI_CN	Number of LLI tasks to be processed in a continuous operation for channel #4	0x0000
15:0	R/W	FDMA_CH4_LLI_TN	Total number of LLI tasks for channel #4	0x0000

Table 551. FDMA_CH4_LLI_SI_REG (0x5006_0418)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	FDMA_CH4_LLI_SI	Starting index of LLI tasks for channel #4	0x0000

Table 552. FDMA_CH4_LLI_STS_REG (0x5006_0420)

Bit	Mode	Symbol	Description	Reset
19:16	R	FDMA_CH4_LLI_ST	Status of current LLI task for channel #4. [3]: 0 Reg, 1 Mem [2:0]: 0 Idle, 1 Set, 2 Run, 3 Done, 4 Wait	0x0
15:0	R	FDMA_CH4_LLI_CT	Current LLI task for channel #4	0x0000

10.17 SDIO Register

Table 553. SDIO registers

Address	Register	Description
0x5001_0000	-	-
0x5001_0004	-	-
0x5001_0008	SDIO_CIS_FN0_REG	ARM Programming the CIS Function 0 Address Register
0x5001_000C	SDIO_CIS_FN1_REG	ARM Programming the CIS Function 1 Address Register

Address	Register	Description
0x5001_0010	SDIO_CSA_REG	ARM Programming the CSA Address Register
0x5001_0014	SDIO_READ_REG	ARM Programming the Read Address Register
0x5001_0018	SDIO_WRITE_REG	ARM Programming the Write Address Register
0x5001_001C	SDIO_AHB_TRANSCOUNT_REG	AHB Transfer Count Register
0x5001_0020	SDIO_TRANSCOUNT_REG	Transfer Count Register
0x5001_0024	SDIO_CIA_REG	CIA Register
0x5001_0028	SDIO_PROG_REG	Program Register
0x5001_002C	SDIO_INT_STAT_REG	Interrupt Status and Clear Register
0x5001_0030	SDIO_INT_EN_REG	Interrupts Enable Register
0x5001_0034	SDIO_OCR_REG	OCR Register
0x5001_0038	-	-
0x5001_003C	SDIO_BURST_SUPP_REG	Burst Support Register
0x5001_0040	SDIO_SOFT_RESET_REG	Process to Soft Reset for All AHB Clock Domain Register
0x5001_0044	SDIO_AHB_BASE_ADDR_REG	AHB DMA Base Address Register
0x5001_0048	-	-
0x5001_004C	-	-

Table 554. SDIO_CIS_FN0_REG (0x5001_0008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	-	ARM programming the CIS function 0 address	32'h0000

Table 555. SDIO_CIS_FN1_REG (0x5001_000C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	-	ARM programming the CIS function 1 address	32'h0000

Table 556. SDIO_CSA_REG (0x5001_0010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	-	ARM programming the CSA address	32'h0000

Table 557. SDIO_READ_REG (0x5001_0014)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	-	ARM Programming the Read Address Register. The ARM processor writes the starting address of the read DMA (that is the starting address of the memory area from where the data must be taken for read data transfer). This is used for transferring data from ARM to SD host.	32'h0000

Table 558. SDIO_WRITE_REG (0x5001_0018)

Bit	Mode	Symbol	Description	Reset
31:0	R/W		ARM Programming the Write Address Register. The ARM processor writes the destination address of the write DMA (that is the address of the memory area where the data is to be written during a write data transfer to Function 1). This is used for transferring data from SD host to ARM.	32'h0000

Table 559. SDIO_AHB_TRANSCOUNT_REG (0x5001_001C)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R/W		AHB Transfer Count Register. This counter indicates how many bytes of data are available for reading in the ARM memory.	21'h0000

Table 560. SDIO_TRANSCOUNT_REG (0x5001_0020)

Bit	Mode	Symbol	Description	Reset
31:21	-	-	Reserved	-
20:0	R/W		The Arasan SDIO-AHB bridge writes the number of bytes transferred to ARM Processor during write transfer. This is programmed after the completion of Function 1 write data transfer.	21'h0000

Table 561. SDIO_CIA_REG (0x5001_0024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	-
27	R/W	SMPC	Support master power control. These bits tell the host that the card supports Master power control. 1 = Total card current may exceed 200 mA 0 = Total card current is less than 200 mA	1'b1
26	R/W	SHS	Support high speed 1 = High speed supported 0 = High speed not supported	1'b1
25	R/W	SPS	Function 1 supports high power	1'b1
24:17	R/W	EXT_IODC1	This is the extension of the standard I/O device code for function 1.	8'h00
16	R/W	CSA	AHB programs this bit to support for CSA for function 1. 1 = CSA is supported 0 = CSA is not supported	b'b1
15:12	R/W	IODC1	This value denotes the SDIO standard interface supported by this function (function 1). 0: No SDIO standard Interface supported by this function. You should specify the appropriate value based on their application.	4'h7
11:8	R/W	SD_REV	SD format revision. This 4-bit contains the version of the SD physical specification that this card supports. 0: SD Physical Specification 1.01 1: SD Physical Specification 1.10 2: SD Physical Specification 2.0	4'h2
7:4	R/W	SDIO_REV	SDIO specification revision number. This 4-bit contains the version of the SDIO specification that this card supports. 0: SDIO Specification 1.0 1: SDIO Specification 1.1 2: SDIO Specification 1.2 3: SDIO Specification 2.0	4'h3
3:0	R/W	CCCR_REV	CCCR Format Version number. This 4-bit contains the version of the CCCR and FBR format that this card supports. 0: CCCR/FBR Version 1.0 1: CCCR/FBR Version 1.1 2: CCCR/FBR Version 1.2	4'h2

Table 562. SDIO_PROG_REG (0x5001_0028)

Bit	Mode	Symbol	Description	Reset
31:11	-	-	Reserved	-
10	R/W	CARD_RDY	Power on reset is synchronously deasserted on SD clock domain. This bit is set to 1 after power on reset indicating that the card is ready to program.	1'b0
9	R/W	4BLS	This bit denotes that the SDIO card is a low-speed card and supports 4-bit data transfer.	1'b1
8	R/W	LSC	If this bit is set, it indicates that the SDIO card is a low-speed device. If this bit is clear the SDIO card is a full speed device.	1'b0

Bit	Mode	Symbol	Description	Reset
7	R/W	S4MI	This flag reports the SDIO card's ability to generate interrupts during a 4-bit multi block data transfer.	1'b1
6	R/W	SBS	This flag bit reports the card's ability to support the suspend/resume operations at the request of the Host. If this bit is set, all functions except 0 accept a request to suspend operations and resume under host control.	1'b1
5	R/W	SRW	This flag bit reports the card's ability to support the read wait control (RWC) operation.	1'b1
4	R/W	SMB	This flag bit reports the card's ability to execute CMD53 in Block mode.	1'b1
3	R/W	SDC	This flag bit reports the card's ability to execute CMD52 while data transfer is in progress.	1'b1
2	R/W	SCSI	Support continuous SPI interrupt	1'b1
1	R/W	FUN1_RDY	-	1'b0
0	R/W	FUNC_RDY	The ARM processor sets this bit to indicate that the function is ready.	1'b0

Table 563. SDIO_INT_STAT_REG (0x5001_002C)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4	R/W	RSTFUN1_N_INT	Asserted to inform the ARM, that fun 1 is disabled by the host. This is used for per function reset error recovery and this signal does not affect the flops inside the IP.	1'b0
3	R/W	RSTSOFT_N_INT	Asserted to inform the ARM, that controller receives cmd52 soft reset. Active low soft reset asserted only for one clock pulse in SD clock domain. On assertion, (except few flops which need to be reset only in pwr_on_rst_n) all the SD domain flops are Reset.	1'b0
2	R/W	RD_ERR	Set by the Arasan SDIO-AHB bridge when there is an error in function 1 read transaction. This bit is set to 1 when SD Host aborts the read transaction due to some transmission error (CRC mismatch). This bit is cleared when ARMS write 0 to this bit. ARM clear the read error Interrupt by writing 0 to this bit.	1'b0
1	R/W	RD_TRAN_OVR	Set by the Arasan SDIO-AHB bridge when read transaction is completed for function-1 data transfer. This bit is cleared when ARMS write 0 to this bit.	1'b0
0	R/W	WR_TRAM_OVR	Set by the Arasan SDIO-AHB bridge when write transaction is completed for function-1 data transfer. This bit is cleared when ARMS write 0 to this bit. Note: Until this bit is cleared, the AHB DMA engine is prevented from performing an AHB write access from a new cmd53 write. No valid data in FIFO is overwritten. ARM clear the Write over Interrupt by writing 0 to this bit.	1'b0

Table 564. SDIO_INT_EN_REG (0x5001_0030)

Bit	Mode	Symbol	Description	Reset
31:5	-	-	Reserved	-
4	R/W	RSTFUN1_N_INT_EN	Function 1 disable interrupt. 1 = Enable 0 = Disable	1'b0
3	R/W	RSTSOFT_N_INT_EN	Soft reset interrupt. 1 = Enable 0 = Disable	1'b0
2	R/W	RD_ERR_EN	Indicates that the read_error interrupt is enabled.	1'b0
1	R/W	RD_TRAN_OVR_EN	Indicates that the read_tran_over interrupt is enabled.	1'b0
0	R/W	WR_TRAM_OVR_EN	Indicates that the write_tran_over interrupt is enabled.	1'b0

Table 565. SDIO_OCR_REG (0x5001_0034)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	-
23:0	R/W	OCR	ARM Programming the OCR Register. Operational condition register is programmed by the ARM which is used to match with the operating voltage range of the host.	24'hFF_8000

Table 566. SDIO_BURST_SUPP_REG (0x5001_003C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	-
7:0	R/W	-	ARM Programming the Burst Support Register	8'h00

Table 567. SDIO_SOFT_RESET_REG (0x5001_0040)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
0	R/W	-	Process to soft reset for all AHB clock domain flops	1'b0

Table 568. SDIO_AHB_BASE_ADDR_REG (0x5001_0044)

Bit	Mode	Symbol	Description	Reset
31:1	-	-	Reserved	-
31:0	R/W		AHB DMA base address. 1: Be able to set with fn0 cmd53 2: Be able to set with fn1 cmd52 3: Be able to set with CPU write access	32'h0000

11. Application Schematics

11.1 Typical Application: QFN, 3.3 V Flash

Figure 58 shows the schematics for an application that uses the DA16200 in 3.3 V Flash mode.

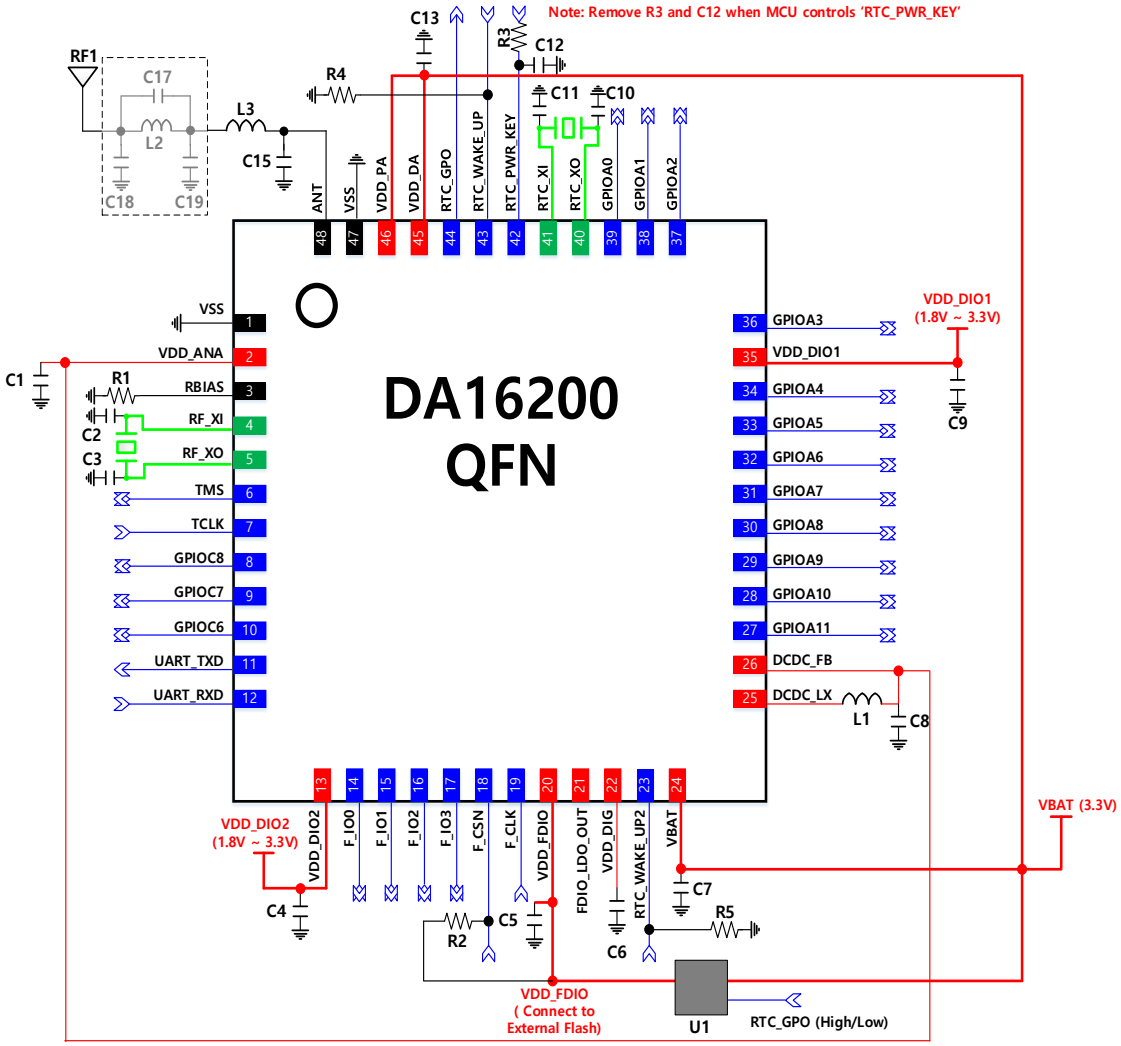

Figure 58. Typical application – QFN, 3.3 V flash

The power supply of the External Flash memory is the same as VDD_FDIO. VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls **RTC_PWR_KEY**.

Table 569 lists the components for an application that uses the DA16200 QFN in 3.3 V Flash mode.

Table 569. Components for DA16200 QFN, 3.3 V flash mode

Quantity	Part reference	Value	Description
1	R1	30 kΩ (1%)	-
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
5	C1, C4, C5, C7, C9	1 µF	-
1	C6	470 nF	-

Quantity	Part reference	Value	Description
1	R2	10 kΩ	-
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	-
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 µF	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1 µF. See Section 6.1 for more information.
2	R4, R5	4.7 kΩ	-
1	C13	4.7 µF	-
1	C15	DNI	Optional
1	L3	2.2 nH	-
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional
1	U1	-	Optional, load switch for disconnecting VBAT for VDD_FDIO.

(Use any 5% tolerance)

Table 570. I/O power domain

I/O power domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

11.2 Typical Application: QFN, 1.8 V Flash

Figure 59 shows the schematics for an application that uses the DA16200 QFN in 1.8 V Flash mode.

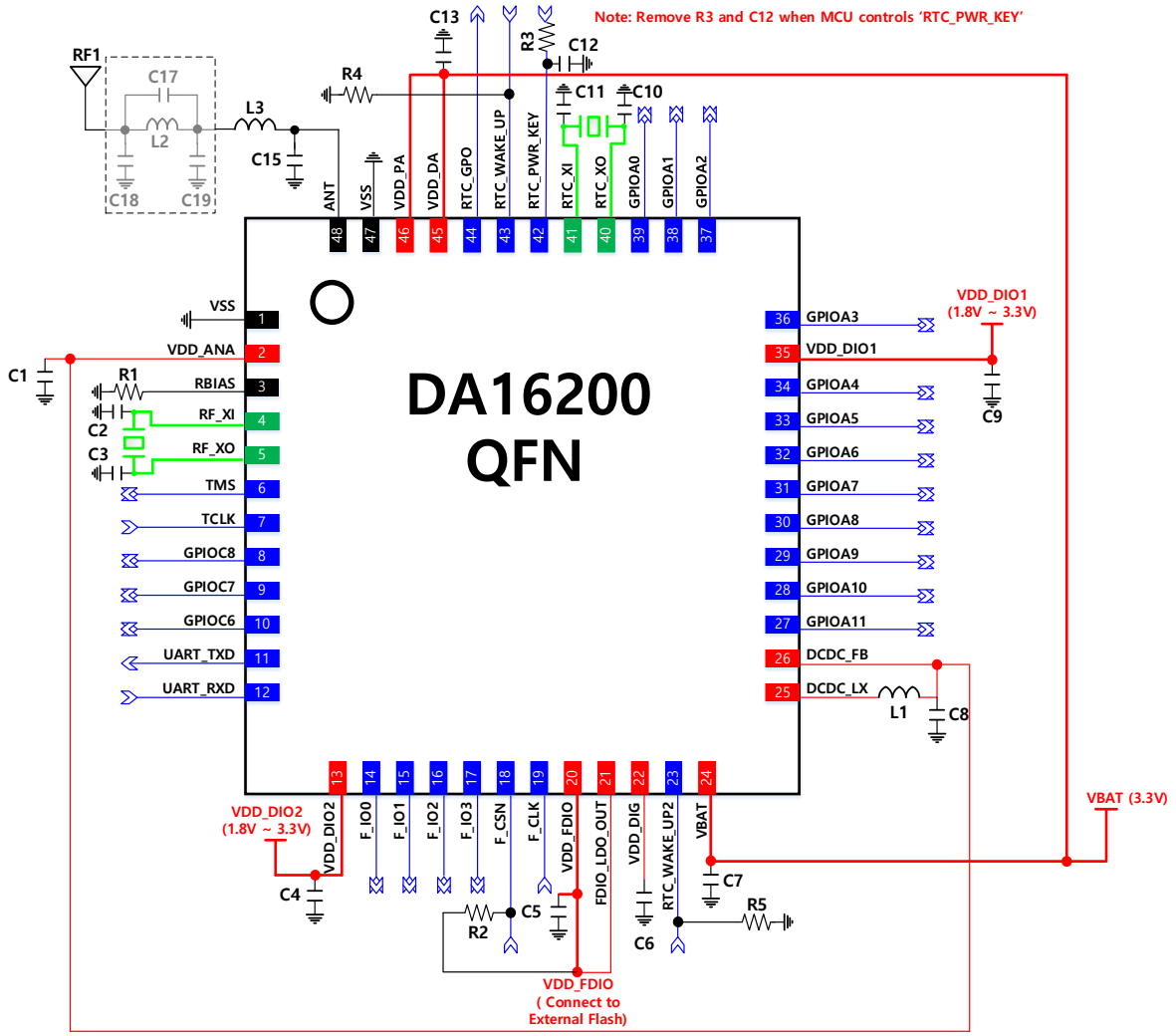

Figure 59. Typical application – QFN, 1.8 V flash

The power supply of the External Flash memory is the same as VDD_FDIO. VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls RTC_PWR_KEY.

Table 571 lists the components for an application that uses the DA16200 QFN in 1.8 V Flash mode.

Table 571. Component for DA16200 QFN, 1.8 V flash mode

Quantity	Part reference	Value	Description
1	R1	30 kΩ (1%)	-
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition. Part: FCX-07L
5	C1, C4, C5, C7, C9	1 µF	-
1	C6	470 nF	-
1	R2	10 kΩ	-
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	-
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control RTC_PWR_KEY.

Quantity	Part reference	Value	Description
			This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. For detail information, see Section 6.1.
1	C12	1 µF	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1 µF. For detail information, see Section 6.1.
2	R4, R5	4.7 kΩ	-
1	C13	4.7 µF	-
1	C15	DNI	Optional
1	L3	2.2 nH	-
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5% tolerance)

Table 572. I/O power domain

I/O power domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO	F_IO[3:0], F_CSN, F_CLK

11.3 Typical Application: fcCSP, 1.8 V Flash Normal Power Mode

Figure 60 shows the schematics for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

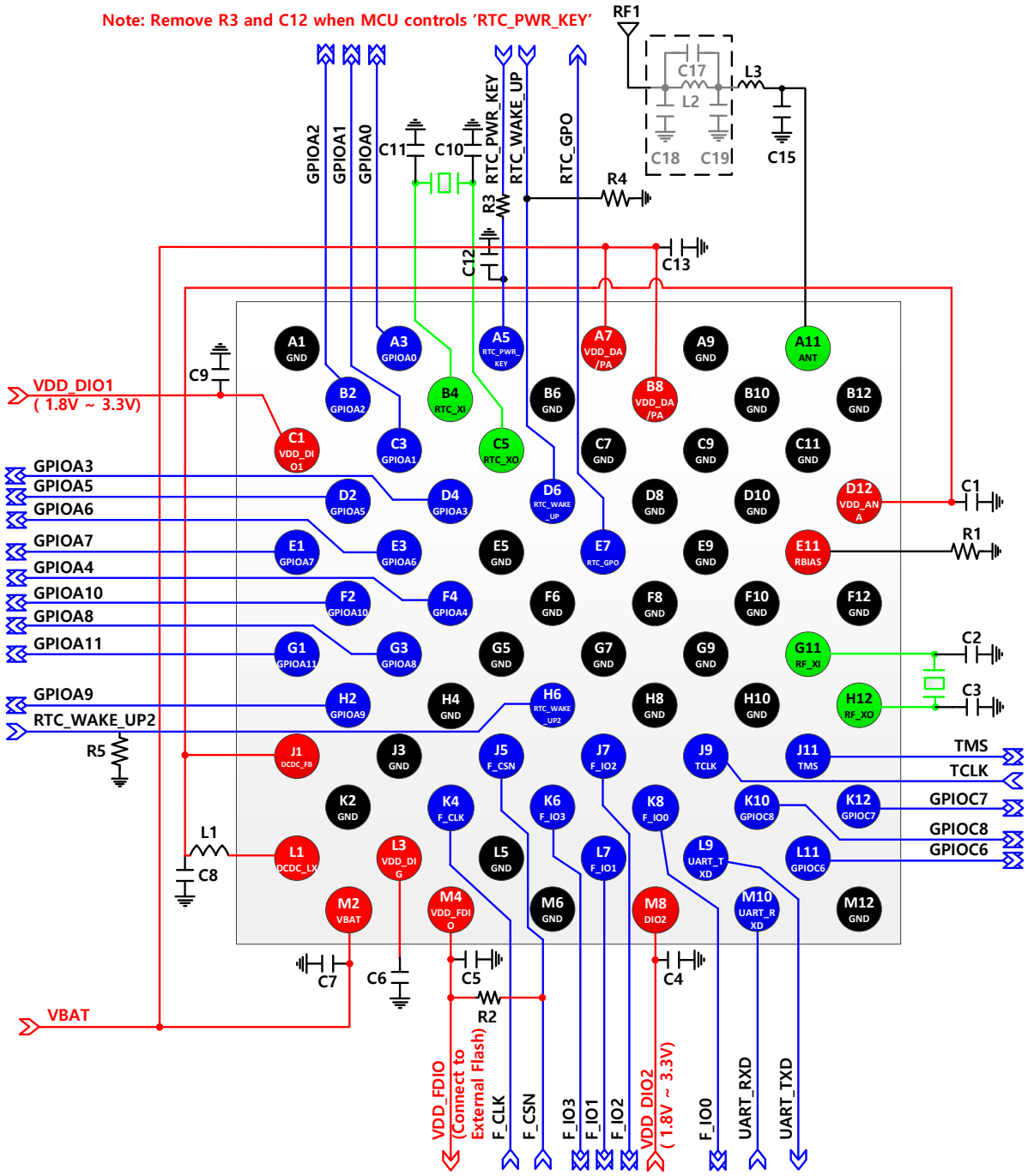

Figure 60. Typical application – fcCSP, 1.8 V flash, normal power mode

The power supply of the External Flash memory is the same as VDD_FDIO. 3.3 V External Flash memory can also be used in this Application. A switch must be used to prevent the addition of flash memory current consumption to the DA16200. Contact Customer support team for details.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls **RTC_PWR_KEY**.

Table 573 lists the components for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

Table 573. Component for DA16200 fcCSP, 1.8 V flash, normal power mode

Quantity	Part reference	Value	Description
1	R1	30 kΩ (1%)	-
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition.

Quantity	Part reference	Value	Description
			Part: FCX-07L
1	C6	470 nF	-
4	C1, C4, C5, C9	1 µF	-
1	C7	2.2 µF	-
1	R2	10 kΩ	-
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	-
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 µF	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1 µF. See Section 6.1 for more information.
1	R4, R5	4.7 kΩ	-
1	C13	4.7 µF	-
1	C15	0.5 pF	Normal power mode
1	L3	2.7 nH	Normal power mode
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5% tolerance)

Table 574. I/O power domain

I/O power domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO (Note 1)	F_IO[3:0], F_CSN, F_CLK

Note 1 VDD_FDIO is internally connected to FDIO_LDO_OUT.

11.4 Typical Application: fcCSP, 1.8 V Flash Low Power Mode

Figure 61 shows the schematics for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

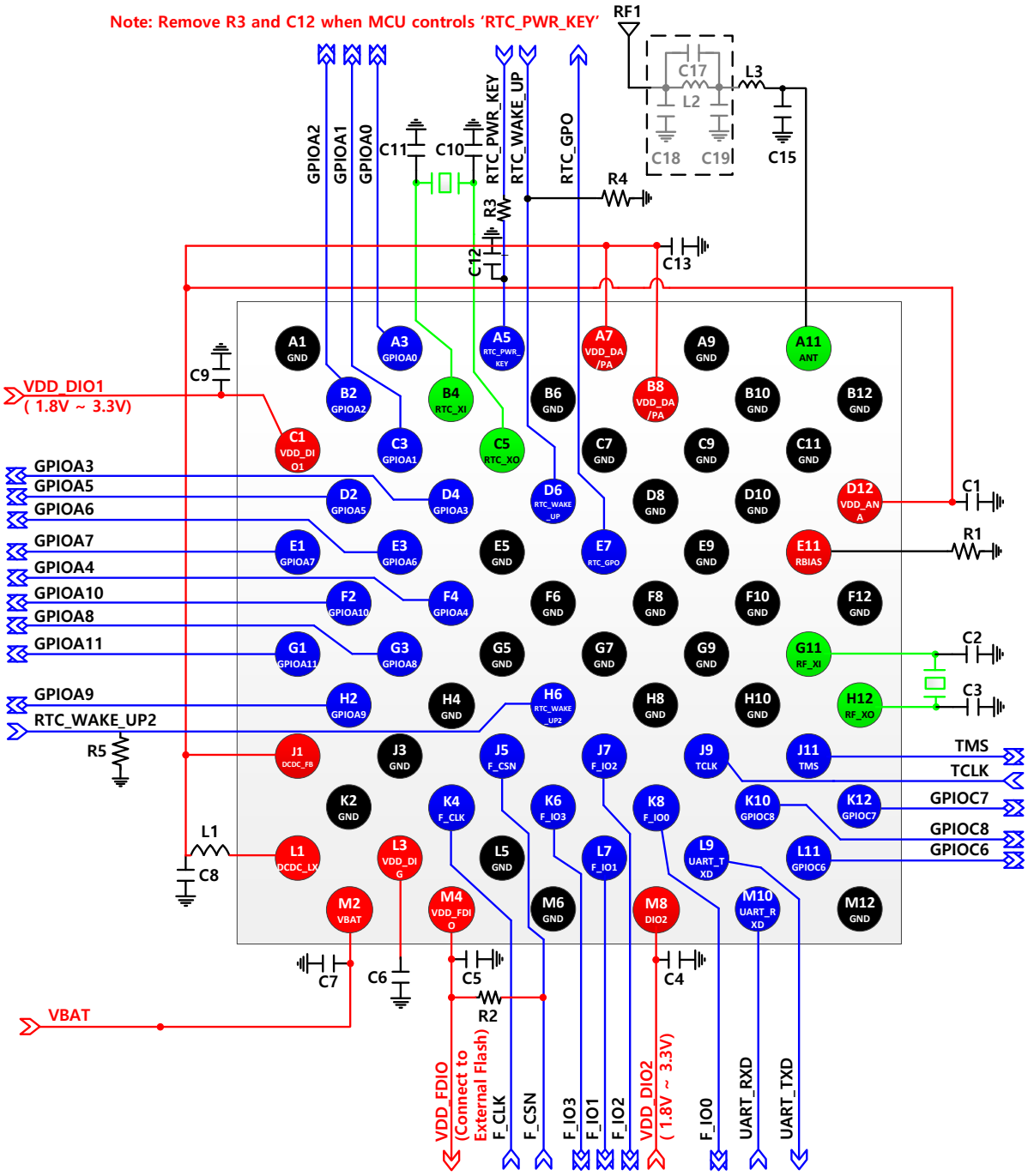

Figure 61. Typical application – fcCSP, 1.8 V flash, low power mode

The power supply of the External Flash memory is the same as VDD_FDIO. 3.3 V External Flash memory can also be used in this Application. A switch must be used to prevent the addition of flash memory current consumption to the DA16200. Contact Customer support team for details.

VDD_DIO1/2 can be connected to the same power source as the external component that is connected to the DA16200. Remove R3 and C12 when an MCU controls **RTC_PWR_KEY**. Table 575 lists the components for an application that uses the DA16200 fcCSP in 1.8 V Flash mode.

Table 575. Component for DA16200 fcCSP, 1.8 V flash, low power mode

Quantity	Part reference	Value	Description
1	R1	30 kΩ (1%)	-
2	C2, C3	1.2 pF	These values may be changed by crystal component characteristics and board condition.

Quantity	Part reference	Value	Description
			Part: FCX-07L
1	C6	470 nF	-
4	C1, C4, C5, C9	1 µF	-
1	C7	2.2 µF	-
1	R2	10 kΩ	-
1	L1	4.7 µH	LQM21PN4R7MGH (Murata)
1	C8	10 µF	-
2	C10, C11	15 pF	These values may be changed by crystal component characteristics and board condition. Part: TFX-03
1	R3	470 kΩ	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. See Section 6.1 for more information.
1	C12	1 µF	Remove when MCU control RTC_PWR_KEY. This value should be chosen by customer application to achieve the enough delay time depending on the power-on time of VBAT. Not to exceed 1 µF. See Section 6.1 for more information.
1	R4, R5	4.7 kΩ	-
1	C13	4.7 µF	-
1	C15	DNI	Low power mode
1	L3	2.2 nH	Low power mode
1	C17	0.5 pF	Optional
2	C18, C19	1 pF	Optional
1	L2	1.8 nH	Optional

(Use any 5% tolerance)

Table 576. I/O power domain

I/O power domain	
VDD_DIO1	GPIOA[11:0]
VDD_DIO2	GPIOC[8:6], TMS, TCLK, UART_TXD, UART_RXD
VDD_FDIO (Note 1)	F_IO[3:0], F_CSN, F_CLK

Note 1 VDD_FDIO is internally connected to FDIO_LDO_OUT.

12. Package Information

12.1 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) rating of an IC determines its floor life before board mounting after the dry pack packing has been opened assuming an environment with a constant 30°C and 60% relative humidity. QFN and fcCSP packages are qualified for MSL 3.

Table 577. Moisture sensitivity level

Moisture sensitivity level (MSL)	Floor life time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85% RH

12.2 Top View: QFN and fcCSP

Figure 62. DA16200 48-pin QFN package

Figure 63. DA16200 72-pin fcCSP package

12.3 Dimension: 48-Pin QFN

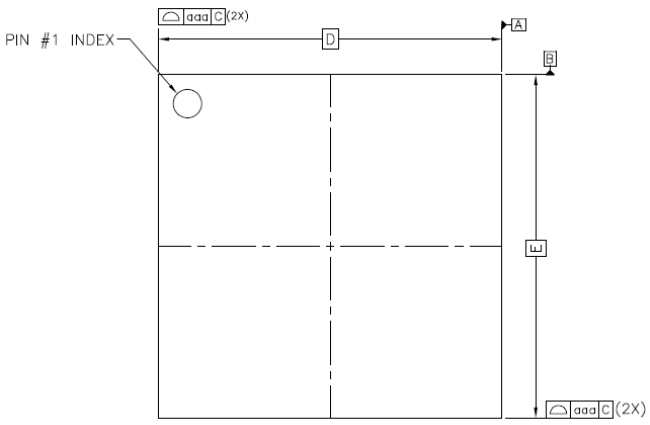

Figure 64. DA16200 48-pin QFN (top view)

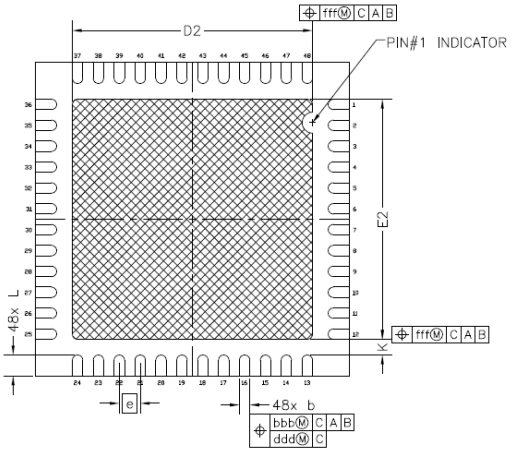

Figure 65. DA16200 48-pin QFN (bottom view)

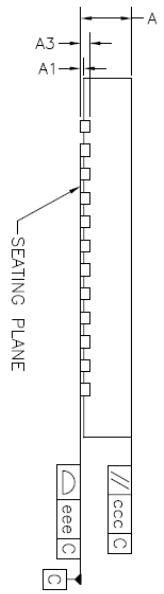

Figure 66. DA16200 48-pin QFN (side view)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D		6.00 BSC	
E		6.00 BSC	
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20		
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 67. DA16200 48-pin QFN package dimension

12.4 Dimension: 72-Pin fcCSP

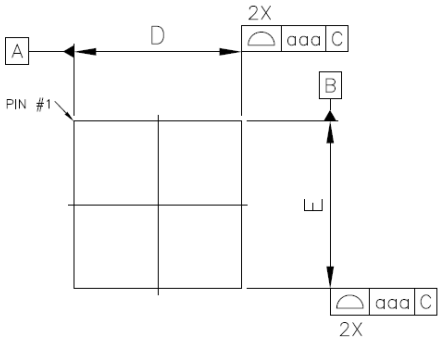

Figure 68. DA16200 72-pin fcCSP (top view)

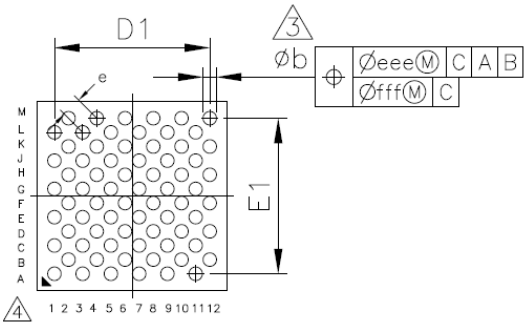

Figure 69. DA16200 72-pin fcSCP (bottom view)

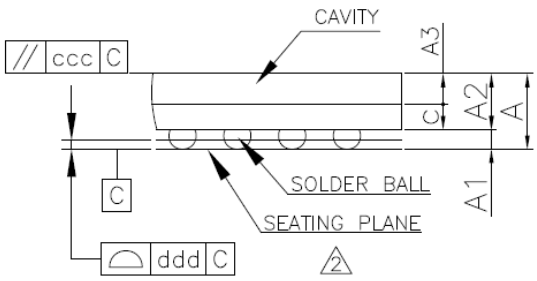

Figure 70. DA16200 72-pin (side view)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.54	0.61	0.68
A1	0.11	0.16	0.21
A2	0.40	0.45	0.50
A3	0.25	0.28	0.31
c	0.14	0.17	0.20
D	3.73	3.80	3.87
E	3.73	3.80	3.87
D1	---	3.11	---
E1	---	3.11	---
e	---	0.40	---
b	0.22	0.27	0.32
aaa	0.07		
ccc	0.10		
ddd	0.08		
eee	0.10		
fff	0.05		
MD/ME	12/12		

Figure 71. DA16200 72-pin fcCSP package dimension

12.5 Land Pattern: 48-Pin QFN

Unit: Millimeters (mm)

Pad: Metal mask = 1:1

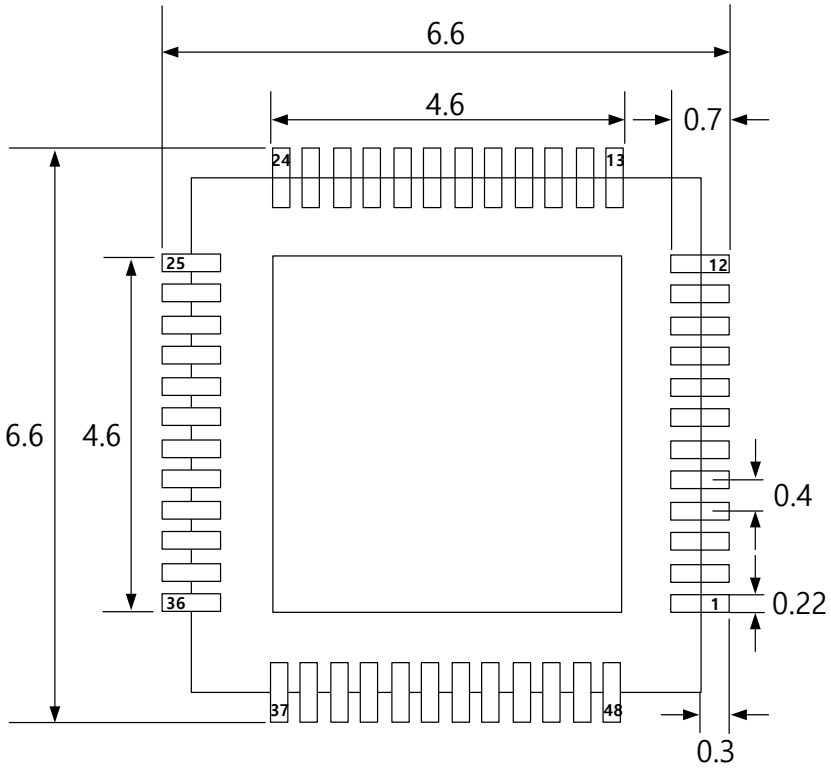

Figure 72. DA16200 48-pin QFN land pattern

12.6 Land Pattern: 72-Pin fcCSP

Unit: Millimeters (mm)

Pad: Metal mask = 1:1

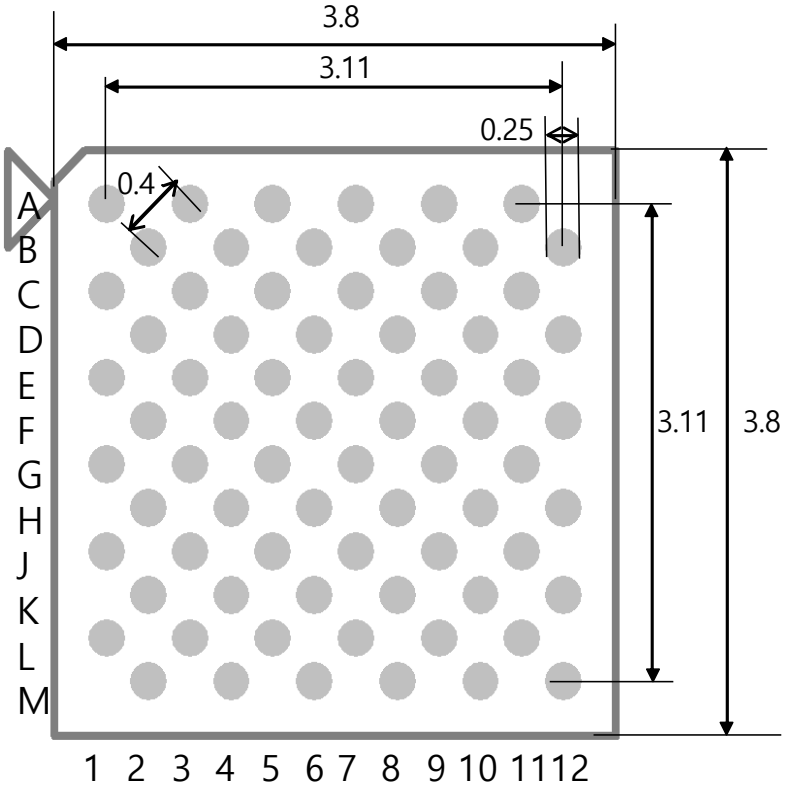

Figure 73. DA16200 72-pin fcCSP land pattern

12.7 Soldering Information

12.7.1 Recommended Condition for Reflow Soldering

Figure 74 shows the typical process flow to install surface mount packages to the PCB.

The reflow profile depends on the solder paste being used and the recommendations from the paste manufacturer should be followed to determine the proper reflow profile. Figure 74 shows a typical reflow profile when a no-clean paste is used. Oven time above liquidus (260 °C for lead-free solder) is 30 to 60 seconds.

Since solder joints are not exposed in QFN packages, any retouching is not possible and the whole package has to be removed if the surface mount process results in shorts or opens. Furthermore, reworking QFN packages can be a challenge due to their small size. In most applications, QFNs are installed on smaller, thinner, and denser PCBs, and introduces further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following steps only provide a guideline and a starting point for the development of a successful rework process for the QFN packages.

The rework process involves the following steps:

- Component removal
- Site redress
- Solder paste application
- Component placement
- Component attachment.

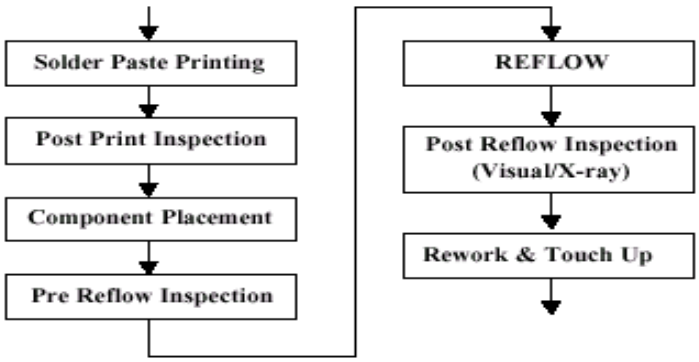

Figure 74. Typical PCB mounting process

Table 578. Typical reflow profile (Lead free): J-STD-020C

Profile feature	Lead free SMD
Average ramp up rate (Ts_{max} to T_p)	3 °C/s Max.
Preheat	
● Temperature Min (Ts_{min}) ● Temperature Max (Ts_{max}) ● Time (Ts_{max} to Ts_{min})	● 150 °C ● 200 °C ● 60 to 180 seconds
Time maintained above	
● Temperature (T_L) ● Time (t_L)	● 217 °C ● 60 to 150 seconds
Peak/Classification temperature (T_p)	260 °C
Time within 5 °C of peak temperature (tp)	20 to 40 seconds
Ramp down rate	6 °C/s Max.
Time from 25 °C to peak temperature	8 minutes Max.

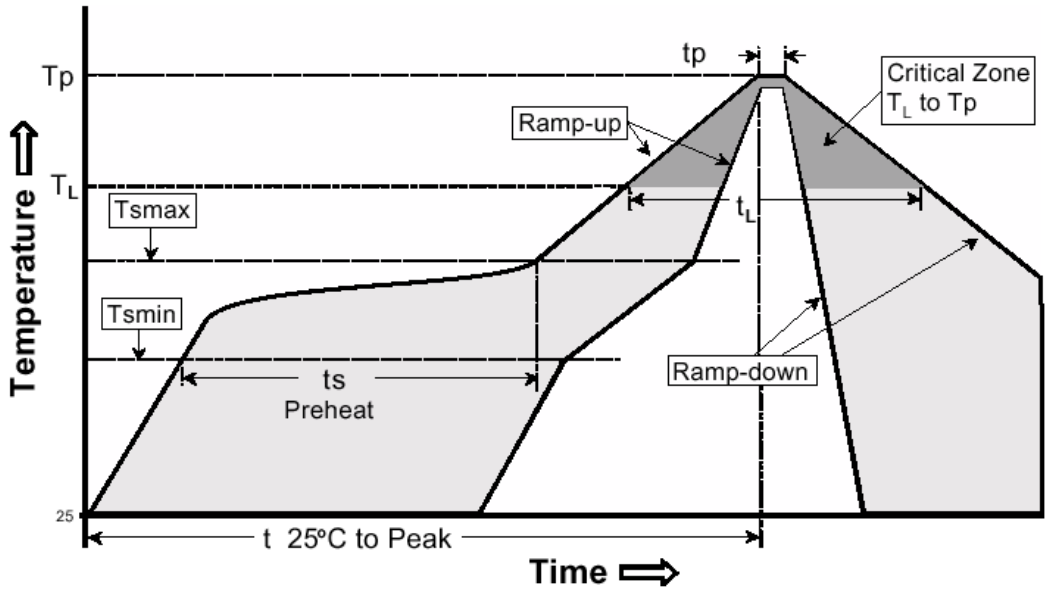

Figure 75. Reflow condition

13. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, visit the Renesas website (https://www.renesas.com/kr/en/products/wireless-connectivity/wi-fi/low-power-wi-fi) or contact your local sales representative.

Table 579. Ordering information (Samples)

Part number	Package	Size (mm)	Shipment form	Pack quantity
DA16200-00000A32	QFN48	6 × 6	Reel	100/500
DA16200-00001A32	QFN48	6 × 6	Reel	100/500
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	100/500
DA16200-00001F22	fcCSP72	3.8 × 3.8	Reel	100/500

Table 580. Ordering information (Production)

Part number	Package	Size (mm)	Shipment form	Pack quantity
DA16200-00000A32	QFN48	6 × 6	Reel	3000
DA16200-00001A32	QFN48	6 × 6	Reel	3000
DA16200-00000F22	fcCSP72	3.8 × 3.8	Reel	4000
DA16200-00001F22	fcCSP72	3.8 × 3.8	Reel	4000

Part number legend:

DA16200-RRXXXYYZ

RR: Chip revision number

YY: package code (A3: QFN48, F2: fcCSP72)

Z: packing method (1: Tray, 2: Reel, A: Mini-Reel)

14. Revision History

Revision	Date	Description
3.9	Oct 30, 2024	● Removed Wi-Fi Direct and Wi-Fi Mesh ● 10.1 GPIO Register: Changed register name ● 10.3 I2S Register: Changed register name ● 10.4 SDeMMC Register: Changed register name ● 10.5 SPI and I2C Register: Added 2 registers ● 10.6 External Interrupt Control Register: Changed register name ● 10.8 ADC Register: Changed register name ● 10.15 QSPI Register: Changed register name and added register table ● 10.17 SDIO Register: Changed register name and added register table ● Added registers of UART_PE_PS and JTAG_PE_PS in Table 62 ● Added descriptions of UART_PE_PS and JTAG_PE_PS in Table 65 and Table 66
3.8	Oct 27, 2023	● Added I2C register map ● Added RTC registers
3.7	July 12, 2023	● Removed Variant 001 details ● Updated the reference section ● Added Register Maps: ○ ADC Register ○ CRC Register ○ PWM Register ○ kDMA Register ○ SYS_CLOCK Register ○ Watchdog Register ○ Timer Register ● Updated Table 3. DA16200 pin multiplexing and Table 4. DA 16600 pin multiplexing (Continued) ● Updated Figure 3. Software block diagram and Section 6.3.3 Sleep Mode 3 Changed the format: Figures 58/59 to Tables 131/132
3.6	Jan 4, 2023	● Section 7.5.1 Introduction, Section 9.8.4 Sensor Wake-up, Table 29. RTC pin description: added details for Sleep modes ● Updated operating temperature in Key Features list ● Updated Table 5. Absolute maximum ratings to add storage temperature range and adjusted min/max voltages
3.5	June 13, 2022	● Section 7.3.1.2 SRAM: Corrected the internal SRAM address range ● Section 7.4.2 Retention I/O Function: Added note about Sleep mode 2 and 3 for retention I/O ● Section 9.3 SPI Slave and Section 10.5 SPI and I2C Register: Added note about SPI slave half-duplex and clock speed calculation ● Table 33. Hardware accelerated crypto algorithms in DA16200: Changed to Chacha20 and Poly1305 ● Table 53. DC specification: Removed Input Tolerance
3.4	Jan 17, 2022	● Section 4.3 Pin multiplexing: Updated pinout multiplexing ● Section 5.8 Clock electrical characteristics: Updated clock electrical characteristics ● Section 9.4 SDIO and Figure 32. SDIO pull-up resistor: Added SDIO interface needs pull-up resistors description ● Section 9.5.3 Interface Pull-up: Added I2C interface pull-up ● Section 9.12 Debug Interface and Table 61. JTAG pin configuration: Updated SWD part

Revision	Date	Description
		● Sections 11.3 Typical Application: fcCSP, 1.8 V Flash Normal Power Mode and 11.4 Typical Application: fcCSP, 1.8 V Flash Low Power Mode: Updated descriptions ● Update to the operating temperature range ● Updates to for variant 001. (OTP Size, Bluetooth Coex, BOR registers) ● Table 9. DC parameters for RTC block, 3.3 V VBAT: Updated the guaranteed logic high level V_{IH} to 2.3 V
3.3	Feb 3, 2021	● Table 1. Pin description: Updated pinout description ● Section 6.1 Power on Sequence: Added note for power on sequence and updated Table 26. Power on sequence timing requirements and Figure 11. Power on sequence ● Section 10 Applications Schematic: Updated RC delay description (Table 61, Table 63, Table 65, Table 67 and Figure 56, Figure 57, Figure 58, and Figure 59 are updated)
3.2	Sep 28, 2020	● Section 6.3 Low Power Operation Mode: Updated Sleep mode description ● Removed F_xx pins in Interface Parts ● Section 4.3 Pin Multiplexing (Table 3): Updated pin multiplexing ● Section 9.8 Timing Diagram (Table 52) Updated ADC reference voltage ● Section 9.5.1 I2C Master and 9.5.2 I2C Slave: Updated I2C speed description ● Table 43. I2C master timing parameters and Table 45. I2C slave timing parameters: Updated I2C interface ● Section 9.7.1 Block Diagram and 9.7.2 I2S Clock Scheme: Added I2S description, block diagram, and clock scheme ● Table 52. DC specification: Swapped SNDR and SNR values
3.1	July 3, 2020	● Section 3 Block Diagram: Modified description to network subsystem layer ● Figure 2. Hardware block diagram modified ● Table 1. Pin description: Reset state changed to initial state ● Table 3. DA16200 pin multiplexing: Updated pin multiplexing ● Table 5. Recommended operating conditions: Updated FDIO_LDO_OUT value ● Section 5.3 Electrical Characteristics: Updated electrical characteristics ● Table 14. WLAN transmitter characteristics - QFN: Updated fcCSP TX min/max values ● Section 5.5 Current Consumption: Updated current consumption values ● Section 6.2 Power Management Unit: Added descriptions and updated block diagram ● Section 6.3 Low Power Operation Mode: Updated Sleep mode description ● Table 28. RTC pin description: Updated RTC_PWR_KEY description and removed one sentence which leads to misunderstanding ● Table 43. I2C master timing parameters and Table 45. I2C slave timing parameters: Updated I2C speed ● Section 9.9.1 Antenna Switching Diversity: Added diversity description and Figure 46. Antenna switching timing diagram ● Section 9.10.3 Baud Rate: Added UART baud rate description ● Section 10.1 Typical Appliaction: QFN, 3.3 V Flash and Section 10.2 Typical Application: QFN, 1.8 V Flash: Updated QFN application schematic and descriptions ● Section 10.3 Typical Application: fcCSP, 1.8 V Flash Normal Power Mode and 10.4 Typical Application: fcCSP, 1.8 V Flash Low Power Mode: Updated fcCSP application schematic and descriptions and added note about I/O power domain ● Updated descriptions about Reach and RoHS Compliance
3.0	Mar 26, 2020	Final release
2.9	Feb 11, 2020	● Details added to Feature and Wi-Fi Alliance certification

Revision	Date	Description
		● Section 5.4.1 WLAN Receiver Characteristics and 5.4.2 WLAN Transmitter Characteristics: measurement condition CH1 added ● Section 9.10.1 RS-232: added ● Section 9.10.3 Hardware Flow Control: added ● Section 9.10.4 Interrupts: added ● Table 3. Pin multiplexing: updated ● Section 11.1 Moisture Sensitivity Level (MSL): added ● Figure 54. DA16200 72-pin fcCSP package: added ● Application circuit (QFN/fcCSP) BOM changed ● Feature deleted: DPD function support ● RX and TX min/max values added for the QFN package (Table 12. WLAN receiver characteristics - QFN and Table 14. WLAN transmitter characteristics - QFN) ● RX and TX min/max values added for the fcCSP package (Table 13. WLAN receiver characteristics - fcCSP and Table 15. WLAN transmitter characteristics – fcCSP (Normal power mode)) ● Table 17. Current consumption in active state - QFN and Table 20. Current consumption in low power operation: updated ● Table 21. QFN package and Table 22. fcCSP package: ESD ratings added for the QFN and fcCSP packages
2.3	Sept 05, 2019	● Pin name "RTC_SEN_OUT" changed to "RTC_GPO" ● Pull-down resistor added in Figure 50, Figure 51, and Figure 52 ● QFN48 package "RTC_WAKE_UP" and "RTC_WAKE_UP2" ● fcCSP72 package "RTC_WAKE_UP" ● Updated Ordering information sample and production pack quantity ● Application circuit in QFN and fcCSP package revised ● RTC_WAKE_UP pull-down resistor added
2.2	Aug 12, 2019	● Figure 71. DA16200 72-Pin fcCSP Land Pattern added ● AC characteristics and current consumption of fcCSP data updated ● Ordering information added
2.1	July 30, 2019	● Added "3.8 mm × 3.8 mm, 0.4 mm pitch, 72-Pin, fcCSP" in package type in key features ● Added Figure 5, Figure 8, and Figure 10 ● Added pin numbers for fcCSP package in Table 1, Table 28, Table 34, Table 38, Table 40, Table 42, Table 44, Table 46, Table 48, Table 53, Table 56, and Table 60 ● Added “GPIOC6~GPIOC8, TMS/TCLK, and TXD/RXD” in the description of Pin13/M8 in Table 1 ● Added "GPIOA0~GPIOA11" in the description of Pin35/C1 in Table 1 ● Added “fcCSP GND Pin A1, A9, B6, B10, B12, C7, C9, C11, D8, D10, F6, F8, F10, F12, G5, G7, G9, H4, H8, H10, J3, K2, L5, M6, M12, E5” in Table 1 ● In Table 3, SPI master contents updated ● Added information on fcCSP pins in section 5.1 and 5.2 ● Added Table 13, Table 15, and Table 18 ● Added section 10.3 ● Updated section 11.1 to include information on fcCSP ● Added section 11.4 ● Changed the caption of Table 27 to "OTP Map"
2.0	July 03, 2019	Preliminary datasheet

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