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## High-Performance, 13 A/20 A Peak, DC-DC Converter

### General Description

The DA9142 is a high efficiency, 13 A continuous and 20 A peak, dual-phase, DC-DC stepdown converter (buck). It is also available as fully AEC-Q100 qualified.

With remote sensing, the DA9142 improves output voltage regulation at the point of load.

Fully integrated switching FETs means no external FETs or Schottky diodes are needed.

A programmable soft startup can be enabled, which limits the inrush current from the input node and secures a slope-controlled rail activation.

The dynamic voltage control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load, via either a direct register write using the communication interface (I<sup>2</sup>C compatible) or with a programmable input pin.

A configurable GPI allows multiple I<sup>2</sup>C address selection for multiple instances of DA9142 in the same application.

DA9142 has integrated over-temperature and over-current protection for increased system reliability, without the need for external sensing components.

### Key Features

- 2.8 V to 5.5 V input voltage
- 0.5 V to 1.3 V output voltage
- Up to 20 A peak output current, 13 A continuous output current
- 4 MHz nominal switching frequency
- Dual-phase operation
- 110 nH inductor per phase
- 110  $\mu$ F output capacitor
- $\pm 1$  % output voltage accuracy (static)
- $\pm 5$  % load transient
- I<sup>2</sup>C-compatible interface (FM+)
- Programmable GPIOs
- Programmable soft startup
- Voltage, current, and temperature supervision
- 60 FC-BGA 4.5 mm x 7 mm (0.65 mm pitch)
- 130 mm<sup>2</sup> total solution area
- Automotive AEC-Q100 qualified also available

### Applications

- Navigation systems
- Telematics
- AI engines
- Automotive infotainment
- Advanced driver assistance systems (ADAS)
- SiPP modules

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**High-Performance, 13 A/20 A Peak, DC-DC Converter****1 Terms and Definitions**

CPU	Central processing unit
DDR	Dual data rate
DVC	Dynamic voltage control
FET	Field effect transistor
FM+	Fast mode plus
GPI	General purpose input
GPIO	General purpose input/output
GPU	Graphics processing unit
IC	Integrated circuit
OTP	One time programmable
PCB	Printed circuit board
SCL	Serial clock
SDA	Serial data
SIPP	Single in-line pin package

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2 Block Diagram

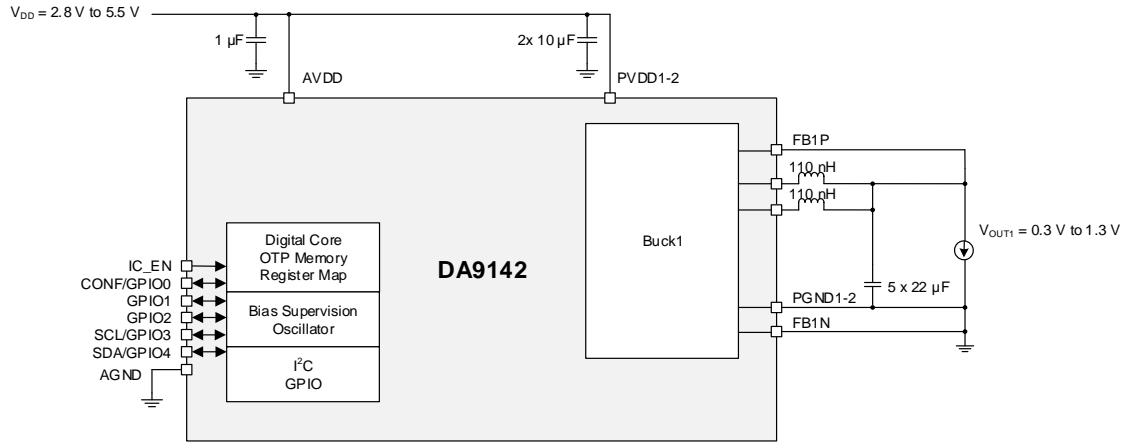
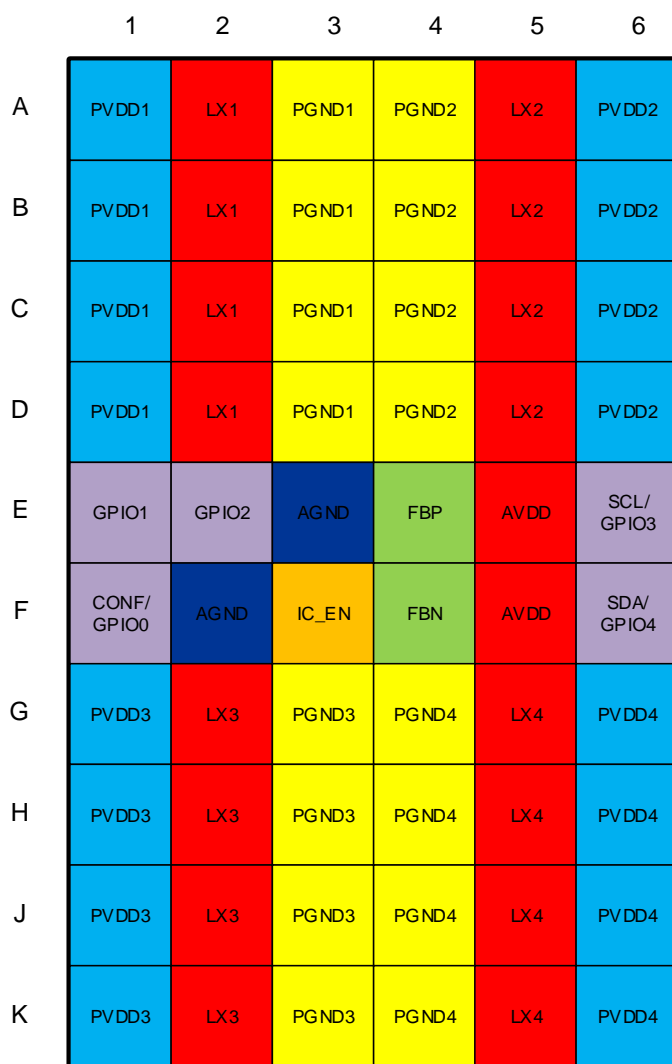


Figure 1: Block Diagram

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### 3 Pinout



Top view

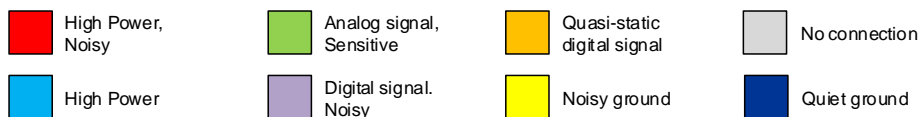


Figure 2: Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Drive (mA)	Description
A1, B1, C1, D1	PVDD1	PWR	10000	Supply voltage for buck power stage, decouple with 10 $\mu$ F and connect to same source as AVDD
A2, B2, C2, D2	LX1	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX1 and output capacitor
A3, B3, C3, D3	PGND1	GND	10000	Buck power stage GND

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Pin #	Pin Name	Type (Table 2)	Drive (mA)	Description
A4, B4, C4, D4	PGND2	GND	10000	Buck power stage GND
A5, B5, C5, D5	LX2	AIO	10000	Switch node of buck, connect a 100 nH inductor between LX2 and output capacitor
A6, B6, C6, D6	PVDD2	PWR	10000	Supply voltage for buck power stage, decouple with 10 $\mu$ F and connect to same source as AVDD
E1	GPIO1	DIO	10	General purpose I/O
E2	GPIO2	DIO	10	General purpose I/O
E3, F2	AGND	GND	10	Analog control and auxiliary circuitry GND
E4	FBP	AI	10	Buck positive node of differential voltage feedback, connect to VOUT1 at point of load
E5, F5	AVDD	PWR	10	Supply rail for analog control circuitry, decouple with 1 $\mu$ F and connect to same source as PVDD
E6	SCL/GPIO3	DIO	15	I <sup>2</sup> C clock or general purpose I/O
F1	CONF/GPIO0	AI/DIO	10	Chip configuration or general purpose I/O
F3	IC_EN	AI	10	Powers up I <sup>2</sup> C control interface and auxiliary circuitry (including bandgap, oscillator, and references)
F4	FBN	AI	10	Buck negative node of differential voltage feedback, connect to GND at point of load
F6	SDA/GPIO4	DIO	15	I <sup>2</sup> C data or general purpose I/O
G1, H1, J1, K1	PVDD3	PWR	10000	Supply voltage for buck power stage, connect to same source as AVDD
G2, H2, J2, K2	LX3	AIO	0	Do Not Connect
G3, H3, J3, K3	PGND3	GND	10000	Buck power stage VSS rail
G4, H4, J4, K4	PGND4	GND	10000	Buck power stage VSS rail
G5, H5, J5, K5	LX4	AIO	0	Do Not Connect
G6, H6, J6, K6	PVDD4	PWR	10000	Supply voltage for buck power stage, connect to same source as AVDD

**Table 2: Pin Type Definition**

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power	GND	Ground



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### 4 Characteristics

#### 4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 3: Absolute Maximum Ratings**

Parameter	Description	Conditions	Min	Max	Unit
T <sub>STG</sub>	Storage temperature		-65	150	°C
T <sub>J</sub>	Junction temperature		-40	150	°C
V <sub>SYS</sub>	System supply voltage		-0.3	6.0	V
V <sub>PIN</sub>	Voltage on pins		-0.3	6.0	V

#### 4.2 Electrostatic Discharge Ratings

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 4: Electrostatic Discharge Ratings**

Parameter	Description	Conditions	Value	Unit
ESD <sub>HBM</sub>	Maximum ESD protection	Human body model (HBM) All exposed pins	2	kV
ESD <sub>CDM</sub>	Maximum ESD protection	Charged device model (CDM)	500 (Note 1)	V

**Note 1** Increased to 750 V for corner balls.

#### 4.3 Recommended Operating Conditions

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 5: Recommended Operating Conditions**

Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>SYS</sub>	System supply voltage		2.8		5.5	V
V <sub>PIN</sub>	Voltage on pins		-0.3		V <sub>SYS</sub> + 0.3	V
T <sub>J</sub>	Junction temperature		-40		150	°C
T <sub>A</sub>	Ambient temperature		-40		125	°C

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### 4.4 Thermal Characteristics

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 6: Package Ratings**

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\theta_{JA}$	Thermal resistance junction to ambient	No heatsink <a href="#">Note 1</a>		16.4		°C/W
		With heatsink <a href="#">Note 2</a>		9.6		°C/W
$\theta_{JB}$	Thermal resistance junction to board	<a href="#">Note 1</a>		9.2		°C/W
$\theta_{JC}$	Thermal resistance junction to case	<a href="#">Note 1</a>		7.0		°C/W
$P_D$	Maximum power dissipation	No heatsink Derating factor above $T_A = 85^\circ\text{C}$ : $60.9 \text{ mW}/^\circ\text{C}$ ( $1/\theta_{JA}$ )	3660	4270		mW
		With heatsink Derating factor above $T_A = 85^\circ\text{C}$ : $104.1 \text{ mW}/^\circ\text{C}$ ( $1/\theta_{JA}$ )	6250	7290		mW

**Note 1** Obtained from package thermal simulations, JEDEC 2S2P four-layer board (114.3 mm x 101.6 mm x 1.6 mm), 70  $\mu\text{m}$  (2 oz) copper thickness power planes, 35  $\mu\text{m}$  (1 oz) copper thickness signal layer traces, natural convection (still air)

**Note 2** As per [Note 1](#) with addition of aluminium heatsink, 114.3 mm x 101.6 mm x 1.0 mm representing the lid of a case.

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### 4.4.1 Power Derating Curves

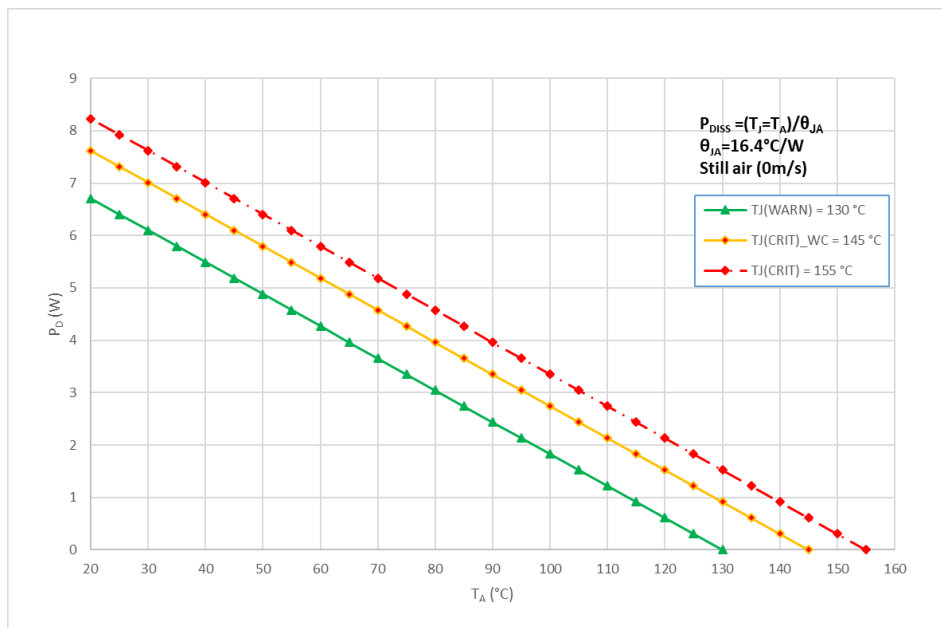


Figure 3: Power Derating Curve

Table 7: Typical Temperatures

	T <sub>A</sub> = 85 °C	T <sub>A</sub> = 105 °C	T <sub>A</sub> = 125 °C
T <sub>J_WARN</sub>	P <sub>D</sub> = 2.74 W	P <sub>D</sub> = 1.52 W	P <sub>D</sub> = 0.30 W
T <sub>J_CRIT_WC</sub>	P <sub>D</sub> = 3.66 W	P <sub>D</sub> = 2.44 W	P <sub>D</sub> = 1.22 W

### 4.5 Buck1 Characteristics

Unless otherwise noted, the following is valid for T<sub>J</sub> = -40 °C to +150 °C, V<sub>sys</sub> = 2.8 V to 5.5 V.

**Note:** Values are preliminary, pending final silicon characterization results.

Table 8: Dual-Phase Buck Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>External Electrical Conditions</b>						
V <sub>IN</sub>	Input voltage	V <sub>IN</sub> = V <sub>sys</sub> = V <sub>AVDD</sub>	2.8		5.5	V
C <sub>OUT</sub>	Total output capacitance, including voltage and temperature coefficient	Typ 8 x 22 μF -40 % to +20 %	106	176	211	μF

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Parameter	Description	Conditions	Min	Typ	Max	Unit
$ESR_{COUT}$	Output capacitor series resistance, per capacitor	$f > 100$ kHz		3		m $\Omega$
L	Inductor value, per phase, including current and temperature dependence		88	110	132	nH
$DCR_L$	Inductor DC resistance			2		m $\Omega$
<b>Electrical Performance</b>						
$V_{OUT}$	Output voltage, configurable in 10 mV steps	$I_{OUT} = 0$ mA to $I_{OUT\_MAX\_PK}$ $V_{IN} = 2.8$ V to 5.5 V	0.5	0.85	1.3	V
$V_{OUT\_ACC}$	Output voltage accuracy, including static line and load regulation		-10		10	mV
$V_{OUT\_ACC}$	Output voltage accuracy, including static line and load regulation	$V_{OUT} \geq 1$ V	-1		1	%
$I_{OUT\_MAX\_CONT}$	Maximum continuous output current	With suitable thermal design	13			A
$I_{OUT\_MAX\_PK}$	Maximum peak output current	With suitable thermal design	20			A
$I_{LIM}$	Current limit, configureable per phase <a href="#">Note 1</a> <a href="#">Note 2</a>			14.5		A
$I_{LIM\_ACC}$	Current limit accuracy <a href="#">Note 2</a>		-20		20	%
$V_{THR\_PG\_HYS}$	Power-good voltage threshold hysteresis	$V_{OUT} = V_{THR\_PG\_DWN}$	70	80	90	mV
$V_{THR\_PG\_DWN}$	Power-good voltage threshold for falling	$V_{OUT} = V_{BUCK}$	-170	-140	-110	mV

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Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>THR_HV</sub>	High V <sub>OUT</sub> voltage threshold	V <sub>OUT</sub> = V <sub>BUCK</sub>	130	160	195	mV
V <sub>OUT_TR_LINE</sub>	Line transient response	V <sub>IN</sub> = 3.0 V to 3.6 V V <sub>OUT</sub> = 1.1 V I <sub>OUT</sub> = 0.5 * I <sub>OUT_MAX_PK</sub> dt = 10 μs		10		mV
f <sub>SW</sub>	Switching frequency			4		MHz
t <sub>ON_MIN</sub>	Minimum turn-on pulse 0 % duty is also supported			10		ns
t <sub>BUCK_EN</sub>	Turn-on time	CH1_EN = high V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> = 0.85 V DVC slew rate: 10 mV/8 μs No load Recommended capacitance		600		μs
R <sub>PD</sub>	Output pull-down resistance for each phase at the LX node, see CH1_PD_DIS	V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> = 0.5 V	140	150	160	Ω
R <sub>ON_P MOS</sub>	On resistance of switching PMOS, per phase	V <sub>IN</sub> = 3.3 V		12		mΩ
R <sub>ON_N MOS</sub>	On resistance of switching NMOS, per phase	V <sub>IN</sub> = 3.3 V		6		mΩ
<b>PWM Mode</b>						
η <sub>PWM</sub>	Efficiency, PWM	V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> = 1.1 V I <sub>OUT</sub> = 5 % (I <sub>OUT_MAX_PK</sub> ) to 80 % (I <sub>OUT_MAX_PK</sub> )		80		%
<b>AUTO Mode</b>						
V <sub>OUT_TR_LD_RISE</sub>	Load transient response, phase shedding enabled	V <sub>OUT</sub> = 1.1 V I <sub>OUT</sub> = 25 % to 75 % of I <sub>OUT_MAX_PK</sub> Load rise time = 1 μs	-5			%
V <sub>OUT_TR_LD_FALL</sub>	Load transient response, phase shedding enabled	V <sub>OUT</sub> = 1.1 V I <sub>OUT</sub> = 75 % to 25 % of I <sub>OUT_MAX_PK</sub> Load fall time = 1 μs			5	%

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Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>PFM Mode</b>						
I <sub>Q_PFM_1PH</sub>	Quiescent current in PFM	V <sub>IN</sub> = 3.3 V No load No switching		120		μA
η <sub>PFM</sub>	Efficiency, PFM	V <sub>IN</sub> = 3.3 V V <sub>OUT</sub> = 1.1 V I <sub>OUT</sub> = 100 mA		80		%

**Note 1** For applications requiring V<sub>OUT</sub> < 0.75 V contact Renesas applications support for configuration setting

**Note 2** t<sub>ON</sub> > 40 ns

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 4.6 Performance and Supervision Characteristics

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 9: Performance and Supervision Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
V <sub>THR_POR</sub>	Power-on-reset threshold	Threshold for AVDD falling		2.1	2.25	V
V <sub>THR_POR_HYS</sub>	Power-on-reset hysteresis			200		mV
T <sub>WARN</sub>	Temperature warning threshold		120	130	140	°C
T <sub>CRIT</sub>	Temperature shutdown threshold		145	155	165	°C
I <sub>IN_OFF</sub>	Supply current	OFF state T <sub>A</sub> = 27 °C IC_EN = 0		0.1	1	μA
I <sub>IN_ON</sub>	Supply current	ON state T <sub>A</sub> = 27 °C IC_EN = 1 Buck off	5	10	20	μA

### 4.7 Digital IO Characteristics

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 10: Digital I/O Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
V <sub>IH_EN</sub>	Input high voltage, IC enable		1.2		AVDD	V
V <sub>IL_EN</sub>	Input low voltage, IC enable				0.4	V
t <sub>IC_EN</sub>	IC enable time				1000	μs
V <sub>IH_GPIO_SCL_SDA</sub>	Input high voltage GPIO, SCL, SDA		1.2		AVDD	V
V <sub>IL_GPIO_SCL_SDA</sub>	Input low voltage GPIO, SCL, SDA				0.4	V
V <sub>OH_GPIO</sub>	Output high voltage GPIO	Push-pull mode I <sub>OUT</sub> = 1 mA	0.8*AV DD		AVDD	V
V <sub>OL_GPIO</sub>	Output low voltage GPIO	Push-pull mode I <sub>OUT</sub> = 1 mA			0.2*AV DD	V

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Parameter	Description	Conditions	Min	Typ	Max	Unit
V <sub>OL_SDA</sub>	Output low voltage SDA	I <sub>OUT</sub> = 3 mA		0.24		V
R <sub>PD</sub>	GPIO pull-down resistor		2	10	120	kΩ
R <sub>PU</sub>	GPIO pull-up resistor		2	10	120	kΩ

### 4.8 Timing Characteristics

**Note:** Values are preliminary, pending final silicon characterization results.

**Table 11: I2C Electrical Characteristics**

Parameter	Description	Conditions	Min	Typ	Max	Unit
<b>Electrical Performance</b>						
t <sub>BUS</sub>	Bus free time between a STOP and START condition		0.5			μs
C <sub>BUS</sub>	Bus line capacitive load				150	pF
f <sub>SCL</sub>	SCL clock frequency		20 Note 1		1000	kHz
t <sub>LO_SCL</sub>	SCL low time		0.5			μs
t <sub>HI_SCL</sub>	SCL high time		0.26			μs
t <sub>RISE</sub>	SCL and SDA rise time	Requirement for input			1000	ns
t <sub>FALL</sub>	SCL and SDA fall time	Requirement for input			300	ns
t <sub>SETUP_START</sub>	Start condition setup time		0.26			μs
t <sub>HOLD_START</sub>	Start condition hold time		0.26			μs
t <sub>SETUP_STOP</sub>	Stop condition setup time		0.26			μs
t <sub>DATA</sub>	Data valid time				0.45	μs
t <sub>DATA_ACK</sub>	Data valid acknowledge time				0.45	μs
t <sub>SETUP_DATA</sub>	Data setup time		50			ns
t <sub>HOLD_DATA</sub>	Data hold time		0			ns

**Note 1** Minimum clock frequency is limited to 20 kHz if I2C\_TIMEOUT is enabled



## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 4.9 Typical Performance

The static efficiency measurement plots depicted in Figure 4 and Figure 5 are performed at 25°C in a temperature-controlled environment. A continuous load was used for the measurements.

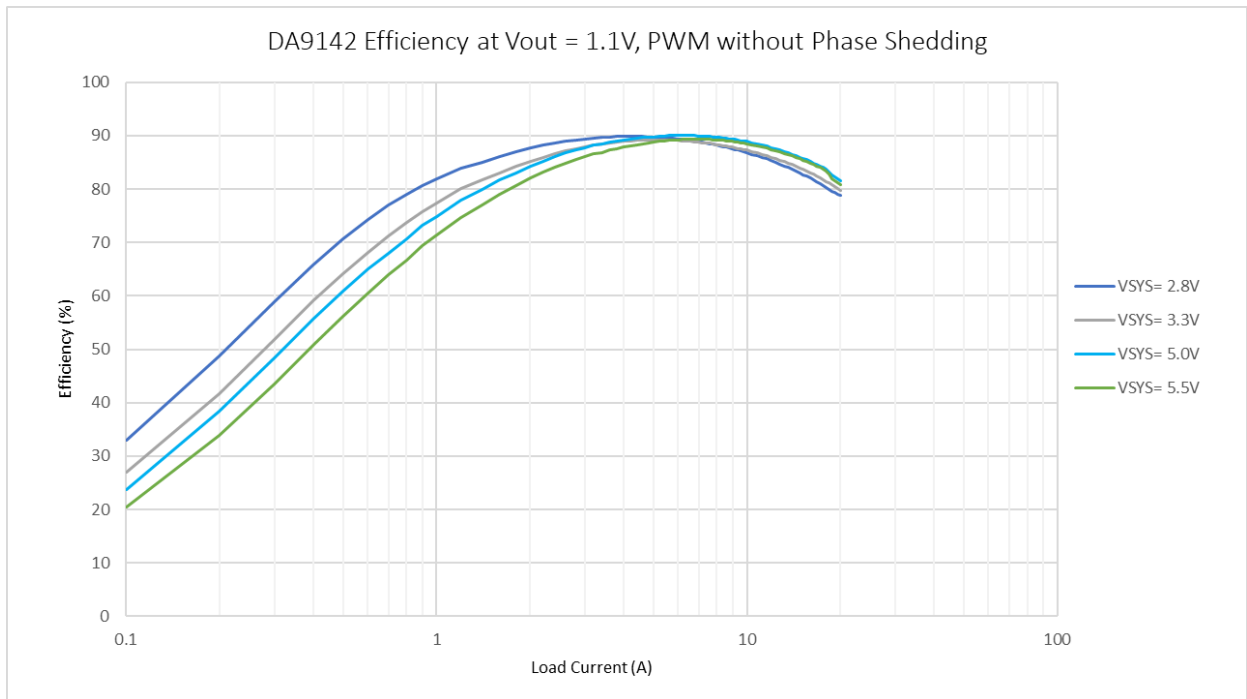


Figure 4: DA9142 Efficiency, PWM Mode without Phase Shedding

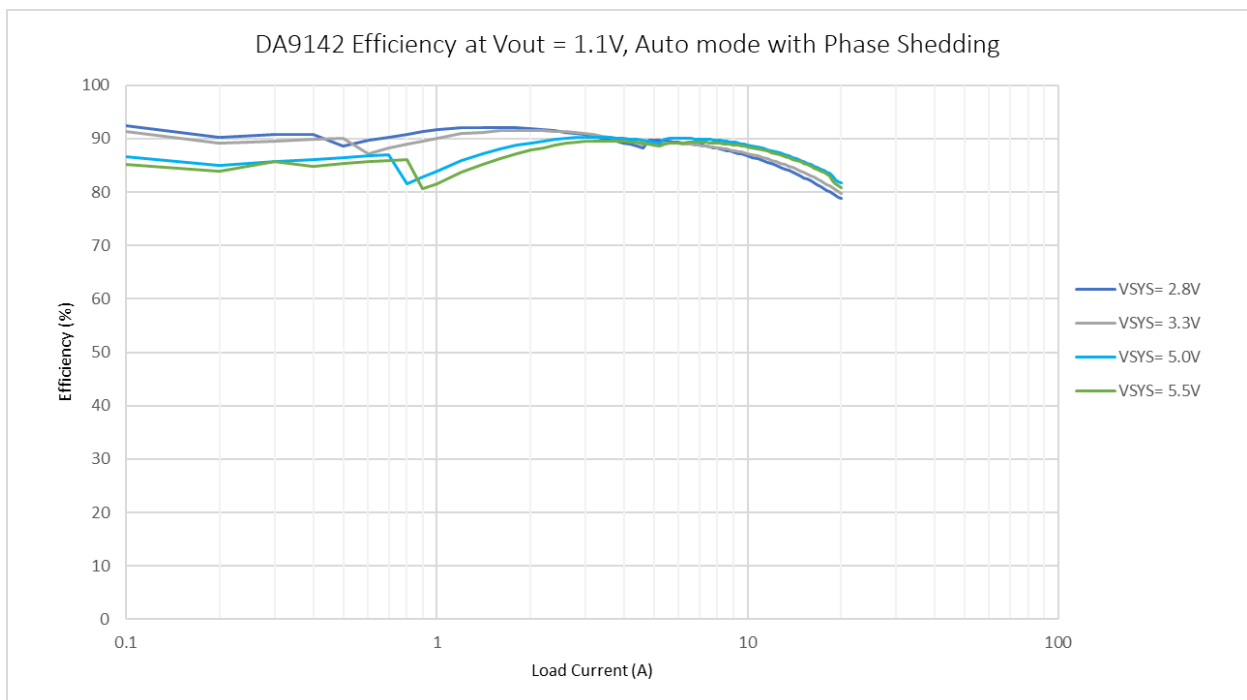


Figure 5: DA9142 Efficiency, Auto Mode with Phase Shedding

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 5 Functional Description

#### 5.1 Operating Modes

##### 5.1.1 ON

DA9142 is ON when the IC\_EN pin is higher than  $V_{IH\_EN}$  and the supply voltage is higher than  $V_{THR\_POR}$ . Once enabled, the host processor can start communicating with DA9142 using the control interface, after the  $t_{IC\_EN}$  delay.

##### 5.1.2 OFF

DA9142 is OFF when the IC\_EN pin is lower than  $V_{IL\_EN}$ . In OFF, the buck is always disabled and the LX nodes are pulled down by a (typically 150  $\Omega$ ) internal pull-down resistor.

#### 5.2 DC-DC Buck Converter

DA9142 operates as a single-channel, dual-phase buck converter which delivers up to 20 A output current at a 0.5 V to 1.3 V output voltage range.

The buck converter has two configurable output voltage settings. One is the normal output voltage (A), the other offers an alternative retention voltage (B). The bits used to configure the outputs are CH1\_A\_VOUT and CH1\_B\_VOUT. In this way, different application power modes are supported. The target output voltage (either A or B) is toggled by either GPI or I<sup>2</sup>C control interface, providing maximum flexibility for the application's host processor.

When the buck is enabled, its output voltage is monitored and a power-good signal indicates that the buck output voltage has reached a level higher than the power-good rise threshold. The power-good status is lost when the voltage drops below  $V_{THR\_PG\_DWN}$  or increases above  $V_{THR\_HV}$ .  $V_{THR\_PG\_HYS}$  is the value that defines the hysteresis between a power-good rise and  $V_{THR\_PG\_DWN}$ . The status of the power-good indicator is read back via I<sup>2</sup>C from the PG1 status bit. Alternatively, it can be assigned to any of the GPIOs by setting the GPIO<x>\_MODE bits to PG1 output.

The buck converter is capable of supporting DVC transitions that occur when:

- the active and selected A- or B-voltage is updated to a new target value, using bits CH1\_A\_VOUT and CH1\_B\_VOUT
- the voltage selection is toggled from the A- to B-voltage (or B- to A-voltage), using bit CH1\_VSEL or via GPI control

The DVC operates in pulse-width-modulation (PWM) mode with synchronous rectification. The slew rate of the DVC ramp up and ramp down transitions is programmed at 10 mV per (8, 4, 2, 1, or 0.5)  $\mu$ s in register bits CH1\_SR\_DVC\_DWN and CH1\_SR\_DVC\_UP.

A pull-down resistor (typically 150  $\Omega$ ) for each phase is always activated when the buck is disabled, unless it is disabled by setting register bits CH1\_PD\_DIS to 0x1.

##### 5.2.1 Switching Frequency

The buck switching frequency is tuned using register bit OSC\_TUNE. The internal 8 MHz oscillator frequency is tuned in  $\pm 160$  kHz steps. This impacts the buck converter frequency in steps of 80 kHz and helps to mitigate possible disturbances to other high frequency systems in the application.

##### 5.2.2 Operation Modes and Phase Selection

The buck converter operates in PWM or PFM modes. The operating mode is selected using register bits CH1\_A\_MODE and CH1\_B\_MODE.

Phase shedding automatically changes between 1- and 2-phase operation at a typical current of 4 A.

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If the automatic operation mode (Auto mode) is selected, the buck converter automatically changes between synchronous PWM mode and PFM mode depending on the load current. This improves the efficiency across the range of output load currents.

### 5.2.3 Output Voltage Selection

The switching converter is configured using the I<sup>2</sup>C interface.

Two output voltages (Value A and Value B in Figure 6) are pre-configured in registers CH1\_A\_VOUT and CH1\_B\_VOUT. The output voltage (VBUCK in Figure 6) is selected by toggling register bit CH1\_VSEL, by re-programming the selected voltage control register, or by toggling a GPI if configured to do so. Any of these options will result in ramped voltage transitions.

After being enabled, the buck converter uses, by default, the register settings in CH1\_A\_VOUT (Value A) unless the output voltage selection is configured via the GPI port to be CH1\_B\_VOUT.

Register bits CH1\_VMAX limit the output voltage that can be set.

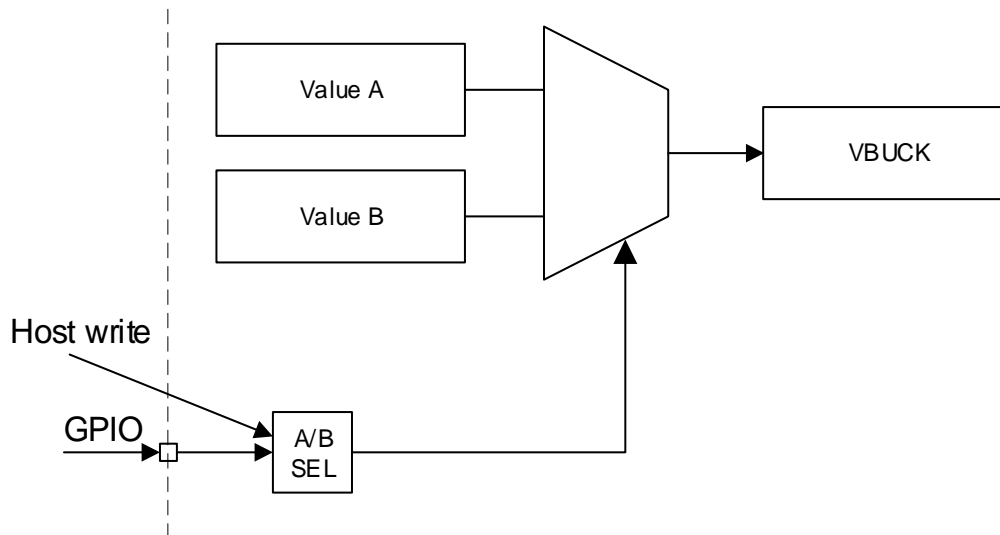


Figure 6: Buck Output Voltage Control Concept

### 5.2.4 Soft Startup and Shutdown

To limit in-rush current from VSYS, the buck converter performs a soft-start after being enabled. The startup behavior is a compromise between acceptable inrush current from the battery and turn-on time. Ramp times are configured in register CH1\_SR\_STARTUP. **Note:** rates higher than 5 mV/μs may produce overshoot during the startup phase.

A ramped power down is selected in register bits CH1\_SR\_SHDN. When no ramp is selected (immediate power down), the output node is discharged only by the pull-down resistor, if enabled, in register CH1\_PD\_DIS.

### 5.2.5 Current Limit

The integrated current limit protects the power stages and external coil from excessive current. It should be configured to at least 40 % higher than the required maximum per phase output current. **Note:** this value is loaded from the OTP.

When the current limit is reached, the buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using bit M\_OC1 in SYS\_MASK\_1. Register bit OC\_DVC\_MASK masks over-current events during DVC transitions.

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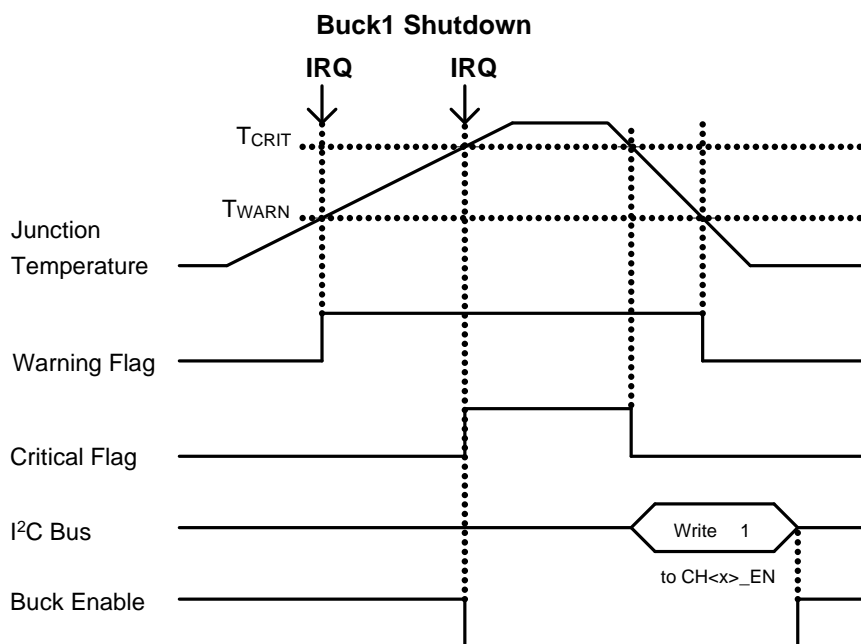
### 5.2.6 Temperature Protection

DA9142 is protected from internal overheating by temperature-triggered shutdown.

There are two kinds of flags concerning temperature protection: temperature warning and temperature critical. The warning flag asserts when  $T_J > T_{WARN}$  and the critical flag asserts when  $T_J > T_{CRIT}$ . When the critical flag asserts, Buck1 shuts down immediately.

**Table 12: Temperature Protection Control Registers**

Category	Register name	Description
Status	TEMP_WARN	Asserts when the temperature warning threshold is reached
	TEMP_CRIT	Asserts when the temperature shutdown threshold is reached
IRQ event	E_TEMP_WARN	TEMP_WARN caused event
	E_TEMP_CRIT	TEMP_CRIT caused event
IRQ mask	M_TEMP_WARN	TEMP_WARN event IRQ mask
	M_TEMP_CRIT	TEMP_CRIT event IRQ mask
	M_VR_HOT	TEMP_WARN status IRQ mask



**Figure 7: Temperature Protection Operation**

## 5.3 Control Circuits

### 5.3.1 Chip Enable and Disable

The IC\_EN pin enables and disables the IC. When IC\_EN = 0 all blocks, except for low I<sub>Q</sub> POR, powerdown and the buck output is pulled down.

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 5.3.2 GPIO

#### 5.3.2.1 GPIO Pin Assignment

The DA9142 provides up to five GPIO pins, three if the I<sup>2</sup>C is enabled, see [Table 13](#). The registers that configure the GPIO pin assignments are OTP programmable.

GPIO0 can be programmed (OTP option) to function as chip configuration (CONF), see Section 5.3.2.3. When the I<sup>2</sup>C interface is enabled (OTP option) any register settings for GPIO3 and GPIO4 are ignored and GPIO3 and GPIO4 function as SCL and SDA respectively.

**Table 13: GPIO Pin Assignment**

OTP Option		GPIO Pin					Available GPIOs
I2C	CONF	CONF/ GPIO0	GPIO1	GPIO2	SCL/ GPIO3	SDA/ GPIO4	
Disabled	Disabled	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	5
	Enabled	CONF	GPIO1	GPIO2	GPIO3	GPIO4	4
Enabled	Disabled	GPIO0	GPIO1	GPIO2	SCL	SDA	3
	Enabled	CONF	GPIO1	GPIO2	SCL	SDA	2

#### 5.3.2.2 GPIO Function

The GPIO pins are configurable as the following functions in register GPIO<x>\_MODE (x = 0 to 4):

- Buck1 enable input (EN1)
- Buck1 DVC control input (DVC1)
- Buck1 OTP setting reload input (RELOAD)
- Buck1 power-good output (PG1)
- Interrupt output (nIRQ)

#### 5.3.2.3 Chip Configuration Select

GPIO0 functions as chip configuration select (CONF) input when enabled as an OTP setting.

Three different chip configurations can be selected according to the CONF pin level (high, low, or Hi-Z).

**Table 14: GPIO0 Configurable Registers when CONF Enabled**

Register Name	Description
IF_SLAVE_ADDR[6:0]	I2C slave address
CH1_A_MODE[1:0]	CH1_A Operation mode select
CH1_B_MODE[1:0]	CH1_B Operation mode select
CH1_VSEL	CH1 output voltage and operation selection
CH1_EN	CH1 enable
CH1_A_VOUT[7:0]	CH1 output voltage setting A
CH1_B_VOUT[7:0]	CH1 output voltage setting B
M_PG1_STAT	IRQ mask setting for CH1 power-good status
M_VR_HOT	IRQ mask setting for temp warning status
GPIO1_MODE[3:0]	GPIO1 mode setting
GPIO2_MODE[3:0]	GPIO2 mode setting

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Register Name	Description
GPIO1_OBUF	GPIO1 output buffer select
GPIO2_OBUF	GPIO2 output buffer select
GPIO1_TRIG[1:0]	GPIO1 input trigger select
GPIO1_POL	GPIO1 polarity select
GPIO1_PUPD	GPIO1 pull-up/pull-down enable
GPIO1_DEB[1:0]	GPIO1 input debounce time setting
GPIO1_DEB_RISE	GPIO1 input debounce rising edge enable
GPIO1_DEB_FALL	GPIO1 input debounce falling edge enable
GPIO2_TRIG[1:0]	GPIO2 input trigger select
GPIO2_POL	GPIO2 polarity select
GPIO2_PUPD	GPIO2 pull-up/pull-down enable
GPIO2_DEB[1:0]	GPIO2 input debounce time setting
GPIO2_DEB_RISE	GPIO2 input debounce rising edge enable
GPIO2_DEB_FALL	GPIO2 input debounce falling edge enable

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### 5.3.3 Interrupt

When an event is triggered, the nIRQ interrupt flag is asserted. Trigger conditions and control registers for each interrupt event are listed in [Table 15](#).

Some of these events are categorized as fault events and affect device operation (for example, buck disable), see [Section 5.2.6](#).

**Table 15: Interrupt List**

Name	Polarity (Note 1)	Trigger	IRQ Status Register	IRQ Mask Register	Deglintch Period
Temperature warning (event)	N	T <sub>J</sub> rising above T <sub>WARN</sub>	E_TEMP_WARN	M_TEMP_WARN	0 s
Temperature critical (event)	N	T <sub>J</sub> rising above T <sub>CRIT</sub>	E_TEMP_CRIT	M_TEMP_CRIT	0 s
Buck1 power-good (event)	P	Buck1 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage)	E_PG1	M_PG1	0 s
Buck1 over-voltage (event)	N	Buck1 V <sub>OUT</sub> rising above over-voltage threshold (target voltage + 150 mV)	E_OV1	M_OV1	Rise: 8 μs Fall: 8 μs
Buck1 under-voltage (event)	N	Buck1 V <sub>OUT</sub> falling below under-voltage threshold (target voltage - V <sub>TH_PG_FALL</sub> )	E_UV1	M_UV1	0 s
Buck1 over-current (event)	N	Buck1 current rising above over-current threshold	E_OC1	M_OC1	0 s
Buck1 power-good (status) (Note 2)	P	Buck1 V <sub>OUT</sub> is in power-good voltage range (not under- or over-voltage)	PG1	M_PG1_STAT (Note 3)	0 s
Temperature warning (status) (Note 2)	N	T <sub>J</sub> rising above T <sub>WARN</sub>	TEMP_WARN	M_VR_HOT (Note 3)	0 s
GPIO0 change (event)	N	Detect GPIO0 change for active trigger selected by GPIO0_TRIG register	E_GPIO0	M_GPIO0	100 μs, 1 ms, or 10 ms 100 ms
GPIO1 change (event)	N	Detect GPIO1 change for active trigger selected by GPIO1_TRIG register	E_GPIO1	M_GPIO1	
GPIO2 change (event)	N	Detect GPIO2 change for active trigger selected by GPIO2_TRIG register	E_GPIO2	M_GPIO2	

**Note 1** Polarity at the source of the flag: P = active high, N = active low.  
General rule is: normal system state is high, and abnormal system state is low (for example, PG = high means power-good, TEMP\_CRIT = low when in temperature critical state).

**Note 2** Interrupt outputs the status as is. I<sup>2</sup>C write is not required for interrupt clear.

**Note 3** OTP load value defined by CONF pin setting (if CONF pin enabled).

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Table 16: Interrupt Registers Except for Power-Good Status

Register	Description
E_<name>	Read-only interrupt event register 0: No interrupt 1: Interrupt occurred <b>Cleared after being written to I<sup>2</sup>C. Set until IRQ is removed.</b>
M_<name>	Interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Event register (E_<name>) is updated.

Table 17: Interrupt Registers for Power-Good and Temperature Warning Status

Register	Description
PG1	Buck1 power-good status. Asserted as long as Buck1 output voltage is in range (under-voltage threshold < buck output voltage < over-voltage threshold) 0: Not power-good 1: Power-good
M_PG1_STAT	Power-good status interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Power-good status register (PG1) is updated
TEMP_WARN	Asserted as long as the temperature warning threshold (T <sub>WARN</sub> ) is reached 0: Junction temperature is below T <sub>WARN</sub> 1: Junction temperature is above T <sub>WARN</sub>
M_VR_HOT	Temperature warning status (TEMP_WARN) interrupt mask register 0: Not masked 1: Masked. No IRQ signal sent. Temperature warning status register (TEMP_WARN) is updated

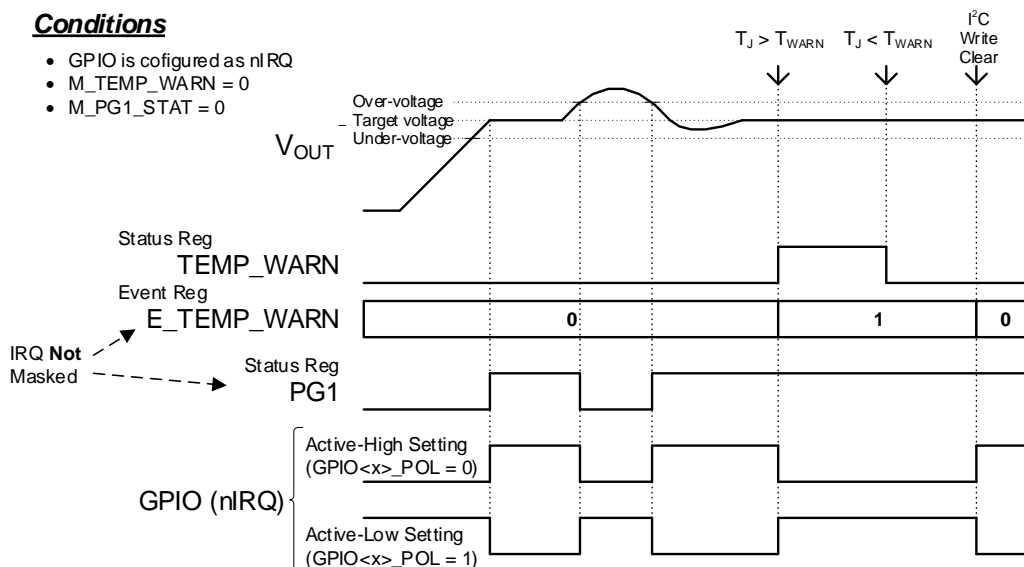


Figure 8: Interrupt Operation Example



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### 5.4 I<sup>2</sup>C Communication

All features of DA9142 can be controlled with the I<sup>2</sup>C interface, which is enabled or disabled as an OTP setting.

I <sup>2</sup> C	Description
Disabled	SCL/GPIO3 and SDA/GPIO4 pins can be used as GPIO
Enabled	SCL/GPIO3 and SDA/GPIO4 pins are used as I <sup>2</sup> C clock input and I <sup>2</sup> C data input/output.

GPIO3 functions as the I<sup>2</sup>C clock (SCL) and GPIO4 carries all the power manager bidirectional I<sup>2</sup>C data (SDA). The I<sup>2</sup>C interface is open drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The standard frequency of the I<sup>2</sup>C bus is 1 MHz in fast-mode plus (FM+), 400 kHz in fast-mode, or 100 kHz in standard mode.

#### 5.4.1 I<sup>2</sup>C Protocol

All data is transmitted across the I<sup>2</sup>C bus in eight-bit groups. To send a bit, the SDA line is driven towards the intended state while the SCL is low (a low SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in idle state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).



Figure 9: I<sup>2</sup>C START and STOP Condition Timing

The I<sup>2</sup>C bus is monitored for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 10 and Figure 11).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit, and the eight-bit register address followed by eight bits of data, terminated by a STOP condition. DA9142 responds to all bytes with acknowledge (A), see Figure 10.

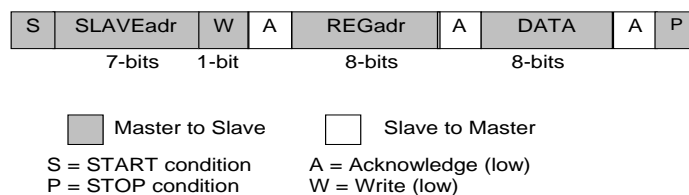


Figure 10: I<sup>2</sup>C Byte Write (SDA Line)



## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 6 Register Definitions

#### 6.1 Register Map

Table 18: Register Map

Addr	Register	7	6	5	4	3	2	1	0
<b>System Module</b>									
0x0001	<a href="#">SYS_STATUS_0</a>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	TEMP_CRIT	TEMP_WARN
0x0002	<a href="#">SYS_STATUS_1</a>	Reserved	Reserved	Reserved	Reserved	PG1	OV1	UV1	OC1
0x0003	<a href="#">SYS_STATUS_2</a>	Reserved	Reserved	Reserved	Reserved	Reserved	GPIO2	GPIO1	GPIO0
0x0004	<a href="#">SYS_EVENT_0</a>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 0	E_TEMP_CRIT	E_TEMP_WARN
0x0005	<a href="#">SYS_EVENT_1</a>	Reserved	Reserved	Reserved	Reserved	E_PG1	E_OV1	E_UV1	E_OC1
0x0006	<a href="#">SYS_EVENT_2</a>	Reserved	Reserved	Reserved	Reserved	Reserved	E_GPIO2	E_GPIO1	E_GPIO0
0x0007	<a href="#">SYS_MASK_0</a>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved 1	M_TEMP_CRIT	M_TEMP_WARN
0x0008	<a href="#">SYS_MASK_1</a>	Reserved	Reserved	Reserved	Reserved	M_PG1	M_OV1	M_UV1	M_OC1
0x0009	<a href="#">SYS_MASK_2</a>	Reserved	Reserved	Reserved	Reserved	Reserved	M_GPIO2	M_GPIO1	M_GPIO0
0x000A	<a href="#">SYS_MASK_3</a>	Reserved	Reserved	Reserved	Reserved	M_VR_HOT	Reserved 1	Reserved	M_PG1_STAT
0x000B	<a href="#">SYS_CONFIG_0</a>	CH1_DIS_DLY<3:0>				CH1_EN_DLY<3:0>			
0x000D	<a href="#">SYS_CONFIG_2</a>	Reserved	OC_LATCHOFF<1:0>		OC_DVC_MASK	PG_DVC_MASK<1:0>		Reserved	Reserved
0x000E	<a href="#">SYS_CONFIG_3</a>	Reserved	OSC_TUNE<2:0>			Reserved	Reserved	I2C_TIMEOUT	Reserved 0
0x0010	<a href="#">SYS_GPIO0_0</a>	Reserved	Reserved	Reserved	GPIO0_MODE<3:0>				GPIO0_OBUF
0x0011	<a href="#">SYS_GPIO0_1</a>	GPIO0_DEB_FALL	GPIO0_DEB_RISE	GPIO0_DEB<1:0>		GPIO0_PUPD	GPIO0_POL	GPIO0_TRIG<1:0>	
0x0012	<a href="#">SYS_GPIO1_0</a>	Reserved	Reserved	Reserved	GPIO1_MODE<3:0>				GPIO1_OBUF
0x0013	<a href="#">SYS_GPIO1_1</a>	GPIO1_DEB_FALL	GPIO1_DEB_RISE	GPIO1_DEB<1:0>		GPIO1_PUPD	GPIO1_POL	GPIO1_TRIG<1:0>	
0x0014	<a href="#">SYS_GPIO2_0</a>	Reserved	Reserved	Reserved	GPIO2_MODE<3:0>				GPIO2_OBUF
0x0015	<a href="#">SYS_GPIO2_1</a>	GPIO2_DEB_FALL	GPIO2_DEB_RISE	GPIO2_DEB<1:0>		GPIO2_PUPD	GPIO2_POL	GPIO2_TRIG<1:0>	
0x0016	<a href="#">SYS_GPIO3_0</a>	Reserved	Reserved	Reserved	GPIO3_MODE<3:0>				GPIO3_OBUF
0x0017	<a href="#">SYS_GPIO3_1</a>	GPIO3_DEB_FALL	GPIO3_DEB_RISE	GPIO3_DEB<1:0>		GPIO3_PUPD	GPIO3_POL	GPIO3_TRIG<1:0>	
0x0018	<a href="#">SYS_GPIO4_0</a>	Reserved	Reserved	Reserved	GPIO4_MODE<3:0>				GPIO4_OBUF
0x0019	<a href="#">SYS_GPIO4_1</a>	GPIO4_DEB_FALL	GPIO4_DEB_RISE	GPIO4_DEB<1:0>		GPIO4_PUPD	GPIO4_POL	GPIO4_TRIG<1:0>	

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Addr	Register	7	6	5	4	3	2	1	0
<b>Buck Control</b>									
<b>Buck1</b>									
0x0020	<a href="#">BUCK_BUCK1_0</a>	Reserved	CH1_SR_DVC_DWN<2:0>			CH1_SR_DVC_UP<2:0>			CH1_EN
0x0021	<a href="#">BUCK_BUCK1_1</a>	Reserved	CH1_SR_SHDN<2:0>			CH1_SR_STARTUP<2:0>			CH1_PD_DIS
0x0022	<a href="#">BUCK_BUCK1_2</a>	Reserved	Reserved	Reserved	Reserved	CH1_ILIM<3:0>			
0x0023	<a href="#">BUCK_BUCK1_3</a>	CH1_VMAX<7:0>							
0x0024	<a href="#">BUCK_BUCK1_4</a>	Reserved	Reserved	Reserved	CH1_VSEL	CH1_B_MODE<1:0>		CH1_A_MODE<1:0>	
0x0025	<a href="#">BUCK_BUCK1_5</a>	CH1_A_VOUT<7:0>							
0x0026	<a href="#">BUCK_BUCK1_6</a>	CH1_B_VOUT<7:0>							
0x0027	<a href="#">BUCK_BUCK1_7</a>	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CH1_RIPPLE_CANCEL<1:0>	
<b>OTP Control</b>									
<b>Serialization</b>									
0x0048	<a href="#">OTP_DEVICE_ID</a>	DEV_ID<7:0>							
0x0049	<a href="#">OTP_VARIANT_ID</a>	MRC<3:0>				VRC<3:0>			
0x004A	<a href="#">OTP_CUSTOMER_ID</a>	CUST_ID<7:0>							
0x004B	<a href="#">OTP_CONFIG_ID</a>	CONFIG_REV<7:0>							

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### 6.2 Register Descriptions

**Table 19: SYS\_STATUS\_0 (0x0001)**

Bit	Type	Field Name	Description
[1]	R	TEMP_CRIT	Asserted when the thermal shutdown threshold is reached
[0]	R	TEMP_WARN	Asserted when the thermal warning threshold is reached

**Table 20: SYS\_STATUS\_1 (0x0002)**

Bit	Type	Field Name	Description
[3]	R	PG1	Asserted when the buck output voltage is in range
[2]	R	OV1	Asserted when the buck exceeds the over-voltage threshold
[1]	R	UV1	Asserted when the buck exceeds the under-voltage threshold
[0]	R	OC1	Asserted when the buck exceeds the over-current threshold

**Table 21: SYS\_STATUS\_2 (0x0003)**

Bit	Type	Field Name	Description
[2]	R	GPIO2	GPIO2 input readback status - asserted if the input on GPIO is seen as logic high
[1]	R	GPIO1	GPIO1 input readback status - asserted if the input on GPIO is seen as logic high
[0]	R	GPIO0	GPIO0 input readback status - asserted if the input on GPIO is seen as logic high

**Table 22: SYS\_EVENT\_0 (0x0004)**

Bit	Type	Field Name	Description
[1]	RW1C	E_TEMP_CRIT	An over-temperature event has occurred. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_TEMP_WARN	A temperature warning event has occurred. Write 0x1 to reset this bit to 0x0 when the event source has been released.

**Table 23: SYS\_EVENT\_1 (0x0005)**

Bit	Type	Field Name	Description
[3]	RW1C	E_PG1	PG1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[2]	RW1C	E_OV1	OV1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[1]	RW1C	E_UV1	UV1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_OC1	OC1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.

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**Table 24: SYS\_EVENT\_2 (0x0006)**

Bit	Type	Field Name	Description
[2]	RW1C	E_GPIO2	GPIO2 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[1]	RW1C	E_GPIO1	GPIO1 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.
[0]	RW1C	E_GPIO0	GPIO0 caused event. Write 0x1 to reset this bit to 0x0 when the event source has been released.

**Table 25: SYS\_MASK\_0 (0x0007)**

Bit	Type	Field Name	Description
[1]	RW	M_TEMP_CRIT	Thermal shutdown can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_TEMP_WARN	Temperature warning can cause an interrupt. Write 0x1 to mask this cause of interrupt.

**Table 26: SYS\_MASK\_1 (0x0008)**

Bit	Type	Field Name	Description
[3]	RW	M_PG1	PG1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[2]	RW	M_OV1	OV1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[1]	RW	M_UV1	UV1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_OC1	OC1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.

**Table 27: SYS\_MASK\_2 (0x0009)**

Bit	Type	Field Name	Description
[2]	RW	M_GPIO2	GPIO2 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[1]	RW	M_GPIO1	GPIO1 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.
[0]	RW	M_GPIO0	GPIO0 event can cause an interrupt. Write 0x1 to mask this cause of interrupt.

**Table 28: SYS\_MASK\_3 (0x000A)**

Bit	Type	Field Name	Description
[3]	RW	M_VR_HOT	Temperature warning status IRQ mask. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[0]	RW	M_PG1_STAT	PG1 status IRQ mask. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Table 29: SYS\_CONFIG\_0 (0x000B)

Bit	Type	Field Name	Description																																		
[7:4]	RW	CH1_DIS_DLY	<p>Delay time (ms) until CH1 is disabled. Active when GPIO is configured as EN1 or IC_EN control. Initial value is determined by CONF pin setting during start up if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>0</td></tr> <tr><td>0x1</td><td>1</td></tr> <tr><td>0x2</td><td>2</td></tr> <tr><td>0x3</td><td>3</td></tr> <tr><td>0x4</td><td>4</td></tr> <tr><td>0x5</td><td>5</td></tr> <tr><td>0x6</td><td>6</td></tr> <tr><td>0x7</td><td>7</td></tr> <tr><td>0x8</td><td>8</td></tr> <tr><td>0x9</td><td>9</td></tr> <tr><td>0xA</td><td>10</td></tr> <tr><td>0xB</td><td>11</td></tr> <tr><td>0xC</td><td>12</td></tr> <tr><td>0xD</td><td>13</td></tr> <tr><td>0xE</td><td>14</td></tr> <tr><td>0xF</td><td>15</td></tr> </tbody> </table>	Value	Description	0x0	0	0x1	1	0x2	2	0x3	3	0x4	4	0x5	5	0x6	6	0x7	7	0x8	8	0x9	9	0xA	10	0xB	11	0xC	12	0xD	13	0xE	14	0xF	15
Value	Description																																				
0x0	0																																				
0x1	1																																				
0x2	2																																				
0x3	3																																				
0x4	4																																				
0x5	5																																				
0x6	6																																				
0x7	7																																				
0x8	8																																				
0x9	9																																				
0xA	10																																				
0xB	11																																				
0xC	12																																				
0xD	13																																				
0xE	14																																				
0xF	15																																				
[3:0]	RW	CH1_EN_DLY	<p>Delay time (ms) until CH1 is enabled. Active when GPIO is configured as EN1 control or IC_EN control. Initial value is determined by CONF pin setting during start up if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>0</td></tr> <tr><td>0x1</td><td>0.5</td></tr> <tr><td>0x2</td><td>1</td></tr> <tr><td>0x3</td><td>1.5</td></tr> <tr><td>0x4</td><td>2</td></tr> <tr><td>0x5</td><td>2.5</td></tr> <tr><td>0x6</td><td>3</td></tr> <tr><td>0x7</td><td>3.5</td></tr> <tr><td>0x8</td><td>4</td></tr> <tr><td>0x9</td><td>4.5</td></tr> <tr><td>0xA</td><td>5</td></tr> </tbody> </table>	Value	Description	0x0	0	0x1	0.5	0x2	1	0x3	1.5	0x4	2	0x5	2.5	0x6	3	0x7	3.5	0x8	4	0x9	4.5	0xA	5										
Value	Description																																				
0x0	0																																				
0x1	0.5																																				
0x2	1																																				
0x3	1.5																																				
0x4	2																																				
0x5	2.5																																				
0x6	3																																				
0x7	3.5																																				
0x8	4																																				
0x9	4.5																																				
0xA	5																																				

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			0xB 5.5
			0xC 6
			0xD 6.5
			0xE 7
			0xF 7.5

**Table 30: SYS\_CONFIG\_2 (0x000D)**

Bit	Type	Field Name	Description										
[6:5]	RW	OC_LATCHOFF	Over-current latch-off time (Debounce duration). Buck shuts down after over-current persists for 8 us, 1 ms or 3 ms unless setting is disabled setting. An IRQ is generated unless masked.  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Latch off disable</td> </tr> <tr> <td>0x1</td> <td>Latch off after 8 us</td> </tr> <tr> <td>0x2</td> <td>Latch off after 1 ms</td> </tr> <tr> <td>0x3</td> <td>Latch off after 3 ms</td> </tr> </tbody> </table>	Value	Description	0x0	Latch off disable	0x1	Latch off after 8 us	0x2	Latch off after 1 ms	0x3	Latch off after 3 ms
Value	Description												
0x0	Latch off disable												
0x1	Latch off after 8 us												
0x2	Latch off after 1 ms												
0x3	Latch off after 3 ms												
[4]	RW	OC_DVC_MASK	Over-current event mask during DVC ramp-up and ramp-down. Write 0x1 to mask over-current during DVC causing IRQ and LATCHOFF.										
[3:2]	RW	PG_DVC_MASK	Power good mask during DVC  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>No mask</td> </tr> <tr> <td>0x1</td> <td>Mask as not power good</td> </tr> <tr> <td>0x2</td> <td>Mask as power good</td> </tr> <tr> <td>0x3</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x0	No mask	0x1	Mask as not power good	0x2	Mask as power good	0x3	Reserved
Value	Description												
0x0	No mask												
0x1	Mask as not power good												
0x2	Mask as power good												
0x3	Reserved												

**Table 31: SYS\_CONFIG\_3 (0x000E)**

Bit	Type	Field Name	Description																
[6:4]	RW	OSC_TUNE	Tune oscillator frequency, tuned frequency = current frequency + OSC_TUNE * 160 kHz  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x3</td> <td>3</td> </tr> <tr> <td>0x2</td> <td>2</td> </tr> <tr> <td>0x1</td> <td>1</td> </tr> <tr> <td>0x0</td> <td>0</td> </tr> <tr> <td>0x7</td> <td>-1</td> </tr> <tr> <td>0x6</td> <td>-2</td> </tr> <tr> <td>0x5</td> <td>-3</td> </tr> </tbody> </table>	Value	Description	0x3	3	0x2	2	0x1	1	0x0	0	0x7	-1	0x6	-2	0x5	-3
Value	Description																		
0x3	3																		
0x2	2																		
0x1	1																		
0x0	0																		
0x7	-1																		
0x6	-2																		
0x5	-3																		



## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			0x4 -4
[1]	RW	I2C_TIMEOUT	Enable automatic reset of 2 wire interface (if SDA stays low for > 50 ms).

**Table 32: SYS\_GPIO0\_0 (0x0010)**

Bit	Type	Field Name	Description																																		
[4:1]	RW	GPIO0_MODE	GPIO function mode select <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>GPIO disable</td></tr> <tr><td>0x1</td><td>EN1 input</td></tr> <tr><td>0x2</td><td>Reserved</td></tr> <tr><td>0x3</td><td>EN1 input</td></tr> <tr><td>0x4</td><td>DVC1 input</td></tr> <tr><td>0x5</td><td>Reserved</td></tr> <tr><td>0x6</td><td>DVC1 input</td></tr> <tr><td>0x7</td><td>RELOAD input</td></tr> <tr><td>0x8</td><td>PG1 output</td></tr> <tr><td>0x9</td><td>Low output</td></tr> <tr><td>0xA</td><td>Low output</td></tr> <tr><td>0xB</td><td>PG1 output</td></tr> <tr><td>0xC</td><td>nIRQ output</td></tr> <tr><td>0xD</td><td>Reserved</td></tr> <tr><td>0xE</td><td>Low output</td></tr> <tr><td>0xF</td><td>High output</td></tr> </tbody> </table>	Value	Description	0x0	GPIO disable	0x1	EN1 input	0x2	Reserved	0x3	EN1 input	0x4	DVC1 input	0x5	Reserved	0x6	DVC1 input	0x7	RELOAD input	0x8	PG1 output	0x9	Low output	0xA	Low output	0xB	PG1 output	0xC	nIRQ output	0xD	Reserved	0xE	Low output	0xF	High output
Value	Description																																				
0x0	GPIO disable																																				
0x1	EN1 input																																				
0x2	Reserved																																				
0x3	EN1 input																																				
0x4	DVC1 input																																				
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0xC	nIRQ output																																				
0xD	Reserved																																				
0xE	Low output																																				
0xF	High output																																				
[0]	RW	GPIO0_OBUF	GPIO output buffer select <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>open-drain output</td></tr> <tr><td>0x1</td><td>push-pull output</td></tr> </tbody> </table>	Value	Description	0x0	open-drain output	0x1	push-pull output																												
Value	Description																																				
0x0	open-drain output																																				
0x1	push-pull output																																				

**Table 33: SYS\_GPIO0\_1 (0x0011)**

Bit	Type	Field Name	Description						
[7]	RW	GPIO0_DEB_FALL	GPI debounce falling edge						
[6]	RW	GPIO0_DEB_RISE	GPI debounce rising edge						
[5:4]	RW	GPIO0_DEB	GPI debounce time <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>100 us debounce</td></tr> <tr><td>0x1</td><td>1 ms debounce</td></tr> </tbody> </table>	Value	Description	0x0	100 us debounce	0x1	1 ms debounce
Value	Description								
0x0	100 us debounce								
0x1	1 ms debounce								

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			0x2      10 ms debounce 0x3      100 ms debounce
[3]	RW	GPIO0_PUPD	GPIO pull-up/pull-down enable <b>Value      Description</b> 0x0      GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1      GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	RW	GPIO0_POL	GPIO polarity <b>Value      Description</b> 0x0      GPIO is active-high 0x1      GPIO is active-low
[1:0]	RW	GPIO0_TRIG	GPI trigger type <b>Value      Description</b> 0x0      Dual-edge triggered 0x1      Positive-edge triggered 0x2      Negative-edge triggered 0x3      Reserved (No trigger)

**Table 34: SYS\_GPIO1\_0 (0x0012)**

Bit	Type	Field Name	Description
[4:1]	RW	GPIO1_MODE	GPIO function mode select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) <b>Value      Description</b> 0x0      GPIO disable 0x1      EN1 input 0x2      Reserved 0x3      EN1 input 0x4      DVC1 input 0x5      Reserved 0x6      DVC1 input 0x7      RELOAD input 0x8      PG1 output 0x9      Low output 0xA      Low output 0xB      PG1 output 0xC      nIRQ output

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Bit	Type	Field Name	Description
			0xD Reserved 0xE Low output 0xF High output
[0]	RW	GPIO1_OBUF	GPIO output buffer select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting).  <b>Value</b> <b>Description</b> 0x0          open-drain output 0x1          push-pull output

**Table 35: SYS\_GPIO1\_1 (0x0013)**

Bit	Type	Field Name	Description
[7]	RW	GPIO1_DEB_FALL	GPIO debounce falling edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[6]	RW	GPIO1_DEB_RISE	GPIO debounce rising edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)
[5:4]	RW	GPIO1_DEB	GPIO debounce time. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <b>Value</b> <b>Description</b> 0x0          100 us debounce 0x1          1 ms debounce 0x2          10 ms debounce 0x3          100 ms debounce
[3]	RW	GPIO1_PUPD	GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <b>Value</b> <b>Description</b> 0x0          GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1          GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	RW	GPIO1_POL	GPIO polarity. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <b>Value</b> <b>Description</b> 0x0          GPIO is active-high 0x1          GPIO is active-low
[1:0]	RW	GPIO1_TRIG	GPI trigger type. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <b>Value</b> <b>Description</b>

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			0x0 Dual-edge triggered
			0x1 Positive-edge triggered
			0x2 Negative-edge triggered
			0x3 Reserved (No trigger)

**Table 36: SYS\_GPIO2\_0 (0x0014)**

Bit	Type	Field Name	Description																																		
[4:1]	RW	GPIO2_MODE	<p>GPIO function mode select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>GPIO disable</td></tr> <tr><td>0x1</td><td>EN1 input</td></tr> <tr><td>0x2</td><td>Reserved</td></tr> <tr><td>0x3</td><td>EN1 input</td></tr> <tr><td>0x4</td><td>DVC1 input</td></tr> <tr><td>0x5</td><td>Reserved</td></tr> <tr><td>0x6</td><td>DVC1 input</td></tr> <tr><td>0x7</td><td>RELOAD input</td></tr> <tr><td>0x8</td><td>PG1 output</td></tr> <tr><td>0x9</td><td>Low output</td></tr> <tr><td>0xA</td><td>Low output</td></tr> <tr><td>0xB</td><td>PG1 output</td></tr> <tr><td>0xC</td><td>nIRQ output</td></tr> <tr><td>0xD</td><td>Reserved</td></tr> <tr><td>0xE</td><td>Low output</td></tr> <tr><td>0xF</td><td>High output</td></tr> </tbody> </table>	Value	Description	0x0	GPIO disable	0x1	EN1 input	0x2	Reserved	0x3	EN1 input	0x4	DVC1 input	0x5	Reserved	0x6	DVC1 input	0x7	RELOAD input	0x8	PG1 output	0x9	Low output	0xA	Low output	0xB	PG1 output	0xC	nIRQ output	0xD	Reserved	0xE	Low output	0xF	High output
Value	Description																																				
0x0	GPIO disable																																				
0x1	EN1 input																																				
0x2	Reserved																																				
0x3	EN1 input																																				
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0x6	DVC1 input																																				
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0xC	nIRQ output																																				
0xD	Reserved																																				
0xE	Low output																																				
0xF	High output																																				
[0]	RW	GPIO2_OBUF	<p>GPIO output buffer select. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0x0</td><td>open-drain output</td></tr> <tr><td>0x1</td><td>push-pull output</td></tr> </tbody> </table>	Value	Description	0x0	open-drain output	0x1	push-pull output																												
Value	Description																																				
0x0	open-drain output																																				
0x1	push-pull output																																				

**Table 37: SYS\_GPIO2\_1 (0x0015)**

Bit	Type	Field Name	Description
[7]	RW	GPIO2_DEB_FALL	GPI debounce falling edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

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Bit	Type	Field Name	Description										
[6]	RW	GPIO2_DEB_RISE	GPI debounce rising edge. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)										
[5:4]	RW	GPIO2_DEB	<p>GPI debounce time. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>100 us debounce</td> </tr> <tr> <td>0x1</td> <td>1 ms debounce</td> </tr> <tr> <td>0x2</td> <td>10 ms debounce</td> </tr> <tr> <td>0x3</td> <td>100 ms debounce</td> </tr> </tbody> </table>	Value	Description	0x0	100 us debounce	0x1	1 ms debounce	0x2	10 ms debounce	0x3	100 ms debounce
Value	Description												
0x0	100 us debounce												
0x1	1 ms debounce												
0x2	10 ms debounce												
0x3	100 ms debounce												
[3]	RW	GPIO2_PUPD	<p>GPIO pull-up/pull-down enable. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</td> </tr> <tr> <td>0x1</td> <td>GPI: pull-down enabled, GPO: pull-up to AVDD enabled</td> </tr> </tbody> </table>	Value	Description	0x0	GPI: pull-down disabled, GPO: pull-up to AVDD disabled	0x1	GPI: pull-down enabled, GPO: pull-up to AVDD enabled				
Value	Description												
0x0	GPI: pull-down disabled, GPO: pull-up to AVDD disabled												
0x1	GPI: pull-down enabled, GPO: pull-up to AVDD enabled												
[2]	RW	GPIO2_POL	<p>GPIO polarity. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPIO is active-high</td> </tr> <tr> <td>0x1</td> <td>GPIO is active-low</td> </tr> </tbody> </table>	Value	Description	0x0	GPIO is active-high	0x1	GPIO is active-low				
Value	Description												
0x0	GPIO is active-high												
0x1	GPIO is active-low												
[1:0]	RW	GPIO2_TRIG	<p>GPI trigger type. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Dual-edge triggered</td> </tr> <tr> <td>0x1</td> <td>Positive-edge triggered</td> </tr> <tr> <td>0x2</td> <td>Negative-edge triggered</td> </tr> <tr> <td>0x3</td> <td>Reserved (No trigger)</td> </tr> </tbody> </table>	Value	Description	0x0	Dual-edge triggered	0x1	Positive-edge triggered	0x2	Negative-edge triggered	0x3	Reserved (No trigger)
Value	Description												
0x0	Dual-edge triggered												
0x1	Positive-edge triggered												
0x2	Negative-edge triggered												
0x3	Reserved (No trigger)												

**Table 38: SYS\_GPIO3\_0 (0x0016)**

Bit	Type	Field Name	Description										
[4:1]	R	GPIO3_MODE	<p>GPIO function mode select</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPIO disable</td> </tr> <tr> <td>0x1</td> <td>EN1 input</td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td>EN1 input</td> </tr> </tbody> </table>	Value	Description	0x0	GPIO disable	0x1	EN1 input	0x2	Reserved	0x3	EN1 input
Value	Description												
0x0	GPIO disable												
0x1	EN1 input												
0x2	Reserved												
0x3	EN1 input												

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Bit	Type	Field Name	Description
			0x4 DVC1 input 0x5 Reserved 0x6 DVC1 input 0x7 RELOAD input 0x8 PG1 output 0x9 Low output 0xA Low output 0xB PG1 output 0xC nIRQ output 0xD Reserved 0xE Low output 0xF High output
[0]	R	GPIO3_OBUF	GPIO output buffer select <b>Value</b> <b>Description</b> 0x0          open-drain output 0x1          push-pull output

**Table 39: SYS\_GPIO3\_1 (0x0017)**

Bit	Type	Field Name	Description
[7]	R	GPIO3_DEB_FALL	GPI debounce falling edge
[6]	R	GPIO3_DEB_RISE	GPI debounce rising edge
[5:4]	R	GPIO3_DEB	GPI debounce time <b>Value</b> <b>Description</b> 0x0          100 us debounce 0x1          1 ms debounce 0x2          10 ms debounce 0x3          100 ms debounce
[3]	R	GPIO3_PUPD	GPIO pull-up/pull-down enable <b>Value</b> <b>Description</b> 0x0          GPI: pull-down disabled, GPO: pull-up to AVDD disabled 0x1          GPI: pull-down enabled, GPO: pull-up to AVDD enabled
[2]	R	GPIO3_POL	GPIO polarity <b>Value</b> <b>Description</b> 0x0          GPIO is active-high 0x1          GPIO is active-low

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description										
[1:0]	R	GPIO3_TRIG	GPI trigger type <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Dual-edge triggered</td> </tr> <tr> <td>0x1</td> <td>Positive-edge triggered</td> </tr> <tr> <td>0x2</td> <td>Negative-edge triggered</td> </tr> <tr> <td>0x3</td> <td>Reserved (No trigger)</td> </tr> </tbody> </table>	Value	Description	0x0	Dual-edge triggered	0x1	Positive-edge triggered	0x2	Negative-edge triggered	0x3	Reserved (No trigger)
Value	Description												
0x0	Dual-edge triggered												
0x1	Positive-edge triggered												
0x2	Negative-edge triggered												
0x3	Reserved (No trigger)												

**Table 40: SYS\_GPIO4\_0 (0x0018)**

Bit	Type	Field Name	Description																																		
[4:1]	R	GPIO4_MODE	GPIO function mode select <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPIO disable</td> </tr> <tr> <td>0x1</td> <td>EN1 input</td> </tr> <tr> <td>0x2</td> <td>Reserved</td> </tr> <tr> <td>0x3</td> <td>EN1 input</td> </tr> <tr> <td>0x4</td> <td>DVC1 input</td> </tr> <tr> <td>0x5</td> <td>Reserved</td> </tr> <tr> <td>0x6</td> <td>DVC1 input</td> </tr> <tr> <td>0x7</td> <td>RELOAD input</td> </tr> <tr> <td>0x8</td> <td>PG1 output</td> </tr> <tr> <td>0x9</td> <td>Low output</td> </tr> <tr> <td>0xA</td> <td>Low output</td> </tr> <tr> <td>0xB</td> <td>PG1 output</td> </tr> <tr> <td>0xC</td> <td>nIRQ output</td> </tr> <tr> <td>0xD</td> <td>Reserved</td> </tr> <tr> <td>0xE</td> <td>Low output</td> </tr> <tr> <td>0xF</td> <td>High output</td> </tr> </tbody> </table>	Value	Description	0x0	GPIO disable	0x1	EN1 input	0x2	Reserved	0x3	EN1 input	0x4	DVC1 input	0x5	Reserved	0x6	DVC1 input	0x7	RELOAD input	0x8	PG1 output	0x9	Low output	0xA	Low output	0xB	PG1 output	0xC	nIRQ output	0xD	Reserved	0xE	Low output	0xF	High output
Value	Description																																				
0x0	GPIO disable																																				
0x1	EN1 input																																				
0x2	Reserved																																				
0x3	EN1 input																																				
0x4	DVC1 input																																				
0x5	Reserved																																				
0x6	DVC1 input																																				
0x7	RELOAD input																																				
0x8	PG1 output																																				
0x9	Low output																																				
0xA	Low output																																				
0xB	PG1 output																																				
0xC	nIRQ output																																				
0xD	Reserved																																				
0xE	Low output																																				
0xF	High output																																				
[0]	R	GPIO4_OBUF	GPIO output buffer select <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>open-drain output</td> </tr> <tr> <td>0x1</td> <td>push-pull output</td> </tr> </tbody> </table>	Value	Description	0x0	open-drain output	0x1	push-pull output																												
Value	Description																																				
0x0	open-drain output																																				
0x1	push-pull output																																				

**Table 41: SYS\_GPIO4\_1 (0x0019)**

Bit	Type	Field Name	Description
[7]	R	GPIO4_DEB_FALL	GPI debounce falling edge
[6]	R	GPIO4_DEB_RISE	GPI debounce rising edge
[5:4]	R	GPIO4_DEB	GPI debounce time

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description										
			<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>100 us debounce</td> </tr> <tr> <td>0x1</td> <td>1 ms debounce</td> </tr> <tr> <td>0x2</td> <td>10 ms debounce</td> </tr> <tr> <td>0x3</td> <td>100 ms debounce</td> </tr> </tbody> </table>	Value	Description	0x0	100 us debounce	0x1	1 ms debounce	0x2	10 ms debounce	0x3	100 ms debounce
Value	Description												
0x0	100 us debounce												
0x1	1 ms debounce												
0x2	10 ms debounce												
0x3	100 ms debounce												
[3]	R	GPIO4_PUPD	GPIO pull-up/pull-down enable <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPI: pull-down disabled, GPO: pull-up to AVDD disabled</td> </tr> <tr> <td>0x1</td> <td>GPI: pull-down enabled, GPO: pull-up to AVDD enabled</td> </tr> </tbody> </table>	Value	Description	0x0	GPI: pull-down disabled, GPO: pull-up to AVDD disabled	0x1	GPI: pull-down enabled, GPO: pull-up to AVDD enabled				
Value	Description												
0x0	GPI: pull-down disabled, GPO: pull-up to AVDD disabled												
0x1	GPI: pull-down enabled, GPO: pull-up to AVDD enabled												
[2]	R	GPIO4_POL	GPIO polarity <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>GPIO is active-high</td> </tr> <tr> <td>0x1</td> <td>GPIO is active-low</td> </tr> </tbody> </table>	Value	Description	0x0	GPIO is active-high	0x1	GPIO is active-low				
Value	Description												
0x0	GPIO is active-high												
0x1	GPIO is active-low												
[1:0]	R	GPIO4_TRIG	GPI trigger type <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Dual-edge triggered</td> </tr> <tr> <td>0x1</td> <td>Positive-edge triggered</td> </tr> <tr> <td>0x2</td> <td>Negative-edge triggered</td> </tr> <tr> <td>0x3</td> <td>Reserved (No trigger)</td> </tr> </tbody> </table>	Value	Description	0x0	Dual-edge triggered	0x1	Positive-edge triggered	0x2	Negative-edge triggered	0x3	Reserved (No trigger)
Value	Description												
0x0	Dual-edge triggered												
0x1	Positive-edge triggered												
0x2	Negative-edge triggered												
0x3	Reserved (No trigger)												

### 6.2.1 Buck1

Table 42: BUCK\_BUCK1\_0 (0x0020)

Bit	Type	Field Name	Description																		
[6:4]	RW	CH1_SR_DVC_DWN	Voltage slew-rate for DVC ramp-down <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>10 mV / 8 us</td> </tr> <tr> <td>0x1</td> <td>10 mV / 4 us</td> </tr> <tr> <td>0x2</td> <td>10 mV / 2 us</td> </tr> <tr> <td>0x3</td> <td>10 mV / 1 us</td> </tr> <tr> <td>0x4</td> <td>20 mV / 1 us</td> </tr> <tr> <td>0x5</td> <td>Reserved</td> </tr> <tr> <td>0x6</td> <td>Reserved</td> </tr> <tr> <td>0x7</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x0	10 mV / 8 us	0x1	10 mV / 4 us	0x2	10 mV / 2 us	0x3	10 mV / 1 us	0x4	20 mV / 1 us	0x5	Reserved	0x6	Reserved	0x7	Reserved
Value	Description																				
0x0	10 mV / 8 us																				
0x1	10 mV / 4 us																				
0x2	10 mV / 2 us																				
0x3	10 mV / 1 us																				
0x4	20 mV / 1 us																				
0x5	Reserved																				
0x6	Reserved																				
0x7	Reserved																				
[3:1]	RW	CH1_SR_DVC_UP	Voltage slew-rate for DVC ramp-up <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> </tbody> </table>	Value	Description																
Value	Description																				



## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			0x0      10 mV / 8 us 0x1      10 mV / 4 us 0x2      10 mV / 2 us 0x3      10 mV / 1 us 0x4      20 mV / 1 us 0x5      40 mV / 1 us 0x6      Reserved 0x7      Reserved
[0]	RW	CH1_EN	Channel enable. Write 0x1 to enable the buck. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)

**Table 43: BUCK\_BUCK1\_1 (0x0021)**

Bit	Type	Field Name	Description
[6:4]	RW	CH1_SR_SHDN	Voltage slew-rate during shut-down  <b>Value      Description</b> 0x0      10 mV / 8 us 0x1      10 mV / 4 us 0x2      10 mV / 2 us 0x3      10 mV / 1 us 0x4      20 mV / 1 us 0x5      Reserved 0x6      Reserved 0x7      Immediate power-down
[3:1]	RW	CH1_SR_STARTUP	Voltage slew-rate during start-up  <b>Value      Description</b> 0x0      10 mV / 8 us 0x1      10 mV / 4 us 0x2      10 mV / 2 us 0x3      10 mV / 1 us 0x4      20 mV / 1 us 0x5      40 mV / 1 us 0x6      Reserved 0x7      Reserved
[0]	RW	CH1_PD_DIS	LX Pull down while BUCK is off. Write 0x1 to disable this function.

## High-Performance, 13 A/20 A Peak, DC-DC Converter

**Table 44: BUCK\_BUCK1\_2 (0x0022)**

Bit	Type	Field Name	Description																																		
[3:0]	RW	CH1_ILIM	Select OCP threshold (A)																																		
			<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Reserved</td> </tr> <tr> <td>0x1</td> <td>6.5</td> </tr> <tr> <td>0x2</td> <td>7.5</td> </tr> <tr> <td>0x3</td> <td>8.5</td> </tr> <tr> <td>0x4</td> <td>9.5</td> </tr> <tr> <td>0x5</td> <td>10.5</td> </tr> <tr> <td>0x6</td> <td>11.5</td> </tr> <tr> <td>0x7</td> <td>12.5</td> </tr> <tr> <td>0x8</td> <td>13.5</td> </tr> <tr> <td>0x9</td> <td>14.5</td> </tr> <tr> <td>0xA</td> <td>15.5</td> </tr> <tr> <td>0xB</td> <td>16.5</td> </tr> <tr> <td>0xC</td> <td>17.5</td> </tr> <tr> <td>0xD</td> <td>18.5</td> </tr> <tr> <td>0xE</td> <td>19.5</td> </tr> <tr> <td>0xF</td> <td>Disable</td> </tr> </tbody> </table>	Value	Description	0x0	Reserved	0x1	6.5	0x2	7.5	0x3	8.5	0x4	9.5	0x5	10.5	0x6	11.5	0x7	12.5	0x8	13.5	0x9	14.5	0xA	15.5	0xB	16.5	0xC	17.5	0xD	18.5	0xE	19.5	0xF	Disable
Value	Description																																				
0x0	Reserved																																				
0x1	6.5																																				
0x2	7.5																																				
0x3	8.5																																				
0x4	9.5																																				
0x5	10.5																																				
0x6	11.5																																				
0x7	12.5																																				
0x8	13.5																																				
0x9	14.5																																				
0xA	15.5																																				
0xB	16.5																																				
0xC	17.5																																				
0xD	18.5																																				
0xE	19.5																																				
0xF	Disable																																				

**Table 45: BUCK\_BUCK1\_3 (0x0023)**

Bit	Type	Field Name	Description																								
[7:0]	R	CH1_VMAX	VOUT max setting (V): From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV This is a read-only register.																								
			<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Reserved</td> </tr> <tr> <td>0x31</td> <td>Reserved</td> </tr> <tr> <td>0x32</td> <td>0.5</td> </tr> <tr> <td>0x33</td> <td>0.51</td> </tr> <tr> <td>...</td> <td>+0.01 steps</td> </tr> <tr> <td>0x63</td> <td>0.99</td> </tr> <tr> <td>0x64</td> <td>1</td> </tr> <tr> <td>0x65</td> <td>1.01</td> </tr> <tr> <td>...</td> <td>+0.01 steps</td> </tr> <tr> <td>0x81</td> <td>1.29</td> </tr> <tr> <td>0x82</td> <td>1.3</td> </tr> </tbody> </table>	Value	Description	0x00	Reserved	0x31	Reserved	0x32	0.5	0x33	0.51	...	+0.01 steps	0x63	0.99	0x64	1	0x65	1.01	...	+0.01 steps	0x81	1.29	0x82	1.3
Value	Description																										
0x00	Reserved																										
0x31	Reserved																										
0x32	0.5																										
0x33	0.51																										
...	+0.01 steps																										
0x63	0.99																										
0x64	1																										
0x65	1.01																										
...	+0.01 steps																										
0x81	1.29																										
0x82	1.3																										

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Bit	Type	Field Name	Description
			0x83      Reserved
			0xFF      Reserved

**Table 46: BUCK\_BUCK1\_4 (0x0024)**

Bit	Type	Field Name	Description										
[4]	RW	CH1_VSEL	Output voltage and operation selection: 0: A, 1: B. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)										
[3:2]	RW	CH1_B_MODE	Operation mode selection. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Force PFM operation</td> </tr> <tr> <td>0x1</td> <td>Force PWM operation (full phase)</td> </tr> <tr> <td>0x2</td> <td>Force PWM operation (with phase shedding)</td> </tr> <tr> <td>0x3</td> <td>Auto mode</td> </tr> </tbody> </table>	Value	Description	0x0	Force PFM operation	0x1	Force PWM operation (full phase)	0x2	Force PWM operation (with phase shedding)	0x3	Auto mode
Value	Description												
0x0	Force PFM operation												
0x1	Force PWM operation (full phase)												
0x2	Force PWM operation (with phase shedding)												
0x3	Auto mode												
[1:0]	RW	CH1_A_MODE	Operation mode selection. Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting)  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>Force PFM operation</td> </tr> <tr> <td>0x1</td> <td>Force PWM operation (full phase)</td> </tr> <tr> <td>0x2</td> <td>Force PWM operation (with phase shedding)</td> </tr> <tr> <td>0x3</td> <td>Auto mode</td> </tr> </tbody> </table>	Value	Description	0x0	Force PFM operation	0x1	Force PWM operation (full phase)	0x2	Force PWM operation (with phase shedding)	0x3	Auto mode
Value	Description												
0x0	Force PFM operation												
0x1	Force PWM operation (full phase)												
0x2	Force PWM operation (with phase shedding)												
0x3	Auto mode												

**Table 47: BUCK\_BUCK1\_5 (0x0025)**

Bit	Type	Field Name	Description																		
[7:0]	RW	CH1_A_VOUT	Output voltage setting A: Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV  <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Reserved</td> </tr> <tr> <td>0x31</td> <td>Reserved</td> </tr> <tr> <td>0x32</td> <td>0.5</td> </tr> <tr> <td>0x33</td> <td>0.51</td> </tr> <tr> <td>...</td> <td>+0.01 steps</td> </tr> <tr> <td>0x63</td> <td>0.99</td> </tr> <tr> <td>0x64</td> <td>1</td> </tr> <tr> <td>0x65</td> <td>1.01</td> </tr> </tbody> </table>	Value	Description	0x00	Reserved	0x31	Reserved	0x32	0.5	0x33	0.51	...	+0.01 steps	0x63	0.99	0x64	1	0x65	1.01
Value	Description																				
0x00	Reserved																				
0x31	Reserved																				
0x32	0.5																				
0x33	0.51																				
...	+0.01 steps																				
0x63	0.99																				
0x64	1																				
0x65	1.01																				

## High-Performance, 13 A/20 A Peak, DC-DC Converter

Bit	Type	Field Name	Description
			... +0.01 steps
			0x81 1.29
			0x82 1.3
			0x83 Reserved
			0xFF Reserved

**Table 48: BUCK\_BUCK1\_6 (0x0026)**

Bit	Type	Field Name	Description																												
[7:0]	RW	CH1_B_VOUT	Output voltage setting B: Initial value is determined by CONF pin setting during start-up and if the CONF pin is enabled (OTP setting) From 0.50 V (0x32) to 1.30 V (0x82) in steps of 10 mV																												
			<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Reserved</td> </tr> <tr> <td>0x31</td> <td>Reserved</td> </tr> <tr> <td>0x32</td> <td>0.5</td> </tr> <tr> <td>0x33</td> <td>0.51</td> </tr> <tr> <td>...</td> <td>+0.01 steps</td> </tr> <tr> <td>0x63</td> <td>0.99</td> </tr> <tr> <td>0x64</td> <td>1</td> </tr> <tr> <td>0x65</td> <td>1.01</td> </tr> <tr> <td>...</td> <td>+0.01 steps</td> </tr> <tr> <td>0x81</td> <td>1.29</td> </tr> <tr> <td>0x82</td> <td>1.3</td> </tr> <tr> <td>0x83</td> <td>Reserved</td> </tr> <tr> <td>0xFF</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	0x00	Reserved	0x31	Reserved	0x32	0.5	0x33	0.51	...	+0.01 steps	0x63	0.99	0x64	1	0x65	1.01	...	+0.01 steps	0x81	1.29	0x82	1.3	0x83	Reserved	0xFF	Reserved
Value	Description																														
0x00	Reserved																														
0x31	Reserved																														
0x32	0.5																														
0x33	0.51																														
...	+0.01 steps																														
0x63	0.99																														
0x64	1																														
0x65	1.01																														
...	+0.01 steps																														
0x81	1.29																														
0x82	1.3																														
0x83	Reserved																														
0xFF	Reserved																														

**Table 49: BUCK\_BUCK1\_7 (0x0027)**

Bit	Type	Field Name	Description										
[1:0]	RW	CH1_RIPPLE_CANCEL	Ripple cancel control										
			<table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>No ripple cancel</td> </tr> <tr> <td>0x1</td> <td>Small ripple cancel</td> </tr> <tr> <td>0x2</td> <td>Mid ripple cancel</td> </tr> <tr> <td>0x3</td> <td>Large ripple cancel</td> </tr> </tbody> </table>	Value	Description	0x0	No ripple cancel	0x1	Small ripple cancel	0x2	Mid ripple cancel	0x3	Large ripple cancel
Value	Description												
0x0	No ripple cancel												
0x1	Small ripple cancel												
0x2	Mid ripple cancel												
0x3	Large ripple cancel												

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 6.2.2 OTP Control

#### 6.2.2.1 Serialization

**Table 50: OTP\_DEVICE\_ID (0x0048)**

Bit	Type	Field Name	Description
[7:0]	R	DEV_ID	Device ID; hard-coded or metal-programmed

**Table 51: OTP\_VARIANT\_ID (0x0049)**

Bit	Type	Field Name	Description
[7:4]	R	MRC	Mask Revision Code
[3:0]	R	VRC	Chip Variant Code; e.g. package variants.

**Table 52: OTP\_CUSTOMER\_ID (0x004A)**

Bit	Type	Field Name	Description
[7:0]	R	CUST_ID	Customer ID

**Table 53: OTP\_CONFIG\_ID (0x004B)**

Bit	Type	Field Name	Description
[7:0]	R	CONFIG_REV	OTP settings revision

High-Performance, 13 A/20 A Peak, DC-DC Converter

7 Package Information

7.1 Package Outlines

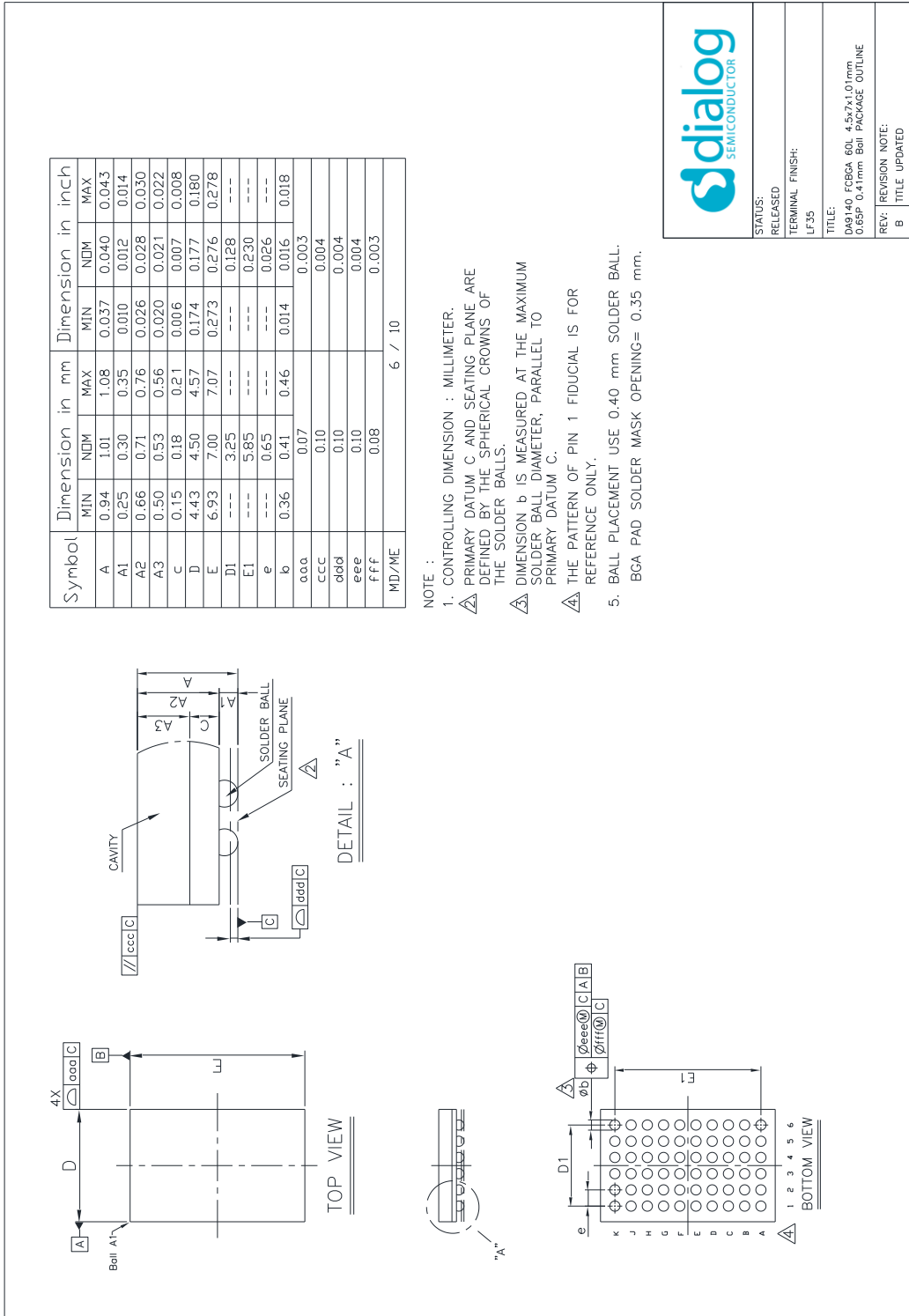


Figure 12: Package Outline Drawing

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 7.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 54](#).

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The DA9142 package is qualified for MSL 3.

**Table 54: MSL Classification**

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

### 7.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 8 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your [Renesas local sales representative](#).

**Table 55: Ordering Information for Consumer / Industrial Applications**

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9142-xxF71	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Tray	364
DA9142-xxF72	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Reel	2600

**Table 56: Ordering Information for Automotive Applications**

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9142-xxF71-A	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Tray	364
DA9142-xxF72-A	60 FCBGA	4.5 x 7 x 1.01 0.65 mm pitch	Reel	2600



## High-Performance, 13 A/20 A Peak, DC-DC Converter

### 9 Application Information

The following recommended components are examples selected from requirements of a typical application.

#### 9.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

**Table 57: Recommended Automotive Grade Capacitor Types**

Application	Value (μF)	Size	Temp. Char.	Tol. (%)	V-Rate (V)	Type
VOUT output bypass	22	1206	X7R ±15%	±20	6.3	Murata GCM31CR70J226ME23L
PVDDx bypass	10	0805	X7R ±15%	±10	16	Murata GCM21BC71C106KE36L
PVDDx bypass for VSYS < 4V	10	0603	X7R ±15%	±10	6.3	Murata GCM188D70J106ME36L
AVDD bypass	1	0805	X7R ±15%	±10	50	Murata GCM21BR71H105KA03L

#### 9.2 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current and ISAT  
ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current at 40°C temperature rise.
- DC resistance  
Critical for the converter efficiency and should therefore be minimized.

**Table 58: Recommended Inductor Types**

Value (nH)	Size (mm)	IMAX (DC) (A)	ISAT (A)	Tol. (%)	DC Resistance (mΩ)	Type
112	3.2 x 2.5 x 2.5	20	31	20	1.9	TDK CLT3225AR11MI3
110	4.0 x 4.0 x 2.1	29	29	20	1.4	Coilcraft XGL4020-111MEC
100	5.3 x 5.1 x 3.0	18.3	37.1	20	2.7	TDK SPM5030VT-R10M-D

High-Performance, 13 A/20 A Peak, DC-DC Converter

10 Layout Guidelines

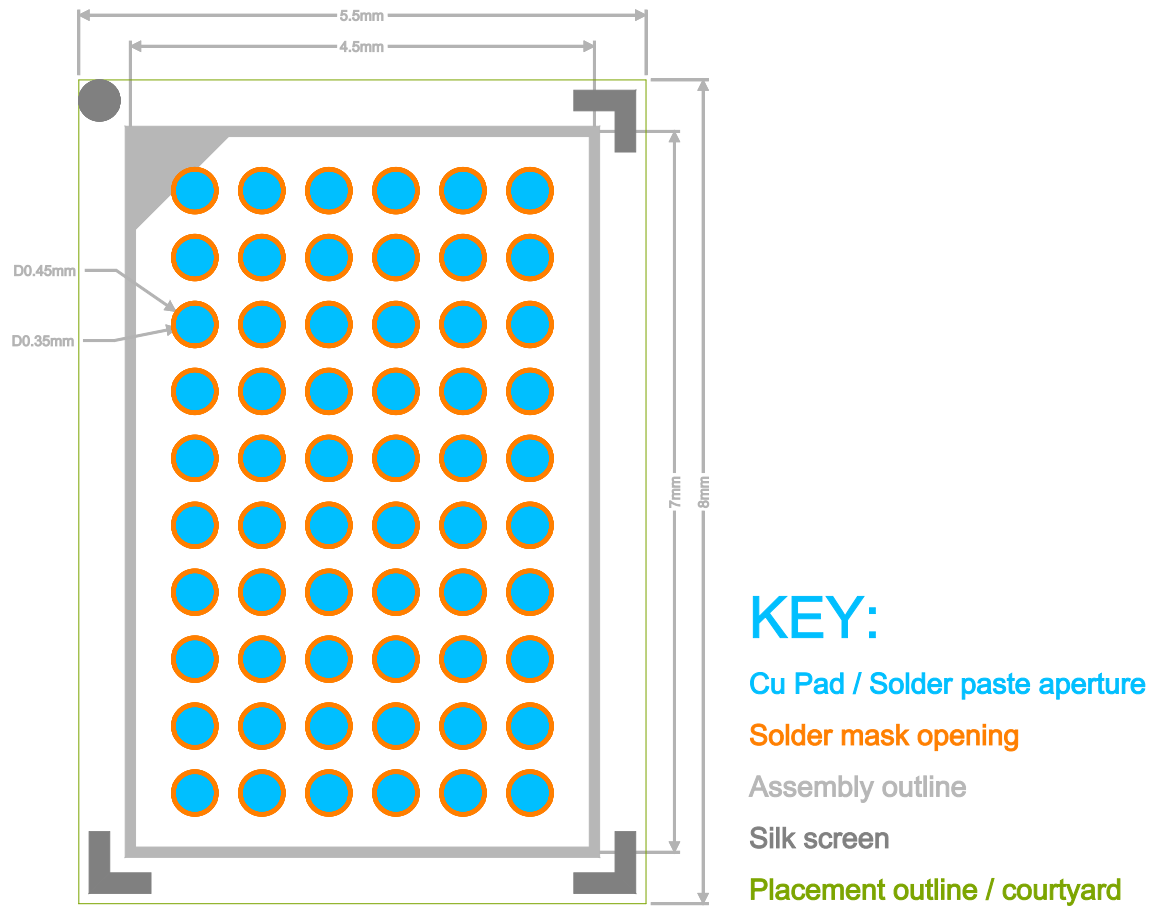


Figure 13: DA9142 Footprint

## High-Performance, 13 A/20 A Peak, DC-DC Converter

### Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via <a href="http://www.dialog-semiconductor.com">www.dialog-semiconductor.com</a> .
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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