General Description

DA9210 is a multi-phase synchronous step-down converter suitable for supplying the CPU power in smartphones, tablets, UltrabooksTM, and other handheld applications, which require high currents to run the processor core.

DA9210 is designed to operate with four phases, each phase using a small external 0.47 µH inductor. The buck is capable of delivering up to 12 A continuous output current with an output voltage of 0.3 V to 1.57 V. The input voltage range of 2.8 V to 5.5 V makes it suited for a wide variety of low voltage systems, including all Li-Ion battery supplied applications. Two DA9210s can be used in parallel to deliver an output current of up to 24 A.

The DA9210 point-of-load remote-sensing feature guarantees the highest accuracy while supporting multiple PCB routing scenarios without loss of performance. The highly-integrated design removes the need for external switching FETs or Schottky diodes.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and ensures a slope controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage dependent on the processor load. This is done via direct register write through the communication interface (I^2C or SPI compatible), via the dedicated DVC control interface, or via a programmable input pin.

DA9210 integrates over-temperature and over-current protection for increased system reliability, without the need for external sensing components. A Power Good and Over-Current Alarm output informs the CPU of an out range voltage output and if the current exceeds a programmable limit, thereby enabling the processor to reduce its consumption before the supply rail collapses.

Key Features

- 2.8 V to 5.5 V input voltage
- 0.3 V to 1.57 V output voltage
- 12 A output current
- 24 A output current in parallel configuration
- 3 MHz nominal switching frequency
  - Enables use of low-profile inductors
- Output voltage accuracy ±2.5 %
- Dynamic Voltage Control (DVC)
- Automatic phase shedding
- Integrated power switches
- Remote sensing at point-of-load
- Power Good and Over-Current Alarm signal
- Interfaces:
  - I^2C and SPI
  - Dedicated DVC
  - GPIO
- Adjustable soft-start
- -40 ºC to +125 ºC junction temperature operation
- Regulator supervision with automatic under-voltage and over-voltage protection
- AEC Q100 grade 3 automotive option
- Package 48 WLCSP (Route Easy™, equivalent to 0.8 mm pitch)
- Package 42 VFBGA 0.8 mm pitch (automotive) DA9210-A

Applications

- High performance multi-core system-on-chip (SoC) applications
- Smartphones
- Mobile phones
- Ultrabooks™
- Tablet PCs
- In-car infotainment/dashboard
- Portable navigation devices
- TV and media players
- Embedded industrial systems

Contents

Figures

Tables

1 Terms and Definitions

CPU	Central Processing Unit
DVC	Dynamic Voltage Control
FET	Field Effect Transistor
GPIO	General Purpose Input/Output
IRQ	Interrupt ReQuest
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMIC	Power Management IC
SoC	System on (a) Chip

2 References

[1] AN-PM-052, Application Note, Dialog Semiconductor.

3 Block Diagram

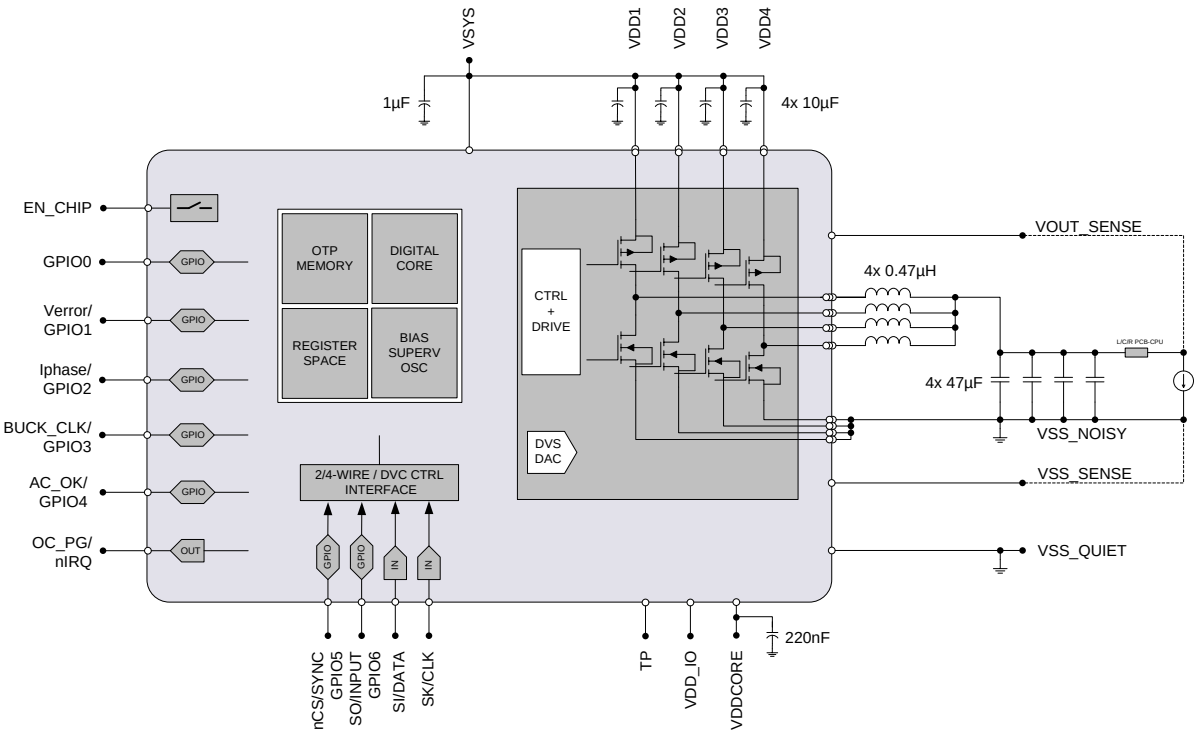


Figure 1: Block Diagram

4 Pinout

4.1 Pin Configuration (48 WLCSP)

Figure 2: Connection Diagram (48 WLCSP)

Table 1: Pin Description (48 WLCSP)

Pin No.	Pin Name	Alternate Function	Type	Description
A1, B2, B4	LX1		AO	Switching node for phase 1
J1, H2, H4	LX2		AO	Switching node for phase 2
A13, B10, B12	LX3		AO	Switching node for phase 3
J13, H10, H12	LX4		AO	Switching node for phase 4
A3, A5	VDD1		PS	Supply voltage for phase 1. To be connected to VSYS
J3, J5	VDD2		PS	Supply voltage for phase 2. To be connected to VSYS
A9, A11	VDD3		PS	Supply voltage for phase 3. To be connected to VSYS
J9, J11	VDD4		PS	Supply voltage for phase 4. To be connected to VSYS
C13	EN_CHIP		DI	IC Enable Signal

Pin No.	Pin Name	Alternate Function	Type	Description
C1	OC_PG	nIRQ	DO	Output for Over Current Alarm and Power Good signal, IRQ line towards the host
G13	VDD_IO		PS	I/O voltage rail
E1	VOUT_SENSE		AI	Output and sense node for the buck
D2	VSS_SENSE		AI	Ground sense node for the buck
F2	VDDCORE		AO	Regulated supply for internal circuitry 2.5 V (decouple with 220 nF)
F12	GPIO0		AI/DIO	General purpose I/O
D12	VERROR	GPIO1	AIO/DIO	Error amplifier voltage signal for dual parallel mode, general purpose I/O
E13	IPHASE	GPIO2	AIO/DIO	Current distribution signal for dual parallel mode, general purpose I/O
G1	BUCK_CLK	GPIO3	DIO	Buck clock input/output (depending on slave/master function in dual parallel mode), general purpose I/O
B8	AC_OK	GPIO4	DIO	Input from safe charger out to OC_PG signaling, general purpose I/O, input of external 6 MHz clock
H8	nCS/SYNC	GPIO5	DIO	4-WIRE chip select, DVC Interface input clock, general purpose I/O
J7	SO/INPUT	GPIO6	DIO	4-WIRE data output, DVC interface input data, general purpose I/O
B6	SI	DATA	DIO	4-WIRE data input, 2-WIRE data
A7	SK	CLK	DI	4-WIRE/2-WIRE Clock
C7	TP		DIO	Test pin connect to VSS
E3, E11	NC		VSS	Electrically not connected Connect to VSS
H6	VSYS		PS	Supply for IC and input for voltage supervision
G7	VSS_QUIET		VSS	
C3, C5, G3, G5, C9, C11, G9, G11	VSS_NOISY		VSS	

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output open Drain	BP	Back drive Protection
PU	Fixed Pull-Up resistor	SPU	Switchable Pull-Up resistor
PD	Fixed Pull-Down resistor	SPD	Switchable Pull-Down resistor
PS	Power Supply	VSS	Ground

4.2 Pin Configuration (42 VFBGA)

Figure 3: Connection Diagram (42 VFBGA)

Table 3: Pin List (42 VFBGA)

Pin No.	Pin name	Alternate function	Type	Description
B1, B2	LX1		AO	Switching node for phase 1
E1, E2	LX2		AO	Switching node for phase 2
B6, B7	LX3		AO	Switching node for phase 3
E6, E7	LX4		AO	Switching node for phase 4
A1, A2	VDD1		PS	Supply voltage for phase 1. To be connected to VSYS
F1, F2	VDD2		PS	Supply voltage for phase 2. To be connected to VSYS
A6, A7	VDD3		PS	Supply voltage for phase 3. To be connected to VSYS
F6, F7	VDD4		PS	Supply voltage for phase 4. To be connected to VSYS
A5	EN_CHIP		DI	IC Enable Signal
C5	OC_PG	nIRQ	DO	Output for Over Current Alarm and Power Good signal, IRQ line towards the host
A4	VDD_IO		PS	I/O voltage rail
D4	VOUT_SENSE		AI	Output and Sense node for the buck
C4	VSS_SENSE		AI	Ground Sense node for the buck
F5	VDDCORE		AO	Regulated supply for internal circuitry (decouple with 220 nF)
B5	GPIO0		AI/DIO	General purpose I/O
B4	VERROR	GPIO1	AIO/DIO	Error amplifier voltage signal for dual parallel mode, general purpose I/O
E4	IPHASE	GPIO2	AIO/DIO	Current distribution signal for dual parallel mode, general purpose I/O
E5	BUCK_CLK	GPIO3	DIO	Buck clock input/output (depending on slave/master function in dual parallel mode), general purpose I/O
C3	AC_OK	GPIO4	DIO	Input from safe charger out to OC_PG signaling, general purpose I/O, input of external 6 MHz clock
D3	nCS/SYNC	GPIO5	DIO	4-WIRE chip select, DVC Interface input clock , general purpose I/O

Pin No.	Pin name	Alternate function	Type	Description
E3	SO/INPUT	GPIO6	DIO	4-WIRE data output, DVC Interface input data, general purpose I/O
B3	SI	DATA	DIO	4-WIRE data input, 2-WIRE data
A3	SK	CLK	DI	4-WIRE/2-WIRE clock
D5	TP		DIO	Test pin, connect to VSS
F3	VSYS		PS	Supply for IC and input for voltage supervision
F4	VSS_QUIET		VSS	
C1, C2, D1, D2, C6, C7, D6, D7	VSS_NOISY		VSS	

Table 4: Pin Type Definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output Open Drain	BP	Backdrive Protection
PU	Fixed Pull-Up resistor	SPU	Switchable Pull-Up resistor
PD	Fixed Pull-Down resistor	SPD	Switchable Pull-Down resistor
PS	Power Supply	VSS	Ground

5 Absolute Maximum Ratings

Table 5: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
TSTG	Storage temperature		-65	+150	°C
TJ	Operating junction temperature		-40	+150 Note 2	°C
VSYS	Supply voltage		-0.3	5.5	V
All pins except above			-0.3	VSYS + 0.3	V
	ESD protection HBM		2000		V

Note 1 Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 See Sections 13.1 and 10.6 for more detail

6 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VSYS	Supply voltage		2.8		5.5	V
VDD_IO	Supply voltage IO		1.2		3.6 Note 1	V
	Maximum power Dissipation Note 2	Derating factor above T_A = 70 °C: 33 mW/°C 48 WL-CSP	1815	2310		mW
		Derating factor above TA = 70°C: 28 mW/°C 42 VF-BGA	1540	1960		mW

Note 1 VDD_IO must not exceed VSYS

Note 2 Obtain from simulation on a 2S2P 4L JEDEC Board. Influenced by PCB technology and layout.

All voltages are referenced to VSS unless otherwise stated. Currents flowing into DA9210 are deemed positive, currents flowing out are deemed negative. All parameters are valid over the recommended temperature range and power supply range unless otherwise noted. Please note that power dissipation must be limited to avoid overheating of DA9210. Maximum power dissipation should not be reached with maximum ambient temperature.

7 Typical Current Consumptions

Table 7: Typical Current Consumption

Operating Mode	Conditions	Battery (typ)	Unit
OFF mode	EN_CHIP Low	<1	µA
ON mode	EN_CHIP High, BUCK_EN = 0 (excluding the current consumption of the buck)	45	µA

8 Electrical Characteristics

Table 8: DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
EN_ON	EN_CHIP Level on		1.1			V
EN_OFF	EN_CHIP Level off				0.35	V
EN_HYST	EN_CHIP Hysteresis			100		mV
I_{EN_CHIP}	EN_CHIP Input current	$V_{EN\_CHIP} \leq 1.1$ V		100		nA
t_{EN}	IC control start-up time			750		µs
VDDCORE	VDDCORE voltage			2.5		V
VIH	GPI0-6, SYNC, INPUT, CLK, DATA, (2-WIRE mode) Input High Voltage	VDDCORE mode VDD_IO mode	0.7*VDDCORE 0.7*VDD_IO			V
VIL	GPI0-6, SYNC, INPUT, CLK, DATA, (2-WIRE mode) Input Low Voltage	VDDCORE mode VDD_IO mode			0.3*VDDCORE 0.3*VDD_IO	V
VIH	SK, nCS, SI (4-WIRE mode) Input High Voltage		0.7*VDD_IO			V

Parameter	Description	Conditions	Min	Typ	Max	Unit
VIL	SK, nCS, SI (4-WIRE mode) Input Low Voltage				0.3*VDD_IO	V
VOH	GPO0-6, OC_PG, SO (4-WIRE ode) Output High Voltage	Push-pull mode @1 mA VDD_IO ≥1.5 V	0.8*VDD_IO			V
VOL@1 mA	GPO0-6, OC_PG, DATA (2-WIRE mode) SO (4-WIRE mode) Output Low Voltage				0.3	V
VOL @3 mA	DATA (2-WIRE mode) Output				0.24	V
VOL @20 mA	DATA (2-WIRE mode) Output Low Voltage				0.4	V
C_{IN}	CLK, DATA (2-WIRE mode) Input Capacitance			2.5	10	pF
t_{SP}	CLK, DATA (2-WIRE mode) Spike Suppression	Fast/Fast+ mode High Speed mode			50 10	ns
t_{fDA}	DATA (2-WIRE mode)	Fast @ Cb<550 pF HS @ 10<Cb<100 HS @ Cb<400 pF	20 + 0.1 Cb 10 20		120 40 80	ns
t_{OC_DEL}	OC_PG Delay	From over-current detection to OC_PG port asserted			10	ns
t_{OC_ASSERT}	OC_PG Assert	From end of over-current to OC_PG port released	100			ns
t_{OC_PD}	OC_PG Power Down	After disabling the buck until OC_PG released			250	µs
f_{GPI4}	Digital clock input frequency	At GPIO4	-7 %	6.0	+7 %	MHz
D_{GPI4}	Digital clock input duty cycle	At GPIO4		50	10	%

8.1 DC/DC Buck Converter

Unless otherwise noted, the following is valid for VDD = 2.8 V to 5.5 V, COUT = 4x 47 µF, local sensing, f = 3 MHz.

Table 9: DC/DC Buck Converter Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDD	Input voltage	VDD = VSYS	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	100	200 (4x47) (8x22)	400	µF
L_{BUCK}	Inductor value (per phase)	Including current and temperature dependence	-50 %	0.47	+30 %	µH
V_{OUT}	Output voltage Note 1	I_{OUT} = 0 mA to IMAX	0.3		1.57	V
	Output voltage accuracy	VDD = 3.8 V V_{OUT} = 0.9 V TA = 25 °C no load	-0.5		+0.5	%
		VDD = 3.8 V V_{OUT} = 0.9 V TA = -25 °C to +85 °C no load	-1.0		+1.0	%
		Including static line/load regulation and voltage ripple VOUT ≥ 1 V	-2.5		+2.5	%
		Including static line/load regulation and voltage ripple VOUT < 1 V		25		mV
VTR_{LOAD}	Load regulation transient Note 2	IOUT = 0 / 5 A dI/dt = 10 A/µs 4-phase operation V_{OUT} = 1 V		±2		%
VTR_{LINE}	Line regulation transient	VDD = 3.0 to 3.6 V I_{OUT} = I_{MAX} tr = tf = 10 µs		10		mV
	Max resistance PCB for remote sensing Note 3	From output capacitor to sense connection at point of load		10		mΩ
	Max inductance PCB for remote sensing Note 4	From output capacitor to sense connection at point of load		10		nH

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{FB}	Feedback comparator input impedance		500			kΩ
I_{MAX}	Output current	4-phase operation	12000			mA
I_{LIM}	Current limit per phase (programmable) Note 5	BUCK_ILIM = 0010	-20 %	2000 Note 6	20 %	mA
		BUCK_ILIM = 1111	-20 %	4600	20 %	mA
I_{ALARM}	Current alarm threshold (programmable)	BUCK_IALARM = 0 and BUCK_ILIM ≥ 1010	ILIM - 600	ILIM – 300	ILIM - 100	mA
		BUCK_IALARM = 1 and BUCK_ILIM ≥ 1010	ILIM - 1000	ILIM – 600	ILIM - 300	mA
IQ_{ON}	Quiescent current in synchronous rectification mode	4-phase operation No load VDD = 3.7 V		60		mA
I_{MIN_PFM}	Minimum output current in PFM mode	Static output voltage, No DVC Note 7		2		mA
	Switching frequency		2.79	3	3.21	MHz
	Minimum on time			20		ns
t_{ON}	Turn-on time	STARTUP_CTRL = 011		50		µs
	Output pull-down resistor	Can be switched off via BUCK_PD_DIS		150	200	Ω

Note 1 Programmable in 10 mV increments

Note 2 Additional to the DC accuracy. The value is intended measured directly at COUT. In case of remote sensing, parasitics of PCB and external components may affect this value.

Note 3 10 mΩ equivalent to a 5 inch (ca 13 cm) copper trace (ρ = 1.7x10-8 Ω/m), width 6 mm, thickness 35 µm

Note 4 10 nH equivalent to a 5 inch (ca 13 cm) trace routed over a ground plane (approx. 1.2 nH/cm)

Note 5 Peak current on the inductor

Note 6 Minimum value of the accuracy is ±400 mA under all conditions

Note 7 For DVC, see Application Note AN-PM-052

8.2 2-WIRE Control Bus

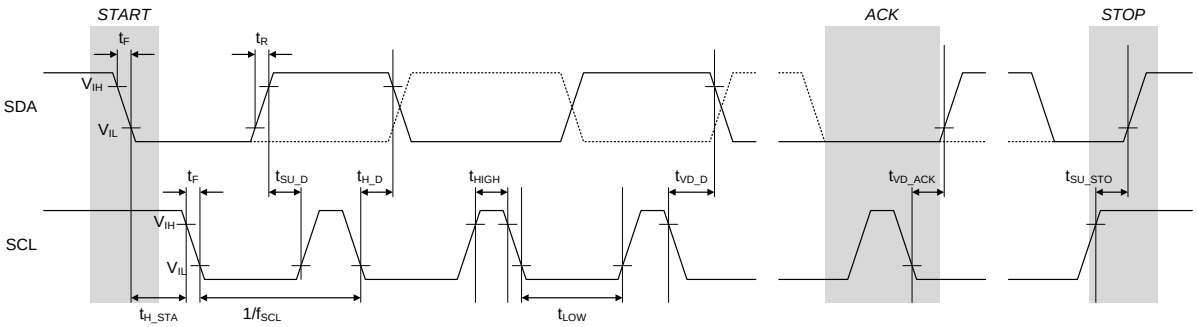


Figure 4: 2-WIRE Interface Timing

Table 10: 2-WIRE Interface Electrical Characteristics

Parameter	Description	Test conditions	Min	Typ	Max	Unit
tBUF	Bus free time STOP to START		0.5			µs
CB	Bus line capacitive load				150	pF
Standard/Fast/Fast mode						
fSCL	SCL clock frequency	Note 1	0		1000	kHz
tSU_STA	Start condition set-up time		0.26			µs
tH_STA	Start condition hold time		0.26			µs
tW_CL	SCL low time		0.5			µs
tW_CH	SCL high time		0.26			µs
tR	2-WIRE SCL and SDA rise time	(input requirement)			1000	ns
tF	2-WIRE SCL and SDA fall time	(input requirement)			300	ns
tSU_D	Data set-up time		50			ns
tH_D	Data hold time		0			ns
tVD_D	Data valid time				0.45	µs
tVD_ACK	Data valid time acknowledge				0.45	µs
tSU_STO	Stop condition set-up time		0.26			µs
High Speed mode						
fSCL	SCL clock frequency	Requires VDDIO ≥ 1.8 V Note 1	0		3400	kHz
tSU_STA	Start condition set-up time		160			ns

Parameter	Description	Test conditions	Min	Typ	Max	Unit
tH_STA	Start condition hold time		160			ns
tW_CL	SCL low time		160			ns
tW_CH	SCL high time		60			ns
tR	2-wire SCL and SDA rise time	(input requirement)			160	ns
tF	2-wire SCL and SDA fall time	(input requirement)			160	ns
tSU_D	Data set-up time		10			ns
tH_D	Data hold-time		0			ns
tSU_STO	Start condition hold time		160			ns

Note 1 Minimum clock frequency is 10 kHz if 2WIRE_TO is enabled

8.3 4-WIRE Control Bus

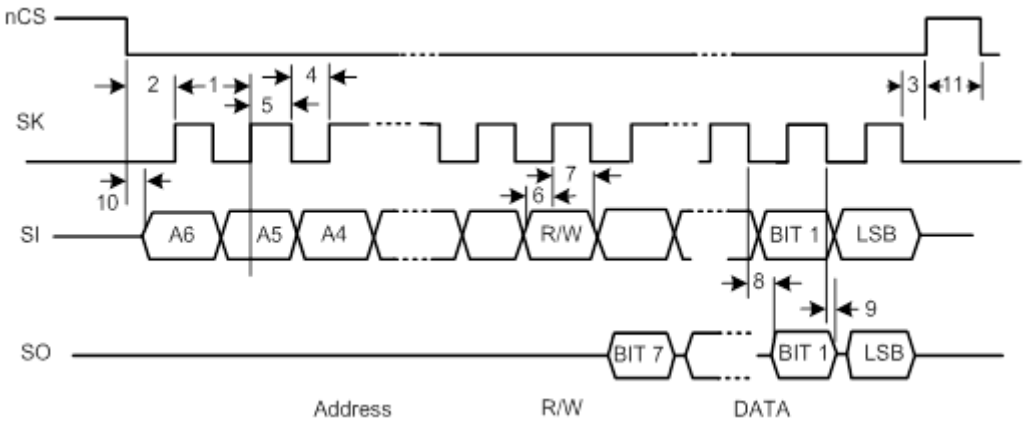


Figure 4: 4-WIRE Bus Timing

NOTE
The above timing is valid for active low and high CS.

Table 11: 4-WIRE Interface Electrical Characteristics

Parameter	Description	Label in Plot	Min	Typ	Max	Unit
C_{LD}	Bus line capacitive load				100	pF
t_C	Cycle time	1	70			ns
t_{CSS}	Enable lead time	2, from CS active to first SK edge	20			ns
t_{SCS}	Enable lag time	3, from last SK edge to CS idle	20			ns

Parameter	Description	Label in Plot	Min	Typ	Max	Unit
t_{CL}	Clock low time	4	0.4 x tC			ns
t_{CH}	Clock high time	5	0.4 x tC			ns
t_{SIS}	Data in setup time	6	5			ns
t_{SIH}	Data in hold time	7	5			ns
t_{SOV}	Data out valid time	8			22	ns
t_{SOH}	Data out hold time	9	6			ns
t_{WCS}	CS inactive time	11	20			ns

8.4 DVC Interface

Table 12: DVC Interface

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{SYNC}	Clock period at SYNC port		40		300	ns
t_{PWH}	High pulse width at SYNC port		12		180	ns
t_{PWL}	Low pulse width at SYNC port		12		180	ns
D_{SYNC}	Duty cycle at SYNC port		40		60	%
t_{SETUP}	Set-up time	INPUT to rising edge of SYNC	10			ns
t_{HOLD}	Hold time	INPUT from rising edge of SYNC	2			ns
t_{RISE}	Rise time	INPUT and SYNC ports	1			ns
t_{FALL}	Fall time	INPUT and SYNC ports	1			ns

8.5 Power Good and Temperature Supervision

Table 13: Power Good and Temperature Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
VGOOD	Power good low threshold			VOUT (Typ) - 0.05		V
VGOOD _HYST	Power good low threshold hyst			50		mV
TEMP_WARN Note 1	Thermal warning		110	125	140	°C
TEMP_CRIT	Thermal shutdown threshold		125	140	155	°C
TEMP_POR	Thermal POR threshold		135	150	165	°C

Note 1 Thermal thresholds are non-overlapping

9 Typical Characteristics

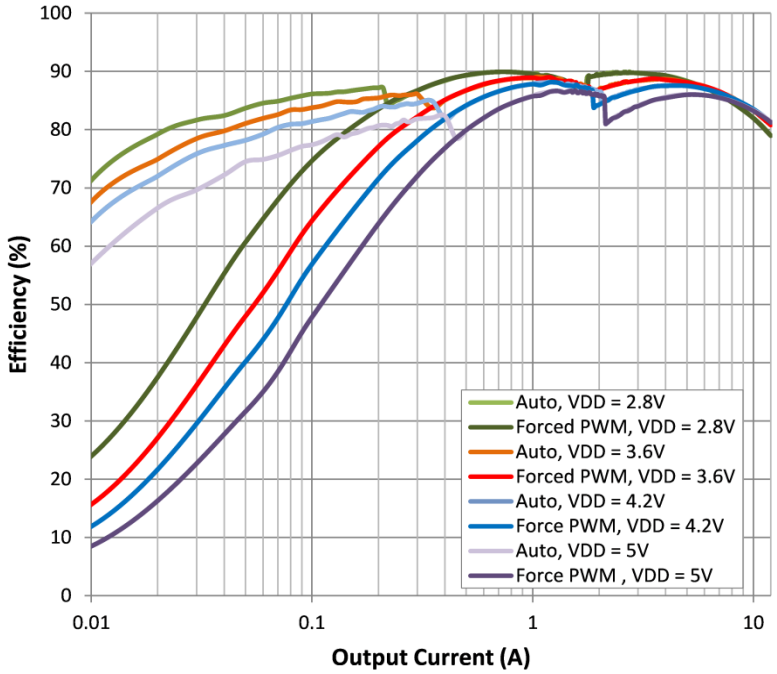


Figure 5: Efficiency vs Output Current V_{OUT} = 1.0 V

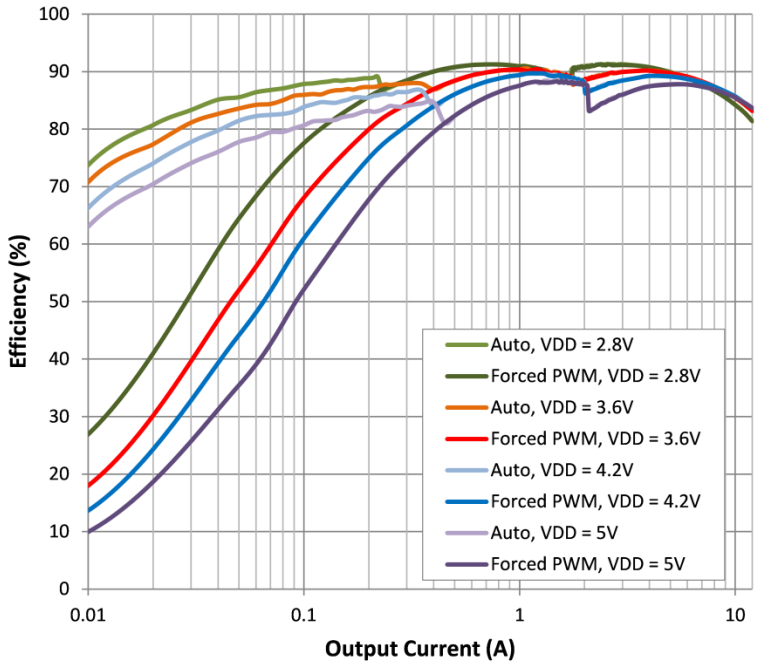


Figure 6: Efficiency vs Output Current V_{OUT} = 1.2 V

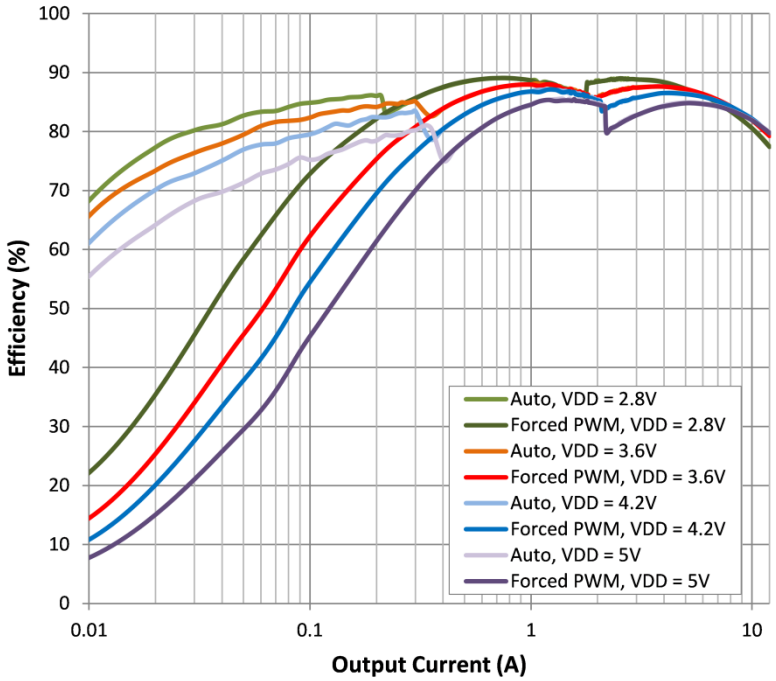


Figure 7: Efficiency vs Output Current V_{OUT} = 0.9 V

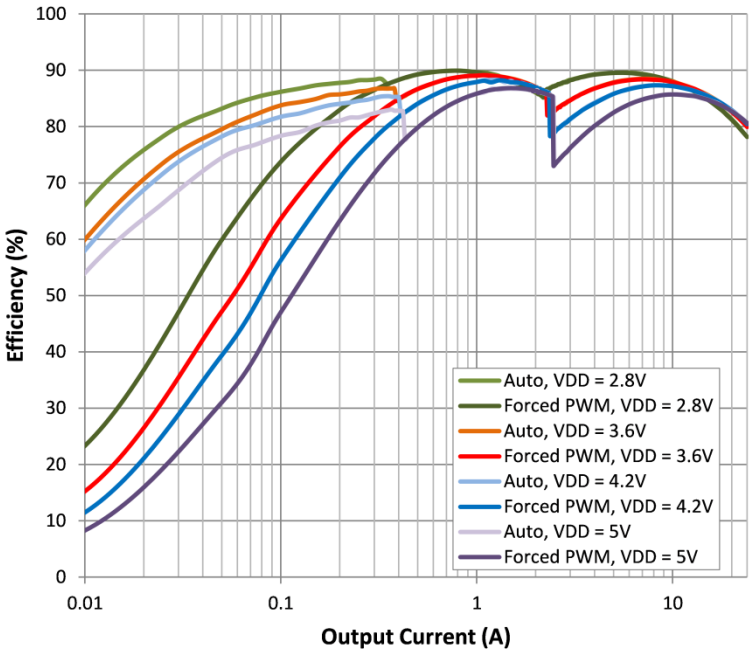


Figure 8: Efficiency vs Output Current V_{OUT} = 1.0 V, dual parallel mode (24 A max)

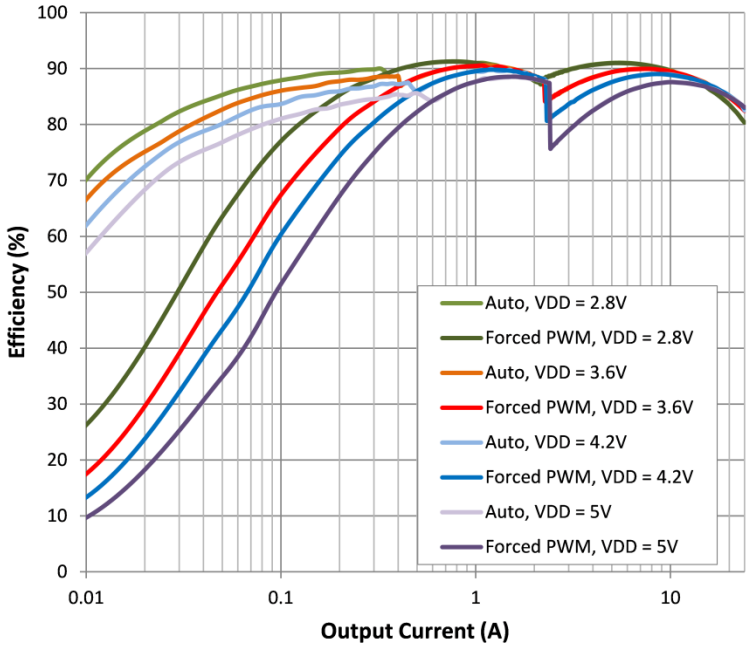


Figure 9: Efficiency vs Output Current V_{OUT} = 1.2 V, dual parallel mode (24 A max)

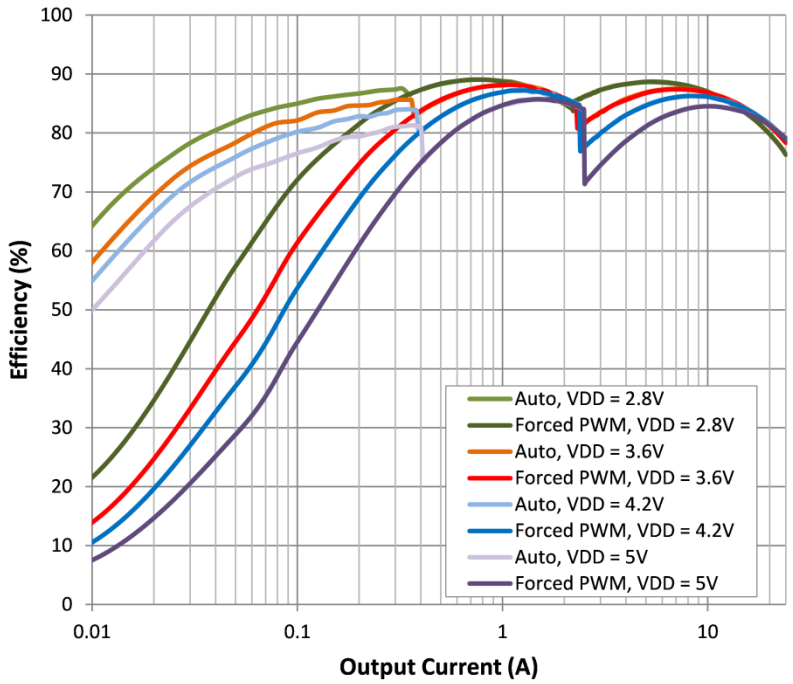


Figure 10: Efficiency vs Output Current V_{OUT} = 0.9 V, dual parallel mode (24 A max)

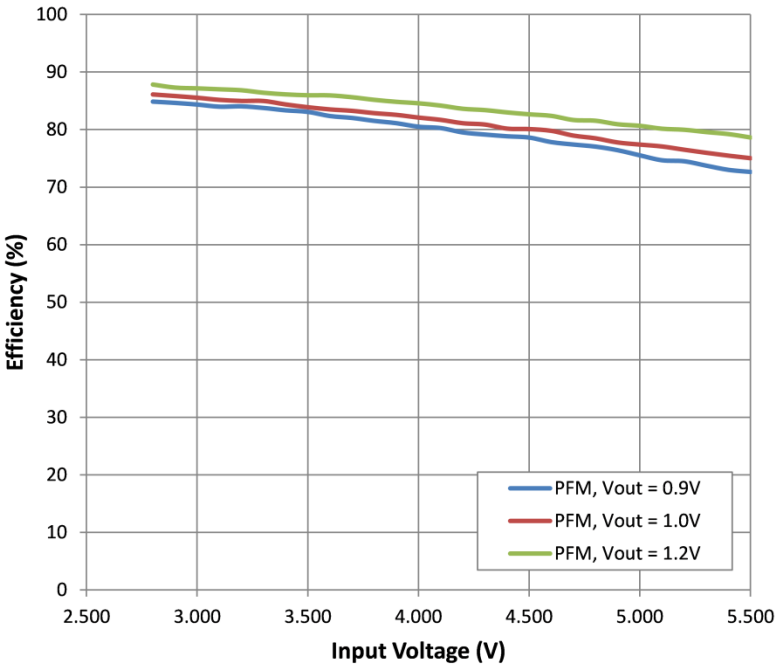


Figure 11: Efficiency vs Input Voltage I_{OUT} = 100 mA

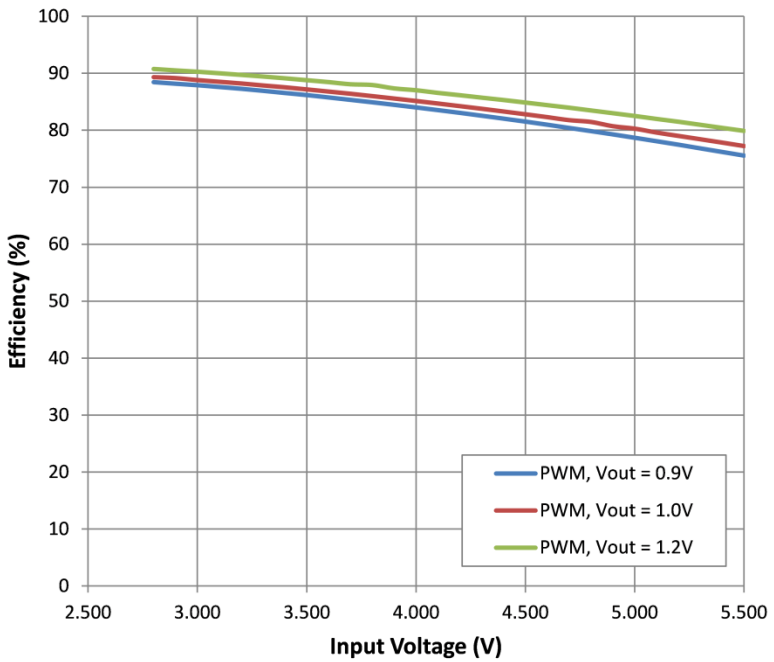


Figure 12: Efficiency vs Input Voltage I_{OUT} = 2 mA

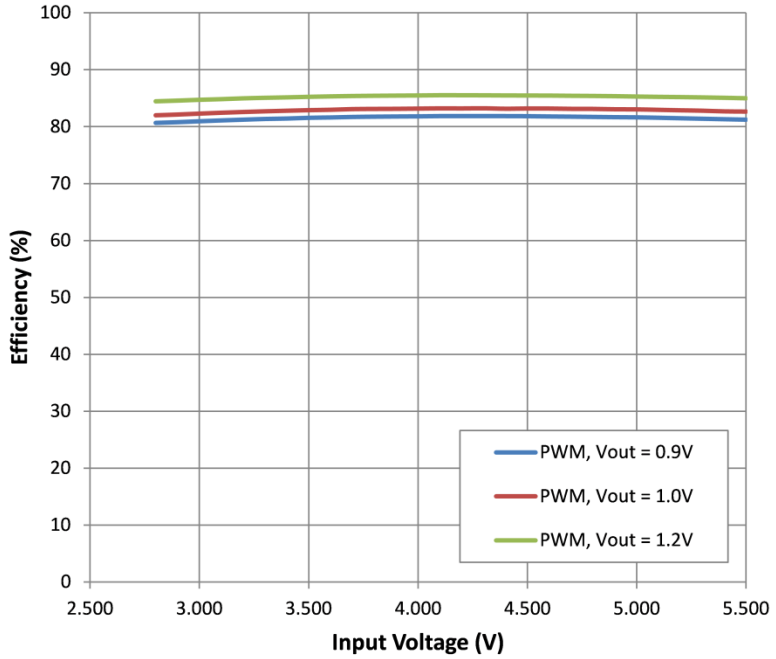


Figure 13: Efficiency vs Input Voltage I_{OUT} = 10 A

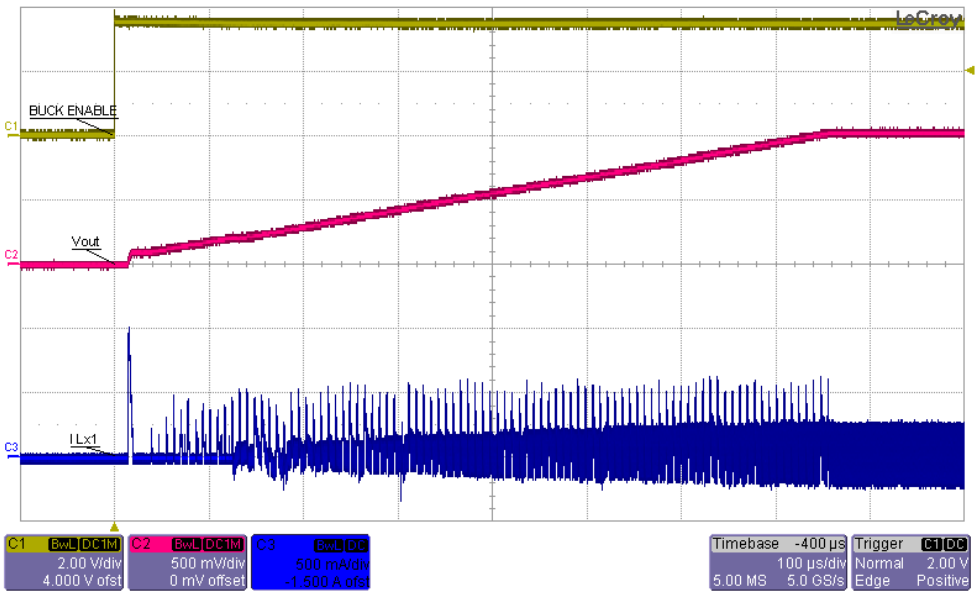


Figure 14: Start-up no load, STARTUP_CTRL = 000 (slowest), VDD = 3.6 V, VOUT = 1.0 V

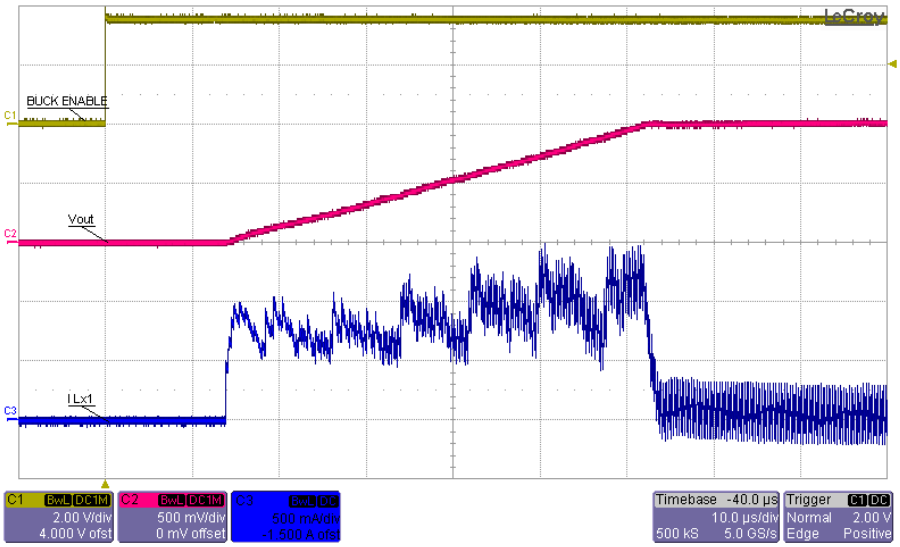


Figure 15: Start-up no load, STARTUP_CTRL = 100, VDD = 3.6 V, VOUT = 1.0 V

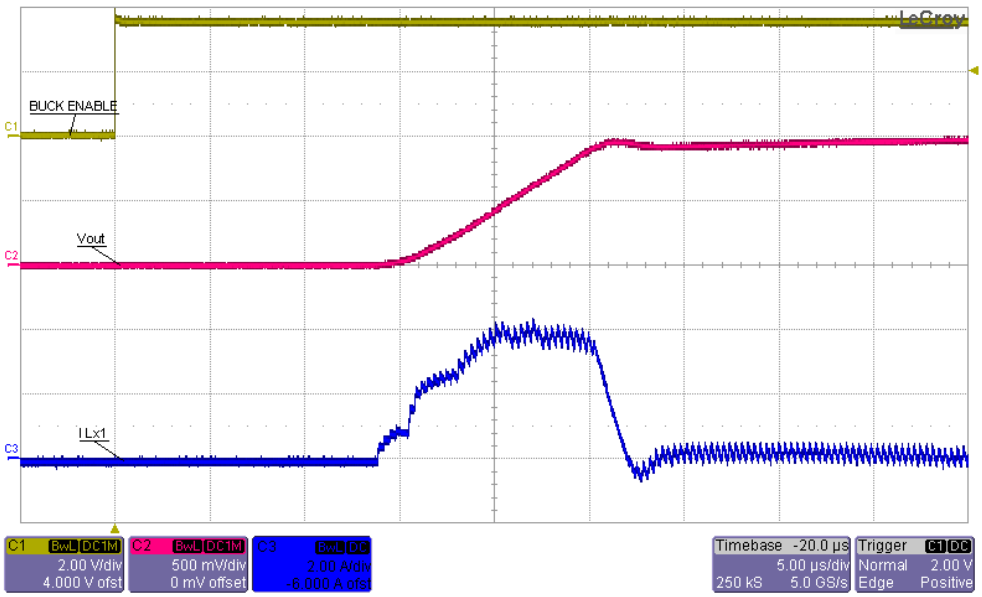


Figure 16: Start-up no load, STARTUP_CTRL = 111 (fastest), VDD = 3.6 V, VOUT = 1.0 V

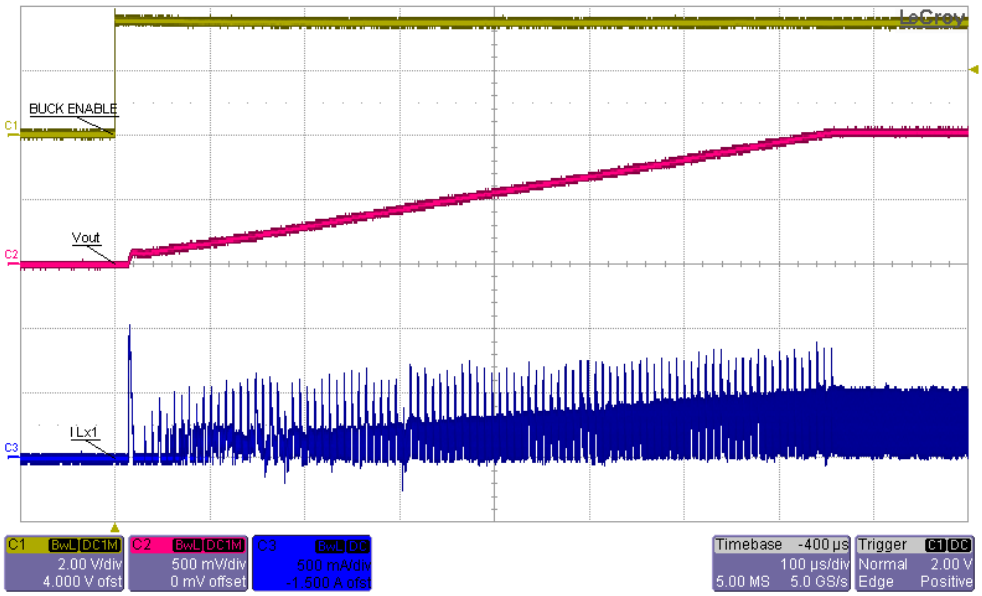


Figure 17: Start-up 1 A load, STARTUP_CTRL = 000 (slowest), VDD = 3.6 V, VOUT = 1.0 V

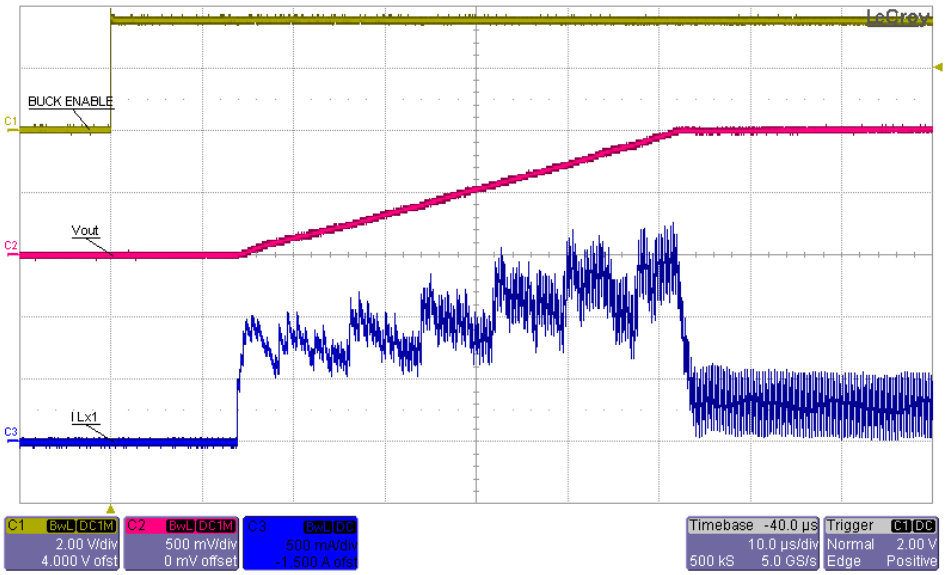


Figure 18: Start-up 1 A load, STARTUP_CTRL = 100, VDD = 3.6 V, VOUT = 1.0 V

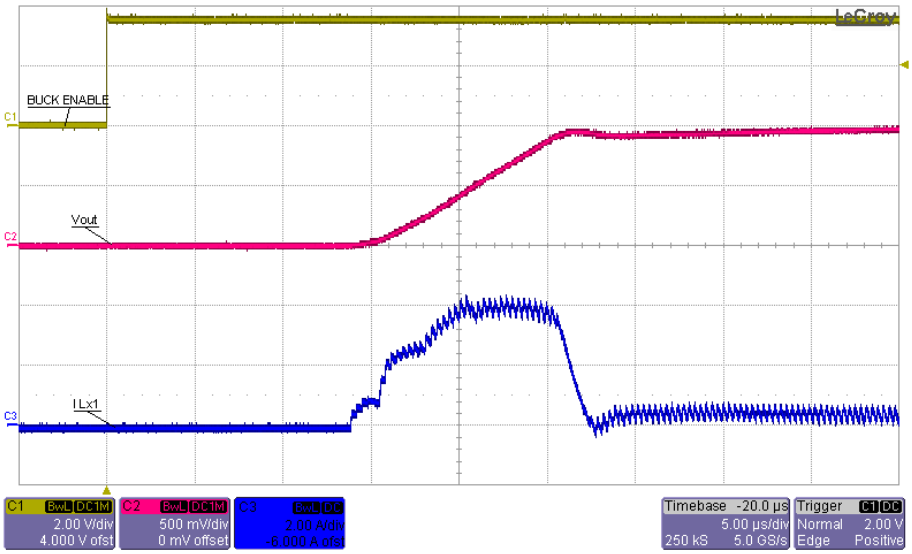


Figure 19: Start-up 1 A load, STARTUP_CTRL = 111 (fastest), VDD = 3.6 V, VOUT = 1.0 V

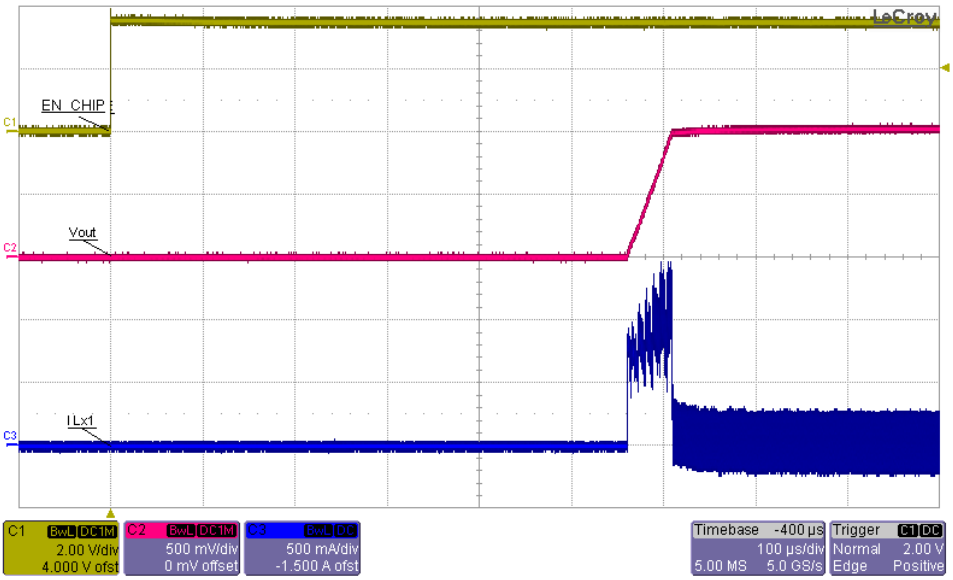


Figure 20: Start-up from EN_CHIP, no load, STARTUP_CTRL = 100, VDD = 3.6 V, VOUT = 1.0 V

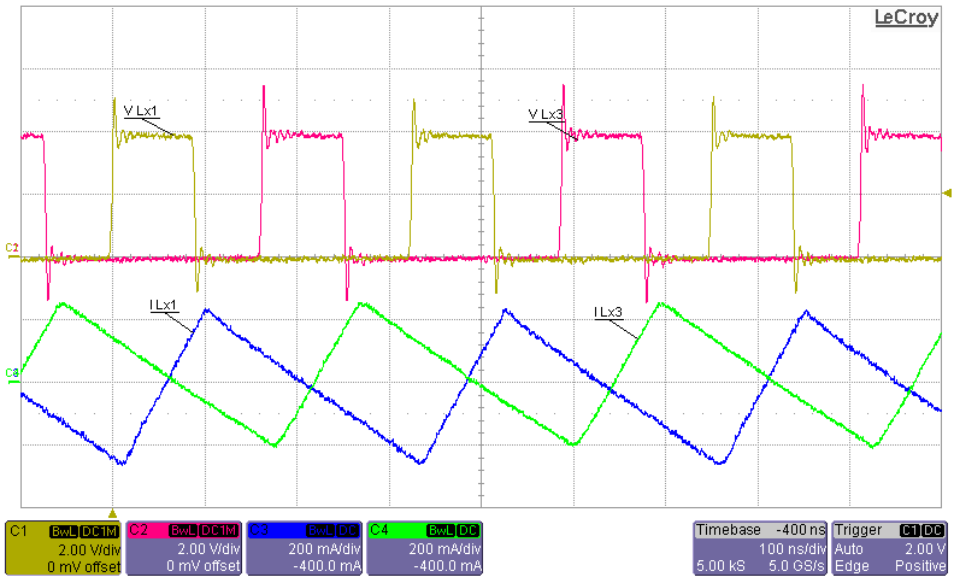


Figure 21: Switching waveforms, PWM, no load, VDD = 3.6 V, VOUT = 1.0 V

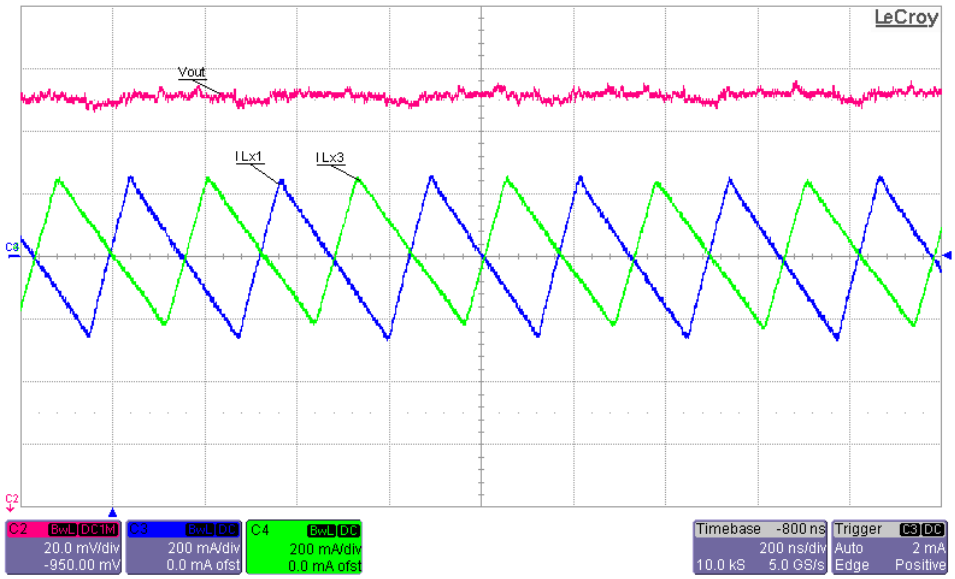


Figure 22: Voltage and current ripple, PWM, no load, VDD = 3.6 V, VOUT = 1.0 V

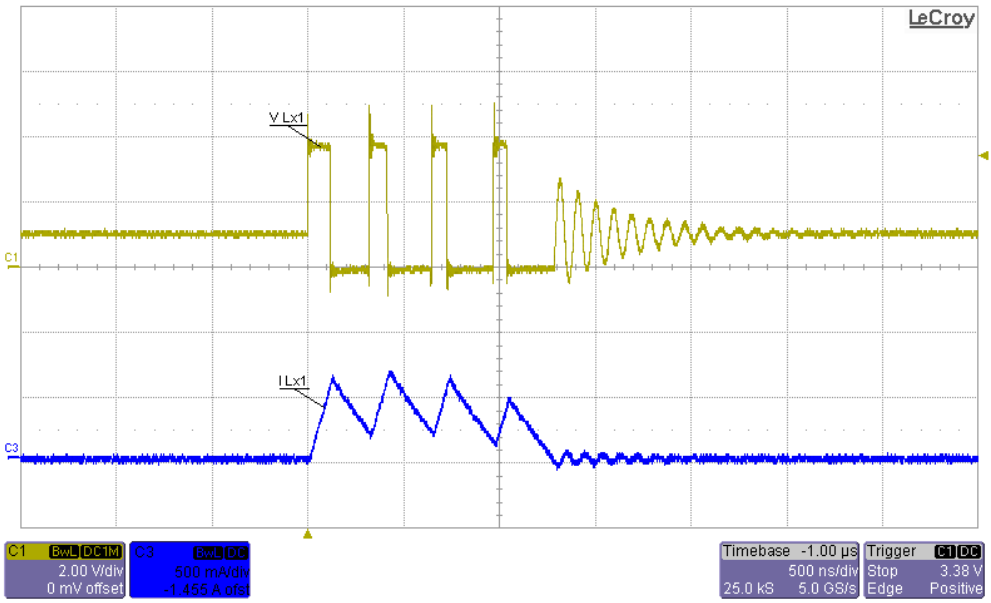


Figure 23: Switching waveforms, PFM, no load, VDD = 3.6 V, VOUT = 1.0 V

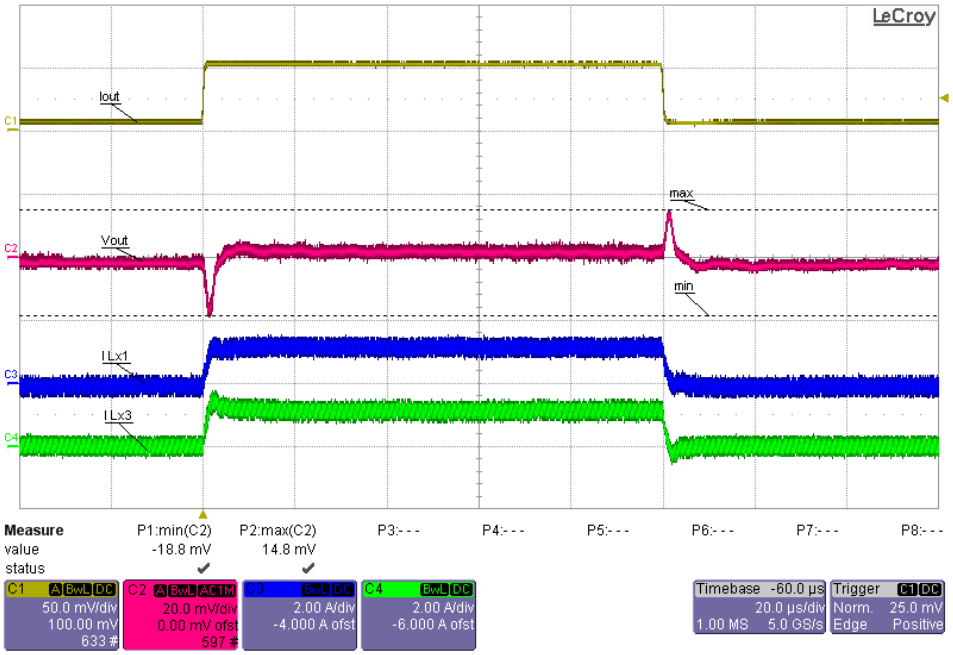


Figure 24: Transient load, PWM, dual mode, 8-phases 5 A to 17 A (12 A/µs), VDD = 3.7 V, VOUT = 1.0 V

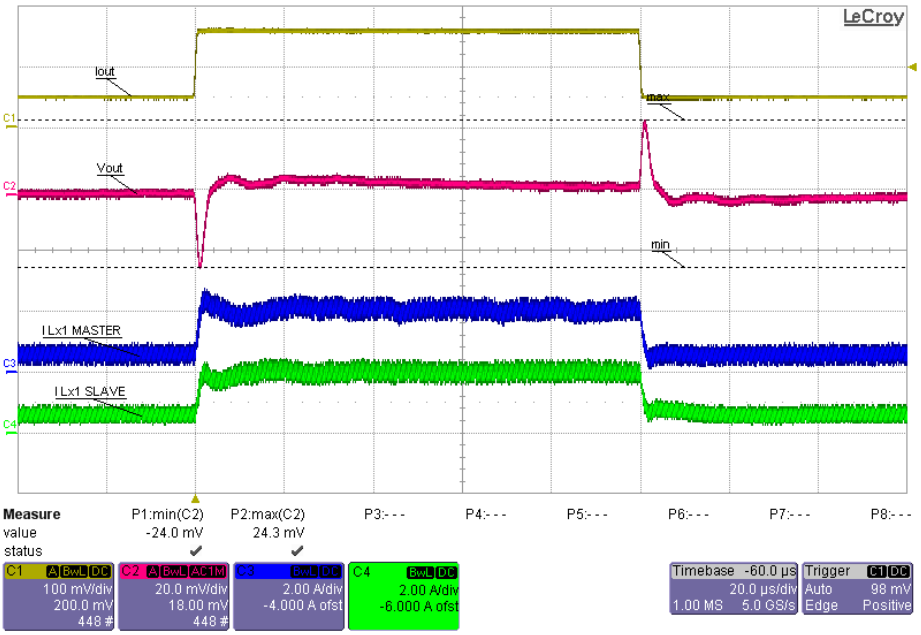


Figure 25: Transient Load, PWM, dual mode, 8-phases 5 to17 A in 12 A/µs, VDD = 3.7 V, VOUT = 1.0 V

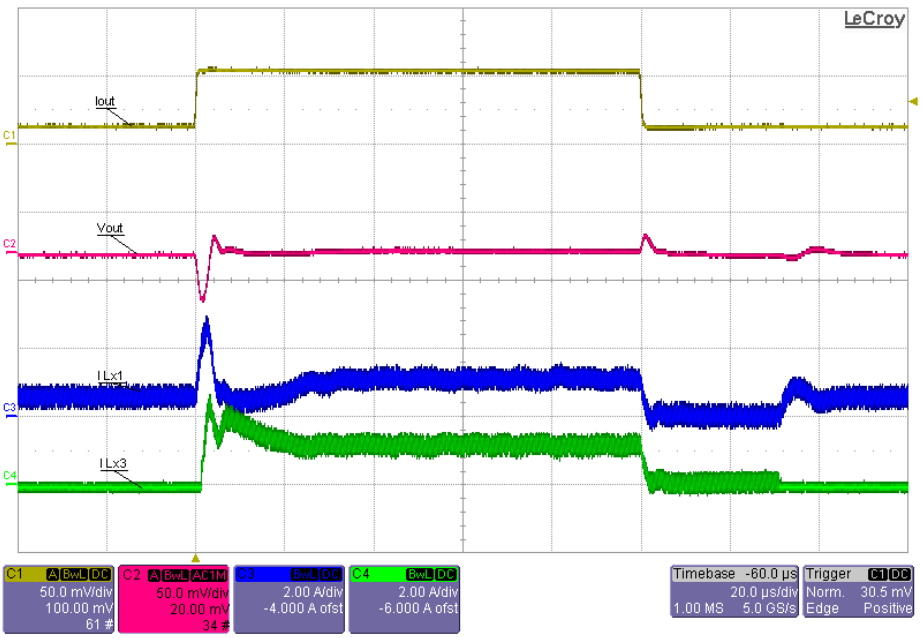


Figure 26: Transient Load, Auto, dual mode, 8-phases 1 to 10 A in 12 A/µs, VDD = 3.7 V, VOUT = 1.0 V

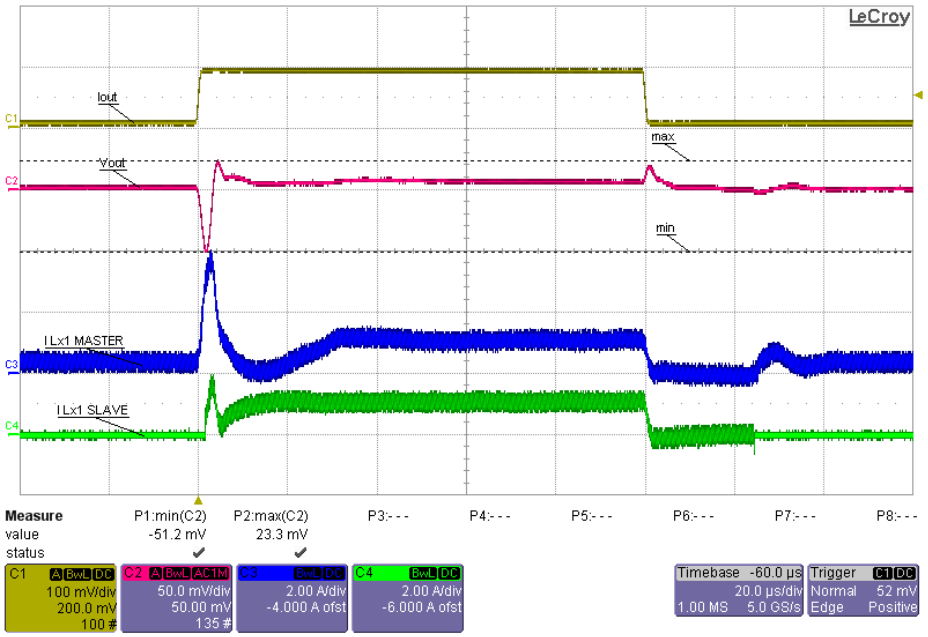


Figure 27: Transient Load, Auto, 4-phases
1 to 5 A in 10 A/µs, VDD = 3.7 V, VOUT = 1.0 V

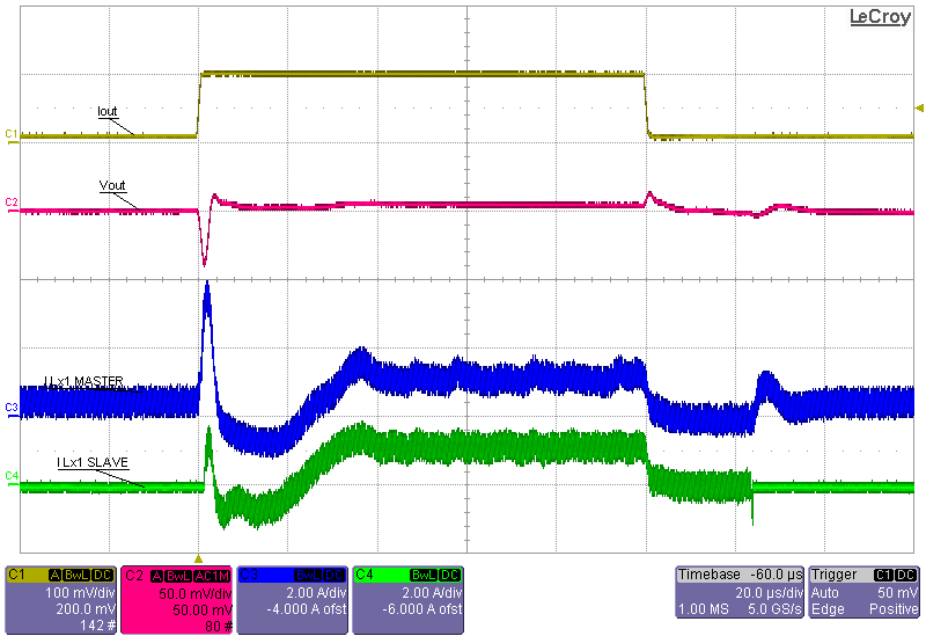


Figure 28: Transient Load, Auto, dual mode, 8-phases, 0.22 µH
1 to 10 A in 12 A/µs, VDD = 3.7 V, VOUT = 1.0 V

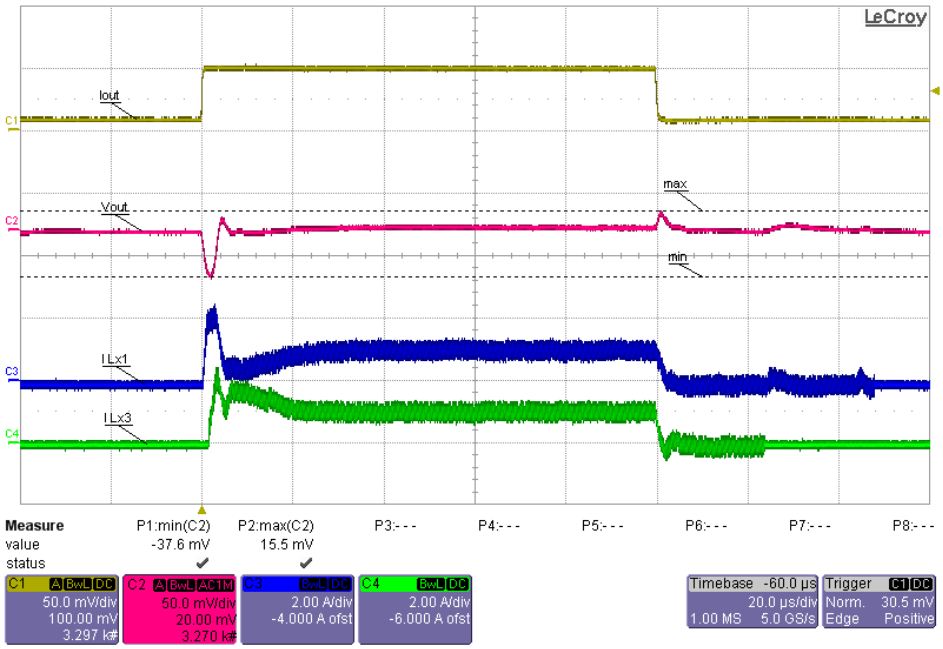


Figure 29: Transient Load, Auto, 4-phases, 10 mA to 5 A in 10 A/µs, VDD = 3.7 V, VOUT = 1.0 V

10 Functional Description

The DA9210 quad-phase buck converter has been designed to operate either as a high-performance stand-alone regulator or as a sub-PMIC that extends the functionality of an integrated system PMIC such as the Dialog DA9063.

In stand-alone operation, the DA9210 provides:

- high performance, 12 A output current capability
- high efficiency, quad-phase operation with phase-shedding
- a small footprint
- an Over-Current Alarm/ Power Good signal to provide real-time status information to the host processor. In the case of an over-current event or loss of power, the host processor is able to react to maximize system integrity

When operated with a Dialog system PMIC such as the DA9063, the system also benefits from the following:

- The DA9210 can be enabled as part of the system start-up sequence by utilizing one of the DA9063 sequenced GPIO signals.
- The DA9210 has been designed to operate seamlessly with the DA9063 by sharing the same control interface (same SPI chip select or I^2C address).
- The DA9210 register map has been designed to interleave with the DA9063 register map. When operated in this way, the two devices appear as a single power management solution to the host processor, thereby simplifying system power control.

By using the general 2-WIRE interface, the DA9210 can easily be integrated into power management systems using system PMICs other than DA9063.

Section 10.1 provides details of the individual blocks of the DA9210 and the configurability available to optimize its performance in any application.

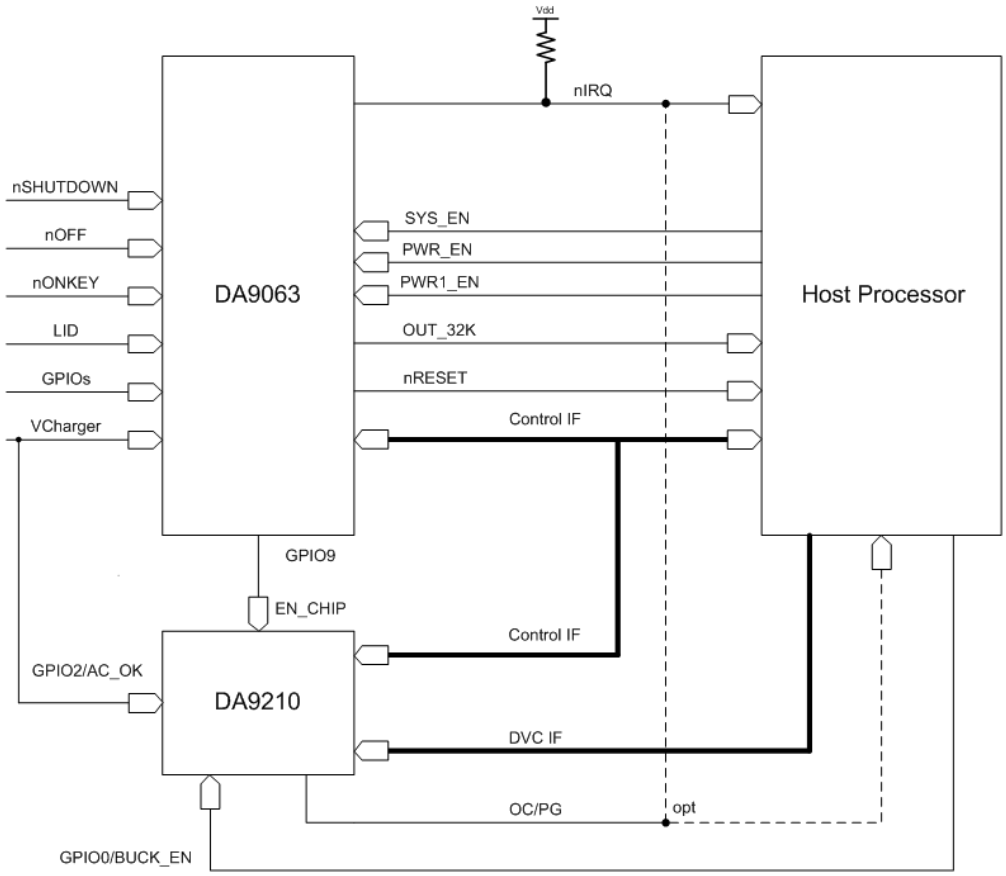


Figure 30: Control ports and interface

As shown in Figure 30, a typical application case includes a host processor, a main PMIC (for example DA9063) and the DA9210 used as companion IC for the high power core supply.

The easiest way of controlling the DA9210 is through the control interface. The host processor is the master that initiates communication and reads and writes to and from the main PMIC's and DA9210's registers. To poll the status of DA9210, the host processor must access the dedicated registers area through the control interface.

Additionally, DA9210 can be controlled by means of hardware inputs. A dedicated hardware signal from the DA9210 to the external host processor is implemented through the OC/PG line.

10.1 DC/DC Buck Converter

The buck converter is a four-phase, high efficiency, synchronous step down DVC regulator, typically operating at 3 MHz.

The buck converter supports the sensing of the configured voltage directly at the point of load (see VOUT_SENSE and VSS_SENSE pins, not supported in tracking mode). The default output voltage is loaded from OTP.

DVC operates in PWM mode (synchronous rectification). The completion of a DVC transition is signaled by GPIO3, assuming the port is configured as GPO and the control bit READY_EN is asserted.

The buck converter has two voltage registers for output voltage A and B. The appropriate values are stored in the registers VBUCK_A and VBUCK_B. The specific output voltage is selected with the bit BUCK_SEL in register BUCK_CONF. This can be operated either via GPI or via the control interface, according to the configuration of VBUCK_GPI.

A DVC transition occurs:

- when the selected voltage VBUCK_A/VBUCK_B is updated to a new target value
- when the voltage selection is changed via BUCK_SEL from VBUCK_A to VBUCK_B or vice versa

The slew rate of the DVC transition is programmed at 10 mV per (4, 2, 1 or 0.5) µs via SLEW_RATE control bits.

The typical input current when four phases are enabled is in the order of 60 mA and drops to < 1 µA when the buck output is disabled.

10.1.1 Switching Frequency

The 3 MHz switching frequency has been chosen to allow the use of a small 0.47 µH inductor (see the complete list of inductors in Section 12). The buck switching frequency can be tuned via register bits OSC_TUNE. This tunes the internal 6 MHz oscillator frequency in steps of 180 kHz. This impacts the buck converter frequency in steps of 90 kHz. This is used to avoid possible disturbances to other HF systems in the application. If a digital input clock is applied at GPIO4 and the port is configured accordingly on register bit GPIO4_PIN it is possible to apply an external oscillator delivering 6 MHz to the system, thereby allowing multiple devices to be synchronized to the same clock source.

10.1.2 Operation Modes and Phase Selection

The operating mode of the buck converter is selected via bits BUCK_MODE in register BUCK_CONF1. The buck converter can be forced to operate in either Normal mode, where all four phases are enabled, or in low-power mode, where the efficiency is optimized for output currents lower than 1 A. In low-power mode, the buck can be forced to operate either with one (default), two, or four phases active, or in PFM mode where the operating frequency varies with the output load current.

NOTE
The low-power mode configuration is programmed in the device OTP and cannot be changed during normal operation. Please contact your local Dialog Semiconductor support for more information.

The BUCK_MODE bits also allow an automatic mode based on the output voltage to be selected. With the BUCK_MODE configured this way the buck will operate in low-power mode as long as the target voltage is lower than the threshold defined in VBUCK_AUTO, or in Normal mode otherwise.

If BUCK_MODE bits = 00, the operating mode is selected dependent on the register bit BUCK_SL_A/B, so the operating mode is set simultaneously with the output voltage. In low-power mode, the buck operates according to different options as previously described.

The number of active phases can be selected by register bits PHASE_SEL in register BUCK_CONF2. This optimizes the efficiency according to the specific output current needed for the application.

If the bit PHASE_SEL is asserted, automatic phase shedding based on the output current load is enabled. The buck automatically changes between 1-phase, 2-phase, and 4-phase operation, thereby optimizing the efficiency in a wide range of output currents. Automatic phase shedding works only in normal mode and the PHASE_SEL field configuration is ignored.

An automatic transition to PFM mode (including automatic phase shedding) can be configured via AUTO_DEF. When this bit is set, in addition to the phase shedding, PFM mode is entered when the output load current becomes low ensuring maximum efficiency.

When operating in dual parallel mode, the master and the slave device will have up to a total of 8 phases enabled. If a phase is never selected for a certain application, the corresponding LX output pin should be left floating and not connected to any external inductor.

10.1.3 Output Voltage Selection

The switching converter can be configured using the 2-WIRE or 4-WIRE interface, or via the dedicated DVC interface.

The DA9210 provides the capability to set two output voltage levels via registers VBUCK_A and VBUCK_B. It is then possible to transition between these two voltages by toggling the register bit BUCK_SEL, or by using a GPI, selected from GPI0, GPI3, or GPI4 in register bit VBUCK_GPI. In addition to setting the output voltage, the VBUCK_A/B registers include the BUCK_MODE setting which allows the selection between normal and low power modes.

When triggered, the transition will ramp between the set voltages following the slew rate set by the SLEW_RATE setting in register CONTROL_A.

The register VBUCK_MAX will limit the output voltage that can be set for the buck converter.

In addition to triggering an A to B voltage transition, the host is able to modify the output voltage by writing to the currently active VBUCK_A/B voltage setting. The current SLEW_RATE setting will be applied to any change triggered by this method.

For security reasons the re-programming of registers that may cause damage if wrongly programmed (for example, voltage settings) can be disabled by asserting the control V_LOCK in the CONTROL_A register. When V_LOCK is asserted, reprogramming the registers 0xD0 to 0x14F from control interfaces is disabled.

DA9210 implements a dedicated control interface supporting direct DVC requests to the buck converter (see also the detailed description in Section 8.4).

When the buck is disabled a 150 Ω (typ) pull-down resistor is activated for each phase dependent on the value stored in register bit BUCK_PD_DIS. Phases disabled via PHASE_SEL will not have any pull-down. The pull-down resistor is always disabled on all phases when DA9210 is in OFF mode.

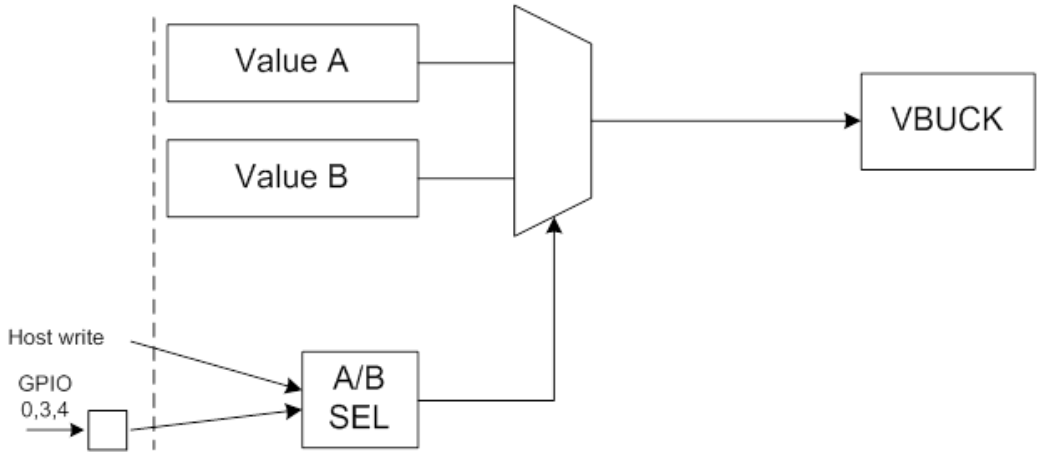


Figure 31: Concept of Control of DA9210's Buck Output Voltage

The buck current limit should be configured to be at least 40 % higher than the required maximum continuous output current.

Table 14: Selection of Buck Current Limit from Coil Parameters

Min. ISAT (mA)	Frequency (MHz)	Buck current limit (mA)	Average current (mA)
5060	3	4600	3300
4180	3	3800	2700
3080	3	2800	2000
1760	3	1600	1100

10.1.4 Soft Start-up

To limit the in-rush current from VSYS input, the buck converter can perform a soft start after being enabled. The start-up behavior is a trade-off between acceptable in-rush current from the battery and turn-on time. In DA9210 different options can be selected using STARTUP bits in BUCK_CONF1 register. Rates faster than 20 mV/µs may produce overshoot during the start-up phase, so they should be considered carefully.

A ramped power-down can be selected on register bit PWR_DOWN_CTRL. If no ramp is selected, the output node will only be discharged by the pull-down resistor, if enabled via BUCK_PD_DIS.

10.2 Ports Description

10.2.1 VDD_IO Rail

VDD_IO is an independent IO supply rail input that can be assigned to the power manager interface and to the GPIOs (see control PM_IF_V and GPI_V). The rail assignment determines the IO voltage levels and logical thresholds (see also the Digital I/O Characteristics).

NOTE
The maximum speed of the 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V.

10.2.2 EN_CHIP

EN_CHIP is a general enable signal for DA9210, turning on and off the internal circuitry (for example the reference, the digital core, and so on). The control of this port has a direct influence on the quiescent current of the whole application and a low level allows the device to reach the minimum quiescent current state. The voltage at this pin is continuously sensed by a dedicated analog circuit.

The EN_CHIP activation threshold is defined with a built-in hysteresis to avoid erroneous transitions being triggered by unstable rising or falling edges. The EN_CHIP port has an integrated pull-down current.

10.2.3 GPIO0

The port behaves like a GPIO extender pin (see Section 10.4). In a typical application GPIO0 can be used as GPI port enable for the buck converter, as shown in Figure 30.

10.2.4 VERROR / GPIO1

This port is multi-functional depending on the configuration of GPIO1_PIN. It can be used as an analog pin to support the dual parallel mode operation of DA9210 (input in case of slave, output in case of master operation, see also Section 10.3.3). Alternatively it behaves like a standard GPIO extender pin, see Section 10.4.

If GPIO1_PIN = 01 the port will be configured for VERROR operation operating as an input or an output, depending on the voltage level on the VOUT_SENSE Pin, see Section 10.3.3. In master mode, the port is an output. In slave mode (VOUT_SENSE must be tied high to VDDCORE), the port is an input.

If GPIO1_PIN = 01 and master mode is configured, whenever the buck converter is enabled, the signal at the output of the buck error amplifier is internally routed to the VERROR pin and is available externally. This allows the DA9210 to operate as a master together with another slave instance of DA9210 in dual DA9210 operation.

If GPIO1_PIN = 01 and slave mode is configured, whenever the buck converter is enabled, the signal applied at the VERROR pin will be internally routed as a replacement for the buck error amplifier output, thereby overriding the functionality of the amplifier in the regulation loop. This allows the DA9210 to operate as a slave together with another master instance of DA9210 in dual DA9210 operation.

10.2.5 IPHASE / GPIO2

This port is multi-functional according to the configuration of GPIO2_PIN. It can be used as an analog pin to support the dual parallel mode operation of DA9210 (input in the case of operation as a

slave, output in the case of operation as a master, see Section 10.3.3. Alternatively it behaves like a standard GPIO extender pin, see Section 10.4.

If GPIO2_PIN = 01 the port will be configured for IPHASE operation as an input or an output, according to the voltage level on the VOUT_SENSE Pin, see Section 10.3.3. In master mode the port is an output. In slave mode (VOUT_SENSE must be tied high to VDDCORE) the port is an input.

If GPIO2_PIN = 01 and master mode is configured, whenever the buck converter is enabled, the signal from the current sense amplifier of one phase is internally routed to the IPHASE pin and is available externally. This allows the DA9210 to operate as a master together with another slave instance of DA9210 in dual DA9210 operation.

If GPIO2_PIN = 01 and slave mode is configured, whenever the buck converter is enabled, the signal applied at the IPHASE pin will be internally routed as a replacement for the current sense amplifier of one phase, thereby overriding the function of that current sense amplifier in the current regulation loop. This allows the DA9210 to operate as a slave together with another master instance of DA9210 in dual DA9210 operation.

10.2.6 BUCK_CLK / GPIO3

This port is multi-functional according to the configuration GPIO3_PIN. It can be used as a digital pin to support the dual parallel mode operation of DA9210 (input in the case of operation as a slave, output in the case of operation as a master, see Section 10.3.3. Alternatively it behaves like a standard GPIO extender pin, see Section 10.4.

If GPIO3_PIN = 01 the port will be configured for buck clock operation as an input or an output, according to the voltage level at VOUT_SENSE pin, see Section 10.3.3. In master mode the port is an output. In slave mode (VOUT_SENSE must be tied high to VDDCORE) the port is an input.

If GPIO3_PIN = 01 and master mode is configured, whenever the buck converter is enabled, the clock signal of the buck converter is internally routed to the BUCK_CLK pin and is available externally. This allows to use DA9210 in dual operation as a master together with another slave instance of DA9210.

If GPIO3_PIN = 01 and slave mode is configured, whenever the buck converter is enabled, the signal applied at BUCK_CLK pin will be internally routed to the clock generation block of the buck converter, thereby overriding the functionality of the internal buck clock. This allows the DA9210 to operate as a slave together with another master instance of DA9210 in dual DA9210 operation.

10.2.7 Digital External Clock Input / GPIO4

This port is multi-functional according to the configuration of GPIO4_PIN. It can be used as digital external clock input for the system, if a signal of typically 6 MHz is applied to the pin.

NOTE
The clock must already be running and stable before configuring the port via GPIO4_PIN and before enabling the buck converter. Missing pulses or signals applied at different frequencies than specified may cause disruption of the IC.

Alternatively it behaves like a standard GPIO extender pin, see Section 10.4.

10.2.8 OC_PG / nIRQ

The OC_PG (Over Current alarm and Power Good) is an output port shared with nIRQ and can be either push-pull or open-drain (selected via OC_PG_IRQ_TYPE). The port can be configured as active high or active low via control OC_PG_IRQ_LEVEL.

If OC_PG_IRQ_CONF = 0 the port is used as IRQ line. It indicates that an interrupt causing event has occurred and that the event/status information is available in the related registers 0x50 to 0x53. Such information can be a warning of critical temperature, fault conditions, or status changes on GPI ports. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted (unless this interrupt is masked by a corresponding bit in the IRQ mask registers 0x54 and 0x55). The nIRQ is not released until all event registers with asserted bits have been read and cleared. New events that occur during event register reading are held until the event register has been read and cleared, ensuring that the host processor does not miss them.

If OC_PG_IRQ_CONF = 1, the OC_PG functionality is selected. The OC_PG function is valid for Li-Ion battery voltage ranging from 2.8 V to 4.4 V. This can be used for a dedicated communication to the host processor. OC_PG remains asserted while as at least one of the STATUS indicators is active (see registers 0x50 and 0x51). This allows the host processor to be immediately informed and to promptly react by, for example, reducing its operating frequency. After the fast reaction, the host processor can then check the STATUS registers to see what is causing the OC_PG port assertion, if the indicator is still active. If the indicator is not active, the host processor is able to track what has caused the OC_PG port assertion through the EVENT registers.

The STATUS indicators causing the assertion of the OC_PG port are reported in the following list:

- Not Buck Power Good
- Over Current Alarm
- Warning Temperature
- VBUCK_MAX Voltage
- GPI Status

When a STATUS bit is set, the OC_PG signal is asserted, unless the related bit is masked in MASK_A and MASK_B registers. An event is produced in parallel when the STATUS bit changes from passive to active state. The OC_PG port is automatically released when no STATUS indicators are active. The EVENT bit remains asserted and needs to be cleared by the host processor.

When EN_CHIP is low, the OC_PG port is configured in high impedance state. When EN_CHIP is high and the buck converter is disabled, the OC_PG port is configured to its passive state. Therefore if it is set as open-drain, active low in CONFIG_A register, a pull-up resistor will be required to achieve a high level on the OC_PG port.

When disabling the buck converter, if OC_PG_REL = 0, the OC_PG port is held asserted during power down for tOC_PD after the buck has been disabled. When this time expires, the OC_PG port will be released to its passive state. If OC_PG_REL = 1, the OC_PG port is held asserted during power down until the down ramp has completed. After that it will be immediately released to its passive state.

Not Buck Power Good

This channel monitors the output voltage of the buck converter and signals an invalid output voltage condition. During power up, the nPWRGOOD indicator is active and is released when the buck output voltage is greater than VGOOD.

During normal operation, the nPWRGOOD indicator is active when the buck output voltage falls below VGOOD – VGOOD_HYST. The indicator is released when the buck output voltage returns above VGOOD.

Over Current Alarm

This channel monitors the peak current through the pass devices of the buck converter. The indicator is active as long as the BUCK_IALARM threshold is hit. This is a pre-warning level information for the host processor.

The control OC_PG_MASK can be used to mask the assertion of OC_PG due to current alarm during the DVC transition of the buck converter until the power up has completed.

If OC_PG_KEEP control bit is asserted, the Over Current Alarm channel is masked for 100 µs after the Power Good condition has been reached, in other words, after the buck rail is valid. This happens when recovering from an out of range condition and during power up of the buck converter.

When triggered due to an over current condition, the OC_PG port is asserted within tOC_DEL thereby ensuring fast feedback of information to the host processor.

After being asserted due to Over Current, the OC_PG port will be released at least tOC_ASSERT after the current has reduced below the BUCK_IALARM threshold. This ensures that very short current spikes triggering the OC_PG will produce pulses with defined minimum width, thereby allowing the host processor to react and take counter-measures.

Over Current Alarm is valid only in PWM mode. When the buck is operated in PFM mode or Auto mode, the M_OVCURR bit should be set.

Warning Temperature

This channel monitors the die temperature of DA9210 and the indicator becomes active as soon as the TEMP_WARN threshold is hit. This is pre-warning level information for the host processor. The indicator returns to inactive only after the die temperature has fallen below TEMP_WARN – TEMP_HYST.

VBUCK_MAX Voltage

This channel monitors the output voltage configured for the buck converter either via dedicated DVC interface (see status register VBUCK_DVC) or via the VBUCK_A and VBUCK_B registers. The indicator is active as long as the configured output voltage is greater than or equal to VBUCK_MAX.

GPI Toggling and External Charger Plugged

To extend the OC_PG functionality, if additional external inputs need to be monitored and their activity needs to be combined on the OC_PG, all DA9210 GPIOs can be configured to trigger the assertion of OC_PG port if they are configured as GPI and not overridden by any alternative function or masked.

If GPIO1, GPIO2 and GPIO3 are used for dual parallel mode operation (GPIO1_PIN = 01, GPIO2_PIN = 01, GPIO3_PIN = 01), the configuration of these pins is ignored and no signaling on the OC_PG port is possible.

GPIO4 is assigned for dedicated communication of an External Charger connection signal. If not masked, it asserts when the charger is disconnected from the system. For this purpose, GPIO4 must be configured as GPI, active low.

If GPIO5 and GPIO6 are used as Interface Ports (GPIO5_PIN = 01, GPIO6_PIN = 01), the configuration of these pins is ignored and no signaling on the OC_PG port is possible.

If configured for HW control of the switching regulator, GPIO0, GPIO3 or GPIO4 will not assert OC_PG when their status is active.

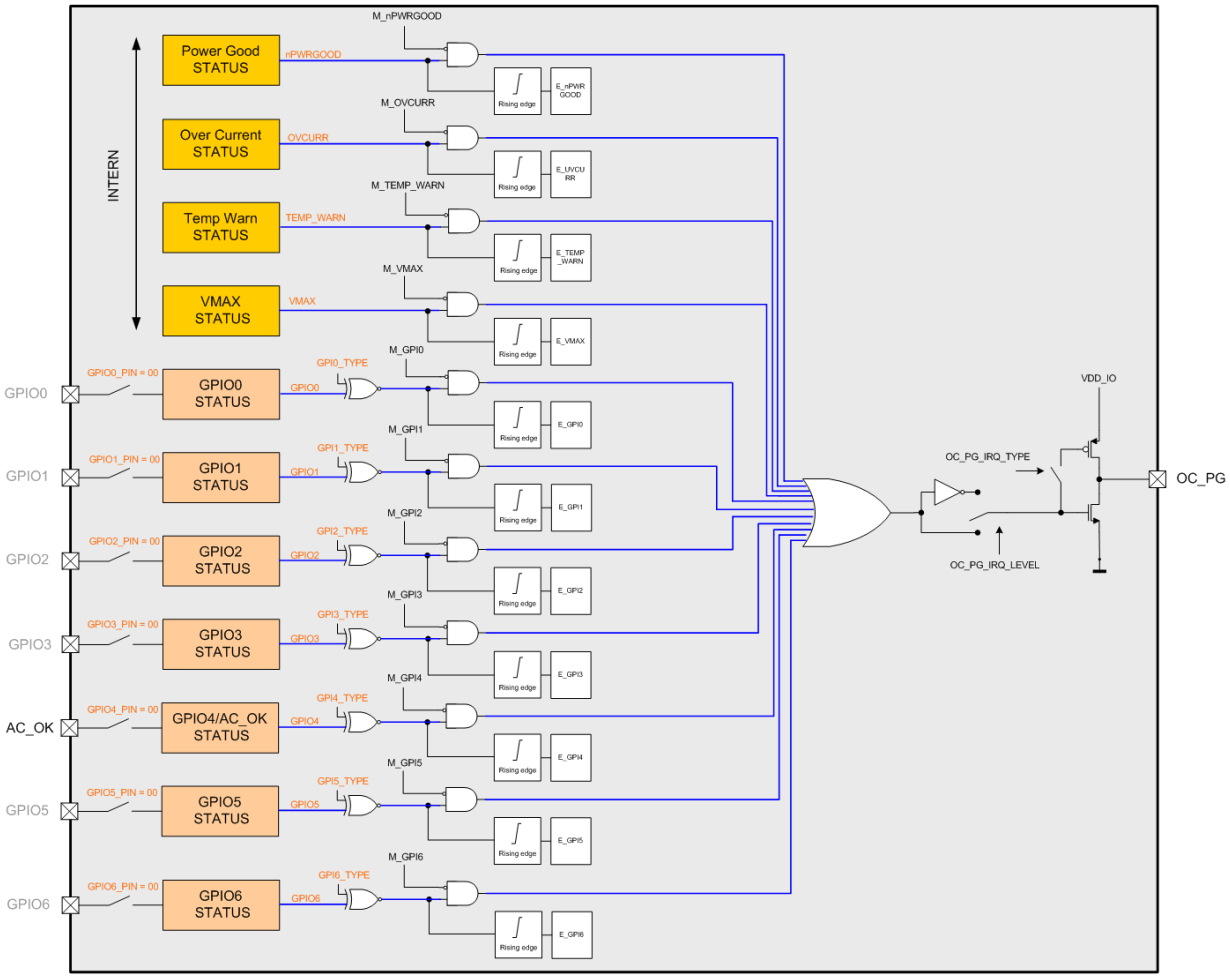
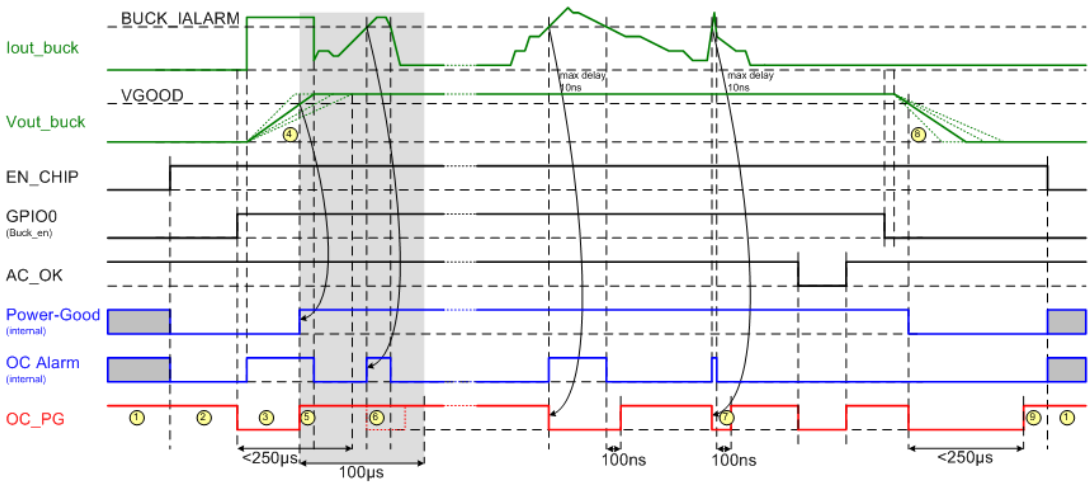


Figure 32: Configuration of OC_PG Pin Functionality



① High impedance (ext. pull-up defines the level)
② OC_PG released to the passive state (ext. pull-up defines the level)
③ OC_PG is actively driven low after enabling the buck because Power-Good is low
④ STARTUP_CTRL defines the slope
⑤ OC Alarm ignored during ramping (also successive voltage changes via DVC ramping) if OC_PG_MASK=1
⑥ If OC_PG_KEEP=1 OC_PG is not asserted during the first 100µs after Power-Good although an over current occurs. The dotted line shows what happens if OC_PG_KEEP = 0.
⑦ In case of short peaks the OC_PG stays low for at least 100ns
⑧ PWR_DOWN_CTRL defines the slope
⑨ Latest 250µs after the buck is enabled OC_PG is released to the passive state (ext. pull-up defines the level)

Figure 33: OC_PG Timing Diagram (CONFIG_A = 0x16)

10.3 DA9210 Operating Modes

10.3.1 ON Mode

DA9210 is in ON mode when the EN_CHIP port is higher than EN_ON. Once enabled, the host processor can start communication with DA9210 via control interface after the tEN delay needed for internal circuit start-up.

If BUCK_EN is asserted when DA9210 is in ON mode, the power up of the buck converter is initiated. If the buck is controlled via GPI (see BUCK_GPI, VBUCK_GPI), the level of the controlling ports is checked when entering ON mode, so that an active will immediately affects the buck. If BUCK_EN is not asserted and all controlling GPI ports are not active, the buck converter remains off with output pull-down resistor enabled or disabled according to BUCK_PD_DIS bit.

10.3.2 OFF Mode

DA9210 is in OFF mode when the EN_CHIP port is lower than EN_OFF. In OFF mode, the buck is always disabled and the output pull-down resistor is disabled independently of BUCK_PD_DIS. All I/O ports of DA9210 are configured to be high impedance.

10.3.3 Dual Parallel Mode

DA9210 is capable of delivering up to 24 A for a high current CPU supply, when operated in dual parallel mode. Two instances of DA9210 are needed with parallel connection of VDD and output node, one acting as master and one as slave (see Figure 34). A DA9210 slave is identified by the connection of VOUT_SENSE pin to VDDCORE, whilst a master has the VOUT_SENSE pin in the normal output voltage operational range. A suitable built in filter avoids noise or short spikes on the VOUT_SENSE line causing the wrong operating mode to be sensed.

To operate in dual parallel mode, both master and slave instances of DA9210 must have GPIO1, GPIO2, and GPIO3 configured respectively as VERROR, IPHASE, BUCK_CLK in the GPIOx_PIN control field.

The configuration of DA9210 in dual parallel mode is transparent to the host processor and does not require any extra effort in terms of register write and maintenance. Only the master device is visible to the host processor. All commands are sent via the control interface by the host processor into the master. In slave mode, DA9210 will not react to any read command from the control interface. Please contact your local Dialog Semiconductor support for more information and dedicated application note on the Dual Parallel Mode.

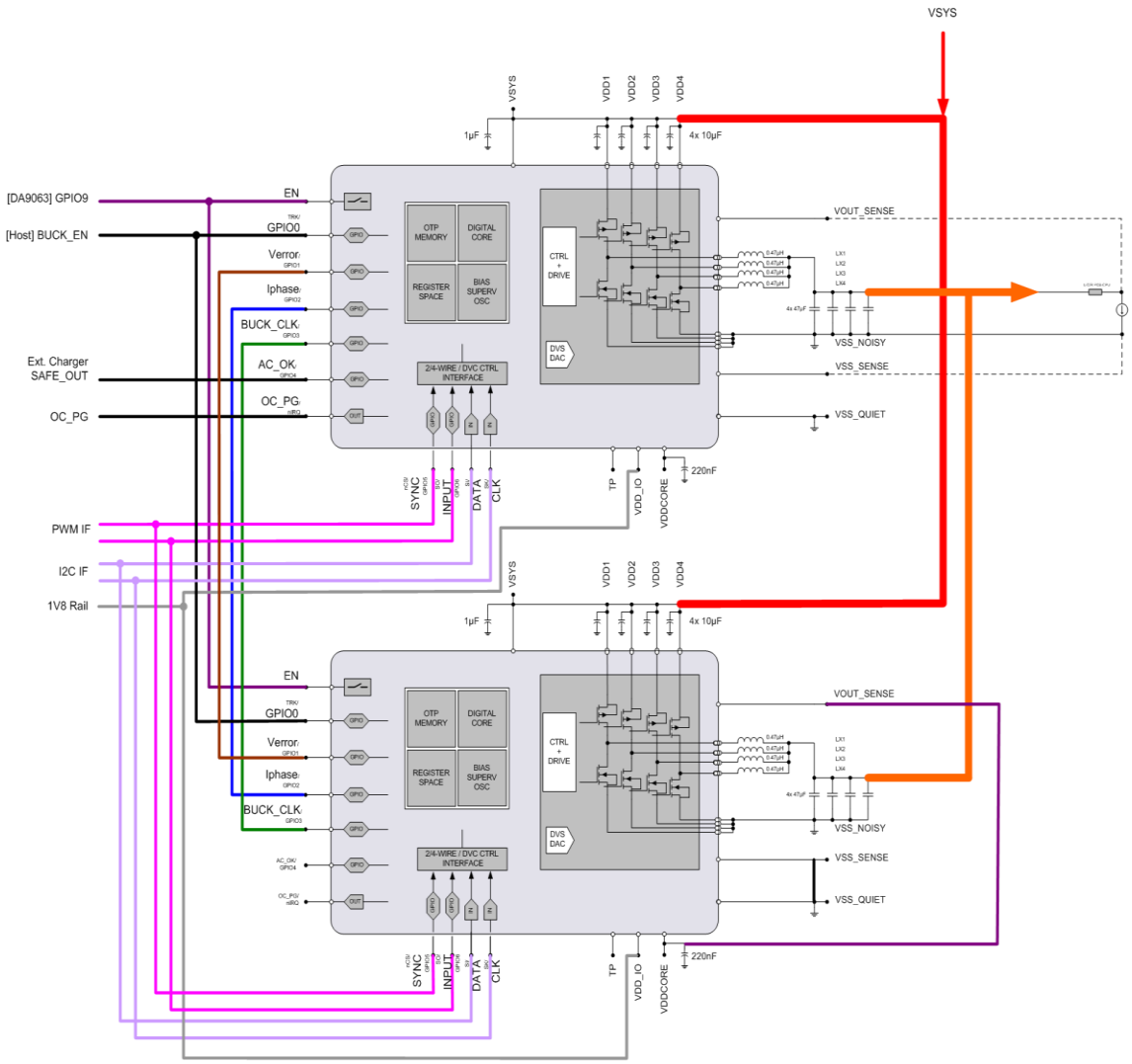


Figure 34: Dual Parallel Mode Configuration

10.4 GPIO Extender

DA9210 includes a GPIO extender that offers up to seven 5 V tolerant, GPIO ports; each controlled via registers from the host processor.

The GPIO ports are pin-shared with the control interface, DVC interface, and dual operation. For instance, if GPIO5_PIN = 01, GPIO6_PIN = 01 (Interface selected), the GPIO5 and GPIO6 ports will be exclusively dedicated to chip select and output signaling for 4-WIRE purposes or to clock and input for DVC interface, depending on the setting of IF_TYPE. If the alternate function is selected, all GPIO configurations as per registers 0x58 to 0x5A and 0x145 will be ignored.

GPIs are supplied from the internal rail VDDCORE or VDD_IO (selected via GPI_V and can be configured to be active high or active low in GPIOx_TYPE. The input signals can be debounced (debouncing time configurable via control DEBOUNCING, 10 ms default) can directly change the state of the assigned status register GPIx to high or low, dependent on the setting of GPIOx_MODE.

If OC_PG_IRQ_CONF = 1, as long as the status is at its configured active state (level sensitive), the OC_PG port is asserted (unless this is masked, see also Figure 32). Whenever the status changes to the active state (edge sensitive), the assigned event register is set (needs to be cleared by the host processor).

If OC_PG_IRQ_CONF = 0, whenever the status changes to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless the nIRQ is masked, see Figure 35).

Whenever DA9210 is enabled and enters ON mode (also when enabled, changing the setting of GPIOx_PIN), the GPI status bits are initiated towards their configured passive state. This ensures that already active signals are detected and create an event immediately after the GPI comparators are enabled.

If enabled via buck control BUCK_GPI, port GPI0, GPI3 and GPI4 enable/disable the switching regulator from the rising and falling edges of these signals (changing BUCK_EN). If GPI ports must be enables for HW control of the switching regulator, do not generate an event and do not assert OC_PG independently of the OC_PG_IRQ_CONF setting, the relative mask bit should also be set.

GPI0, GPI3 and GPI4 can alternatively be selected to toggle the BUCK_SEL bit with rising and falling edges at these inputs. In addition to changing the regulator output voltage this also provides a HW control of regulator mode (normal/low power mode) from the settings BUCK_SL_A, BUCK_SL_B (enabled via BUCK_MODE = ‘00’).

All GPI ports have the additional option of activating a 100 kΩ pull-down resistor via GPIOx_PUPD, which ensures a well-defined level in case the input is not actively driven.

If defined as an output, GPIOs can be configured to be open-drain or push-pull. The supply rail in case of push-pull is VDD_IO. By disabling the internal 120 kΩ pull-up resistor in open-drain mode, the GPO can also be supplied from an external rail. The output state will be determined by the GPIO register bit GPIOx_MODE.

Whenever the GPIO unit is off (POR or OFF mode), all ports are configured as open-drain active high (pass device switched off, high impedance state). When leaving POR, the pull-up or pull-down resistors are configured from register CONFIG_C

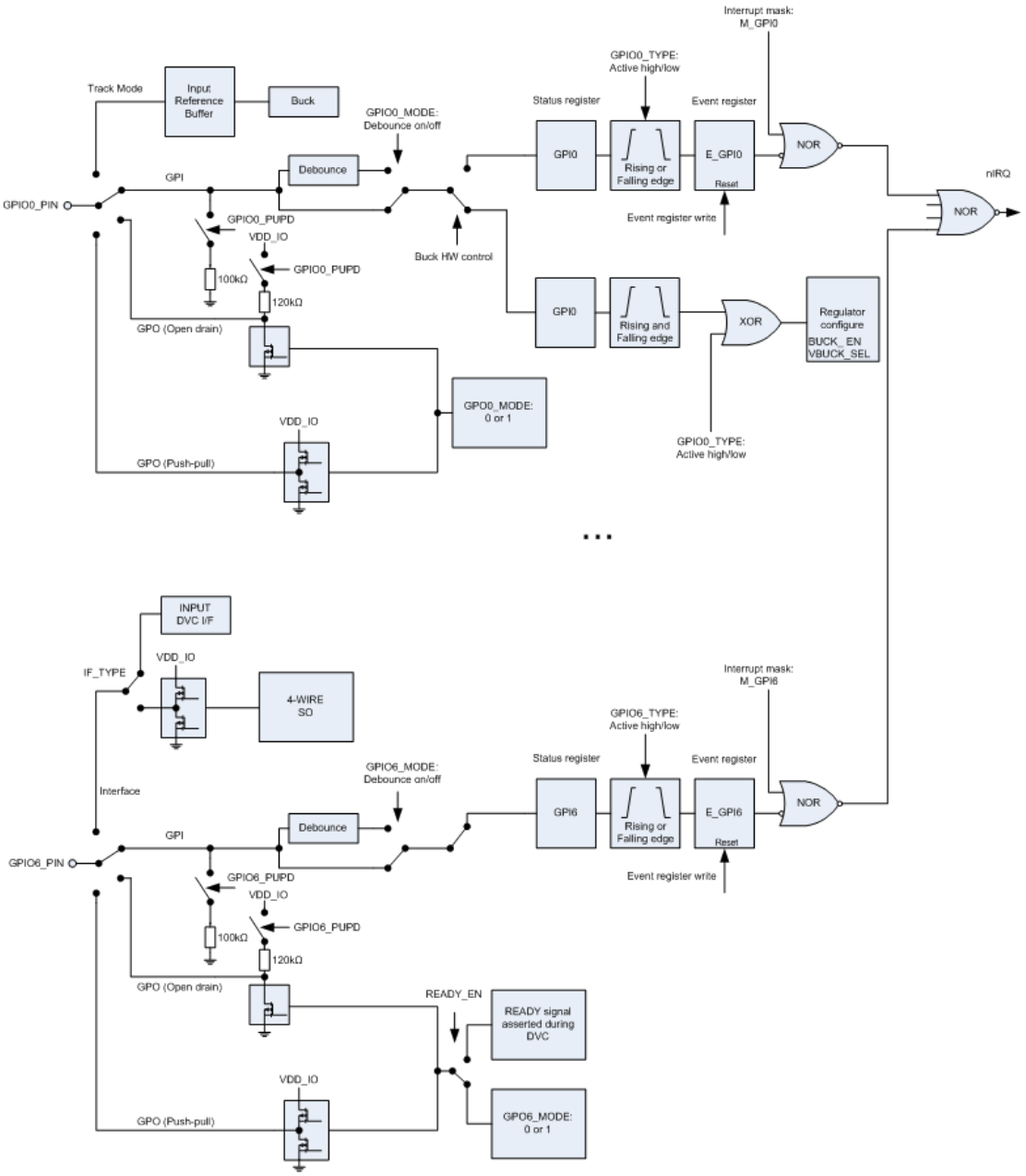


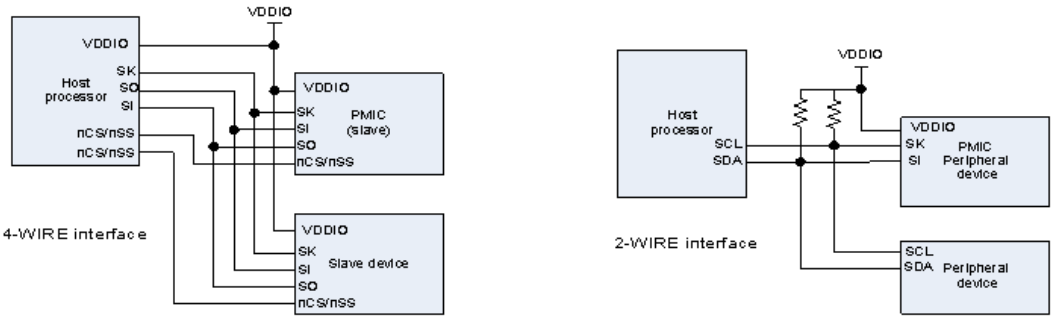
Figure 35: GPIO Principal Block Diagram with nIRQ Signal (Example Paths)

10.5 Control Interfaces

The DA9210 can be SW-controlled by the host. The DA9210 offers access to its registers via a serial control interface. The communication is selectable to be either a 2-WIRE (I^2C compliant) or a 4-WIRE (SPI compliant) connection via control IF_TYPE which is selected during the initial OTP read. In both configurations, the DA9210 will act as a slave device, data is shifted into or out from DA9210 under the control of the host processor that also provides the serial clock. The interface is usually only configured once from OTP values, which are loaded during the initial start-up of DA9210.

NOTE
DA9210 reacts only on read/write commands where the transmitted register address (using the actual page bits as an MSB address range extension) is within 0x50 to 0x6F, 0xD0 to DF, 0x140 to 0x14F, or (read only) 0x200 to 0x280. Host access to registers outside these ranges will be ignored (no acknowledge after receiving the register address in 2-WIRE mode, SO stays HI-Z in 4-WIRE mode). DA9210 reacts only to write commands where the transmitted register address is 0x00, 0x80, 0x100, 0x101, 0x105, 0x106, or 0x200. If STAND_ALONE is asserted (OTP bit), DA9210 also reacts to read commands. If DA9210 is in slave configuration (VOUT_SENSE tied to VDDCORE) it does not react to any read command, see Section 10.3.3.

DA9210 provides an additional interface supporting direct DVC requests from the host processor to the buck. The DVC interface can be enabled via control DVC_CTRL_EN, provided that the GPIO5_PIN, GPIO6_PIN, and IF_TYPE controls are appropriately configured.



10.5.1 4-WIRE Communication

In 4-WIRE mode, the interface uses a chip-select line (nCS/nSS), clock line (SK), data input (SI), and data output line (SO).

The DA9210 register map is split into four pages with each page containing up to 128 registers, in order to be transparent to the main PMIC (DA9063) and compliant to its register map. The register at address 0x00 on each page is used as a page control register. The default active page after turn on includes registers 0x50 to 0x6F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted, after modifying the active page it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

All registers out of the DA9210 range are write only that is the DA9210 will not answer to a read command and the data bus is tri-state (they are implicitly directed to DA9063). In particular, the information contained in registers 0x105 and 0x106 is used by DA9210 to configure the control interface. They must be the same as the main PMIC (DA9063), so that a write to those registers configures both the main PMIC and DA9210. The default OTP settings need also to be identical for correct operation of the system.

The 4-WIRE interface features half-duplex operation (data can be transmitted and received within a single 16 bit frame) at an enhanced clock speed (up to 14 MHz). The interface operates at the clock frequency provided by the host.

A transmission begins when initiated by the host. Reading and writing is accomplished using an 8-bit command, sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0x01 to 0x07) which will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, this, together with the control bit R/W_POL, specifies the direction of the following data exchange. During a register write, the host continues sending out data during the following eight SK clocks. For a read, the host stops transmitting and the 8-bit register is clocked out of DA9210 during the following eight SK clocks of the frame. Address and data are transmitted MSB first. The polarity (active state) of nCS is defined by control bit nCS_POL. nCS resets the interface when inactive and must be released between successive cycles.

The SO output from DA9210 is normally in a high-impedance state and is active only during the second half of a read cycle. A pull-up or pull-down resistor may be needed on the SO line if a floating logic signal could result in unintended current consumption inside other circuits.

The DA9210 4-WIRE interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low CPOL= 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0, DA9210 latches data on the SK rising edge. If the CPHA is set to 1, the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9210 must be set to the same CPOL and CPHA states to communicate with each other, see Table 15.

Table 15: 4-WIRE Clock Configurations

CPHA clock polarity	CPOL clock phase	Output data is updated at SK edge	Input data is registered at SK edge	CPHA clock polarity
0 (idle low)	0	falling	rising	0 (idle low)
0 (idle low)	1	rising	falling	0 (idle low)
1 (idle high)	0	rising	falling	1 (idle high)
1 (idle high)	1	falling	rising	1 (idle high)

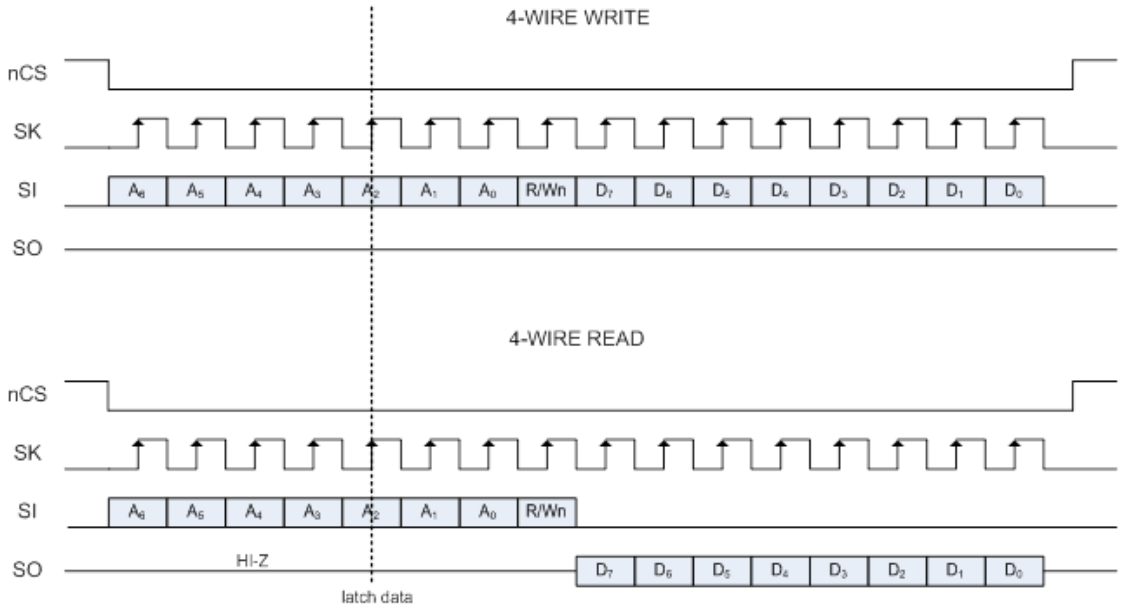


Figure 36: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '0', CPHA = '0')

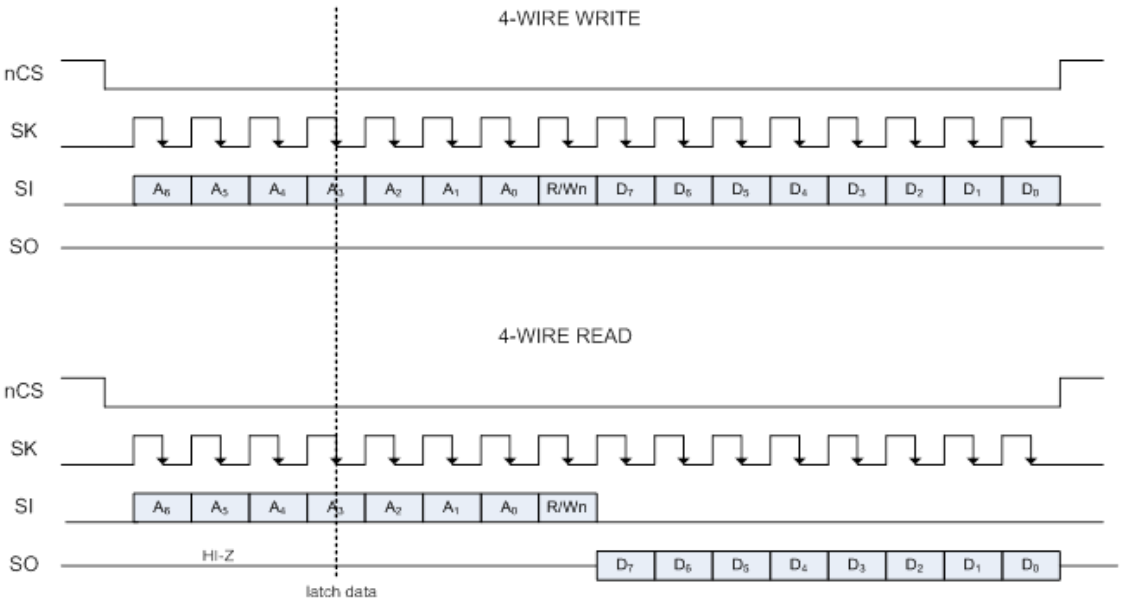


Figure 37: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '0', CPHA = '1')

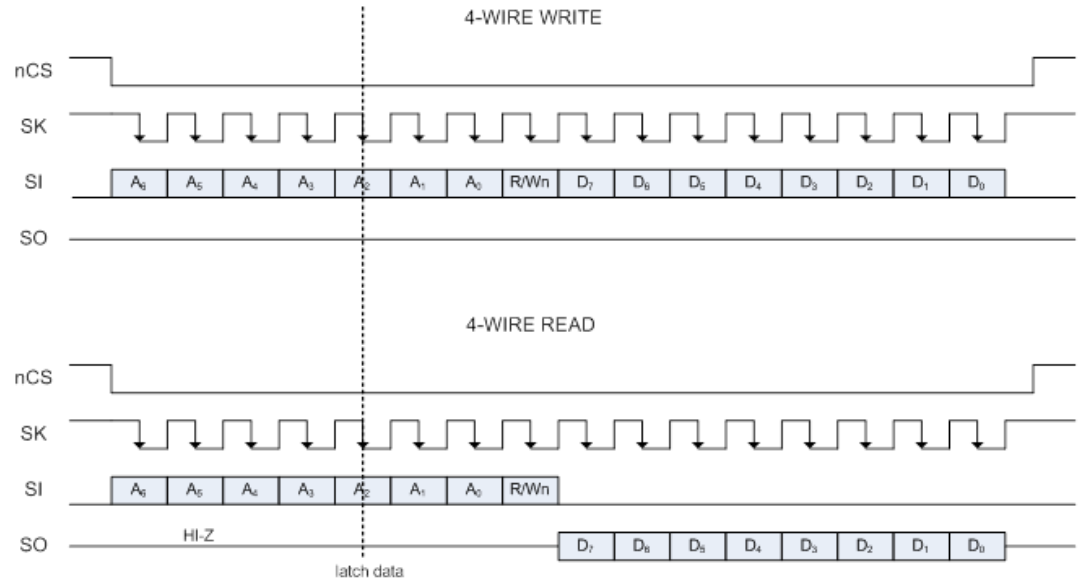


Figure 38: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '0')

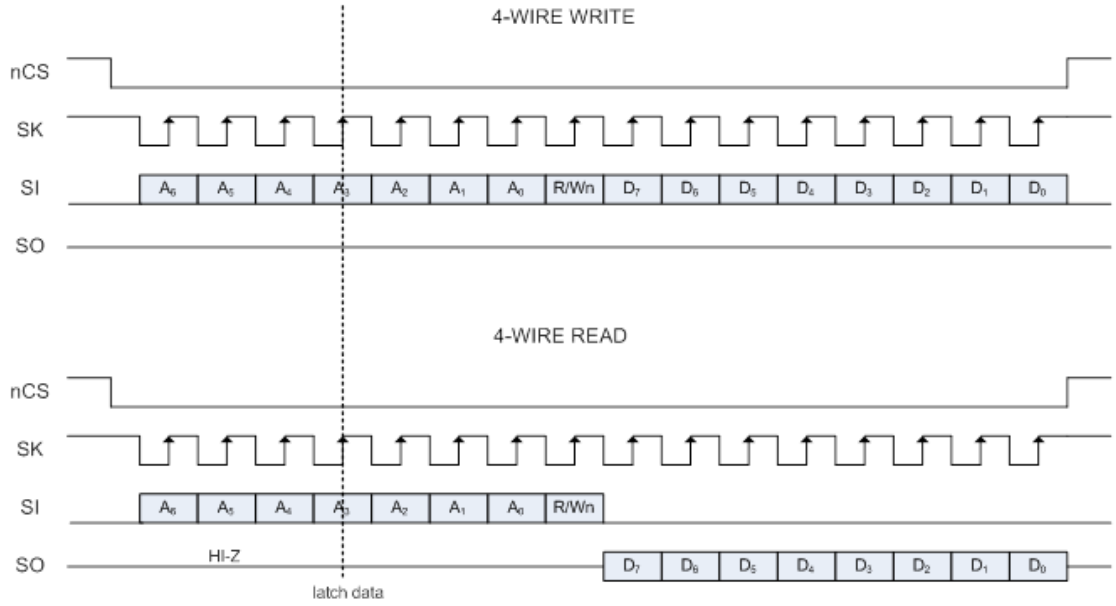


Figure 39: 4-WIRE Host Write and Read Timing (nCS_POL = '0', CPOL = '1', CPHA = '1')

Table 16: 4-WIRE Interface Summary

Parameter		
Signal Lines	nCS	Chip select
	SI Serial input data	Master out Slave in
	SO Serial output data	Master in Slave out
	SK	Transmission clock

Parameter		
Interface	Push-pull with tristate	
Supply voltage	Selected from VDD_IO	1.6 V to 3.3 V
Data rage	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16 bit cycles	7bit address, 1 bit read/write, 8 bit data
Configuration	CPOL	clock polarity
	CPHA	clock phase
	nCS_POL	nCS is active low/high

Note 1 Reading a register at high clock rates directly after writing to it does not guarantee a correct value. A delay of one frame is recommended before re-accessing a register that has just been written (for example by writing/reading another register address in between)

10.5.2 2-WIRE Communication

With control IF_TYPE, the DA9210 power manager interface can be configured towards a 2-WIRE serial data exchange. It has a configurable device write address (default: 0xD0) and a configurable device read address (default: 0xD1). For details of configurable addresses, see control IF_BASE_ADDR.

The SK pin provides the 2-WIRE clock (SCL), and SI carries all the power manager bidirectional 2-WIRE data, (SDA). The 2-WIRE interface is open-drain supporting multiple devices on a single line. The bus lines require external pull-up resistors (2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode, the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9210 internal clock signals. DA9210 follows the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. An automatic reset of the interface can be triggered via control 2WIRE_TO if the clock signal stops toggling for more than 35 ms (compatible with SMBus).

The interface supports operation compatible with Standard, Fast, Fast-Plus and High Speed modes of the I^2C bus specification Rev 4 (UM10204_4). Operation in high speed mode at 3.4 MHz requires mode changing in order to change spike suppression and slope control characteristics to be compatible with the I^2C bus specification. The high speed mode can be enabled on a transfer by transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. DA9210 does not make use of clock stretching and delivers read data up to 3.4 MHz, without additional delay.

Communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9210 only operates as a slave.

Unlike 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the register map (up to 256 addresses). The register at address 0x00 on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control REG_PAGE). Writing to the page control register changes the active page for all subsequent read/write operations, unless an automatic return to page 0 is selected by asserting control REVERT. After modifying the active page, unless REVERT is asserted, it is recommended to read back the page control register to ensure that future data exchange accesses the intended registers.

In 2-WIRE operation DA9210 offers an alternative way to access register page 2 and 3. It removes the need for the preceding page selection writes by increasing the device write/read address by one (default 0xD2/0xD3) for any direct access of page 2 and 3 (page 0 and 1 access requires the basic write/read device address with the MSB of REG_PAGE ‘0’).

Details of the 2-WIRE Control Bus Protocol

The following description uses the standard terms SDA for the serial data, pin SI, and SCL for the serial clock, pin SK.

All data is transmitted across the 2-WIRE bus in 8-bit groups. To send a bit, the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL stores the SDA bit in the receiver’s shift register.

A 2-byte serial protocol is used: one address byte and one data byte. The data and address are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master, during which the bus is in IDLE state (the bus is free). It is initiated by a high-to-low transition on the SDA line while the SCL is in high state. A STOP condition is indicated by a low-to-high transition on the SDA line while the SCL is in high state. The START and STOP conditions are illustrated in Figure 40.

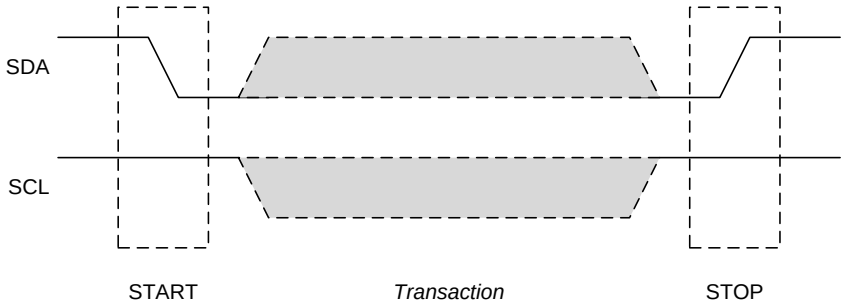


Figure 40: Timing of the START and STOP Conditions

DA9210 monitors the 2-wire bus for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. DA9210 responds to all bytes with an ACK. A register write operation is illustrated in Figure 41.

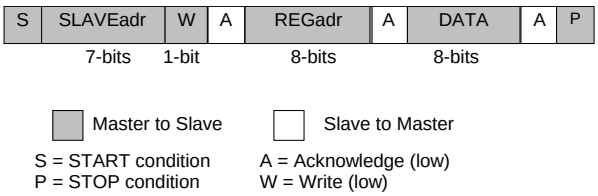


Figure 41: Byte Write Operation

When the host reads register data, the DA9210 first has to access the target register address with write access and then with read access and a repeated START, or alternatively a second START, condition. After receiving the data, the host sends NACK and terminates the transmission with a STOP condition, see Figure 42.

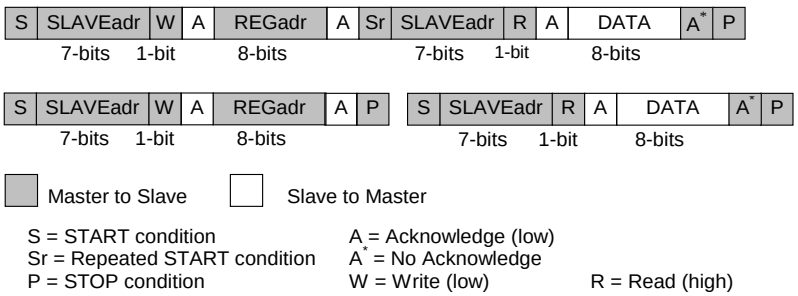


Figure 42: Examples of Byte Read Operations

Consecutive (page) read-out mode is initiated from the master by sending an ACK instead of NACK after receiving a byte, see Figure 43. The 2-wire control block then increments the address pointer to the next register address and sends the data to the master. The data bytes are read continuously until the master sends a NACK followed by a subsequent STOP condition directly after receiving the data. If a non-existent 2-wire address is read out, then the DA9210 returns code zero.

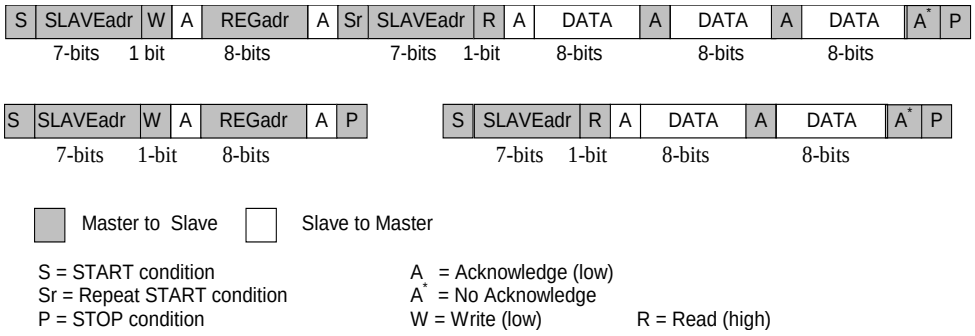


Figure 43: 2-WIRE Page Read

The slave address after the repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes after sending the register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an ACK until the master sends a STOP condition. The page write mode is illustrated in Figure 44.

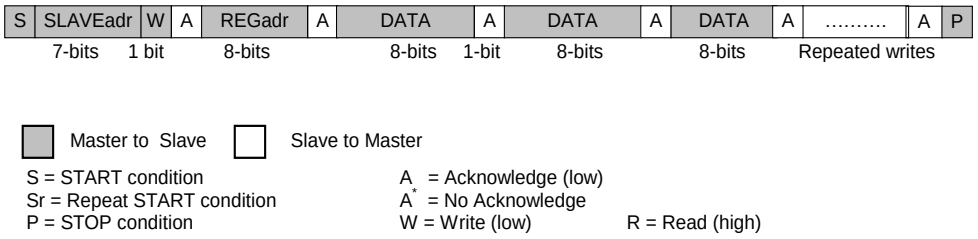


Figure 44: 2-WIRE Page Write

A repeated write mode can be enabled with WRITE_MODE control. In this mode, the master can execute back-to-back write operations to non-consecutive addresses by transmitting register addresses and data pairs. The data is stored in the address specified by the preceding byte. The repeated write mode is illustrated in Figure 45.

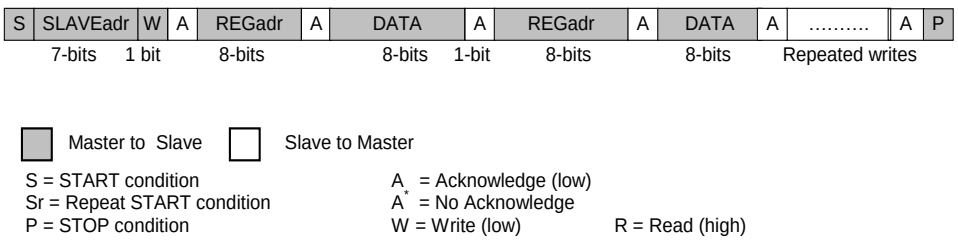


Figure 45: 2-WIRE Repeated Write

If a new START or STOP condition occurs within a message, the bus returns to idle mode.

10.5.3 DVC Interface

With control DVC_CTRL_EN, GPIO5 and GPIO6 can be dedicated to an alternative mode of defining the buck output voltage (supporting direct DVC) from the host processor to the buck. This is only enabled if GPIO5 and GPIO6 are configured for interface (setting 01) and IF_TYPE is asserted. Since the logical levels of the I/O are referenced to VDD_IO, a valid voltage at this port is needed.

After the DVC interface has been activated and synchronized, the buck converter target voltage is derived by adding a delta value to the voltage base register configured in VBUCK_BASE. The delta value is decoded by DA9210 from the number of clock rising edges at the SYNC pin while INPUT is kept high. During control via the DVC interface, the setting of registers VBUCK_A, VBUCK_B are ignored and the target output voltage is calculated as:

VOUT = VBUCK_BASE + (N x VSTEPS)

Where VVSTEPS is 10 mV and N can range from 0 to 32. The principle derivation of the target voltage is shown in Figure 46.

Example

The INPUT port is sampled high for 16 of the 32 samples, thus N = 16. If VBUCK_BASE = 0.8 V, the target voltage is VOUT = 0.8 V + (16 x 10 mV) = 0.96 V. Once the DVC interface is enabled, DA9210 will maintain the voltage set in VBUCK_A/VBUCK_B until the valid completion of the first 32 clock sample. The new value of the output voltage is automatically updated after the completion of 32 clock sample. The clocking SYNC signal can be stopped after a multiple of 32 cycles or it can run continuously. The value used for setting the target voltage is always based on the last 32 clock sample frame. There is no explicit frame sync signal. Once the DVC interface is enabled, the frame sync is implicit on the rising edge of the INPUT port, which indicates the start of a 32 clock frame. If a new rising edge occurs before the previous 32 clocks have been sampled, the current accumulated sample is discarded and a new 32 clock sample is started. The previous voltage setting for the buck converter is used as target in the meantime, until a valid sequence is decoded. If a zero value is sent to the INPUT port, VOUT will be equal to VBUCK_BASE so there is no rising edge and thus no frame sync. DA9210 will keep counting the clock edges at the SYNC port. In a similar way, if a high value is continuously sent to the INPUT port, VOUT will be equal to VBUCK_BASE + (32 x vSTEPS) although no frame sync takes place.

The host processor can monitor the configured target voltage on the (read only) register VBUCK_DVC.

The DVC interface is interrupted when DVC_CTRL_EN is released or the IF_TYPE/GPI4/GPIO5 configuration is changed. After disabling the DVC interface, the normal control of the output voltage via select register VBUCK_A, VBUCK_B will revert automatically. If FORCE_DVC_IF is not asserted, the DVC interface is disabled when the buck is disabled (this automatically clears DVC_CTRL_EN bit). Otherwise the DVC interface remains armed and, at the next enable of the buck converter, the target output value will be derived from the SYNC and INPUT ports, as soon as a valid completion of the first 32 clock sample takes place. Until a valid 32 clock sample is received, the output voltage is set via select register BUCK_SEL and VBUCK_A or VBUCK_B values.

If DVC_STEP_SIZE is asserted the output voltage will increase by double the amount of consecutive asserted bits (VVSTEPS will correspond to 20 mV instead of 10 mV).

Example

The INPUT port is sampled high for 16 of the 32 samples, thus N = 16. If DVC_STEP_SIZEis asserted and VBUCK_BASE = 0.8 V, the target voltage is VOUT = 0.8 V + (16 x 20 mV) = 1.12 V.

To limit the buck output voltage and prevent any failures in case of a communication error, a maximum value for the buck output target voltage can be stored in VBUCK_MAX. This value represents the absolute maximum voltage and it has priority over any value resulting from the addition of VBUCK_BASE and (N x VSTEPS) as well as over any value set on VBUCK_A and VBUCK_B, if the DVC interface is disabled. When the output voltage exceeds VBUCK_MAX, an event is generated and the OC_PG port is asserted, if not masked by M_VMAX. If the OC_PG port is configured for IRQ operation, an interrupt is generated instead.

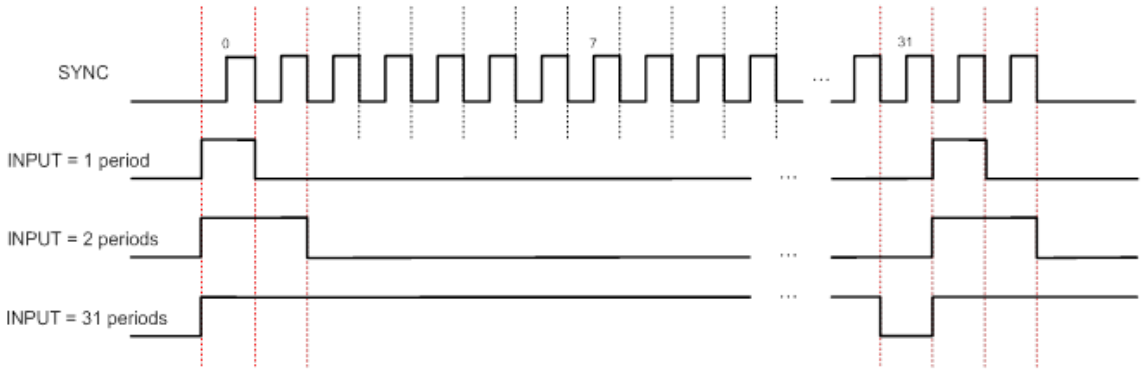


Figure 46: DVC Control Interface

10.6 Internal Temperature Supervision

To protect the DA9210 from damage due to excessive power dissipation, the internal temperature is continuously monitored. There are three temperature thresholds, TEMP_WARN, TEMP_CRIT, and TEMP_POR, respectively at typically 125 °C, 140 °C, and 150 °C.

When the junction temperature reaches the TEMP_WARN threshold, DA9210 asserts the bit TEMP_WARN and generates the event E_TEMP_WARN. If not masked via bit M_TEMP_WARN, the output port OC_PG/nIRQ is asserted. The status bit TEMP_WARN remains asserted while the junction temperature is higher than TEMP_WARN.

When the junction temperature increases further over TEMP_CRIT, the DA9210 immediately disables the buck converter, asserts the bit TEMP_CRIT and generates the event E_TEMP_WARN. If not masked via bit M_TEMP_WARN, the output port OC_PG/nIRQ is asserted. The status bit TEMP_CRIT remains asserted while the junction temperature is higher than TEMP_CRIT. The buck converter is disabled as long as the junction temperature is greater than TEMP_CRIT and is automatically re-enabled after the temperature recovers below the valid threshold (even if the controlling GPI is asserted). A direct write into BUCK_EN or a toggling of the controlling GPI is needed to enable the buck converter.

Whenever the junction temperature exceeds TEMP_POR, a power-on reset to the digital core is immediately asserted, which stops all functionality in DA9210. This is needed to prevent possible permanent damage in case of a fast temperature increase.

11 Register Definitions

11.1 Register Map

All bits loaded from OTP are marked in bold.

Addr	Function	7	6	5	4	3	2	1	0
Register Page 0									
0x00	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	REG_PAGE			
0x50	STATUS_A	Reserved	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
0x51	STATUS_B	Reserved	Reserved	Reserved	VMAX	TEMP_CRIT	TEMP_WARN	nPWRGOOD	OVCURR
0x52	EVENT_A	Reserved	E_GPI6	E_GPI5	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0
0x53	EVENT_B	Reserved	Reserved	Reserved	E_VMAX	E_TEMP_CRIT	E_TEMP_WARN	E_nPWRGOOD	E_OVCURR
0x54	MASK_A	Reserved	**M_GPI6**	**M_GPI5**	**M_GPI4**	**M_GPI3**	**M_GPI2**	**M_GPI1**	**M_GPI0**
0x55	MASK_B	Reserved	Reserved	Reserved	**M_VMAX**	**M_TEMP_CRIT**	**M_TEMP_WARN**	**M_nPWRGOOD**	**M_OVCURR**
0x56	CONTROL_A	Reserved	Reserved	**V_LOCK**	**SLEW_RATE**		**DEBOUNCING**		
0x57	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x58	GPIO0-1	**GPIO0_MODE**	**GPIO1_TYPE**	**GPIO1_PIN**		**GPIO0_MODE**	**GPIO0_TYPE**	**GPIO0_PIN**	
0x59	GPIO2-3	**GPIO3_MODE**	**GPIO3_TYPE**	**GPIO3_PIN**		**GPIO2_MODE**	**GPIO2_TYPE**	**GPIO2_PIN**	
0x5A	GPIO4-5	**GPIO5_MODE**	**GPIO5_TYPE**	**GPIO5_PIN**		**GPIO4_MODE**	**GPIO4_TYPE**	**GPIO4_PIN**	
0x5B	GPIO6	Reserved	Reserved	Reserved		**GPIO6_MODE**	**GPIO6_TYPE**	**GPIO6_PIN**	
0x5C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x5D	BUCK_CONT	**DVC_CTRL_EN**	**VBUCK_GPI**		**VBUCK_SEL**	**BUCK_PD_DIS**	**BUCK_GPI**		**BUCK_EN**

Addr	Function	7	6	5	4	3	2	1	0
Register Page 1									
0x80	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
0xD0	BUCK_ILIM	Reserved	Reserved	Reserved	**BUCK_IALARM**	**BUCK_ILIM**			
0xD1	BUCK_CONF1	**PWR_DOWN_CTRL**			**STARTUP_CTRL**			**BUCK_MODE**	
0xD2	BUCK_CONF2	Reserved	Reserved	Reserved	**AUTO_DEF**	**PH_SH_EN**	**PHASE_SEL**		
0xD3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0xD4	VBUCK_AUTO	Reserved	**VBUCK_AUTO**						
0xD5	VBUCK_BASE	Reserved	**VBUCK_BASE**						
0xD6	VBUCK_MAX	Reserved	**VBUCK_MAX**						
0xD7	VBUCK_DVC	Reserved	VBUCK_DVC						
0xD8	VBUCK_A	**BUCK_SL_A**	**VBUCK_A**						
0xD9	VBUCK_B	**BUCK_SL_B**	**VBUCK_B**						

Addr	Function	7	6	5	4	3	2	1	0
Register Page 2									
0x100	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved	REG_PAGE		
	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x105	INTERFACE	**IF_BASE_ADDR**				**R/W_POL**	**CPHA**	**CPOL**	**nCS_POL**
0x106	INTERFACE 2	**IF_TYPE**	**PM_IF_HSM**	**PM_IF_FMP**	**PM_IF_V**	Reserved	Reserved	Reserved	Reserved
0x140	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x141	Reserved	Reserved							
0x142	Reserved	Reserved							
0x143	CONFIG_A	Reserved	Reserved	Reserved	**2WIRE_TO**	**GPI_V**	**OC_PG_IRQ_CONF**	**OC_PG_IRQ_TYPE**	**OC_PG_IRQ_LEVEL**
0x144	CONFIG_B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x145	CONFIG_C	Reserved	**GPIO6_PUPD**	**GPIO5_PUPD**	**GPIO4_PUPD**	**GPIO3_PUPD**	**GPIO2_PUPD**	**GPIO1_PUPD**	**GPIO0_PUPD**
0x146	CONFIG_D	**OC_PG_KEEP**	**OC_PG_REL**	**OC_PG_MASK**		**READY_EN**	**FORCE_DVC_IF**	**DVC_STEP_SIZE**	Reserved
0x147	CONFIG_E	Reserved	Reserved	**OSC_TUNE**		Reserved	Reserved	Reserved	**STAND_ALONE**
0x14F	MISC_SUPP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**OTP_CLK_ON**

Figure 47: Register Map

11.2 Register Page Control

Table 17: PAGE_CON (0x00)

Bit	Type	Label	Description
7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
6	R/W	WRITE_MODE Note 1	2-WIRE multiple write mode 0: Page Write mode 1: Repeated Write mode
5:3	R/W	(Reserved)	
2:0	R/W	REG_PAGE	I^2C: 00x: Selects register 0x00 to 0xFF 01x: Selects register 0x100 to 0x17F SPI: 000: Selects register 0x00 to 0x7F 001: Selects register 0x80 to 0xFF 100: Selects register 0x100 to 0x17F >010: Reserved for production and test

Note 1 Not used for 4-WIRE-IF

11.3 Register Page 0

11.3.1 System Control and Event

The STATUS registers report the current value of the various signals at the time that it is read out.

NOTE
All the status bits have the same polarity as their corresponding signals.

Table 18: STATUS_A (0x50)

Bit	Type	Label	Description
7	R	Reserved	
6	R	GPI6	GPI6 level
5	R	GPI5	GPI5 level
4	R	GPI4	GPI4 level
3	R	GPI3	GPI3 level
2	R	GPI2	GPI2 level
1	R	GPI1	GPI1 level
0	R	GPI0	GPI0 level

Table 19: STATUS_B (0x51)

Bit	Type	Label	Description
7:5	R	Reserved	
4	R	VMAX	Asserted as long as the voltage configured for the buck converter is equal or greater than VBUCK_MAX
3	R	TEMP_CRIT	Asserted as long as the thermal shutdown threshold is reached
2	R	TEMP_WARN	Asserted as long as the thermal warning threshold is reached
1	R	nPWRGOOD	Asserted as long as the buck output voltage is out of range
0	R	OVCURR	Asserted as long as the buck is in overcurrent

The EVENT registers hold information about events detected by the DA9210.

If the OC_PG port is configured as IRQ line:

- The events are triggered by a change in the status register which contains the status of monitored signals.
- When an EVENT bit is set in the event register the IRQ signal shall be asserted, unless the event is masked by setting the associated bit in the mask register. The IRQ triggering event register is cleared from the host by writing back its read value. New events occurring during clearing is delayed before they are passed to the event register, ensuring that the host controller does not miss them.

If the OC_PG port is configured for dedicated communication to the host processor as described in Section 10.2.8, the port will be asserted according to the STATUS bits and the polarity of the STATUS indication (active high/low) can be selected separately (see GPIOxx_TYPE control). An EVENT is generated only during transition of the STATUS from inactive to active.

Table 20: EVENT_A (0x52)

Bit	Type	Label	Description
7	R	Reserved	
6	R	E_GPI6	GPI6 event according to active state setting
5	R	E_GPI5	GPI5 event according to active state setting
4	R	E_GPI4	GPI4 event according to active state setting
3	R	E_GPI3	GPI3 event according to active state setting
2	R	E_GPI2	GPI2 event according to active state setting
1	R	E_GPI1	GPI1 event according to active state setting
0	R	E_GPI0	GPI0 event according to active state setting

Table 21: EVENT_B (0x53)

Bit	Type	Label	Description
7:5	R	Reserved	
4	R	E_VMAX	VMAX caused event
3	R	E_TEMP_CRIT	TEMP_CRIT caused event

Bit	Type	Label	Description
2	R	E_TEMP_WARN	TEMP_WARN caused event
1	R	E_nPWRGOOD	nPWRGOOD caused event
0	R	E_OVCURR	OVCURR caused event

Table 22: MASK_A (0x54)

Bit	Type	Label	Description
7	R/W	Reserved	
6	R/W	M_GPI6	GPI6 nIRQ Mask
5	R/W	M_GPI5	GPI5 nIRQ Mask
4	R/W	M_GPI4	GPI4 nIRQ Mask
3	R/W	M_GPI3	GPI3 nIRQ Mask
2	R/W	M_GPI2	GPI2 nIRQ Mask
1	R/W	M_GPI1	GPI1 nIRQ Mask
0	R/W	M_GPI0	GPI0 nIRQ Mask

Table 23: MASK_B (0x55)

Bit	Type	Label	Description
7:5	R/W	Reserved	
4	R/W	M_VMAX	VMAX nIRQ / OC_PG Event Mask
3	R/W	M_TEMP_CRIT	Mask TEMP_CRIT nIRQ / OC_PG Event Mask
2	R/W	M_TEMP_WARN	TEMP_WARN nIRQ / OC_PG Event Mask
1	R/W	M_nPWRGOOD	PWRGOOD nIRQ / OC_PG Event Mask
0	R/W	M_OVCURR	OVCURR IRQ / OC_PG Event Mask

Table 24: CONTROL_A (0x56)

Bit	Type	Label	Description
7	R/W	Reserved	
5	R/W	V_LOCK	0: Allows host writes into registers 0xD0 to 0x14F 1: Disables register 0xD0 to 0x14F re-programming from control interfaces
4:3	R/W	SLEW_RATE	DVC slewing is executed at 00: 10 mV every 4.0 µs 01: 10 mV every 2.0 µs 10: 10 mV every 1.0 µs 11: 10 mV every 0.5 µs

Bit	Type	Label	Description
2:0	R/W	DEBOUNCING	GPI debounce time: 000: no debounce time 001: 0.1 ms 010: 1.0 ms 011: 10 ms 100: 50 ms 101: 250 ms 110: 500 ms 111: 1000 ms

11.3.2 GPIO Control

Table 25: GPIO0-1 (0x58)

Bit	Type	Label	Description
7	R/W	GPIO1_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
6	R/W	GPIO1_TYPE	0: GPI: active low 1: GPI: active high
5:4	R/W	GPIO1_PIN	PIN assigned to: 00: GPI 01: Verror signal 10: GPO (open-drain) 11: GPO (push-pull)
3	R/W	GPIO0_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
2	R/W	GPIO0_TYPE	0: GPI: active low 1: GPI: active high
1:0	R/W	GPIO0_PIN	PIN assigned to: 00: GPI 01: Reserved 10: GPO (open-drain) 11: GPO (push-pull)

Table 26: GPIO2-3 (0x59)

Bit	Type	Label	Description
7	R/W	GPIO3_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
6	R/W	GPIO3_TYPE	0: GPI: active low 1: GPI: active high
5:4	R/W	GPIO3_PIN	PIN assigned to: 00: GPI 01: BUCK_CLK signal 10: GPO (open-drain) 11: GPO (push-pull)
3	R/W	GPIO2_MODE	00: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
2	R/W	GPIO2_TYPE	0: GPI: active low 1: GPI: active high
1:0	R/W	GPIO2_PIN	PIN assigned to: 00: GPI 01: Iphase signal 10: GPO (open-drain) 11: GPO (push-pull)

Table 27: GPIO4-5 (0x5A)

Bit	Type	Label	Description
7	R/W	GPIO5_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
6	R/W	GPIO5_TYPE	0: GPI: active low 1: GPI: active high
5:4	R/W	GPIO5_PIN	PIN assigned to: 00: GPI 01: Interface 10: GPO (open-drain) 11: GPO (push-pull)
3	R/W	GPIO4_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level

Bit	Type	Label	Description
2	R/W	GPIO4_TYPE	0: GPI: active low 1: GPI: active high
1:0	R/W	GPIO4_PIN	PIN assigned to: 00: GPI (AC_OK) 01: Digital external clock input 10: GPO (open-drain) 11: GPO (push-pull)

Table 28: GPIO6 (0x5B)

Bit	Type	Label	Description
7:4	R/W	Reserved	
3	R/W	GPIO6_MODE	0: GPI: debounce off GPO: Sets output to low level 1: GPI: debounce on GPO: Sets output to high level
2	R/W	GPIO6_TYPE	0: GPI: active low 1: GPI: active high
1:0	R/W	GPIO6_PIN	PIN assigned to: 00: GPI 01: Interface 10: GPO (open-drain) 11: GPO (push-pull)

11.3.3 Regulator Control

Table 29: BUCK_CONT (0x5D)

Bit	Type	Label	Description
7	R/W	DVC_CTRL_EN	Main control of the dedicated DVC Interface: 0: Disabled 1: Enabled
6:5	R/W	VBUCK_GPI	GPIO select target voltage VBUCK_B on passive to active transition, selects target voltage VBUCK_A on active to passive transition (ramping) 00: Not controlled by GPIO 01: GPIO0 controlled 10: GPIO3 controlled 11: GPIO4 controlled
4	R/W	VBUCK_SEL Note 1	BUCK voltage is selected from (ramping): 0: VBUCK_A 1: VBUCK_B

Bit	Type	Label	Description
3	R/W	BUCK_PD_DIS	0: Enable pull-down resistor in disabled mode 1: No pull-down resistor in disabled mode
2:1	R/W	BUCK_GPI	GPIO enables the BUCK on passive to active state transition, disables the BUCK on active to passive state transition 00: Not controlled by GPIO 01: GPIO0 controlled 10: GPIO3 controlled 11: GPIO4 controlled
0	R/W	BUCK_EN	0: BUCK disabled 1: BUCK enabled

Note 1 Automatically set to 0 by default when the buck converter is enabled, except when the output voltage is controlled via GPI port.

11.4 Register Page 1

Table 30: PAGE_CON (0x80)

Bit	Type	Label	Description
7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
6	R/W	WRITE_MODE Note 1	2-WIRE multiple write mode 0: Page write mode 1: Repeated write mode
5:3	R/W	Reserved	
2:0	R/W	REG_PAGE	I^2C: 00x: Selects register 0x00 to 0xFF 01x: Selects register 0x100 to 0x17F SPI: 000: Selects register 0x00 to 0x7F 001: Selects register 0x80 to 0xFF 100: Selects register 0x100 to 0x17F >010: Reserved for production and test

Note 1 Not used for 4-WIRE-IF.

11.4.1 Regulators Settings

Table 31: BUCK_ILIM (0xD0)

Bit	Type	Label	Description
7:5	R/W	Reserved	
4	R/W	BUCK_IALARM	Current Alarm threshold is: 0: BUCKILIM – 300 mA 1: BUCKILIM – 600 mA
3:0	R/W	BUCK_ILIM	Current limit per phase: 0000: 1600 mA 0001: 1800 mA 0010: 2000 mA 0011: 2200 mA 0100: 2400 mA 0101: 2600 mA 0110: 2800 mA 0111: 3000 mA 1000: 3200 mA 1001: 3400 mA 1010: 3600 mA 1011: 3800 mA 1100: 4000 mA 1101: 4200 mA 1110: 4400 mA 1111: 4600 mA

Table 32: BUCK_CONF1 (0xD1)

Bit	Type	Label	Description
7:5	R/W	PWR_DOWN_CTRL	Voltage ramping during power down 000: 1.25 mV/µs 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs 101: 30 mV/µs 110: 40 mV/µs 111: no ramped power down

Bit	Type	Label	Description
4:2	R/W	STARTUP_CTRL	Voltage ramping during start-up 000: 1.25 mV/µs Soft startup with controlled slew rate 001: 2.5 mV/µs 010: 5 mV/µs 011: 10 mV/µs 100: 20 mV/µs Note 1 101: 30 mV/µs 110: 40 mV/µs 111: target voltage applied immediately (no soft start)
1:0	R/W	BUCK_MODE	00: Low Power/Normal mode controlled via voltage A and B registers 01: BUCK always operates in Low power mode 10: BUCK always operates in Normal mode 11: Automatic mode

Note 1 Settings higher than 20 mV/µs may cause significant overshoot

Table 33: BUCK_CONF2 (0xD2)

Bit	Type	Label	Description
7:5	R/W	Reserved	
4	R/W	AUTO_DEF	The buck Automatic Mode functions: 0: based on the voltage threshold VBUCK_AUTO 1: based on the output current load
3	R/W	PH_SH_EN	Enable current dependent phase shedding during Normal mode
2:0	R/W	PHASE_SEL	Phase selection of the multi-phase buck in synchronous mode: 000: 1 phase is selected 001: 2 phases are selected 010: 3 phases are selected (uneven 0/90/180 phase shift) 011: 4 phases are selected 1xx: 8 phases are selected (dual mode only)

Table 34: VBUCK_AUTO (0xD4)

Bit	Type	Label	Description
7	R/W	Reserved	
6:0	R/W	VBUCK_AUTO	Threshold voltage for the Automatic mode: 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Table 35: VBUCK_BASE (0xD5)

Bit	Type	Label	Description
7	R/W	Reserved	
6:0	R/W	VBUCK_BASE	Sets the base voltage for the buck output when using the DVC interface 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Table 36: VBUCK_MAX (0xD6)

Bit	Type	Label	Description
7	R/W	Reserved	
6:0	R/W	VBUCK_MAX	Sets the maximum voltage allowed for the buck output voltage 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Table 37: VBUCK_DVC (0xD7)

Bit	Type	Label	Description
7	R	Reserved	
6:0	R	VBUCK_DVC	Internal status of actual target voltage configured via DVC interface 0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Table 38: VBUCK_A (0xD8)

Bit	Type	Label	Description
7	R/W	BUCK_SL_A	0: Configures the BUCK to Normal mode, whenever selecting A voltage settings 1: Configures the BUCK to Low Power mode, whenever selecting A voltage settings
6:0	R/W	VBUCK_A	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Table 39: VBUCK_B (0xD9)

Bit	Type	Label	Description
7	R/W	BUCK_SL_B	0: Configures the BUCK to Normal mode, whenever selecting B voltage settings 1: Configures the BUCK to Low Power mode, whenever selecting B voltage settings
6:0	R/W	VBUCK_B	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V … 1000110: 1.0 V … 1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

11.5 Register Page 2

Table 40: PAGE_CON (0x100)

Bit	Type	Label	Description
7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
6	R/W	WRITE_MODE Note 1	2-WIRE multiple write mode 0: Page Write mode 1: Repeated Write mode
5:2	R/W	Reserved	
2:0	R/W	REG_PAGE	000: Selects register 0x01 to 0x3F 001: Selects register 0x81 to 0xCF 010: Selects register 0x101 to 0x1CF >010: Reserved for production and test

Note 1 Not used for 4-WIRE-IF

11.5.1 Interface and OTP Settings (shared with DA9063)

Table 41: INTERFACE (0x105)

Bit	Type	Label	Description
7:4	R	IF_BASE_ADDR	4 MSB of 2-WIRE control interfaces base address XXXX0000 11010000 = 0xD0 write address of PM 2-WIRE interface (page 0 and 1) 11010001 = 0xD1 read address of PM 2-WIRE interface (page 0 and 1) 11010010 = 0xD2 write address of PM-2-WIRE interface (page 2 and 3) 11010011 = 0xD3 read address of PM-2-WIRE interface (page 2 and 3) Code ‘0000’ is reserved for unprogramed OTP (triggers start-up with hardware default interface address)
3	R	R/W_POL	4-WIRE: Read/Write bit polarity 0: Host indicates reading access via R/W bit = ‘0’ 1: Host indicates reading access via R/W bit = ‘1’
2	R	CPHA	4-WIRE IF clock phase (see Table 3: 4-WIRE Clock Configurations)
1	R	CPOL	4-WIRE IF clock polarity 0: SK is low during idle 1: SK is high during idle

Bit	Type	Label	Description
0	R	nCS_POL	4-WIRE chip select polarity 0: low, (nCS) 1: high, (CS)

Note 1 Not used for 4-WIRE-IF.

Note 2 DA9210

Table 42: INTERFACE2 (0x106)

Bit	Type	Label	Description
7	R22	IF_TYPE	0: Power manager IF is 4-WIRE 1: Power manager IF is 2-WIRE
6	R/W	PM_IF_HSM	Enables continuous high speed mode on 2-WIRE interface if asserted (no master code required)
5	R/W	PM_IF_FMP	Enables 2-WIRE interface operating with fast mode+ timings if asserted
4	R/W	PM_IF_V	Power manager IF in 2-WIRE mode is supplied from: 0: VDDCORE 1: VDD_IO (4-WIRE always from VDD_IO)
3:0	R/W	Reserved	

11.5.3 Application Configuration Settings

Table 43: CONFIG_A (0x143)

Bit	Type	Label	Description
7:5	R	Reserved	
4	R/W	2WIRE_TO	Enables automatic reset of 2-WIRE IF in case of clock stays low for >35 ms 0: Disabled 1: Enabled
3	R/W	GPI_V	GPIs (not configured as Power Manager control inputs) are supplied from: 0: VDDCORE 1: VDD_IO
2	R/W	OC_PG_IRQ_CONF	Configuration for the OC_PG port: 0: Interrupt line 1: Over Current and Power Good
1	R/W	OC_PG_IRQ_TYPE	OC_PG output port is: 0: Push-pull 1: Open-drain (requires external pull-up resistor)
0	R/W	OC_PG_IRQ_LEVEL	OC_PG output port is: 0: Active low 1: Active high

Table 44: CONFIG_B (0x144)

Bit	Type	Label	Description
7:0	R/W	Reserved	

Table 45: CONFIG_C (0x145)

Bit	Type	Label	Description
7	R/W	Reserved	
6	R/W	GPIO6_PUPD	0: GPI: pull-down resistor disabled GPO (open-drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor enabled
5	R/W	GPIO5_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor enabled
4	R/W	GPIO4_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor enabled
3	R/W	GPIO3_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor
2	R/W	GPIO2_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor enabled
1	R/W	GPIO1_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor enabled
0	R/W	GPIO0_PUPD	0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor) 1: GPI: pull-down resistor enabled GPO (open-drain): pull-up resistor

Table 46: CONFIG_D (0x146)

Bit	Type	Label	Description
7	R/W	OC_PG_KEEP	0: Normal operation of OC_PG port 1: Over current alarm at OC_PG is masked for 100 µs after the buck rail is valid (when recovering from an out of range condition and during power up)
6	R/W	OC_PG_REL	0: OC_PG port is released 250 µs after BUCK_EN goes low 1: OC_PG port is released after the ramp down has completed
5:4	R/W	OC_PG_MASK	Over current alarm at OC_PG port is: 00: always active during DVC transitions of the buck converter 01: masked during DVC transitions of the buck converter + 2 µs extra masking at the end 10: masked during DVC transitions of the buck converter + 10 µs extra masking at the end 11: masked during DVC transitions of the buck converter + 50 µs extra masking at the end
3	R/W	READY_EN	GPIO3 is used as READY signal to inform the host processor of DVC ongoing (the GPIO3 needs to be configured as output and any write to GPIO3_MODE will be ignored): 0: Disabled 1: Enabled
2	R/W	FORCE_DVC_IF	0: The DVC_CTRL_EN is automatically reset when the buck converter is disabled 1: The DVC_CTRL_EN is not reset when the buck converter is disabled
1	R/W	DVC_STEP_SIZE	0: VSTEPS is configured to 10 mV when using the DVC interface 1: VSTEPS is configured to 20 mV when using the DVC interface
0	R/W	Reserved	

Table 47: CONFIG_E (0x147)

Bit	Type	Label	Description
7:6	R/W	Reserved	
5:4	R/W	OSC_TUNE	Tune the main 6 MHz oscillator frequency: 00: no tune 01: +180 kHz 10: +360 kHz 11: +540 kHz
3:1	R/W	Reserved	
0	R/W	STAND_ALONE	0: DA9210 is used as companion IC to DA9063 or compliant 1: DA9210 is stand alone or as companion IC with another PMU not DA9063 compliant

Table 48: MISC_SUPP (0x14F)

Bit	Type	Label	Description
7:1	R/W	Reserved	
0	R/W	OTP_CLK_ON	Forces the oscillator and the OTP clock on if asserted

Table 49: DEVICE_ID (0x201)

Bit	Type	Label	Description
7:0	R	DEV_ID	Device ID

Table 50: DEVICE_ID (0x202)

Bit	Type	Label	Description
7:4	R	MRC	Mask Revision Code
3:0	R	VRC	Chip Variant Code

Table 51: DEVICE-ID (0x203)

Bit	Type	Label	Description
7:0	R	CUST_ID	Customer ID

Table 52: CONFIG_ID (0x204)

Bit	Type	Label	Description
7:0	R	CONFIG_REV	OTP Settings Revision

12 Application Information

The components recommended in this section are examples selected from requirements of a typical application.

12.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors on all VDD and output rails. When selecting a capacitor, especially for types with high capacitance and small physical dimension, the DC bias characteristic has to be taken into account.

Table 53: Recommended Capacitor Types

Application	Value	Size	Temp. Char.	Tol	Rated Voltage	Type
VDDCORE output bypass	220 nF	0402	X5R +/- 15%	+/-10%	6.3 V	Murata GRM155R60J224KE01(ME01)
	220 nF	0201	X5R +/- 15%	+/-20%	6.3 V	Murata GRM033R60J224ME90
	200 nF	0201	X5R +/- 15%	+/-10%	16 V	Semco CL03A224KO3NNNC
	220 nF	0402	X7R +/- 15%	+/-10%	16 V	Murata GRM155R71C224KA12D (automotive)
VOUT_SENSE output bypass	47 µF	0805	X5R +/- 15%	+/-20%	4 V	Murata GRM21BR60G476ME15
	47 µF	0603	X5R +/- 15%	+/-20%	4 V	Semco CL10A476MR8NZN
	22 µF	0402	X5R +/- 15%	+/-20%	4 V	Semco CL05A226MR5NZNC
	47 µF	0805	X5R +/- 15%	+/-20%	10 V	Murata GRM21BR61A476ME15L (automotive)
	22 µF	0603	X5R +/- 15%	+/-20%	10 V	Murata GRM188R61A226ME15D (automotive)
	22 µF	0805	X6S +/- 22%	+/-20%	10 V	Murata GRM21BC81A226ME44L (automotive)
VDDx bypass	10 µF	0603	X5R +/- 15%	+/-20%	6.3 V	Murata GRM188R60J106ME84
	10 µF	0805	X7R +/- 15%	+/-10%	6.3 V	Murata GRM21BR70J106KE76L (automotive)
	10 µF	0603	X6S +/- 22%	+/-20%	10 V	Murata GRM188C81A106MA73D (automotive)
VSYS bypass	1 µF	0402	X5R +/- 15%	+/-10%	10 V	Murata GRM155R61A105KE15#

Application	Value	Size	Temp. Char.	Tol	Rated Voltage	Type
	1 µF	0402	X6S +/- 22%	+/-10%	10 V	Murata GRM155C81A105KA12D (automotive)

12.2 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated maximum current: Usually a coil provides two current limits: The Isat specifies the maximum current at which the inductance drops by 30 % of the nominal value. The Imax is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance: Critical to converter efficiency and should therefore be minimized.
- Inductance: Given by converter electrical characteristics; 0.47 µH for all DA9210 phases.

Table 54: Recommended Inductor Types (including only typical values for the parts)

Application	Value	Size	Imax(dc)	Isat	Tolerance	DC Res.	Type
BUCK	4x 0.47 µH	2.0x1.6x1.0 mm	3.3 A	3.5 A	+/-30%	48 mΩ	TOKO DFE201610C 1285AS-H-R47M
	4x 0.47 µH	2.0x1.6x1.2 mm	3.8 A	4.2 A	+/-30%	40 mΩ	TOKO DFE201612C 1286AS-H-R47M
	4x 0.47 µH	2.5x2.0x1.0 mm	3.6 A	3.9 A	+/-20%	35 mΩ	TOKO DFE252010C 1269AS-H-R47M
	4x 0.47 µH	2.5x2.0x1.2 mm	4.4 A	4.7 A	+/-20%	29 mΩ	TOKO DFE252012C 1239AS-H-R47M
	4x0.47 µH	2.0x1.6x1.0 mm	2.7 A	3.5 A	+/-20%	38 mΩ	TDK TFM201610A R47M
	4x0.47 µH	2.5x2.0x1.0 mm	2.8 A	4.5 A	+/-20%	34 mΩ	TDK TFM252010A R47M
	4x0.47 µH	2.0x1.6x1.0 mm	2.7 A	3.56 A	+/-20%	38 mΩ	Cyntec PIFE20161T
	4x0.47 µH	2.5x2.0x1.0 mm	3.5 A	4.5 A	+/-20%	34 mΩ	Cyntec PIFE25201T
	4x0.47 µH	2.5x2.0x1.2 mm	4.5 A	5.0 A	+/-20%	23 mΩ	Cyntec PIFE25201B
	4x0.47 µH	2.5x2.0x1.2 mm	3.7 A	3.9 A	+/-20%	25 mΩ	Cyntec PST25201B
	4x0.47 µH	2.0x2.0x1.2 mm	2.8 A	4.2 A	+/-30%	30 mΩ	Taiyo Yuden MDMK2020T R47M
	4x0.47 µH	2.5x2.0x1.2 mm	3.9 A	4.8 A	+/-20%	30 mΩ	Taiyo Yuden MAMK2520T R47M
	4x0.47 µH	2.0x1.6x1.0 mm	3.2 A	3.6 A	+/-20%	32 mΩ	Murata LQM2MPNR47MGH
	4x 0.47 µH	4x4x1.2 mm	8.7 A	6.7 A	+/-20%	14mΩ	Coilcraft XFL4012-471ME

12.3 Layout Guidelines

12.3.1 General Recommendations

- Appropriate trace width and amount of vias should be used for all power supply paths.
  Too high trace resistances can prevent the system operating correctly, for example, efficiency and current ratings of switch mode converters and charger might be degraded. Furthermore the PCB might be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.
  Special care must be taken with the DA9210 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row, connection to an inner layer is recommended (depending on the maximum current two or more vias might be required).
- A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references like VREF should be referred to a silent ground which is connected at a star point underneath or close to the DA9210 main ground connection.
- Generally all power tracks with discontinuous and / or high currents should be kept as short as possible.
- Noise sensitive analog signals like feedback lines should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or shielding of quiet signals by ground traces.

12.3.2 Switched Mode Supplies

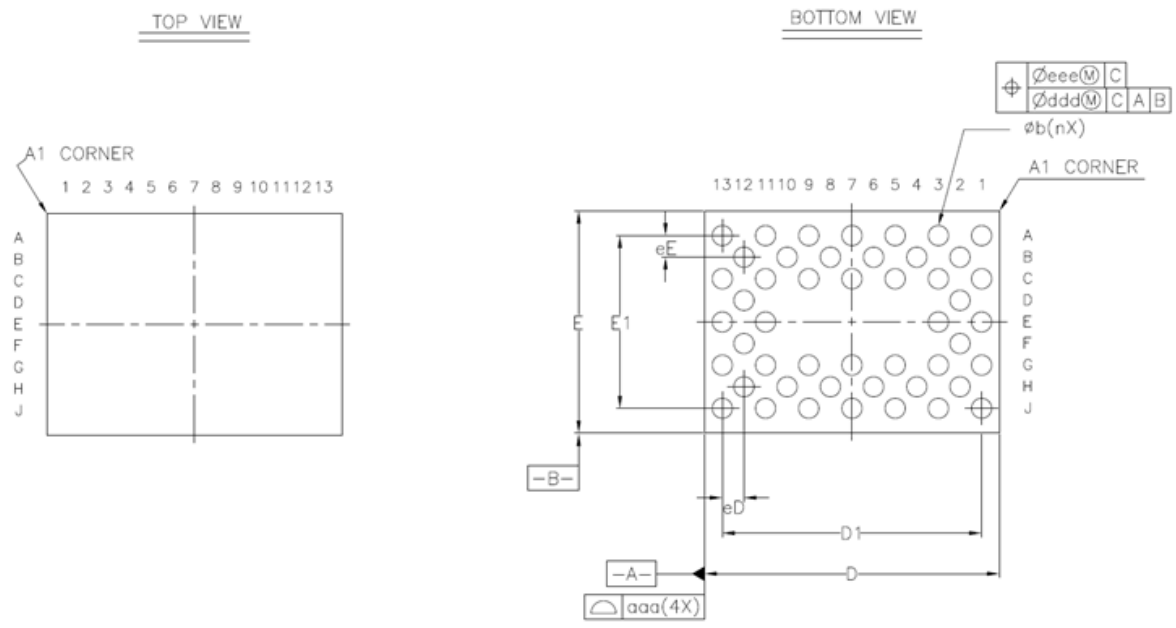
- The placement of the distributed capacitors at VSYS must ensure that all VDD inputs are connected to a bypass capacitor close to the pads. Using a local power plane underneath the chip for VSYS might be considered.
- The area of switched mode converter transient current loops should be minimized.
- Output capacitors of the LDOCORE should be placed close to DA9210.
- Care must be taken that no current is carried on feedback lines of the buck output voltage VOUT_SENSE.
- The inductor placement is less critical as parasitic inductances do not matter.

12.3.3 DA9210 Thermal Connection, Land Pad and Stencil Design

- The DA9210 provides a center ground area of balls, which are soldered to the PCB’s center ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB’s main ground plane in order to achieve good thermal performance.
- Solder mask openings for the ball landing pads must be arranged to prohibit solder balls flowing into vias.

13 Package Information

13.1 Package Outline Drawing (48 WLCSP)



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.471	0.511	0.551
Stand Off	A1	0.177	–	0.205
Wafer Thickness	A2	0.279 ±0.025		
Body Size	D	3.96 +/– 0.040		
	E	2.98 +/– 0.040		
Ball Diameter (Size)		0.25		
Ball/Bump Width	b	0.255	0.270	0.285
Ball/Bump Pitch	eD	0.29		
	eE	0.29		
Ball/Bump Count	n	48		
Edge Ball Center to Center	D1	3.48 BSC		
	E1	2.32 BSC		
Package Edge Tolerance	aaa	0.03		
Coplanarity (whole wafer)	ccc	0.03		
Ball/Bump Offset (Package)	ddd	0.05		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 48: Package Outline Drawing (48 WLCSP)

The package uses Dialog's innovative RouteEasy™ technology (Patent pending) implementing a high number of IOs on a small footprint package without the need for cost intensive PCB technology. All signals can be routed within two signal layers of a standard PCB (single trace between IC lands) and the inter layer connection uses drilled VIAs (no need for micro-VIA or VIA-in-land technology). Please contact your local Dialog Semiconductor support for more information about PCB Layout Guidelines

13.1.1 RouteEasy™ Technology Chart

BGA ball diameter: 0.27 (10 mm)

BGA land size: 0.25 (10 mm)

Via hole size (FHS): ≤ 0.2 - 0.25 (8 – 10 mm)

Via pad size: ≤ 0.45 (18 mm)

Anti-pad size: ≤ 0.65 (26 mm)

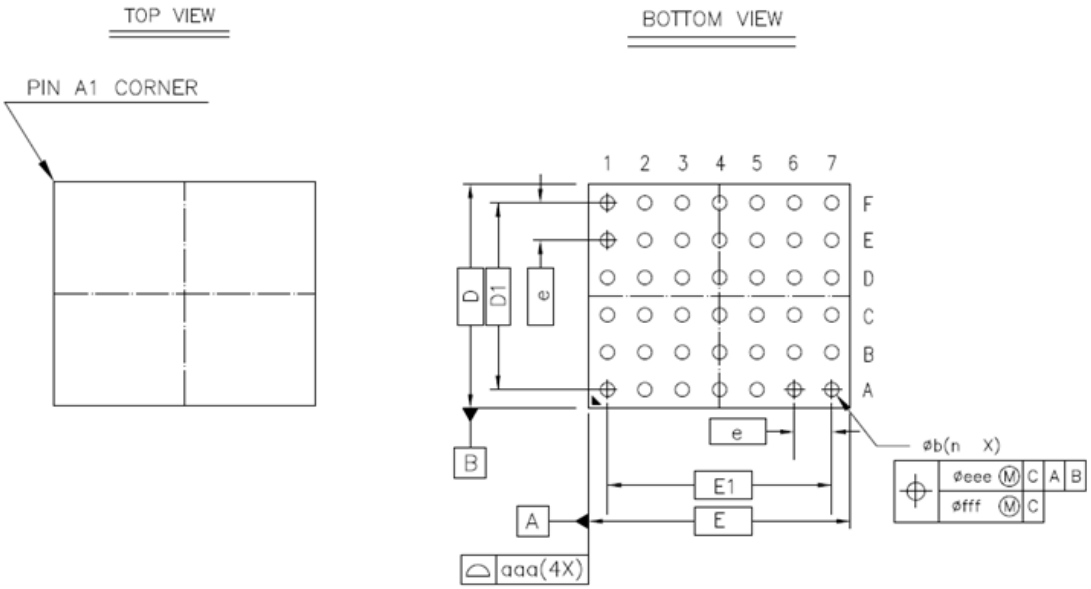
Trace width: ≥ 0.1 – 0.125 (4 – 5 mm)

Trace/Trace space: ≥ 0.1 – 0.125 (4 – 5 mm)

Trace/Pad/Land space: ≥ 0.1 (4 mm)

NOTE
Dimensions are in millimeter. The PCB design complexity is compatible with 0.8 mm BGA pin pitch (similar to IPC 6012B Class 2). Better thermal relief and improved high current return paths are achieved by using a reduced copper-to-hole distance for the inner layer reference planes (inner anti-pad size: 0.55 mm or 0.6 mm).

13.2 Package Outline Drawing (42 VF-BGA)



		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			MFC VFBGA		
Body Size:	X	E	5.600		
	Y	D	4.800		
Ball Pitch :		e	0.800		
Total Thickness :		A	0.850	0.920	0.990
Mold Thickness :		M	0.540 Ref.		
Substrate Thickness :		S	0.170 Ref.		
Ball Diameter :			0.300		
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa	0.070		
Mold Parallelism :		bbb	0.100		
Coplanarity:		ddd	0.080		
Ball Offset (Package) :		eee	0.120		
Ball Offset (Ball) :		fff	0.050		
Ball Count :		n	42		
Edge Ball Center to Center :	X	E1	4.800		
	Y	D1	4.000		

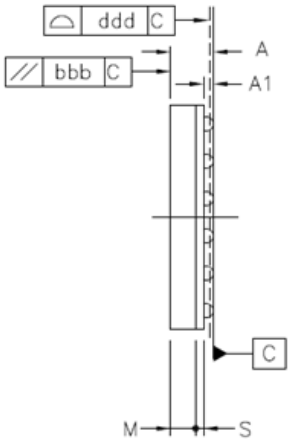


Figure 49: Package Outline Drawing (42 VF-BGA)

13.3 Soldering Information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

14 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 55: Ordering Information

Part number	Package	Size (mm)	Shipment form	Pack quantity	Comments
DA9210-xxUK2	48 WLCSP		Tape and Reel	5000	
DA9210-xxFN2-A	42 VFBGA		Tape and Real	5000	Automotive AEC-Q100 Grade 3

Appendix A Definitions

A.1 Power Dissipation and Thermal Design

When designing with the DA9210, consideration must be given to power dissipation because if the device exceeds the package power dissipation, the internal thermal sensor shuts the device down until it has cooled sufficiently.

The package includes a thermal management paddle to enable improved heat spreading on the PCB.

Linear regulators operating with a high current and high differential voltage between input and output will dissipate the following power:

$$P_{diss} = (V_{in} - V_{out}) * I_{out}$$

Example – a regulator supplying 150 mA @ 2.8 V from a fully charged lithium battery (VDD = 4.1 V)

Pdiss = (4.1 V - 2.8 V) * 0.15 A = 195 mW

For switching regulators

POUT = PIN * efficiency

Therefore

Pdiss = PIN – POUT

$$P_{diss} = \frac{P_{out}}{Efficiency} - P_{out}$$

$$P_{diss} = P_{out} * \left(\frac{1}{Efficiency} - 1 \right)$$

$$P_{diss} = I_{out} * V_{out} * \left(\frac{1}{Efficiency} - 1 \right)$$

Example – an 85 % efficient buck converter supplying 1.2V@ 400 mA

$$P_{diss} = 1.2V * 0.4A * \left(\frac{1}{0.85} - 1 \right) = 85mW$$

As the DA9210 is a multiple regulator configuration each supply must be considered and summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

A.2 Regulator Parameter - Dropout Voltage

In the DA9210, a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and when entering the dropout condition the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on the output voltage tracks the input voltage and regulation ceases. As the DA9210 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the ON resistance of the device. In the device, the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm process, Dialog are able to achieve very small pass transistor sizes for superior performance.

VDROPOUT = VIN – VOUT = RDSON * IOUT

When defining dropout voltage, it is specified in relation to a minimum acceptable change in output voltage. For example, all Dialog regulators have the dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest ON resistance for internal device) and maximum load current.

A.3 Regulator Parameter – Power Supply Rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 A before reaching a steady state of 1.4 A (see Figure 50). Due to the battery having a finite internal resistance (typically 0.5 Ω), these current peaks induce ripple on the battery voltage of up to 500 mV. As the supplies to the audio and RF are derived from this supply, it is essential that this ripple is removed, otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions when the battery is at its minimum operating voltage, when there is minimum headroom available due to dropout.

A.4 Regulator Parameter – Line Regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage Vreg (regulator operating with a constant load current) in response to a change in the input voltage Vin. Transient line regulation is a measurement of the peak change Vreg in regulated voltage seen when the line input voltage changes.

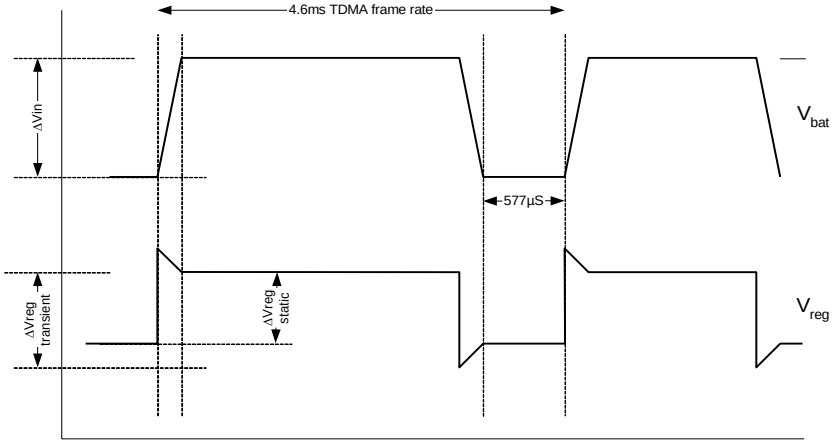


Figure 50: Line Regulation

A.5 Regulator Parameter – Load Regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage ΔVreg in response to a change in the regulator loading Δload whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage ΔVreg seen when the regulator load changes.

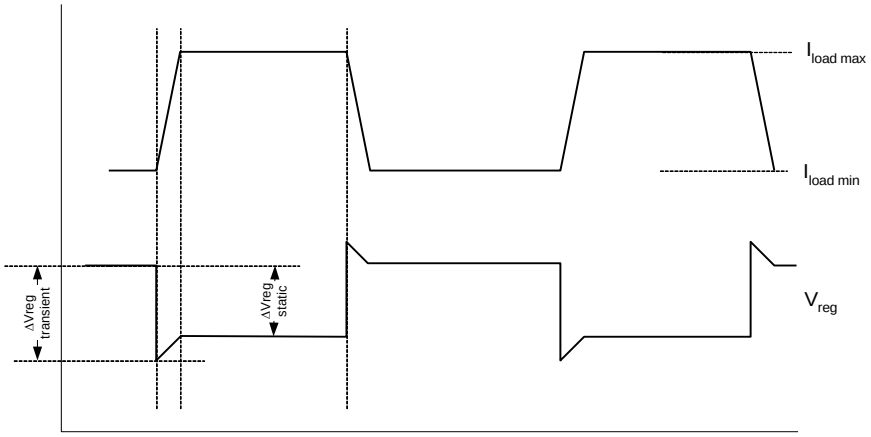


Figure 51: Load Regulation

Please contact Dialog Semiconductor for the latest application information on the DA9210 and other power management devices.

Revision History

Revision	Date	Description
1.0	Oct 2011	Initial release
1.1 to 1.x	Mar 2015	Regular updates for development and specification alignment
2.0, 2.1	Sep 2016	Updated and standardized to latest publishing guidelines
2.2	Sep 2017	Addition of automotive application disclaimer
2.3	Feb 2022	Rebranded file with new logo, copyright and disclamer

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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