



# V850E2/FL4

## 32-bit Single-Chip Microcontroller

**μPD70F3559**

**μPD70F4011**

**μPD70F3560**

**μPD70F4012**

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## Notes for CMOS Devices

### (1) Precaution against ESD for semiconductors

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### (2) Handling of unused input pins for CMOS

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### (3) Status before initialization of MOS devices

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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# Chapter 1 Overview

## 1.1 Naming

### 1.1.1 Alternative function pins

Peripheral	Prefix	Function name	Suffix
Short-cut of macro name	Consecutive number for same peripheral module <sup>a</sup>	Peripheral Macro pin naming	Consecutive number for same pin names <sup>a</sup>

a) This is an option that can be omitted if meaning is obvious

Example:

- TAUB0I0, TAUB1I5
- URTE0TX, URTE0RX, URTE1TX, URTE1RX
- CSIG0SO, CSIG0SI, CSIG0SC, CSIG0RY

### 1.1.2 Power supply pins

Function	Prefix	Kind of supply	Suffix
Symbol	Consecutive number for different functions <sup>a</sup>	VDD or VSS	Consecutive number for different pins with same meaning <sup>a</sup>

a) This is an option that can be omitted if meaning is obvious

Example:

- E0VDDn, REG0VSS

**Table 1-1 Selection for Functions**

Function	Explanation
C	Core supply
REG	Internal regulator supply
OSC	Oscillator supply
F	Flash module supply
E	Standard buffer supply (mainly 5V or up to 40Mhz)
B	Standard buffer supply (mainly 3.3V or beyond 40Mhz)
A	Analog module supply (e.g. ADC)

If not mentioned otherwise this document neglects suffixes for power supply pins with same functions that can be treated as equal.

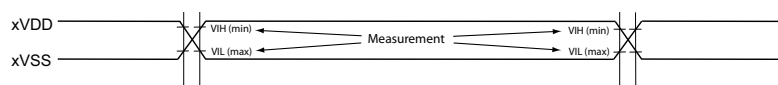
## 1.2 Pin Groups

Symbol	Pin group supplied by	Related pins / ports
PgE0	E0VDD	JP0, P0, _RESET, FLMD0, WAKE, VCPC0IN, VCPC1IN
PgE1	E1VDD / E1VSS	P1, P2, P3, P4
PgB0	B0VDD / B0VSS	P21, P24, P25, P27
PgOSC	OSCVDD / OSCVSS	X1, X2, XT1, XT2
PgA0	A0VDD / A0VSS	P10, P11, ADCA0Im

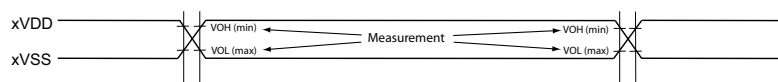
## 1.3 General measurement conditions

### 1.3.1 AC characteristic measurement condition

#### AC test input waveform

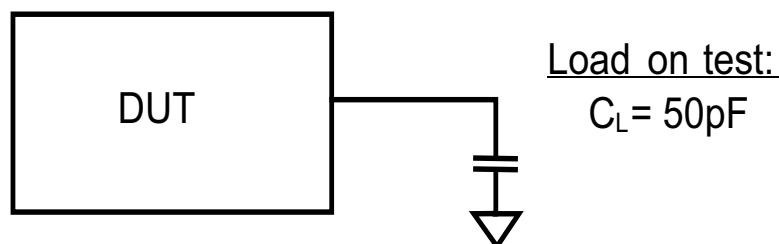


#### AC test output waveform



Standard AC test condition is 70%/30% of the applied IO supply voltage ( $XmVDD$ ) if not otherwise stated in the according AC timing specification of an interface.

#### AC Test Condition: Ext. Capacitive Load



## Chapter 2 Absolute maximum ratings

### 2.1 Supply voltages

Table 2-1 VDD Data

Parameter	Symbol	Condition	Ratings	Unit
System	CVDD	M2 products only	-0.5 ~ 1.6	V
System	FVDD		-0.5 ~ 6.0	V
	OSCVDD		-0.5 ~ 6.0	V
	REG0VDD		-0.5 ~ 6.0	V
	REG1VDD		-0.5 ~ 6.0	V
	REG2VDD		-0.5 ~ 6.0	V
	REG3VDD		-0.5 ~ 6.0	V
Ports	E0VDD		-0.5 ~ 6.0	V
	E1VDD		-0.5 ~ 6.0	V
Port	B0VDD		-0.5 ~ 6.0	V
ADCA0	A0VREFP		-0.3 ~ A0VDD+0.3 -0.3~6.0	V
ADCA0	A0VDD		-0.5 ~ 6.0	V
ADCA1	A1VDD		-0.5 ~ 6.0	V
	A1VREFP		-0.3 ~ A1VDD+0.3 -0.3~6.0	V

Table 2-2 VSS Data

Parameter	Symbol	Condition	Ratings	Unit
System	CVSS	M2 products only	-0.5 ~ 0.5	V
System	FVSS		-0.5 ~ 0.5	V
	OSCVSS		-0.5 ~ 0.5	V
	REG0VSS		-0.5 ~ 0.5	V
	REG1VSS		-0.5 ~ 0.5	V
	REG2VSS		-0.5 ~ 0.5	V
	REG3VSS		-0.5 ~ 0.5	V
Ports	E1VSS		-0.5 ~ 0.5	V
	B0VSS		-0.5 ~ 0.5	V
ADC0	A0VSS		-0.5 ~ 0.5	V
	A0VREFM		-0.3 ~ A0VDD+0.3 -0.3~6.0	V
ADC1	A1VSS		-0.5 ~ 0.5	V
	A1VREFM		-0.3 ~ A1VDD+0.3 -0.3~6.0	V

## 2.2 Port voltages

Table 2-3 Port Input voltage

Parameter	Pin Group	Symbol <sup>a</sup>	Condition	Ratings	Unit
Input voltage <sup>b</sup>	PgE0	$V_{I0}$	$E0VDD \leq 5.5$	$-0.5 \sim E0VDD + 0.5$	V
	PgE1	$V_{I1}$	$E1VDD \leq 5.5$	$-0.5 \sim E1VDD + 0.5$	V
	PgB0	$V_{I2}$	$B0VDD \leq 5.5$	$-0.5 \sim B0VDD + 0.5$	V
	PgOSC	$V_{I5}$	$OSCVDD \leq 5.5$	$-0.5 \sim OSCVDD + 0.5$	V
	PgA0	$V_{I3}$		$A0VDD + 0.3$	V
	PgA1	$V_{I4}$		$A1VDD + 0.3$	V

- a) The symbols reflect all supplies within the device series. Therefore not every symbol is available for each product.
- b) The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

## 2.3 Port current

Table 2-4 High level port output current

Parameter	Pin Group <sup>a</sup>	Symbol	Condition	Max. spec	Unit
High level output current	PgE0	IOH	1 pin of PgE0	-10	mA
			Power supply of PgE0	-50	
	PgE1		1 pin of PgE1	-10	
			Power supply of PgE1	-150	
	PgA0		1 pin of PgA0	-10	
			Power supply of PgA0	-25	
High level output current	PgA1	1 pin of PgA1	-10	mA	
		Power supply of PgA1	-25		
High level output current	Pgb0	1 pin of Pgb0	-10	mA	
		Power supply of Pgb0	-200		

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

Table 2-5 Low level port output current

Parameter	Pin Group <sup>a</sup>	Symbol	Condition	Max. spec	Unit
Low level output current	PgE0	IOL	1 pin of PgE0	10	mA
			Power supply of PgE0	50	
	PgE1		1 pin of PgE1	10	
			Power supply of PgE1	150	
	PgA0		1 pin of PgA0	10	
			Power supply of PgA0	25	
Low level output current	PgA1	1 pin of PgA1	10	mA	
		Power supply of PgA1	25		
Low level output current	Pgb0	1 pin of Pgb0	10	mA	
		Power supply of Pgb0	150		

a) The column reflects all supplies within the device series. Therefore not each pin group is available for each product.

## 2.4 Capacitance

Parameter	Symbol	Condition	Max. spec	Unit
Input capacitance	$C_I$	f = 1 MHz 0V for non measurement pins	15	pF
Input/Output capacitance	$C_{IO}$		15	pF
Output capacitance	$C_O$		15	pF

## 2.5 Thermal characteristics

Table 2-6 Thermal characteristics

Parameter	Symbol	Condition	Ratings	Unit
Storage temperature	$T_{STG}$		-65 ~150	°C
Operating ambient temperature	$T_a$	(A) grade products	-40 ~85	
		(A1) grade products	-40 ~110	
Junction temperature	$T_j$		-40 ~150	

This section specifies the absolute maximum limitation of operating and storage temperature.

The device's functions are not guaranteed outside of the specified maximum temperature ratings.

## Chapter 3 Power supply specification

### 3.1 Requirements for external power supply connections

The user has to ensure a low resistive connection of all VSS pins on the PCB. This specification denotes ground supply pins as:

- VSS = OSCVSS = REGnVSS = EnVSS = BnVSS = AnVSS = AnVREM = CVSS = 0V

in the further text.

With

- EnVSS = E1VSS
- BnVSS = B0VSS
- REGnVSS = REG0VSS = REG1VSS = REG2VSS = REG3VSS
- AnVSS = A0VSS = A1VSSAnVREFM = A0VREFM = A1VREFM

The user has to ensure a low resistive connection of all VDD pins to the related power supply. This specification denotes power supply pins as:

- EnVDD, BnVDD, FVDD, REGnVDD, OSCVDDCVDD, AnVDD and AnVREFFP.

in the further text.

With

- EnVDD = E0VDD = E1VDD
- BnVDD = B0VDD
- REGnVDD = REG0VDD = REG1VDD = REG2VDD = REG3VDD.
- AnVDD = A0VDD = A1VDD
- AnVREFFP = A0VREFFP = A1VREFFP
- I/OVDD = AnVDD, EnVDD, B0VDD, FVDD, OSCVDD

### 3.2 Power area definitions

The device consists of the following power areas:

- AWO (Always On area)
- ISO0 (Isolated area 0)
- ISO1 (Isolated area 1)

The table below lists the related core and port voltage supply of each power area:



Table 3-1 Power areas supply voltages

Power Area	Supply voltage	Related pins
AWO	Core supply	REG0VDD, REG0VSS, REG0C
	Port Supply	E0VDD
	Other	OSCVDD, OSCVSS FVDD0
ISO0	Core supply	REG1VDD, REG1VSS, REG1C REG2VDD, REG2VSS, REG2C REG3VDD, REG3VSS, REG3C
	Port Supply	E1VDD, E1VSS
	Other	A0VREFP, A0VREFM A0VDD, A0VSS
ISO1	Core supply	REG1VDD, REG1VSS, REG1C REG2VDD, REG2VSS, REG2C REG3VDD, REG3VSS, REG3C CVDD, CVSS
	Port Supply	B0VDD, B0VSS
	Other	A1VDD, A1VSS A1VREFP, A1VREFM

### 3.3 Power supply groups

For each of the following power supply groups the same voltage must be supplied:

Table 3-2 Power supply groups

Power supply group	Related pins
#1	REG0VDD, REG1VDD, FVDD, OSCVDD, E0VDD, E1VDD
#2	B0VDD
#3	M1 products: REG2VDD, REG3VDD M2 products: n.a.
#4	M1 products: n.a. M2 products: CVDD
#5	A0VDD, A0VREFP
#6	A1VDD, A1VREFP
#7	All VSS

### 3.4 Supply voltages

Table 3-3 VDD Data

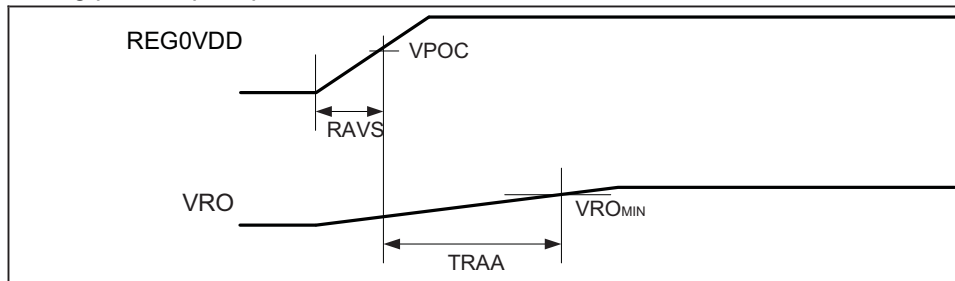
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
System supply voltage	FVDD		VPOC	-	5.5	V
System supply voltage	OSCVDD		VPOC	-	5.5	V
System supply voltage	REG0VDD	REG0VDD = REG1VDD = REG2VDD = REG3VDD	VPOC	-	5.5	V
System supply voltage	REG1VDD		VPOC	-	5.5	V
System supply voltage	REG2VDD		VPOC	-	5.5	V
System supply voltage	REG3VDD		VPOC	-	5.5	V
System supply voltage	CVDD	M2 products only	1.1	-	1.3	V
System supply voltage slopes	AIVS	M2 products; REG1VDD = 3.0V to 5.5V	-	-	5.6	V/ms
Port supply voltages	E0VDD		VPOC	-	5.5	V
Port supply voltages	E1VDD		VPOC	-	5.5	V
Port supply voltages	B0VDD	$B0VDD \leq$ power supply group #1 voltages	VPOC	-	5.5	V
ADC supply voltages	A0VDD	12bit resolution	4.5	-	5.5	V
ADC supply voltages	A0VDD	10bit resolution	VPOC	-	5.5	V
ADC supply voltages	A0VREFP		A0VDD	-	A0VDD	V
ADC supply voltages	A1VDD	12bit resolution	4.5	-	5.5	V
ADC supply voltages		10bit resolution	VPOC	-	5.5	V
ADC supply voltages	A1VREFP	$A1VREFP - A1VREFM > A1VDD/2$	A1VDD	-	A1VDD	V

### 3.4.1 AWO Regulator characteristics

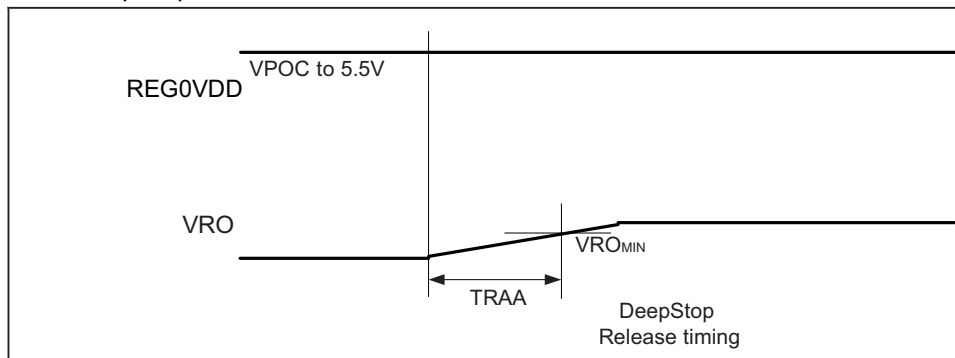
Table 3-4 AWO Regulator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Regulator Output voltage	VRO		1.1	1.2	1.3	V
System supply voltage slope	RAVS	0V to 3.0V	-	-	1800	V/ms
Capacitance on REG0C	REG0C		3.29	4.7	6.11	$\mu$ F
Output voltage stabilization time	TRAA	After REG0VDD reaches 3.0V	-	-	1	ms
		After DeepStop mode	-	-	0.5	ms

During power-up sequence



After DeepStop mode



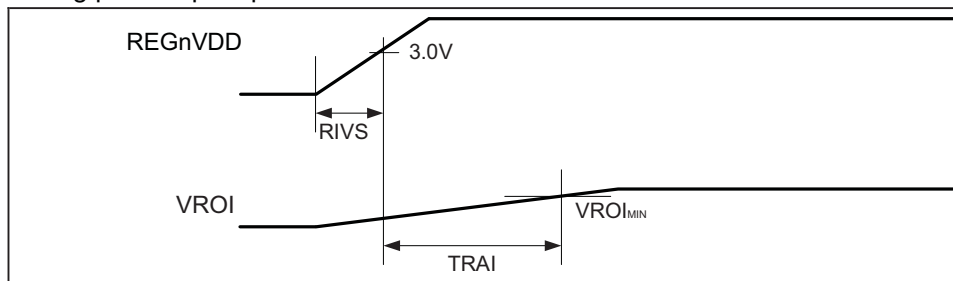
### 3.4.2 ISO0/ISO1 Regulator characteristics (M1 products)

Table 3-5 ISO0/ISO1 regulator characteristics

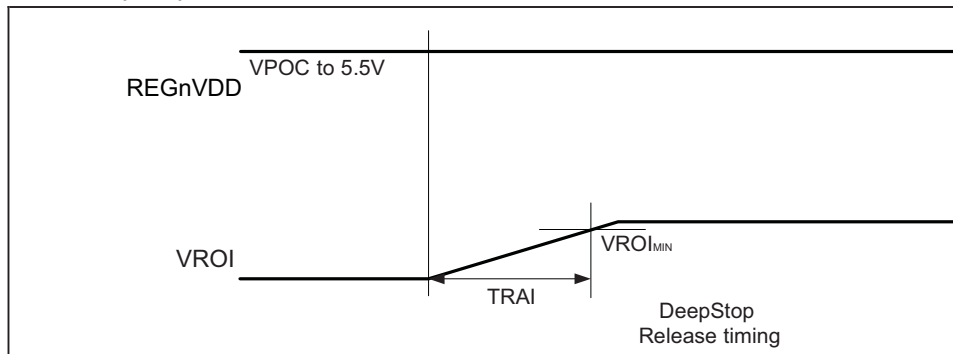
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Output voltage	VROI		1.1	1.2	1.3	V
Capacitance on REGnC	REGnC		3.29	4.7	6.11	$\mu\text{F}$
Voltage slope	RIVS	0V to 5.5V	-	-	5600	V/s
Output voltage stabilization time	TRAJ	After REGnVDD reaches 3.0V	-	-	1	ms
		After DeepStop mode	-	-	0.5	ms

Note n=1-3

During power-up sequence



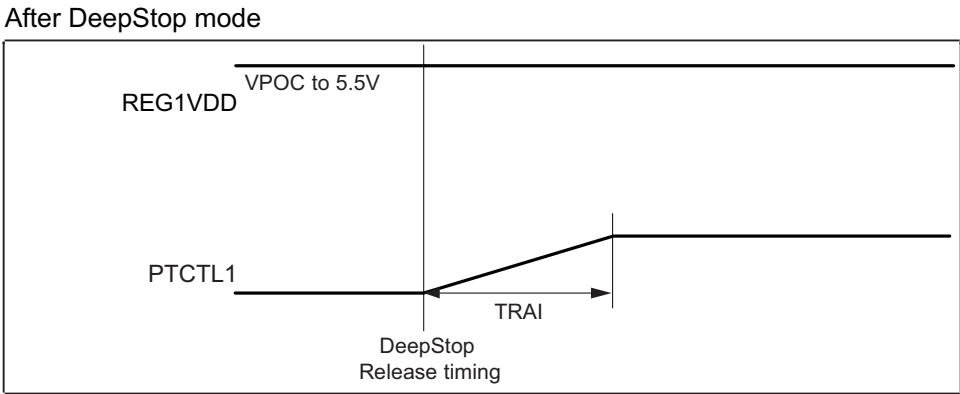
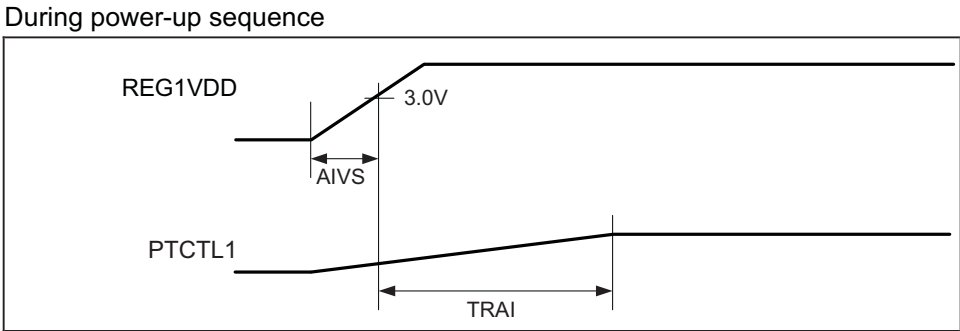
After DeepStop mode



### 3.4.3 Amplifier characteristics (M2 products)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
System supply voltage	REG1VDD		VPOC		5.5	V
Capacitance on CVDD	CVDDC	For each CVDD <sup>a</sup>	3.29	4.7	6.11	$\mu\text{F}$
Voltage slope	AIVS	3.0V to 5.5V	-	-	5.6	V/ms
PTCTL1 stabilization time	TRAJ	After REG1VDD reaches 3.0V	-	-	1	ms
		After DeepStop mode	-	-	0.5	ms
PTCTL1 output current	IPTCTL		-	-	1.55	mA

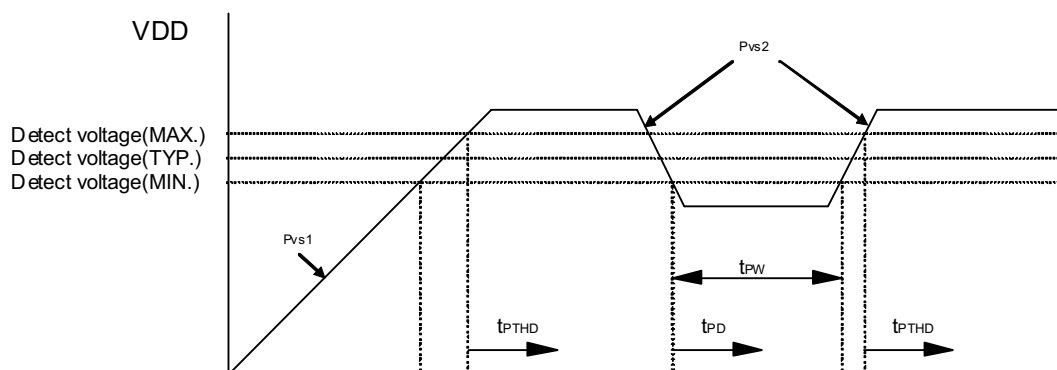
a) Required when using an external power transistor such as 2SD1584 (base connected to PTCTL1)



### 3.4.4 POC characteristics

Table 3-6 POC characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VPOC		2.8	2.9	3.0	V
Voltage slope 1	PVS1		0.18	-	1800	V/ms
Voltage slope 2	PVS2		0.0018	-	1800	V/ms
Response time 1	tPTH	From detect voltage to release of reset signal. Voltage slope = PVS1, PVS2	-	-	2	ms
Response time 2	tPD	From detect voltage to occurrence of reset signal Voltage slope = PVS2	-	-	2	ms
VDD minimum width	tPW		0.2	-	-	ms



### 3.4.5 Voltage Comparator characteristics

Table 3-7 VCMP characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Input voltage range of VCPCnIN	VICMP		REG0VSS	-	REG0VDD	V

Note VDD: REG0VDD

## 3.5 Power-up/-down sequence of external supply voltages

### 3.5.1 External FLMDn Resistors

Valid for all conditions described in the following

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 external pull-down resistor	R1		82	-	-	k $\Omega$
FLMD1 external pull-down resistor	R2		-	10	-	k $\Omega$

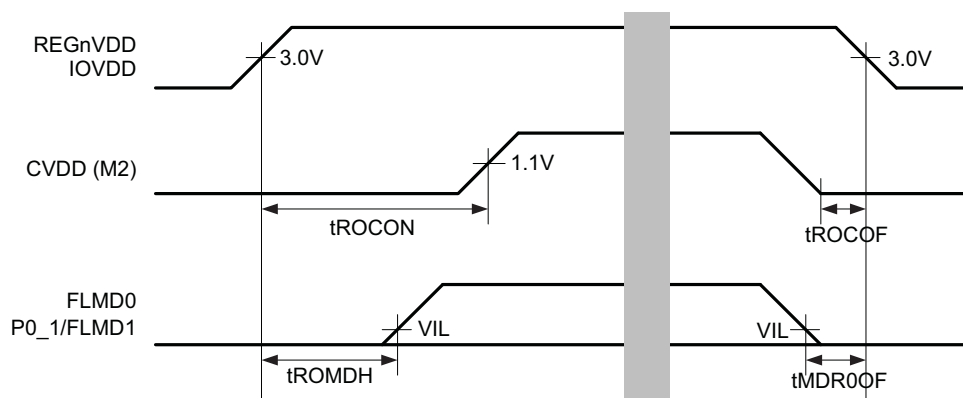
### 3.5.2 Condition 1

M1 products: RESET is not used

M2 products: RESET, WAKE and PTCTL1 are not used

Normal operating mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (rise)	tROCON		1	-	10	ms
REG0VDD, IOVDD (rise) to FLMD0,1 ( $\leq$ VIL) hold time	tROMDH		2	-	-	ms
FLMD0,1 ( $\leq$ VIL) to REG0VDD, IOVDD (fall)	tMDR0OF		0	-	-	ms
CVDD (0V) to REG0VDD, IOVDD (fall)	tCR0OF		0	-	-	ms



**Note** IOVDD: AnVDD, B0VDD, EnVDD, FVDD, OSCVDD

## 3.5.3 Condition 2

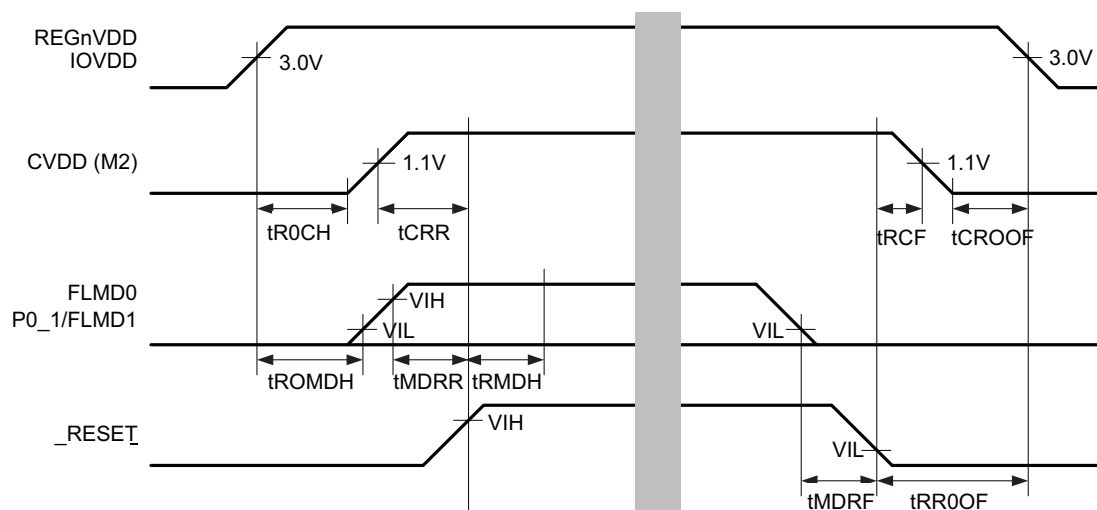
M1 products: RESET is used

M2 products: RESET is used; WAKE and PTCTL1 are not used

Normal operating mode / Serial programming mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REGnVDD, IOVDD (rise) to CVDD (0V) hold time	tR0CH		1	-	-	ms
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1( $\leq$ VIL) hold time	tROMDH		1	-	-	ms
CVDD (rise) to _RESET (rise)	tCRR		0	-	-	ms
FLMD0,1 ( $\geq$ VIH or VIL1) <sup>a</sup> to _RESET( $\leq$ VIL) (rise)	tMDRR		1	-	-	ms
_RESET (rise) to FLMD0,1( $\geq$ VIH or $\leq$ VIL) hold time	tRMDH		1	-	-	ms
FLMD0,1,MODE0,1( $\leq$ VIL) to _RESET ( $\geq$ VIH) (fall) setup time	tMDRF		0	-	-	ms
_RESET (fall) to CVDD (fall)	tRCF		0	-	-	ms
CVDD (0V) to REGnVDD, IOVDD (fall)	tCROOF		0	-	-	ms
_RESET ( $\leq$ VIL) (fall) to REGnVDD, IOVDD (fall) hold time	tRROOF		0	-	-	ms

a) In case of BSCAN mode set also the MODE0,1 pins.



**Note** There is no specification for \_RESET rise and fall times.

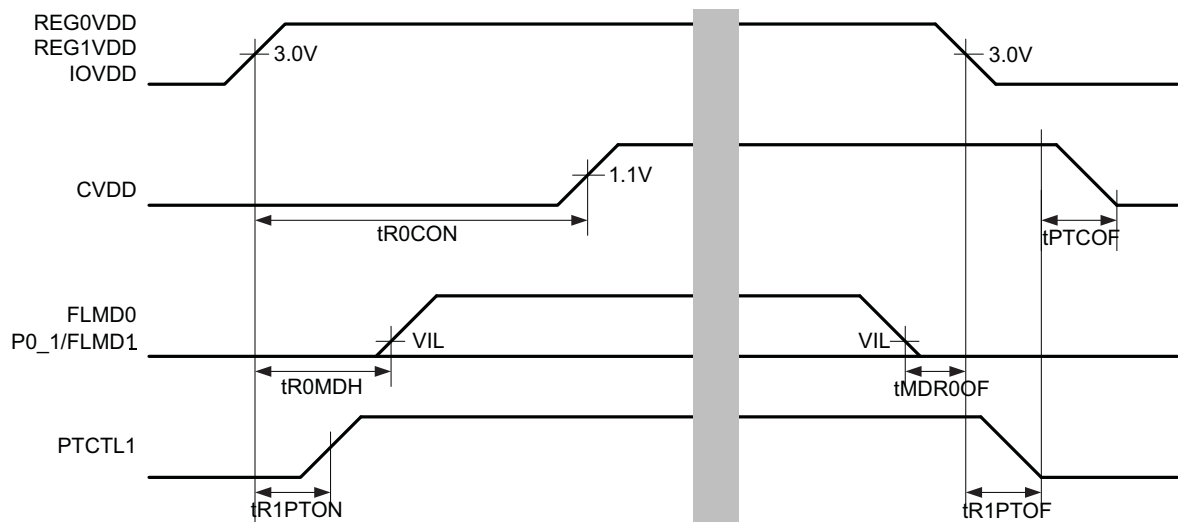


### 3.5.4 Condition 5

M2 products only. RESET is not used; PTCTL1 is used

Normal operating mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to PTCTL1 (rise) setup time	tR1PTON		-	-	1	ms
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (rise) byPTCTL1 (rise)	tR0CON		1	-	10	ms
REG0VDD, REG1VDD, IOVDD (rise) to FLMD0,1(≤VIL) hold time	tR0MDH		2	-	-	ms
FLMD0,1 (≤VIL) to REG0VDD, REG1VDD, IOVDD (fall)	tMDR0OF		0	-	-	ms
REG0VDD, REG1VDD, IOVDD (fall) to PTCTL1 (fall)	tR1PTOF		-	-	1	ms
PTCTL1 (fall) to CVDD (fall)	tPTCOF		0	-	8	ms



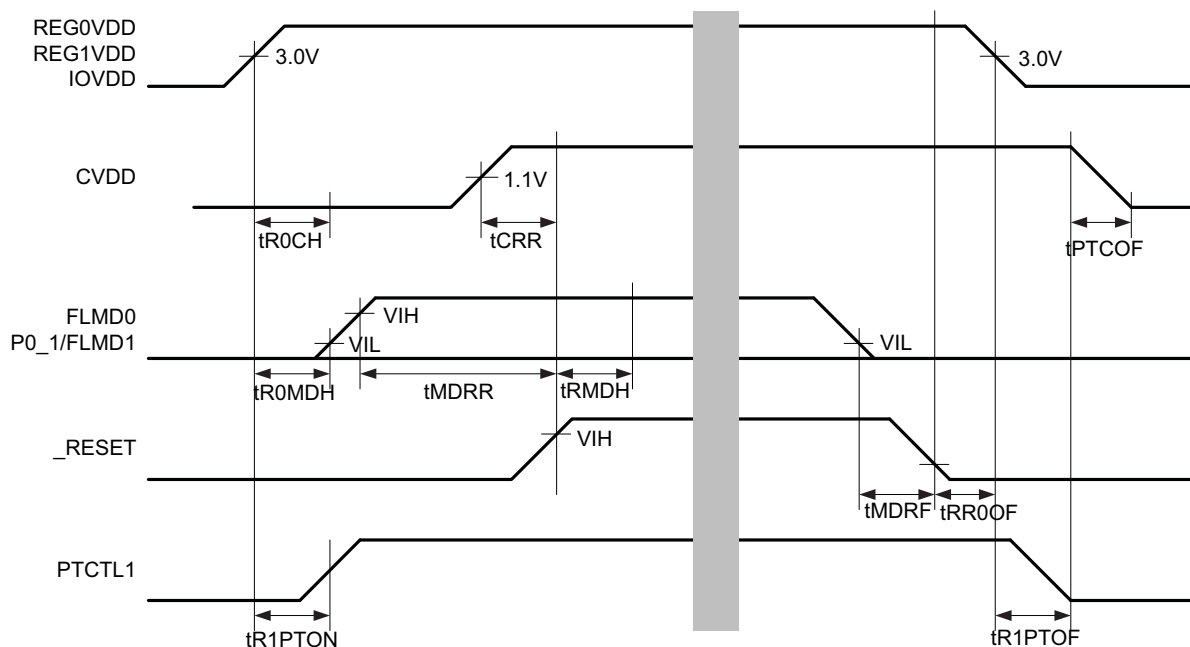
## 3.5.5 Condition 6

M2 products only. RESET is used; PTCTL1 is used

Normal operating mode / Serial programming mode / BSCAN mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
REG0VDD, REG1VDD, IOVDD (rise) to CVDD (0V) hold time	tR0CH		-	-	1	ms
REG1VDD (rise) to PTCTL1 (rise) setup time	tR1PTON		-	-	1	ms
REG0VDD, IOVDD (rise) to FLMD0,1 ( $\leq$ VIL) hold time	tR0MDH		1	-	-	ms
CVDD (rise) to _RESET (rise)	tCRR		0	-	-	ms
FLMD0,1 (VIH or VIL) <sup>a</sup> to _RESET (rise)	tMDRR		1	-	-	ms
_RESET (rise) to FLMD0,1 (VIH or VIL) hold time	tRMDH		1	-	-	ms
FLMD0,1,MODE0,1 ( $\leq$ VIL) <sup>a</sup> to _RESET (fall)	tMDRF		0	-	-	ms
_RESET (fall) to REG0VDD, IOVDD (fall)	tRR0OF		0	-	-	ms
REG1VDD (fall) to PTCTL1 (fall)	tR1PTOF		-	-	1	ms
PTCTL1 (fall) to CVDD (fall)	tPTCOF		0	-	8	ms

a) In case of BSCAN mode set also the MODE0,1 pins.



**Note** There is no specification for \_RESET rise and fall times.

## Chapter 4 Clock generators

### 4.1 CPU clock

Table 4-1 CPU clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
CPU clock frequency	fCPU	PLL based	-	-	80	MHz
		SSCG based	-	-	88.32	MHz

### 4.2 Peripheral clock

Table 4-2 Peripheral clock frequency

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Peripheral clock frequency	fPERI		-	-	48 <sup>a</sup>	MHz

a) Some peripherals can be operated at 80MHz. Refer to the chapter 'Clock Selection' in the UM for details.

### 4.3 Oscillator characteristics

#### 4.3.1 Main oscillator

A ceramic or crystal resonator can be connected to the main clock input pins as shown in figure 4-1 "Recommended Main Oscillator Circuit"

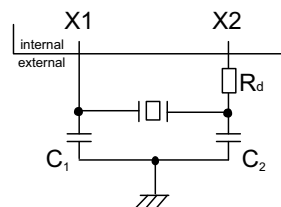


Figure 4-1 Recommended Main Oscillator Circuit

**Caution** Values of  $C_1$ ,  $C_2$  and  $R_d$  and the best setting for MOSCC.AMPSEL[1:0] register depend on the used ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

The main oscillator amplifier gain for the external resonator can be selected by MOSCC.MOSCCAMPSEL[1:0]. Thereby it can be adjusted to support a wide range of frequencies to cope with different external resonators and their external circuitry.

As an example a typical setting for quartz crystals is shown in Table 4-3 “Typical setting of MOSCC.AMPSEL[1:0] for different quartz crystals frequencies”.

**Note** For details to the setting of MOSCC.MOSCCAMPSEL[1:0] please refer to the user manual.

**Table 4-3** Typical setting of MOSCC.AMPSEL[1:0] for different quartz crystals frequencies

MOSCC.AMPSEL[1:0]	Amplification gain	Typical condition for quartz crystals
00	high	$16 < f_{\text{MOSC}} \leq 20 \text{ MHz}$
01	medium	$8 < f_{\text{MOSC}} \leq 16 \text{ MHz}$
10	low	$4 < f_{\text{MOSC}} \leq 8 \text{ MHz}$
11	very low	4 MHz

#### (1) Main oscillator characteristics

**Table 4-4** Main oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MainOSC frequency	$f_{\text{MOSC}}$		4	-	20	MHz

- Cautions**
1. External clock input is prohibited.
  2. General guidance for PCB layout:
    - Keep the wiring length as short as possible.
    - Do not cross the wiring with other signal lines.
    - Do not route this circuit close to a signal line with high fluctuating current flow.
    - Always make the ground point of the oscillator capacitor the same potential as REG0VSS and OSCVSS.
    - Do not ground the capacitor to a ground pattern with high current flow.
    - Do not tap signals from the oscillator.

#### 4.3.2 Sub-oscillator

A crystal resonator can be connected to the sub clock input pins as shown in figure 4-2 “Recommended Sub Oscillator Circuit”

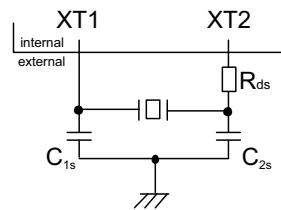


Figure 4-2 Recommended Sub Oscillator Circuit

**Caution** Values of  $C_{1s}$ ,  $C_{2s}$  and  $R_{ds}$  depend on the used crystal and must be specified in cooperation with crystal manufacturer.

### (1) Sub-oscillator characteristics

Table 4-5 Sub-oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MainOSC frequency	fSOSC		-	32.768	-	kHz

### 4.3.3 Internal oscillator

Table 4-6 Internal oscillator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Lowspeed OSC frequency	fRL	<ul style="list-style-type: none"> <li>Other than DeepStop mode</li> <li>DeepStop mode with PSC0.REGSTP = 0</li> </ul>	220.8	240	259.2	kHz
	fRLLP	<ul style="list-style-type: none"> <li>DeepStop mode with PSC0.REGSTP = 1</li> </ul>	216	240	264	kHz
Highspeed OSC frequency	fRH	<ul style="list-style-type: none"> <li>Other than DeepStop mode</li> <li>DeepStop mode with PSC0.REGSTP = 0</li> </ul>	7.2	8.0	8.8	MHz
	fRHLP	<ul style="list-style-type: none"> <li>DeepStop mode with PSC0.REGSTP = 1</li> </ul>	6.64	8.0	8.8	MHz
Highspeed OSC stabilization time	TRHSTB		-	-	19	μs

## 4.4 PLL Characteristics

Table 4-7 PLL characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Input frequency	fxn	PLL mode and SSCG mode	4	-	20	MHz
Output frequency	fxxn	PLL mode	25	-	80	MHz
		SSCG mode	22.40	-	88.32	MHz
Lock time	TLCKPn	PLL mode	-	-	650	μs
	TLCKSn	SSCG mode	-	-	1300	μs
Period jitter <sup>a</sup>	tPJn	Peak to peak, fixed frequency mode, Pr=2	-150	-	150	ps
Long term jitter <sup>a</sup>	tLTJn	PLL mode, Peak to peak, term=1μs f <sub>VCOOUT</sub> =160MHz (Pr=2)	-1.275	-	1.275	ns

<sup>a)</sup> Not tested in production. Specified by design.

## Chapter 5 Supply current specification

### 5.1 Supply current for $\mu$ PDF70F4011 / $\mu$ PDF70F4012

Item	Power <sup>a</sup>		Condition <sup>b</sup>						Specification				Unit
	ISO0	ISO1	8MHz intOSC	Main OSC	Sub OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	
RUN mode	ON	ON	ON	ON	ON	ON	80	WORKING	-	144	184	186	mA
	ON	ON	ON	ON	ON	ON	80	STOPPED	-	76	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING	-	28	47	48	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
	ON	OFF	ON	ON	ON	ON	80	WORKING	-	104	138	139	mA
	ON	OFF	ON	ON	ON	ON	80	STOPPED	-	74	-	-	mA
	ON	OFF	ON	OFF	ON	OFF	8	WORKING	-	22	40	41	mA
	ON	OFF	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
HALT mode	ON	ON	ON	ON	ON	ON	80	WORKING	-	137	178	180	mA
	ON	ON	ON	ON	ON	ON	80	STOPPED	-	74	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING	-	27	47	47	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
STOP mode	ON	ON	OFF	OFF	OFF	OFF	-	STOPPED	-	0.7	19	20	mA
	ON	OFF	OFF	OFF	OFF	OFF	-	STOPPED	-	0.6	19	19	mA
DEEPSTOP mode	OFF	OFF	OFF	OFF	OFF	OFF	-	STOPPED	-	0.06	0.86	0.88	mA
	OFF	OFF	ON	OFF	OFF	OFF	-	STOPPED	-	0.60	2.1	2.3	mA
	OFF	OFF	ON	OFF	ON	OFF	-	STOPPED	-	0.60	2.1	2.3	mA

a) The AWO is always ON.

b) The 240kHz IntOSC is always ON.

- Notes**
1. The above currents do not include port buffer currents or ADC currents.
  2. The currents in run mode include currents for self-programming and EEPROM emulation.
  3. The current of FlexRay is not included in case of CPU frequency = 8MHz.
  4. The 'typical' specification is for reference only and not a guaranteed value. The 'typical' specification is applicable under the following conditions:
    - Ta = 25°C
    - REGnVDD=FVDD=OSCVDD=EmVDD=B0VDD=AmVDD=AmVREFP=5.0V (n=0-3, m=0-1).
    - M2 products: CVDD = 1.2V
    - REGnVSS=OSCVSS=EmVSS=B0VSS=AmVSS=AmVREFM=0V (n=0-3, m=0-1)

## 5.2 Supply current for $\mu$ PDF70F3559 / $\mu$ PDF70F3560

Item	Power <sup>a</sup>		Condition <sup>b</sup>						Specification				Unit
	ISO0	ISO1	8MHz intOSC	Main OSC	Sub OSC	PLL	CPU Freq	Peripherals	Min.	Typ.	(A)	(A1)	
RUN mode	ON	ON	ON	ON	ON	ON	80	WORKING	-	126	164	165	mA
	ON	ON	ON	ON	ON	ON	80	STOPPED	-	73	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING	-	28	47	48	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
	ON	OFF	ON	ON	ON	ON	80	WORKING	-	94	126	127	mA
	ON	OFF	ON	ON	ON	ON	80	STOPPED	-	72	-	-	mA
	ON	OFF	ON	OFF	ON	OFF	8	WORKING	-	22	40	41	mA
	ON	OFF	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
HALT mode	ON	ON	ON	ON	ON	ON	80	WORKING	-	118	155	156	mA
	ON	ON	ON	ON	ON	ON	80	STOPPED	-	71	-	-	mA
	ON	ON	ON	OFF	ON	OFF	8	WORKING	-	27	47	47	mA
	ON	ON	ON	OFF	ON	OFF	8	STOPPED	-	19	-	-	mA
STOP mode	ON	ON	OFF	OFF	OFF	OFF	-	STOPPED	-	0.7	19	20	mA
	ON	OFF	OFF	OFF	OFF	OFF	-	STOPPED	-	0.6	19	19	mA
DEEPSTOP mode	OFF	OFF	OFF	OFF	OFF	OFF	-	STOPPED	-	0.06	0.86	0.88	mA
	OFF	OFF	ON	OFF	OFF	OFF	-	STOPPED	-	0.60	2.1	2.3	mA
	OFF	OFF	ON	OFF	ON	OFF	-	STOPPED	-	0.60	2.1	2.3	mA

a) The AWO is always ON.

b) The 240kHz IntOSC is always ON.

- Notes**
1. The above currents do not include port buffer currents or ADC currents.
  2. The currents in run mode include currents for self-programming and EEPROM emulation.
  3. The 'typical' specification is for reference only and not a guaranteed value. The 'typical' specification is applicable under the following conditions:
    - Ta = 25°C
    - REGnVDD=FVDD=OSCVDD=EmVDD=B0VDD=AmVDD=AmVREFP=5.0V (n=0-3, m=0-1).
    - M2 products: CVDD = 1.2V

REGnVSS=OSCVSS=EmVSS=B0VSS=AmVSS=AmVREFM=0V  
(n=0-3, m=0-1)

## 5.3 Voltage Comparator characteristics

Table 5-1 VCMP characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VCMP current	IVCMP		-	200	300	$\mu$ A



## Chapter 6 I/O specification

### 6.1 Port Characteristics

#### 6.1.1 Condition settings

Some of the conditions mentioned in this chapter can be selected by software. The related register settings are described below:

##### (1) Input characteristic

The input characteristics can be selected by the registers PIS and PISE with the following coding:

Table 6-1 Input characteristic selection

PISE	PIS	Reference in UserManual	Electrical characteristic
0	0	Type 1	CMOS <sup>a)</sup>
0	1	Type 2	Schmitt2
1	0	Type 3	Schmitt1
1	1	Type 4	Schmitt4

<sup>a)</sup> Default setting after reset

## 6.1.2 PgE0

Table 6-2 PgE0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	$0.7 \cdot E0VDD$	-	$E0VDD+0.3$	V
		Schmitt1	$0.7 \cdot E0VDD$	-	$E0VDD+0.3$	
		Schmitt2	$0.8 \cdot E0VDD$	-	$E0VDD+0.3$	
		Schmitt4 ( $E0VDD=VPOC \sim 3.0$ )	$0.84 \cdot E0VDD$	-	$E0VDD+0.3$	
		Schmitt4 ( $E0VDD=3.0 \sim 5.5$ )	$0.8 \cdot E0VDD$	-	$E0VDD+0.3$	
Low level input voltage	VIL	CMOS	-0.5	-	$0.3 \cdot E0VDD$	V
		Schmitt1	-0.5	-	$0.3 \cdot E0VDD$	
		Schmitt2	-0.5	-	$0.2 \cdot E0VDD$	
		Schmitt4 ( $E0VDD=VPOC \sim 3.0$ )	-0.5	-	$0.4 \cdot E0VDD$	
		Schmitt4 ( $E0VDD=3.0 \sim 5.5$ )	-0.5	-	$0.5 \cdot E0VDD$	
High level output voltage	VOH	IOH = -5mA	$E0VDD-1.0$	-		V
		IOH = -100 $\mu$ A	$E0VDD-0.5$	-		
Low level output voltage	VOL	IOL = 5mA	-	-	0.4	V
		IOL = 100 $\mu$ A	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-		V
		Schmitt2	0.3	-		
		Schmitt4	0.1	-		
Internal pull-up resistor	RU		20	40	100	k $\Omega$
Internal pull-down resistor	RD		20	40	100	k $\Omega$
High level port output current	IOH	Power supply of PgE0	-	-	-20	mA
Low level port output current	IOL	Power supply of PgE0	-	-	20	mA
High level input leakage current	ILIH	VI = E0VDD	-	-	0.5	$\mu$ A
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	$\mu$ A
High level output leakage current	ILOH	VO = E0VDD	-	-	0.5	$\mu$ A
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	$\mu$ A
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	

## 6.1.3 PgE1

Table 6-3 PgE1 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·E1VDD	-	E1VDD+0.3	V
		Schmitt1	0.7·E1VDD	-	E1VDD+0.3	
		Schmitt2	0.8·E1VDD	-	E1VDD+0.3	
		Schmitt4 (E1VDD=VPOC~3.0)	0.84·E1VDD	-	E1VDD+0.3	
		Schmitt4 (E1VDD=3.0~5.5)	0.8·E1VDD	-	E1VDD+0.3	
Low level input voltage	VIL	CMOS	-0.5	-	0.3·E1VDD	V
		Schmitt1	-0.5	-	0.3·E1VDD	
		Schmitt2	-0.5	-	0.2·E1VDD	
		Schmitt4 (E1VDD=VPOC~3.0)	-0.5	-	0.4·E1VDD	
		Schmitt4 (E1VDD=3.0~5.5)	-0.5	-	0.5·E1VDD	
High level output voltage	VOH	IOH = -5mA <sup>a</sup>	E1VDD-1.0	-		V
		IOH = -100μA	E1VDD-0.5	-		
Low level output voltage	VOL	IOL = 5mA <sup>a</sup>	-	-	0.4	V
		IOL = 100μA	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-		V
		Schmitt2	0.3	-		
		Schmitt4	0.1	-		
Internal pull-up resistor	RU		20	40	100	kΩ
Internal pull-down resistor	RD		20	40	100	kΩ
High level port output current	IOH	Power supply of PgE1	-	-	-150	mA
Low level port output current	IOL	Power supply of PgE1	-	-	150	mA
High level input leakage current	ILIH	VI = E1VDD	-	-	0.5	μA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	μA
High level output leakage current	ILOH	VO = E1VDD	-	-	0.5	μA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	μA
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns

a) The maximum number of PgE1 pins with 'ON' signal at the same time is 5 in 'Slow mode'.  
The maximum number of PgE1 pins with 'ON' signal at the same time is 8 in 'Fast mode'.  
See the UM for the related description of the Port drive strength control.

## 6.1.4 PgB0

Table 6-4 PgB0 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	0.7·B0VDD	-	B0VDD+0.3	V
		Schmitt1	0.7·B0VDD	-	B0VDD+0.3	
		Schmitt2	0.8·B0VDD	-	B0VDD+0.3	
		Schmitt4 (B0VDD=VPOC~3.0)	0.84·B0VDD	-	B0VDD+0.3	
		Schmitt4 (B0VDD=3.0~5.5)	0.8·B0VDD	-	B0VDD+0.3	
Low level input voltage	VIL	CMOS	-0.5	-	0.3·B0VDD	V
		Schmitt1	-0.5	-	0.3·B0VDD	
		Schmitt2	-0.5	-	0.2·B0VDD	
		Schmitt4 (B0VDD=VPOC~3.0)	-0.5	-	0.4·B0VDD	
		Schmitt4 (B0VDD=3.0~5.5)	-0.5	-	0.5·B0VDD	
High level output voltage	VOH	IOH = -5mA <sup>a</sup>	B0VDD-1.0	-	-	V
		IOH = -100μA	B0VDD-0.5	-	-	
Low level output voltage	VOL	IOL = 5mA <sup>a</sup>	-	-	0.4	V
		IOL = 100μA	-	-	0.4	
Input hysteresis of Schmit	VH	Schmitt1	0.3	-	-	V
		Schmitt2	0.3	-	-	
		Schmitt4	0.1	-	-	
Internal pull-up resistor	RU		20	40	100	kΩ
Internal pull-down resistor	RD		20	40	100	kΩ
High level port output current	IOH	Power supply of PgB0	-	-	-150	mA
Low level port output current	IOL	Power supply of PgB0	-	-	150	mA
High level input leakage current	ILIH	VI = B0VDD	-	-	0.5	μA
Low level input leakage current	ILIL	VI = 0V	-	-	-0.5	μA
High level output leakage current	ILOH	VO = B0VDD	-	-	0.5	μA
Low level output leakage current	ILOL	VO = 0V	-	-	-0.5	μA
Output frequency	fO	Slow mode	-	-	25	MHz
		Fast mode	-	-	40	
Rise time (output)	tKRP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns
Fall time (output)	tKFP	Slow mode	-	-	15	ns
		Fast mode	-	-	8	ns

a) The maximum number of PgB0 pins with 'ON' signal at the same time is 5 in 'Slow mode' (Except the pins related to the external memory interface (MEMC)).  
The maximum number of PgB0 pins with 'ON' signal at the same time is 8 in 'Fast mode'.  
See the UM for the related description of the Port drive strength control.

### 6.1.5 PgA0 and PgA1

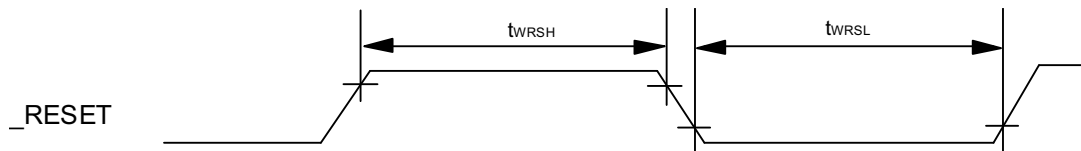
Table 6-5 PgA0 and PGA1 characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
High level input voltage	VIH	CMOS	$0.7 \cdot \text{AnVDD}$	-	$\text{AnVDD} + 0.3$	V
Low level input voltage	VIL	CMOS	-0.5	-	$0.3 \cdot \text{AnVDD}$	V
High level output voltage	VOH	IOH = -1mA	$\text{AnVDD} - 1.0$	-	-	V
		IOH = -100 $\mu$ A	$\text{AnVDD} - 0.5$	-	-	
Low level output voltage	VOL	IOL = 1mA	-	-	0.4	V
		IOL = 100 $\mu$ A	-	-	0.4	
High level port output current	IOH	Power supply of PgA0 and PgA1	-	-	-20	mA
Low level port output current	IOL	Power supply of PgA0 and PgA1	-	-	20	mA
High level input leakage current	ILIH	VI = AnVDD	-	-	0.2	$\mu$ A
Low level input leakage current	ILIL	VI = 0V	-	-	-0.2	$\mu$ A
High level output leakage current	ILOH	VO = AnVDD	-	-	0.2	$\mu$ A
Low level output leakage current	ILOL	VO = 0V	-	-	-0.2	$\mu$ A
Output frequency	fO		-	-	25	MHz
Rise time (output)	tKRP		-	-	15	ns
Fall time (output)	tKFP		-	-	15	ns

## Chapter 7 Peripherals specification

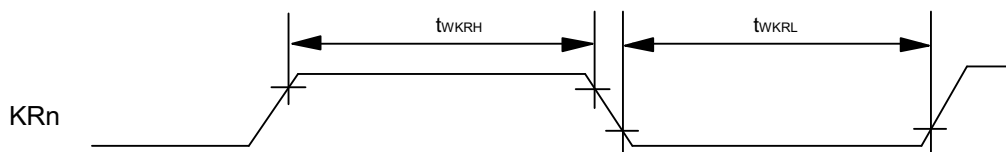
### 7.1 Reset timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
RESET input High level width	tWRSH	Highspeed OSC is operating	450	-	-	ns
		Highspeed OSC is stopped	4.7	-	-	μs
RESET input Low level width	tWRSL	Highspeed OSC is operating	450	-	-	ns
		Highspeed OSC is stopped	4.7	-	-	μs



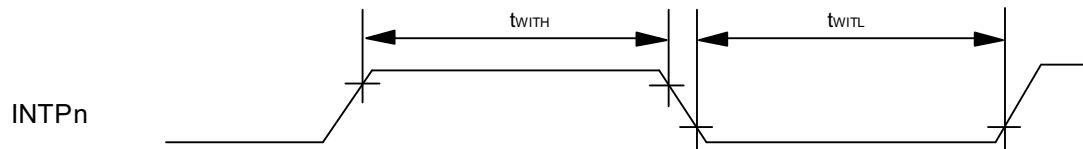
### 7.2 NMI timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
NMI input High level width	tWNIH		300	-	-	ns
NMI input Low level width	tWNIL		300	-	-	ns



### 7.3 INTP timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
INTPn input High level width	t <sub>WITH</sub>		300	-	-	ns
INTPn input Low level width	t <sub>WITL</sub>		300	-	-	ns



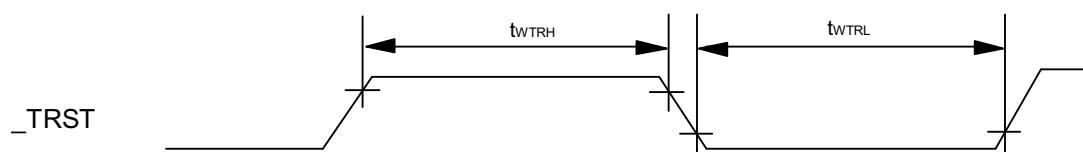
### 7.4 FLMD0 timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 input High level width	t <sub>WMDH</sub>		300	-	-	ns
FLMD0 input Low level width	t <sub>WMDL</sub>		300	-	-	ns
FLMD0 external pull down resistor	R <sub>FLMD0</sub>		82	-	-	kΩ



### 7.5 \_DCUTRST timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
_DCUTRST input High level width	t <sub>WRH</sub>		450	-	-	ns
_DCUTRST input Low level width	t <sub>WTRL</sub>		450	-	-	ns



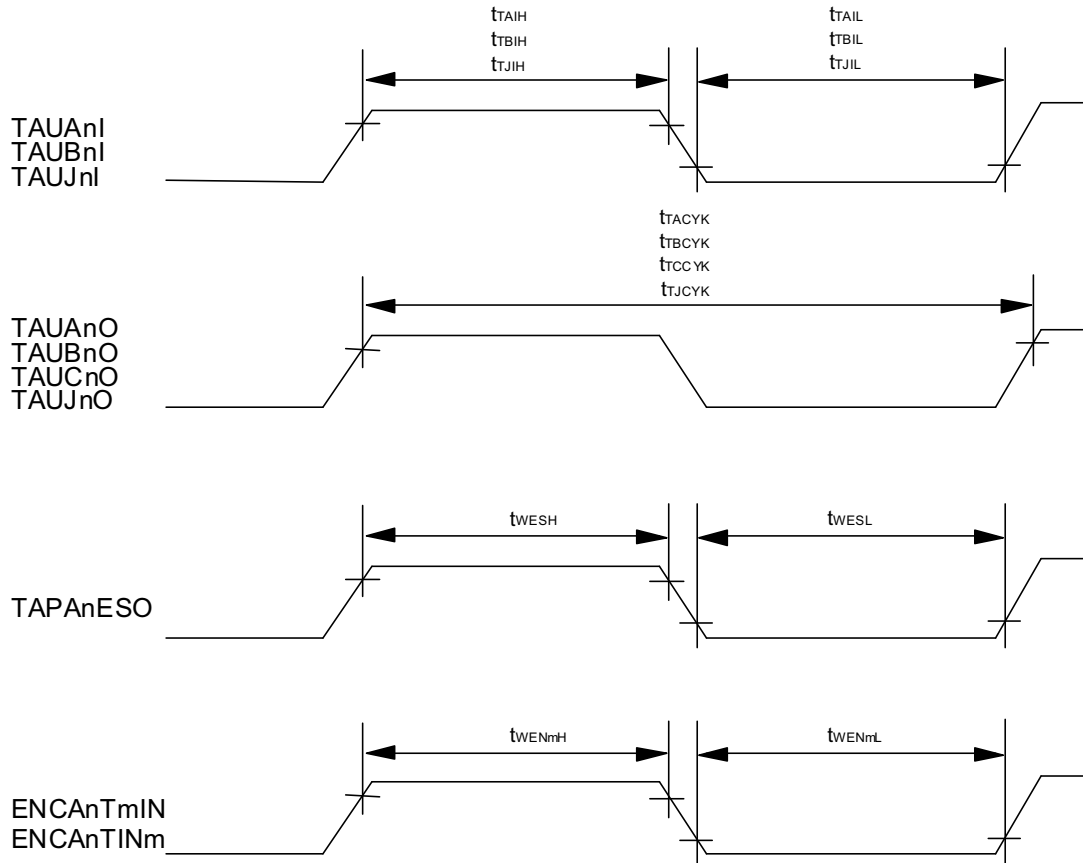
## 7.6 Timer timing

Table 7-1 Timer timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
TAUAnI input High level width	tTAIH	n=0	a,b	-	-	ns
TAUAnI input Low level width	tTAIL	n=0	a,b	-	-	ns
TAUBnI input High level width	tTBIH	n=1	a,b	-	-	ns
TAUBnI input Low level width	tTBIL	n=0	a,b	-	-	ns
TAUJnI input High level width	tTJIH	n=0,1	300	-	-	ns
TAUJnI input High level width	tTJIH		4.7	-	-	μs
TAUJnI input High level width	tTJIH		b	-	-	ns
TAUJnI input Low level width	tTJIL	n=0,1	300	-	-	ns
TAUJnI input Low level width	tTJIL		4.7	-	-	μs
TAUJnI input Low level width	tTJIL		b	-	-	ns
TAUAnO output cycle	tTACYK	n=0	-	-	20	MHz
TAUBnO output cycle	tTBCYK	n=1	-	-	20	MHz
TAUCnO output cycle	tTCCYK	n=2-7	-	-	20	MHz
TAUJnO output cycle	tTJCYK	n=0,1	-	-	20	MHz
TAPAnESO input High level width	tWESH	n=0	300	-	-	ns
TAPAnESO input Low level width	tWESL	n=0	300	-	-	ns
ENCAnTmIN high level width	tWENmH	n=0, m=A,B,Z	a,b	-	-	ns
ENCAnTmIN low level width	tWENmL	n=0, m=A,B,Z	a,b	-	-	ns
ENCAnTINm high level width	tWENmH	n=0, m=0-1	a,b	-	-	ns
ENCAnTINm low level width	tWENmL	n=0, m=0-1	a,b	-	-	ns

- a) With digital noise filter enabled:  $2, 3, 4$  or  $5 \times T_{\text{samp}} + 20$  ( $T_{\text{samp}}$  shows sampling period specified in Noise filter macro. More than 1 PCLK width of Timer macro must be kept regarding DNF pass through pulse width.)
- b) With digital noise filter disabled:  $1 \times t_{\text{SYNC}} + 20$  ( $t_{\text{SYNC}}$ : 1 PCLK of Timer macro)

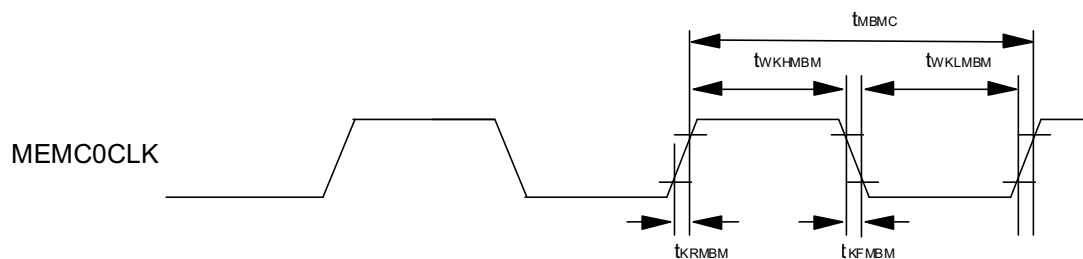




### 7.7 Multiplexed bus timing

Table 7-2 MEMC0CLK timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
MEMC0CLK output cycle	tMEMC		25	-	-	ns
MEMC0CLK high level width	tWKHMEM		tMEMC / 2 - 10	-	-	ns
MEMC0CLK low level width	tWKLMEM		tMEMC / 2 - 10	-	-	ns
MEMC0CLK rise time	tKRMEM		-	-	10	ns
MEMC0CLK fall time	tKFMEM		-	-	10	ns

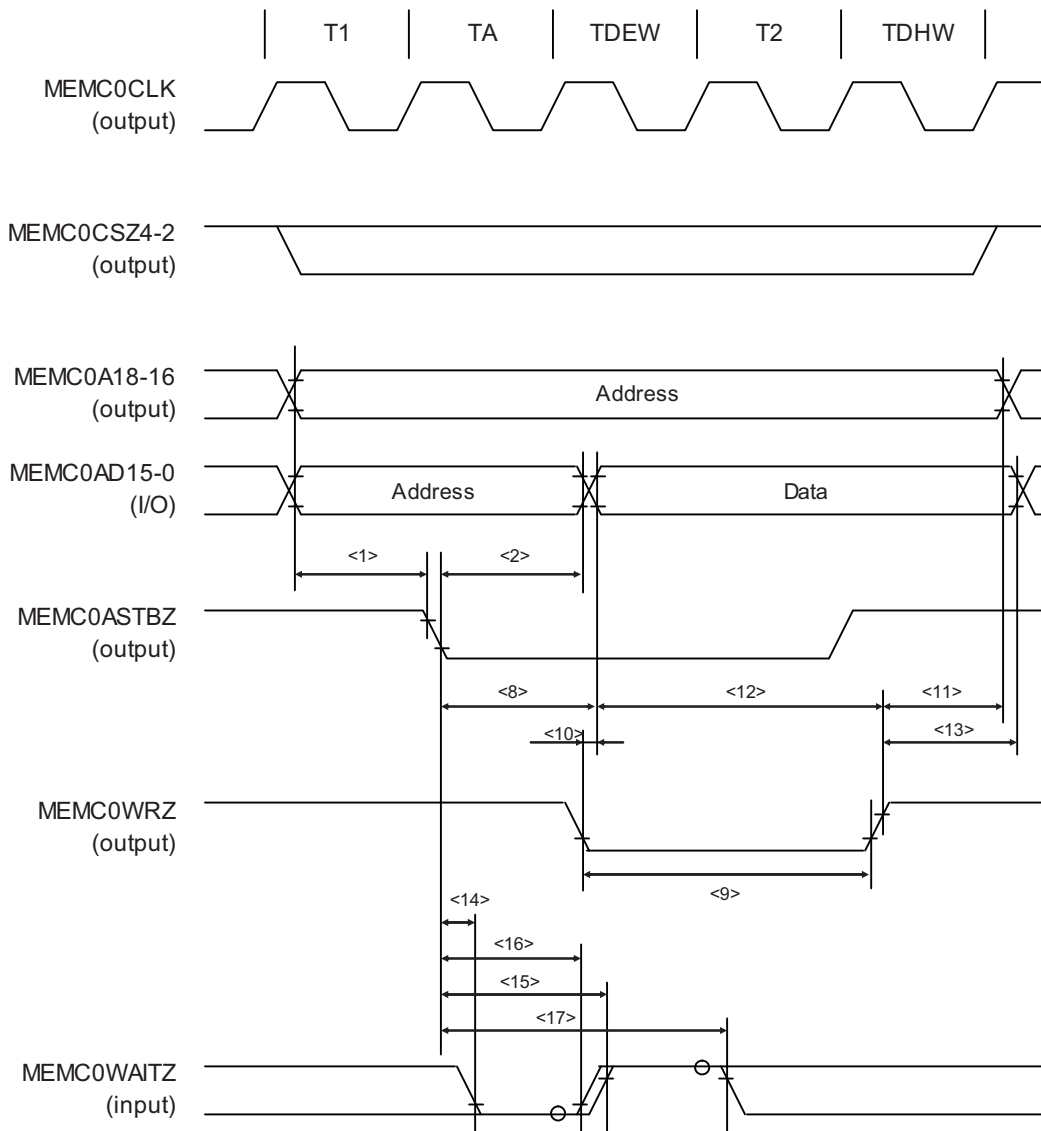


## 7.7.1 MEMC0CLK asynchronous timing

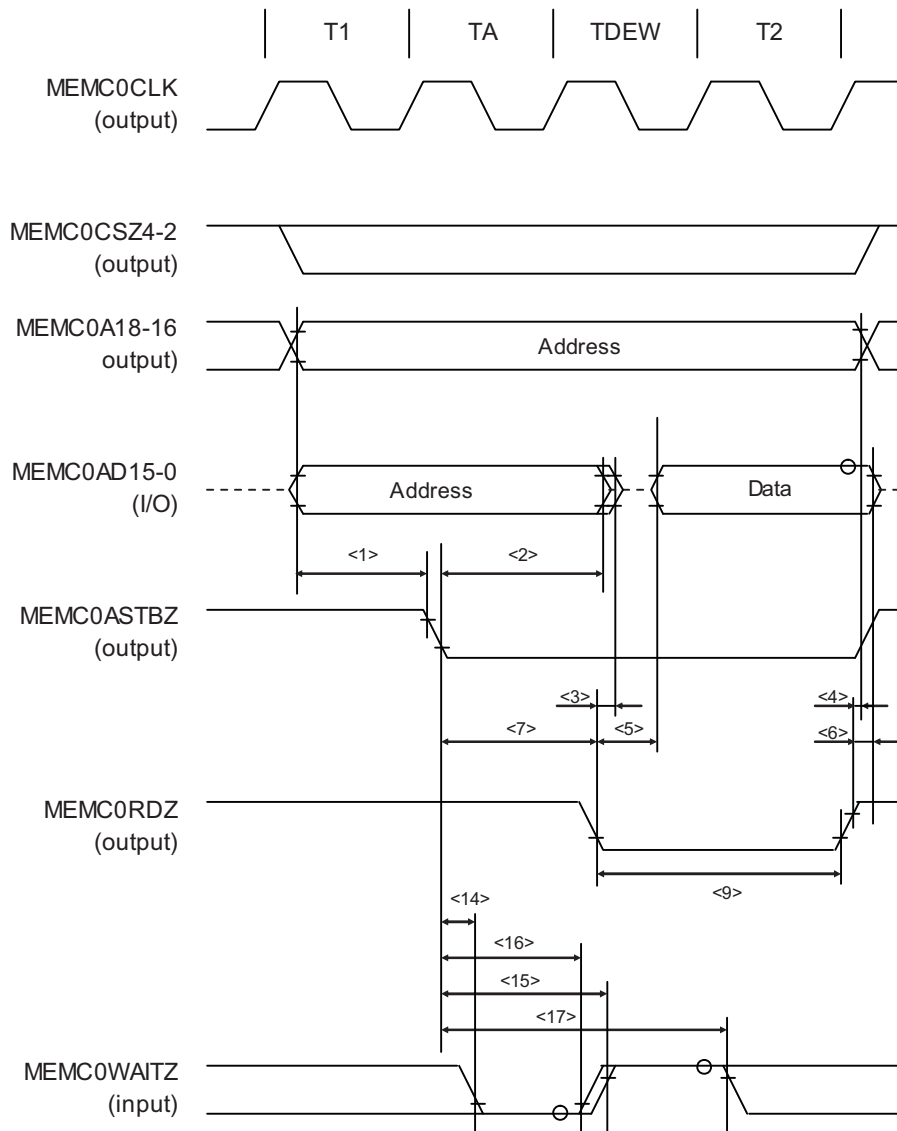
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Bus operational period	T	-	25	-	-	ns
Address setup time to MEMC0ASTBZ (f)	tSAST	<1>	$(1+ASW) \cdot T-15$	-	-	ns
Address hold time from MEMC0ASTBZ (f)	tHSTA	<2>	$(1+AHW) \cdot T-15$	-	-	ns
Address float delay time from MEMC0RDZ (f)	tFRDA	<3>	-	-	6	ns
Address hold time from MEMC0RDZ (r)	tHRDA	<4>	0	-	-	ns
Data input delay time from MEMC0RDZ (f)	tDRDID	<5>	6	-	$(1+w) \cdot T-35$	ns
Data input hold time from MEMC0RDZ (r)	tHRDID	<6>	0	-	-	ns
Delay time from ASTB(f) to MEMC0RDZ (f)	tDSTRD	<7>	$(1+AHW) \cdot T-15$	-	-	ns
Delay time from ASTB(f) to MEMC0WRZ (f)	tDSTWR	<8>	$(1+AHW) \cdot T-15$	-	-	ns
MEMC0RDZ, MEMC0WRZ low level width	tWRDST	<9>	$(1+w) \cdot T-10$	-	-	ns
Data output delay time from MEMC0WRZ (f)	tDWROD	<10>	-	-	10	ns
Address hold time from MEMC0WRZ (r)	tHWRA	<11>	T-15	-	-	ns
Data output setup time to MEMC0WRZ (r)	tSODWR	<12>	$(1+w) \cdot T-15$	-	-	ns
Data output hold time from MEMC0WRZ (r)	tHWROD	<13>	T-15	-	-	ns
MEMC0WAITZ setting delay from MEMC0ASTBZ (f)	tSSTWT1	<14>	-	-	$(1+AHW) \cdot T - (2 \cdot \text{HEAPCLK} + 35)$	ns
MEMC0WAITZ hold time from MEMC0ASTBZ (f)	tSSTWT2	<15> $w \geq 1$	-	-	$(1+w+AHW) \cdot T - (2 \cdot \text{HEAPCLK} + 35)$	ns
MEMC0WAITZ setting delay from Address	tHSTWT1	<16> $w \geq 1$	$(w+AHW) \cdot T - (2 \cdot \text{HEAPCLK} + 20)$	-	-	ns
MEMC0WAITZ hold time from Address	tHSTWT2	<17> $w \geq 1$	$(1+w+AHW) \cdot T - 2 \cdot \text{HEAPCLK} + 20$	-	-	ns

- Notes**
1. ASW: Number of Address Setup Wait for multiplex bus
  2. AHW: Number of Address Hold Wait for multiplex bus
  3. w: Number of data wait
  4. In case the bus operational period (T) is shorter than 41ns, tDRDID requires at least 1 data wait ( $w=1$ ).

(1) Multiplex write cycle (Asynchronous; 1 data wait)



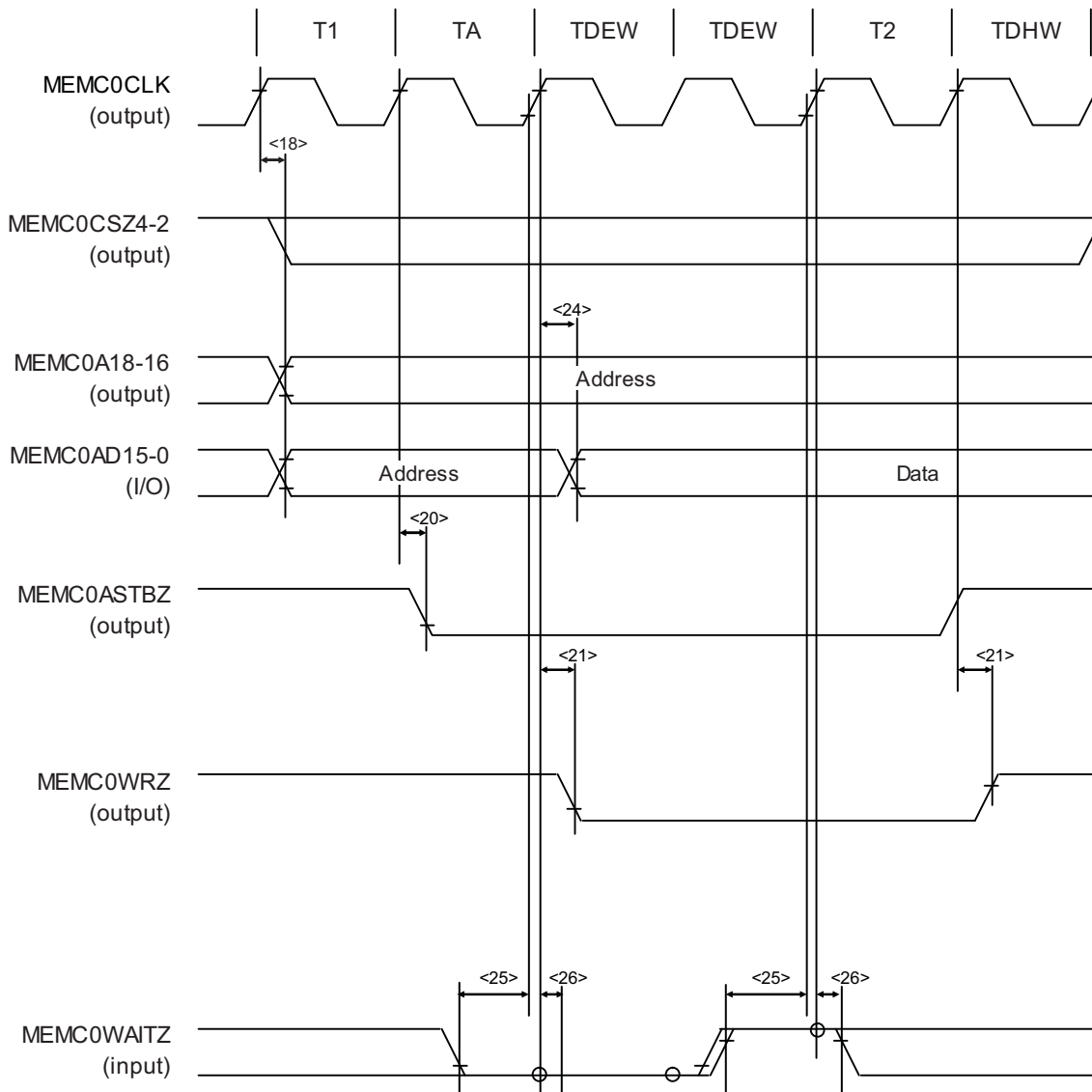
(2) Multiplex read cycle (Asynchronous; 1 data wait)



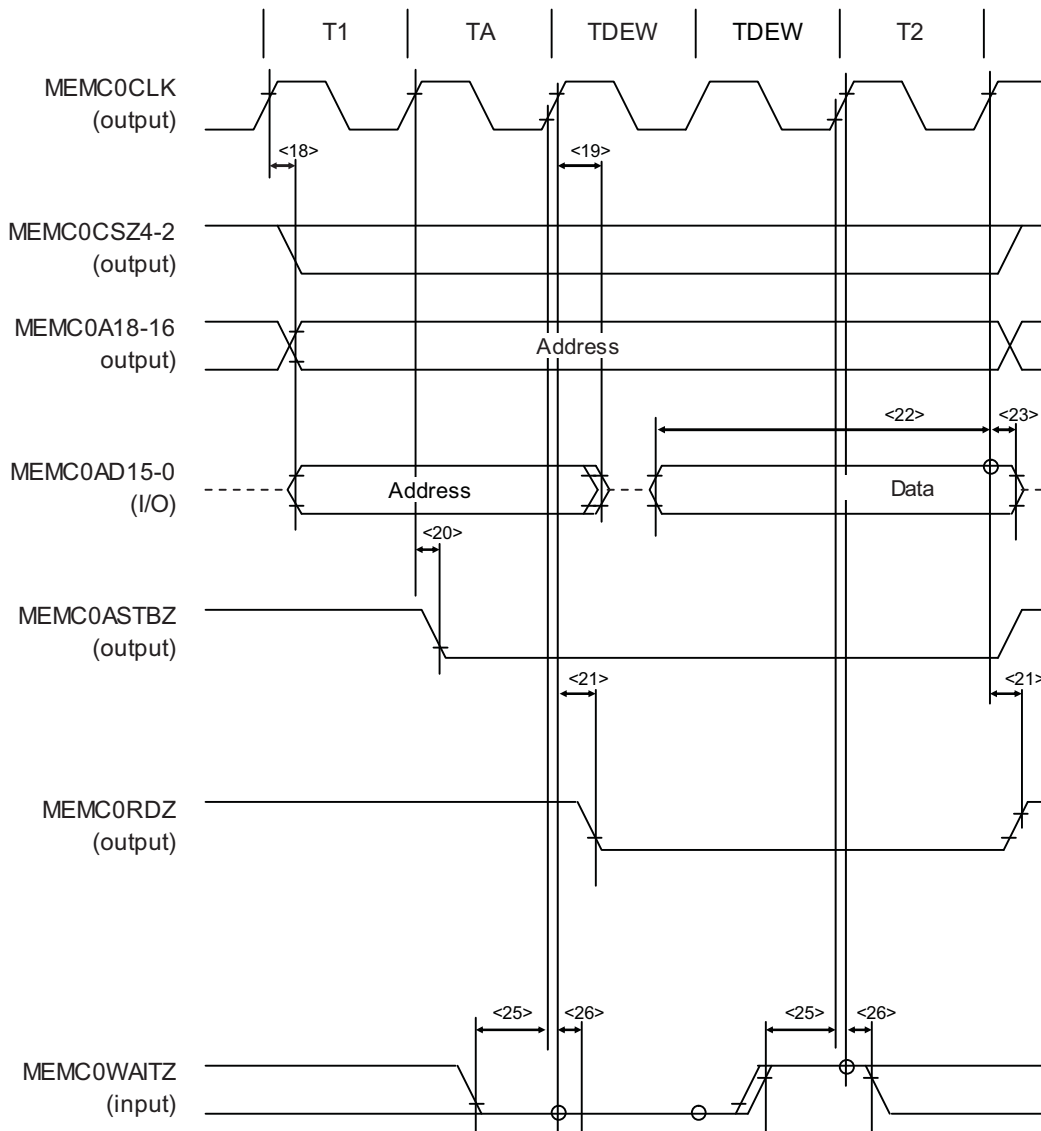
## 7.7.2 MEMC0CLK synchronous timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Bus operational period	T		25	-	-	ns
Delay time from MEMC0CLK (r) to address	tDKA	<18>	0	-	12	ns
Delay time from MEMC0CLK (r) to address float	tFKA	<19>	0	-	12	ns
Delay time from MEMC0CLK (r) to ASTB (f)	tDKST	<20>	0	-	11	ns
Delay time from MEMC0CLK (r) to MEMC0RDZ and MEMC0WRZ	tDKRDWR	<21>	-2.5	-	6	ns
Data input setup time (from MEMC0CLK (r))	tSIDK	<22>	10	-	-	ns
Data input hold time (from MEMC0CLK (r))	tHKID	<23>	2.5	-	-	ns
Data output delay time (from MEMC0CLK (r))	tDKOD	<24>	-	-	11	ns
MEMC0WAITZ setup time (to MEMC0CLK (r))	tSWTK	<25> B0VDD $\geq$ 3.5V	23	-	-	ns
		<25> B0VDD<3.5V	27	-	-	ns
MEMC0WAITZ hold time (from MEMC0CLK (r))	tHKWT	<26>	2.5	-	-	ns

(1) Multiplex write cycle (Synchronous; 1 data wait)



(2) Multiplex read cycle (Synchronous; 1 data wait)



## 7.8 CSI timing

### 7.8.1 Master modes

#### (1) CSIG timing

Table 7-3 CSIG timing (Master mode)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		20.8	-	-	ns
CSIGnSC cycle time	tKCYMGn		100	-	-	ns
CSIGnSC high level width	tKWHMGn		$0.5 \cdot tKCYMGn - 10$	-	-	ns
CSIGnSC low level width	tKWLMGn		$0.5 \cdot tKCYMGn - 10$	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSIMGn	CSIGnSC@PDSC=1	30	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSIMGn	CSIGnSC@PDSC=0	38	-	-	ns
CSIGnSI hold time (vs. CSIGnSC)	tHSIMGn		0	-	-	ns
CSIGnSO output delay (vs. CSIGnSC)	tDSOMGn		-	-	7	ns
CSIGnRYI setup time (vs. CSIGnSC)	tSRYIGn	CSIGnCTL1.CSIGnSIT=x CSIGnCTL1.CSIGnHSE=1	$2 \cdot tKCYGn + 25$	-	-	ns
CSIGnRYI High level width	tWRYIGn	CSIGnCTL1.CSIGnHSE=1	$tKCYGn - 5.0$	-	-	ns

**Note** n: Number of macro instances. Refer to the User Manual for the detailed specification.



## (2) CSIH timing master mode

Table 7-4 CSIH timing (Master mode)

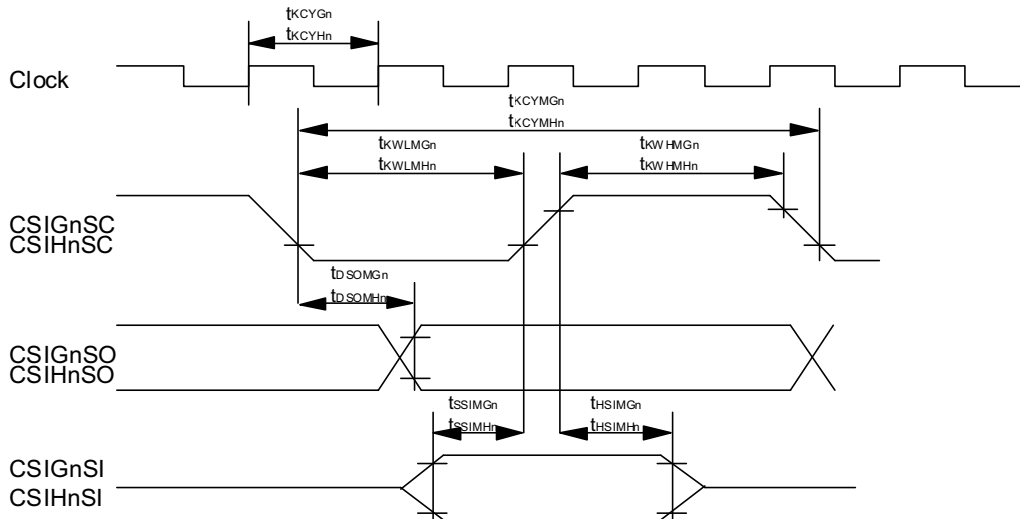
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYHn		20.8	-	-	ns
CSIHnSC cycle time	tKCYMHn		100	-	-	ns
CSIHnSC high level width	tKWHMHn		$0.5 \cdot tKCYMHn - 10$	-	-	ns
CSIHnSC low level width	tKWLMHn		$0.5 \cdot tKCYMHn - 10$	-	-	ns
CSIHnSI setup time (vs. CSIHnSC)	tSSIMHn	CSIHnSC@PDSC=1	30	-	-	ns
		CSIHnSC@PDSC=0	38	-	-	ns
CSIHnSI hold time (vs. CSIHnSC)	tHSIMHn		0	-	-	ns
CSIHnSO output delay (vs. CSIHnSC)	tDSOMHn		-	-	7	ns
CSIHnRYI setup time (vs. CSIHnSC)	tSRYIHn	CSIHnCTL1.CSIHnSIT=x CSIHnCTL1.CSIHnHSE=1	$2 \cdot tKCYHn + 25$	-	-	ns
CSIHnRYI High level width	tWRYIHn	CSIHnCTL1.CSIHnHSE=1	$tKCYHn - 5.0$	-	-	ns
CSIHnCSS0-7 inactive width	tWSCSBHn		$CSIDLE \times tKCYMHn - 5.0$	-	-	ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	tSSCSBHn0	CSIHnCTL1.CSIHnDAP=0	$CSSETUP \times tKCYMHn - 5.0$	-	-	ns
	tSSCSBHn1	CSIHnCTL1.CSIHnDAP=1	$(CSSETUP + 0.5) \times tKCYMHn - 5.0$	-	-	ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	tHSCSBHn0	CSIHnCTL1.CSIHnSIT=0	$CSHOLD \times tKCYMHn - 10.0$	-	-	ns
	tHSCSBHn1	CSIHnCTL1.CSIHnSIT=1	$(CSSHOLD + 0.5) \times tKCYMHn - 5.0$	-	-	ns

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. CSSETUP: Value of CSIHnCFG0-7.CSIHnSP0-7[3:0]
  3. CSHOLD: Value of CSIHnCFG0-7.CSIHnHD0-7[3:0]
  4. CSIDLE: Value of CSIHnCFG0-7.CSIHnID0-7[2:0]

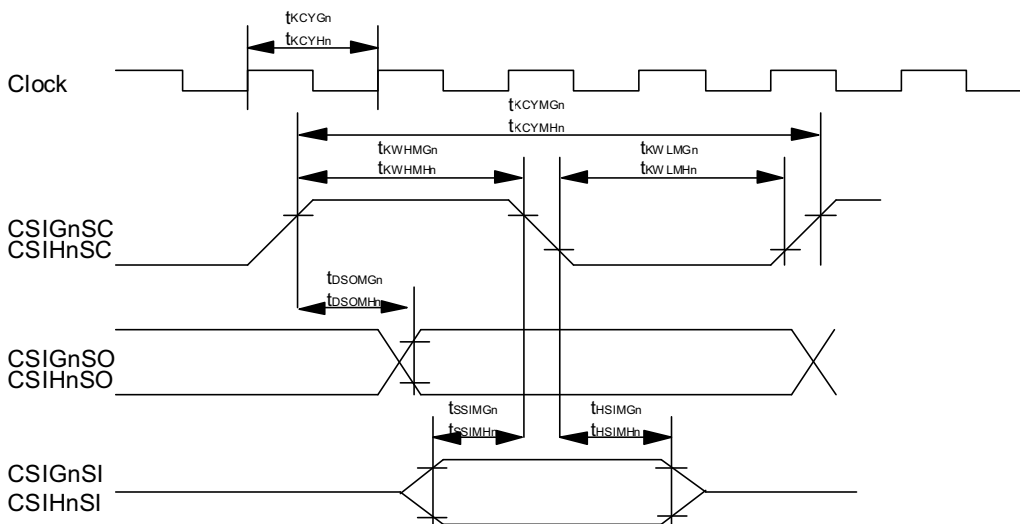
(3) Timing diagrams

SCKO / SI / SO

CSIG ( CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0 / 0 or 1 / 1 )  
 CSIH ( CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0 /0 or 1/1 )



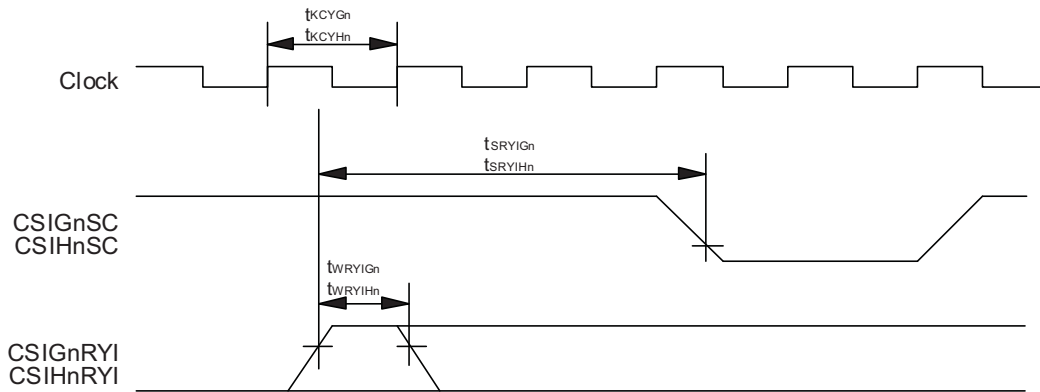
CSIG( CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1 / 0 or 0 / 1 )  
 CSIH ( CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/ 0 or 0/ 1 )



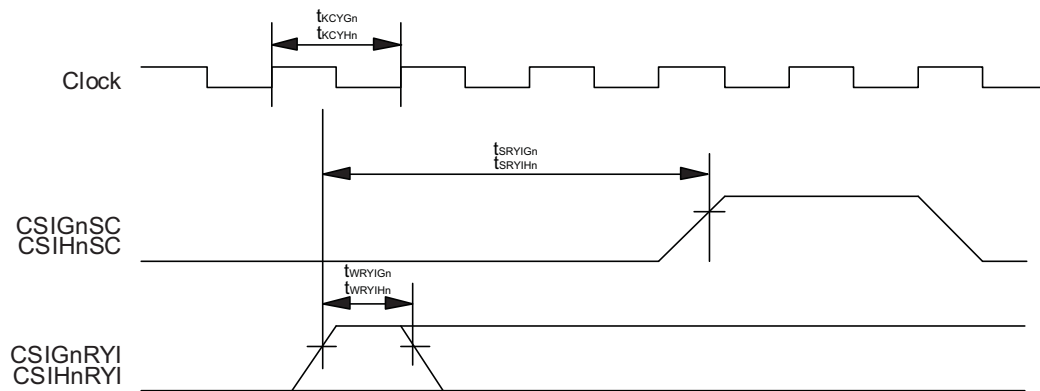
**RYI**

CSIGnCTL1 : CSIGnHSE=1, CSIGnCTL1 : CSIGnSIT = 0 )  
 CSIHnCTL1 : CSIHnHSE=1, CSIHnCTL1 : CSIHnSIT = 0 )

CSIG (CSIGnCTL1 :CSIGnCKR= 0)  
 CSIH (CSIHnCFGm:CSIHnCKPm= 0)

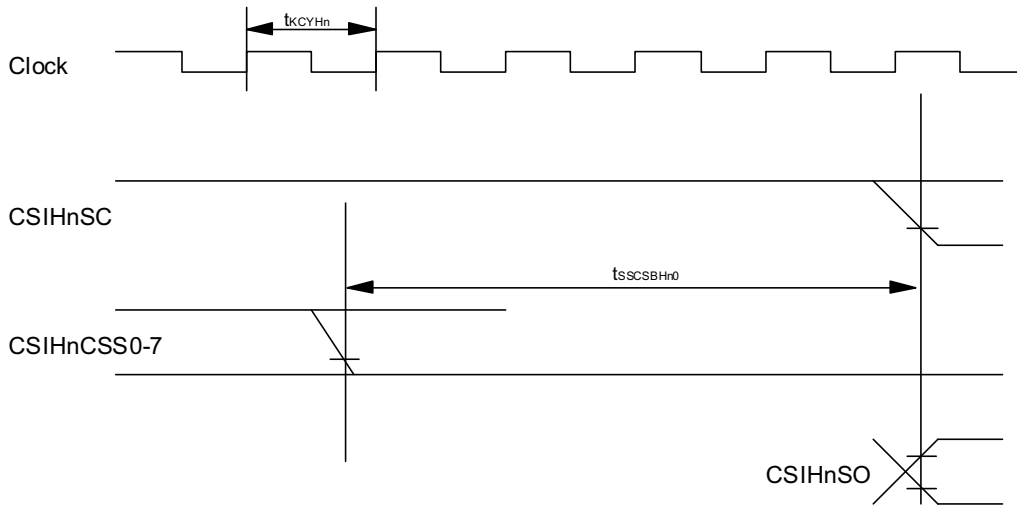


CSIG (CSIGnCTL1 :CSIGnCKR= 1)  
 CSIH (CSIHnCFGm:CSIHnCKPm= 1)

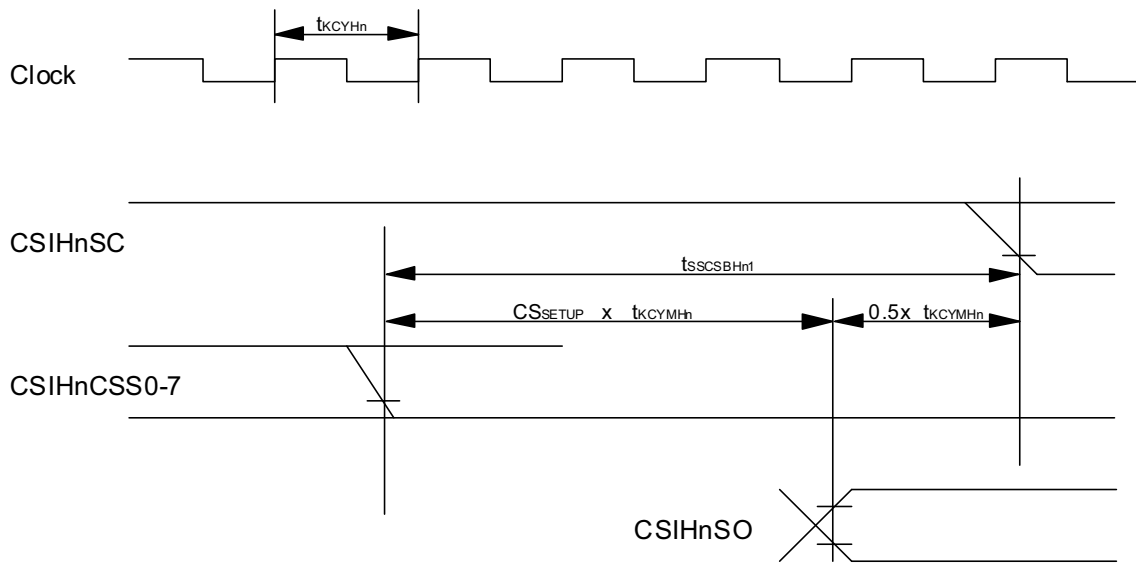


CSSn

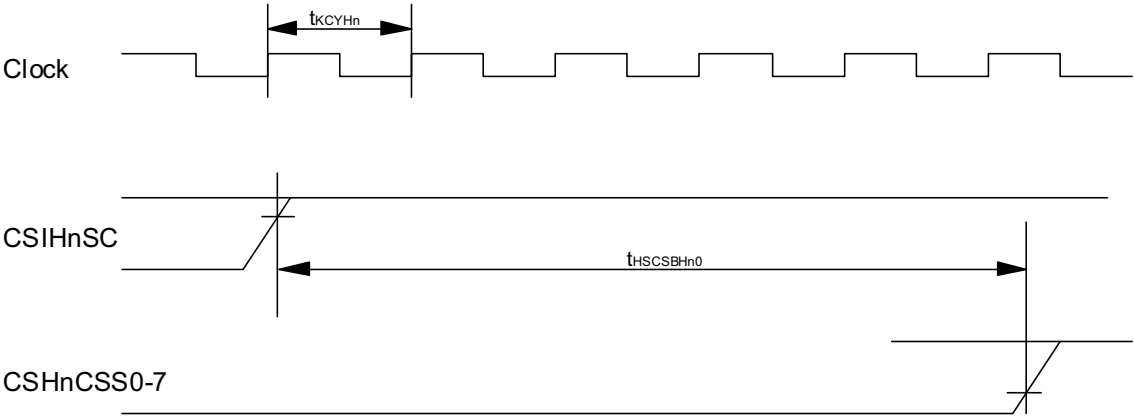
CSIHnCFGm:CSIHnCKPm= 0,CSIHnCFGm:CHIHnDAPm= 0



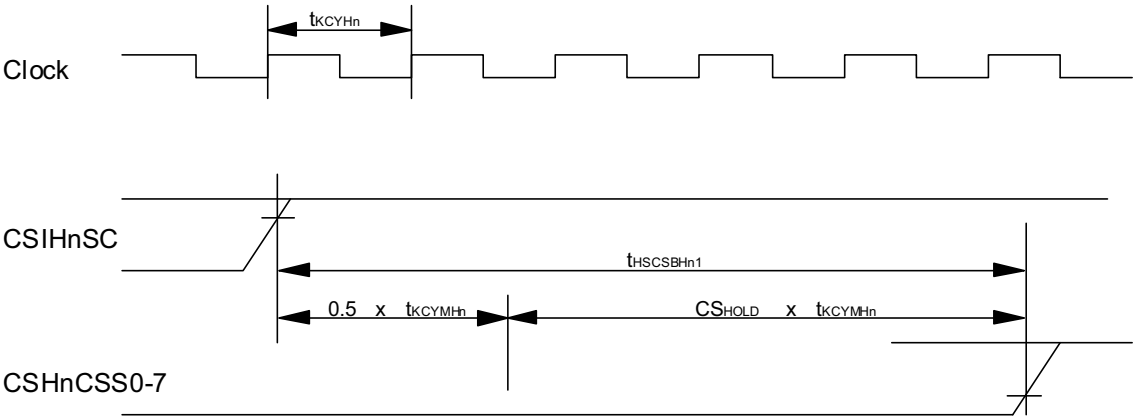
CSIHnCFGm:CSIHnCKPm= 0,CSIHnCFGm:CHIHnDAPm= 1



CSIHnCTL1 : CSIHnSIT=0, CSIHnCFGm: CSIHnCKPm= 0,CSIHnCFGm: CHIHnDAPm= 0



CSIHnCTL1 : CSIHnSIT=1, CSIHnCFGm: CSIHnCKPm= 0,CSIHnCFGm: CHIHnDAPm= 0



## 7.8.2 Slave mode

### (1) CSIG timing slave mode

Table 7-5 CSIG timing (Slave mode)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYGn		20.820.83	-	-	ns
CSIGnSC cycle time	tKCYSGn		200	-	-	ns
CSIGnSC high level width	tKWHSn		$0.5 \cdot tKCYSGn-10$	-	-	ns
CSIGnSC low level width	tKWLSn		$0.5 \cdot tKCYSGn-10$	-	-	ns
CSIGnSI setup time (vs. CSIGnSC)	tSSISn		20	-	-	ns
CSIGnSI hold time (vs. CSIGnSC)	tHSISn		$tKCYGn+5.0$	-	-	ns
SO output delay (vs SCKI)	tDSOSn		-	-	35	ns
CSIGnRYO output delay	tSRYOGn		-	-	35	ns
_CSIGnSSI setup time (vs CSIGnSC)	tSSSISn		$0.5 \cdot tKCYSn-5.0$	-	-	ns
_CSIGnSSI hold time (vs CSIGnSC)	tHSSISn		$tKCY+5.0$	-	-	ns

**Note** n: Number of macro instances. Refer to the User Manual for the detailed specification.

### (2) CSIH timing slave mode

Table 7-6 CSIH timing (Slave mode)

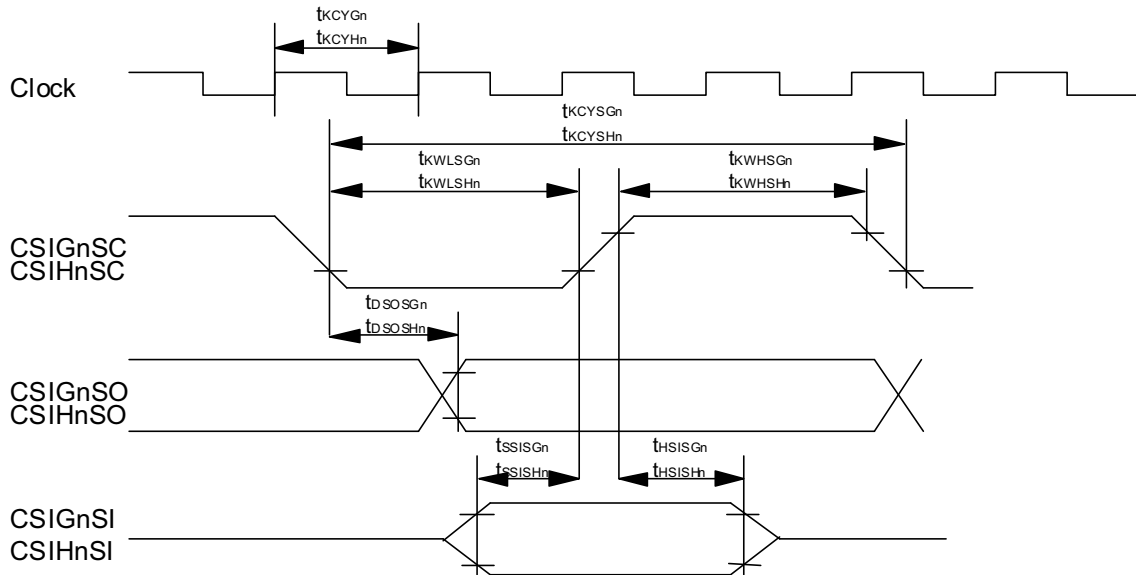
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Macro Operation clock cycle time	tKCYHn		20.8	-	-	ns
CSIHnSC cycle time	tKCYSHn		200	-	-	ns
CSIHnSC high level width	tKWHSn		$0.5 \cdot tKCYSHn-10$	-	-	ns
CSIHnSC low level width	tKWLSn		$0.5 \cdot tKCYSHn-10$	-	-	ns
CSIHnSI setup time (vs. CSIHnSC)	tSSISHn		20	-	-	ns
CSIHnSI hold time (vs. CSIHnSC)	tHSISHn		$tKCYHn+5.0$	-	-	ns
SO output delay (vs SCKI)	tDSOSHn		-	-	35	ns
CSIHnRYO output delay	tSRYOHn		-	-	35	ns
CSIHnSSI setup time (vs. CSIHnSC)	tSSSISHn		$0.5 \cdot tKCYSn-5.0$	-	-	ns
CSIHnSSI hold time (vs. CSIHnSC)	tHSSISHn		$tKCYn* 5.0$	-	-	ns

**Note** n: Number of macro instances. Refer to the User Manual for the detailed specification.

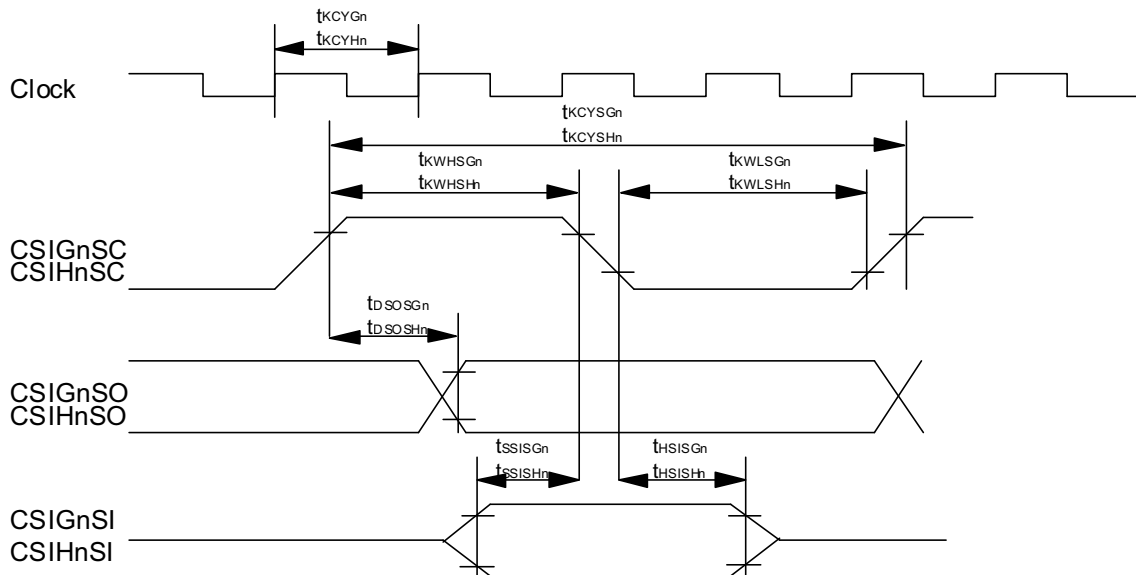
(3) Timing diagrams

**SCKO / SI / SO**

CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0 or 1/1)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/0 or 1/1)

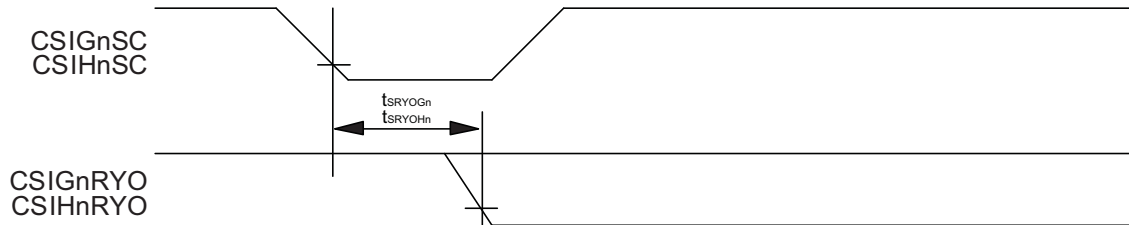


CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0 or 0/1)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/0 or 0/1)

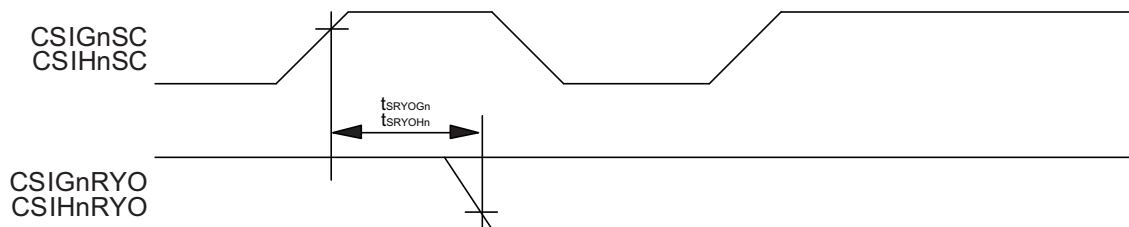


**RYO**

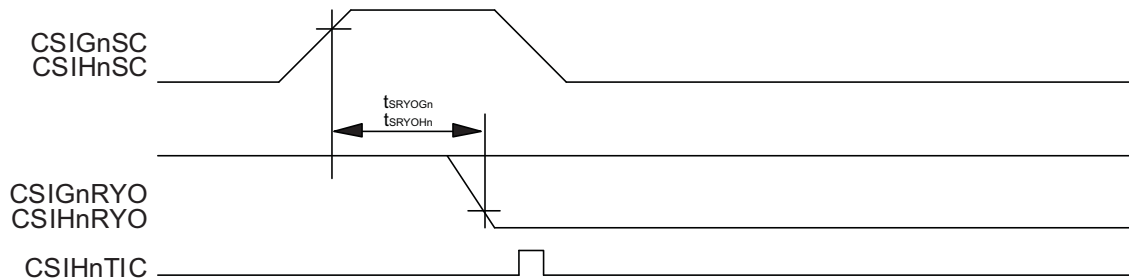
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/0)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/0)



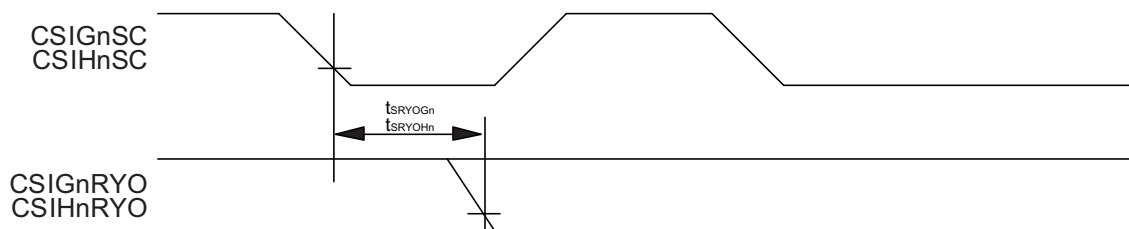
CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 0/1)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 0/1)



CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/0)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/0)



CSIG (CSIGnCTL1 : CSIGnCKR/ CSIGnCFG0 :CHIGnDAP0 = 1/1)  
 CSIH (CSIHnCFGm:CSIHnCKPm/ CSIHnCFGm: CHIHnDAPm= 1/1)

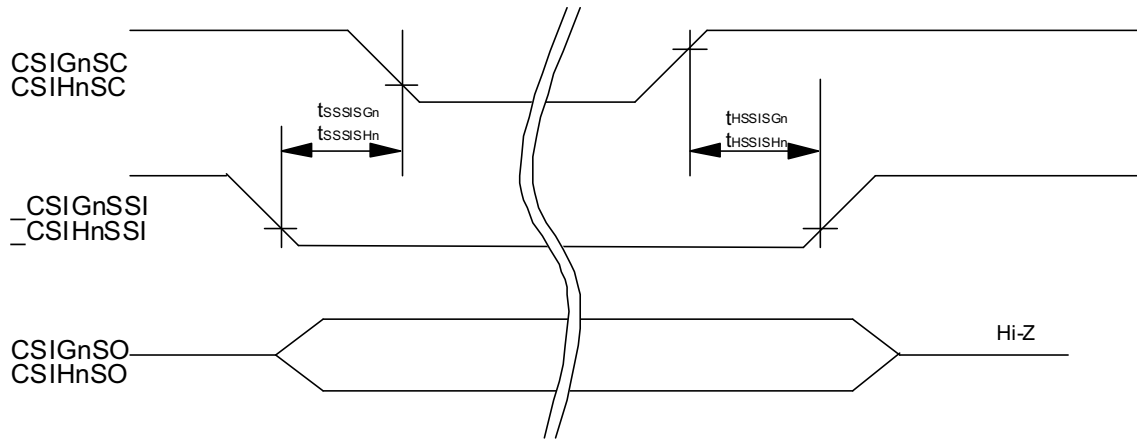




**SSI:**

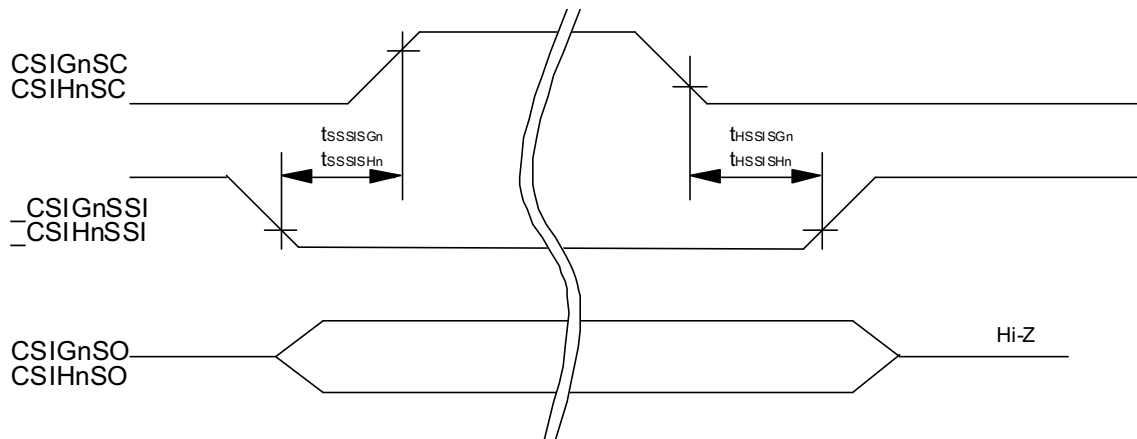
CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 0/0 or 1/1)

CSIH (CSIHnCTL1 : CSIHnSSE=1, CSIHnCFGm : CSIHnCKPm / CSIHnCFGm : CHIHnDAPm = 0/0 or 1/1)



CSIG (CSIGnCTL1 :CSIGnSSE=1, CSIGnCTL1 : CSIGnCKR,/ CSIGnCFG0 : CHIGnDAP0 = 1/0 or 0/1 ) n=0, 4

CSIH (CSIHnCTL1 : CSIHnSSE=1, CSIHnCFGm : CSIHnCKPm / CSIHnCFGm : CHIHnDAPm = 1/0 or 0/1)

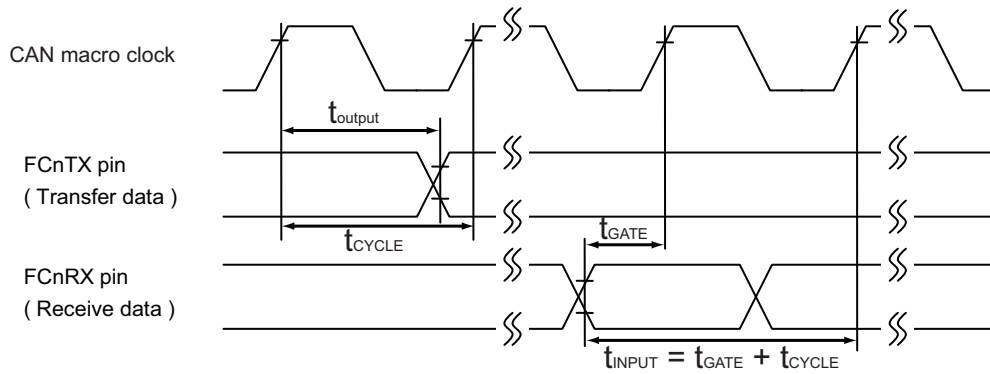


**7.9 UART timing**

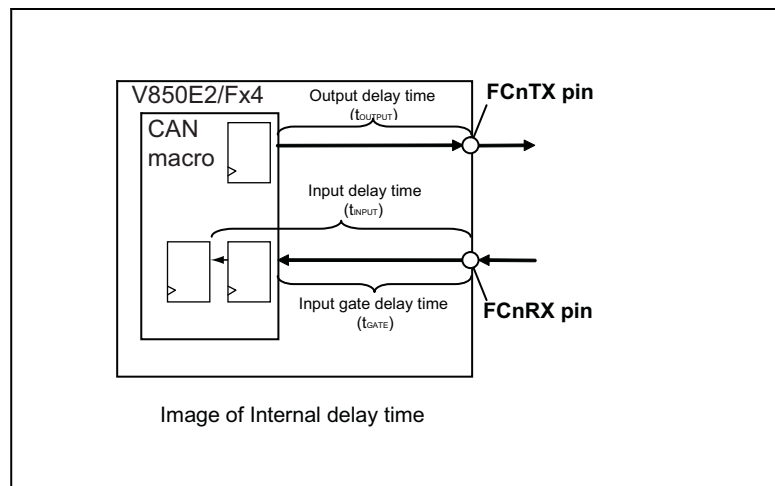
Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	1.5	Mbps

### 7.10 FCN timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	1	Mbps
Internal delay time	t <sub>INTDEL</sub>		-	-	37.5	ns
CAN Node delay time	t <sub>NODE</sub>	t <sub>CYCLE</sub> = 62.5ns	-	-	100	ns

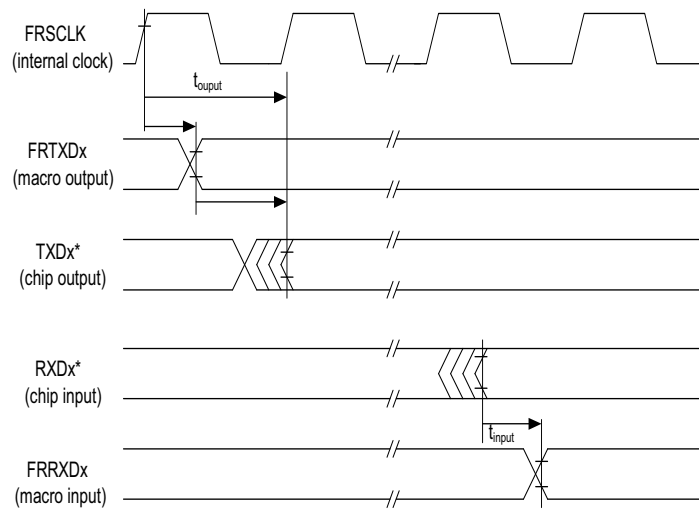
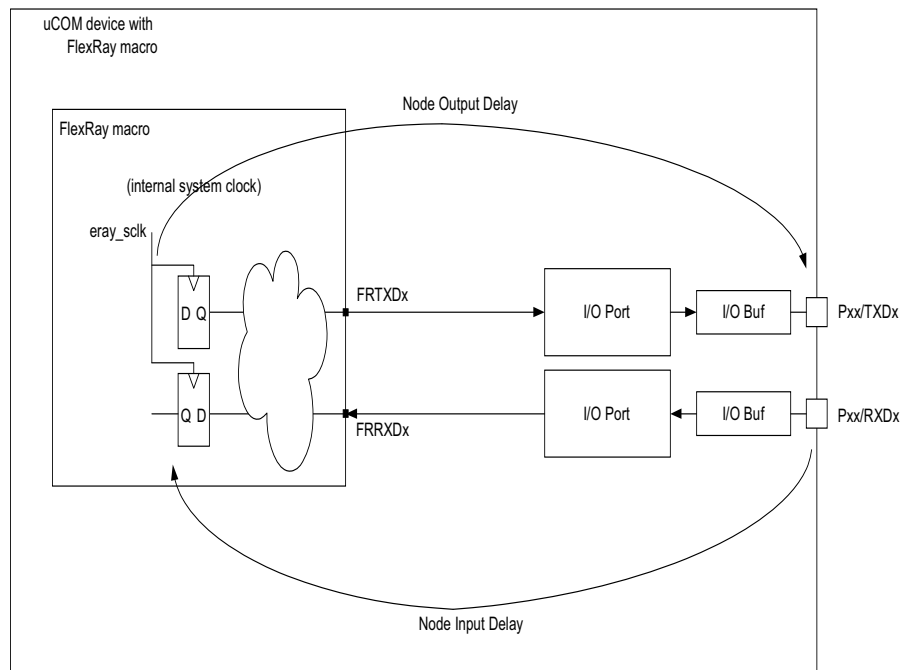


CAN node delay time (t<sub>NODE</sub>) = INPUT delay time (t<sub>input</sub>) + Output delay time (t<sub>output</sub>)  
 Internal delay time (t<sub>INTDEL</sub>) = Internal gate delay time (t<sub>GATE</sub>) + Output delay time (t<sub>output</sub>)



## 7.11 FlexRay timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Transfer rate			-	-	10	Mbps
Node Output Delay	t <sub>OUTPUT</sub>	FLX0TXDA, FLX0TXDB,	-	-	25	ns
		FLX0TXENA, FLX0TXENB	-	-		
Node Input Delay	t <sub>INPUT</sub>	FLX0RXDA, FLX0RXDB	-	-	10	ns



Port	Name	Condition	Ratings			Unit
			Min	Typ	Max	
FLX0TXENA FLX0TXENB	dTxEN <sub>RISE-FALL</sub>	Clod=25pF, measured at 20-80% E1VDD	-	-	9	ns
	dCCTxEN01		-	-	25	ns
	dCCTxEN10		-	-	25	ns
FLX0TXDA FLX0TXDB	dCCTxAsym	measured at 50% E1VDD	-	-	2.45	ns
	dCCTxDRISE25 + dCCTxDFALL25	Clod=25pF, measured at 20-80% E1VDD	-	-	9	ns
		Clod=10pF, measured at 20-80% E1VDD at the end of a 50ohm, 1ns microstripline	-	-	9	ns
	dCCTxD01	-	-	-	25	ns
dCCTxD10	-	-	-	25	ns	
FLX0RXDA FLX0RXDB	dCCRxAsmAccept	measured at 50% of E1VDD Input signal: Clod=25pF, 6.5ns (20-80% E1VDD)	-	-	5.5	ns
	C_CCRxD	-	-	-	10	pf
	uLogic_1	-	35	-	70	%
	uLogic_0	-	30	-	65	%
	dCCRxD01	-	-	-	10	ns
	dCCRxD10	-	-	-	10	ns

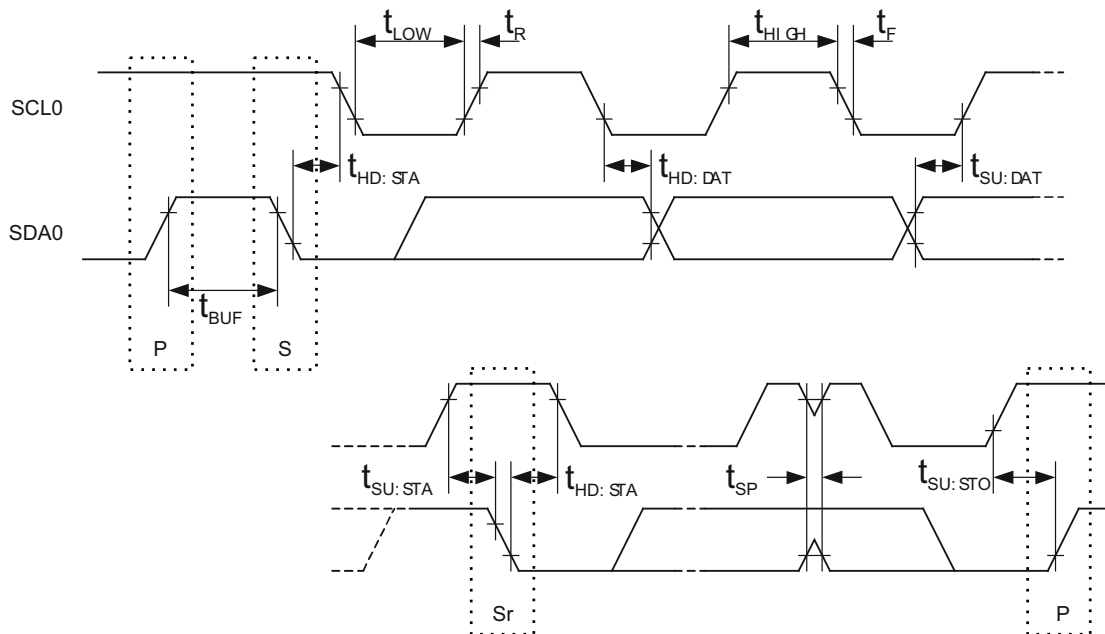
## 7.12 IIC timing

Table 7-7 Normal mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0		100	kHz
Bus free time (between stop condition and start condition)	tBUF		4.7	-	-	μs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	tHD:STA		4	-	-	μs
SCL clock low state hold time	tLOW		4.7	-	-	μs
SCL clock high state hold time	tHIGH		4	-	-	μs
Setup time for start/restart condition	tSU:STA		4.7	-	-	μs
Data hold time	tHD:DAT	CBUS compatible	5	-	-	μs
		IIC bus	0	-	-	μs
Data setup time	tSU:DAT		250	-	-	ns
Rising transition time of SDA or SCL	tR		-	-	1000	ns
Falling transition time of SDA or SCL	tF		-	-	300	ns
Setup time of stop condition	tSU:STO		4	-	-	μs
Bus capacitance	Cb		-	-	400	pF

Table 7-8 Fast mode

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
SCL clock period	fCLK		0	-	400	kHz
Bus free time (between stop condition and start condition)	t <sub>BUF</sub>		1.3	-	-	μs
Start/Restart Hold time (New clock pulse is generated after this hold time as a master.)	t <sub>HD:STA</sub>		0.6	-	-	μs
SCL clock low state hold time	t <sub>LOW</sub>		1.3	-	-	μs
SCL clock high state hold time	t <sub>HIGH</sub>		0.6	-	-	μs
Setup time for start/restart condition	t <sub>SU:STA</sub>		0.6	-	-	μs
Data hold time	t <sub>HD:DAT</sub>	IIC bus	0	-	0.9	μs
Data setup time	t <sub>SU:DAT</sub>		100	-	-	ns
Rising transition time of SDA or SCL	t <sub>R</sub>		20+0.1Cb	-	300	ns
Falling transition time of SDA or SCL	t <sub>F</sub>		20+0.1Cb	-	300	ns
Setup time of stop condition	t <sub>SU:STO</sub>		0.6	-	-	μs
Noise elimination width	t <sub>SP</sub>		0	-	50	ns
Bus capacitance	Cb		-	-	400	pF



Notes 1. P: Stop condition

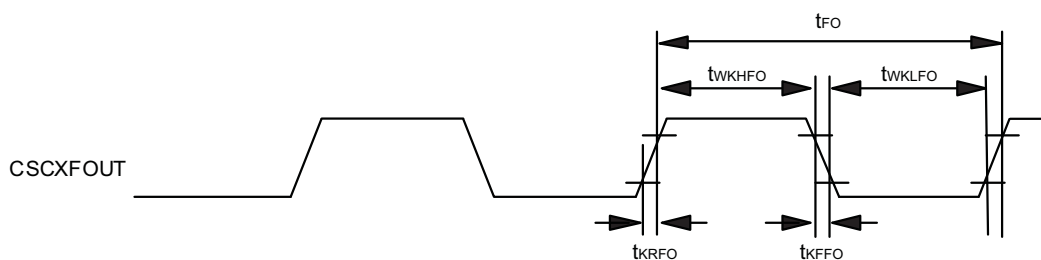
Notes 1. S: Start condition

Notes 1. Sr: Restart condition

### 7.13 Frequency Output Function (FOUT)

Table 7-9 Frequency Output Function (FOUT)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
CSCXFOUTP output cycle	tFO		50	-	-	ns
CSCXFOUTP high level width	tWKHFO		tFO / 2 - 10	-	-	ns
CSCXFOUTP low level width	tWKLFO		tFO / 2 - 10	-	-	ns
CSCXFOUTP rise time	tKRFO		-	-	10	ns
CSCXFOUTP fall time	tKFFO		-	-	10	ns

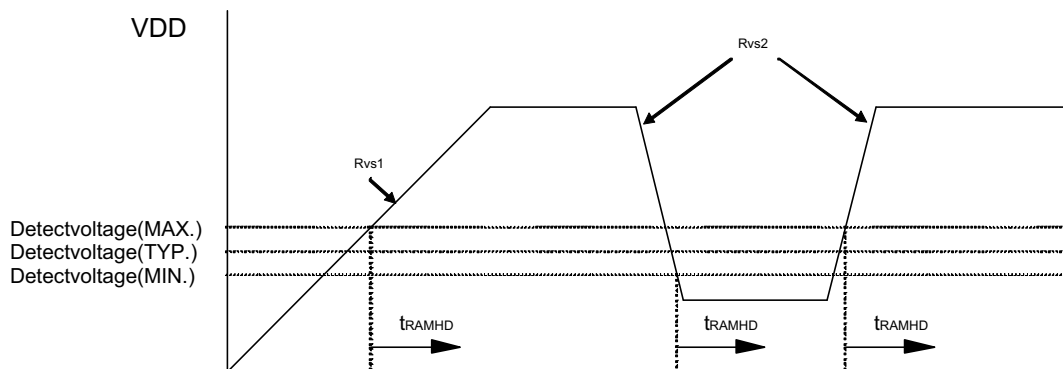


### 7.14 VLVI characteristics

Table 7-10 VLVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VRAMHF		1.8	1.9	2.0	V
Voltage slope1	Rvs1		0.18	-	1800	V/ms
Voltage slope2	Rvs2		0.0018	-	1800	V/ms
Response time <sup>a)</sup>	tRAMHD		-	-	2	ms

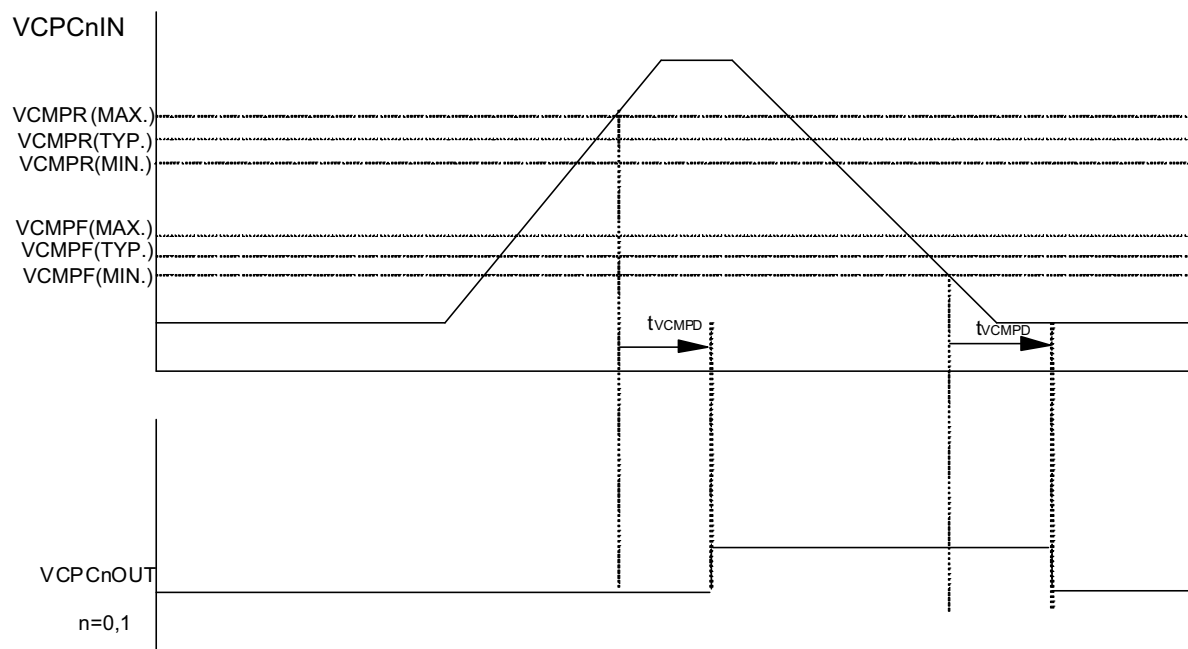
a) From detection voltage to setting of VLVI bit (VLVI.bit0)



Note VDD: REG0VDD

## 7.15 Voltage comparator characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
VCMP current	IVCMP		-	200	300	$\mu\text{A}$
Threshold voltage (rise)	VCMPR		1.745	1.780	1.815	V
Threshold voltage (fall)	VCMPF		1.645	1.680	1.715	V
Voltage slope	VCVS		-	-	50	$\text{mV}/\mu\text{s}$
Detection time	tVCMPD		-	-	2	$\mu\text{s}$
Stabilization time	tVCMPST	VCMP operation readiness after VCPC00En is set to 1	-	-	2	ms

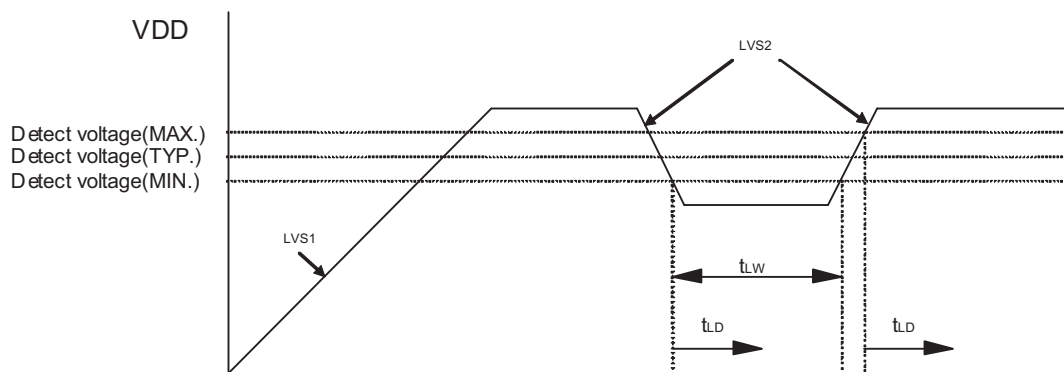




## 7.16 LVI characteristics

Table 7-11 LVI characteristics

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Detection voltage	VLVI0	LVICNT.LVICNT[2:0]=001 <sub>B</sub>	3.9	4.0	4.1	V
	VLVI1	LVICNT.LVICNT[2:0]=010 <sub>B</sub>	3.6	3.7	3.8	V
	VLVI2	LVICNT.LVICNT[2:0]=011 <sub>B</sub>	3.4	3.5	3.6	V
Voltage slope1	LVS1		0.18	-	1800	V/ms
Voltage slope2	LVS2		0.0018	-	1800	V/ms
Response time	t <sub>LD</sub>		-	-	2.0	ms
VDD minimum width	t <sub>LW</sub>		2	-	-	ms
Stabilization time	t <sub>LVIST</sub>	LVICNT0,1 is set to 1, then LVI is ready to operate	-	-	350	μs



## 7.17 A/D Converter characteristics

### 7.17.1 12bit A/D (for ADC channels without S/H functionality)

Table 7-12 12bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RESn		12	12	12	bit
Total conversion time	TCONn		1.5	-	10	μs
Overall error <sup>a</sup>	TOEn		-	-	±6.0	LSB
Non-linearity error <sup>a</sup>	ILEn		-	-	±2.5	LSB
Differential linearity error <sup>a</sup>	DLEn		-	-	±1.5	LSB
Zero scale error <sup>a</sup>	ZSEn		-	-	±5.0	LSB
Full scale error <sup>a</sup>	FSEn		-	-	±5.0	LSB
Analog input voltage <sup>a</sup>	VAIN		AnVREFM		AnVREFP	V
Power on stabilization time <sup>b</sup>			-	-	1	μs
AnVDD current	AIDDn	ADAnBPC=0, with Diagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDDnPD	Power down	-	1	-	μA
AnVREFP current	AIREFn		-	650	-	μA
Conversion result by Diagnosis function <sup>c</sup>	TESHn	AnVDD was converted	4015	-	4095	LSB
	TESHLn3	2/3 AnVDD was converted	2691	2731	2771	LSB
	TESHLn2	1/2 AnVDD was converted	2018	2048	2078	LSB
	TESHLn1	1/3 AnVDD was converted	1325	1365	1405	LSB
	TESLn	AGND was converted	0	-	80	LSB

a) The specification does not include the quantization error.

b) 'Power on' refers to  
- setting ADCAnGPS = 1

c) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.

### 7.17.2 12bit A/D (For channel ADCA0I0-5 when the S/H function is not used)

Table 7-13 12bit A/D (When channel Sample & Hold function is not used)

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0SN		12	12	12	bit
Total conversion time	TCON0SN		1.5	-	10	μs
Overall error <sup>a</sup>	TOE0SN		-	-	±6.0	LSB
Non-linearity error <sup>a</sup>	ILE0SN		-	-	±2.5	LSB
Differential linearity error <sup>a</sup>	DLE0SN		-	-	±1.5	LSB
Zero scale error <sup>a</sup>	ZSE0SN		-	-	±5.0	LSB
Full scale error <sup>a</sup>	FSE0SN		-	-	±5.0	LSB
Analog input voltage <sup>a</sup>	VAIN0SN		A0VREFM	-	A0VREFP	V
Power on stabilization time <sup>b</sup>			-	-	1	μs
A0VDD current	AIDD0SN	ADA0BPC=0, with Diagnosis function	-	4.0	6.3	mA
		ADA0BPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADA0BPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADA0BPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDD0SNPD	Power down	-	1	-	μA
A0VREFP current	AIREF0SN		-	650	-	μA
Conversion result by Diagnosis function <sup>c</sup>	TESH0SN	A0VDD was converted	4015	-	4095	LSB
	TESHL0SN3	2/3 A0VDD was converted	2691	2731	2771	LSB
	TESHL0SN2	1/2 A0VDD was converted	2018	2048	2078	LSB
	TESHL0SN1	1/3 A0VDD was converted	1325	1365	1405	LSB
	TESL0SN	AGND was converted	0	-	80	LSB

a) The specification does not include the quantization error.

b) 'Power on' refers to  
- setting ADCAnGPS = 1

c) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.

### 7.17.3 12bit A/D (When channel S/H function is used)

Table 7-14 12bit A/D (When channel Sample & Hold function is used [ADCA010 to ADCA015])

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0S		12	12	12	bit
Total conversion time	TCON0SN		1.8	-	12	μs
Sample & Hold time			50	-	-	μs
Overall error <sup>a</sup>	TOE0S		-	-	±8.0	LSB
Non-linearity error <sup>a</sup>	ILE0S		-	-	±4.0	LSB
Differential linearity error <sup>a</sup>	DLE0S		-	-	±2.5	LSB
Zero scale error <sup>a</sup>	ZSE0S		-	-	±6.0	LSB
Full scale error <sup>a</sup>	FSE0S		-	-	±6.0	LSB
Analog input voltage	VAIN0S		0.2	-	A0VREFP-0.2	V
Power on stabilization time <sup>b</sup>			-	-	1	μs
A0VDD current	AIDD0S	withDiagnosis function	-	Note3	22.1	mA
		w/o Diagnosis function	-	Note3	24.0	mA
	AIDD0SPD	Power down	-	1	-	μA
A0VREFP current	AIREF0S		-	650	-	μA
Conversion result by Diagnosis function <sup>c</sup>	TESHLS3	2/3 A0VDD was converted	2689	2731	2773	LSB
	TESHLS2	1/2 A0VDD was converted	2016	2048	2080	LSB
	TESHLS1	1/3 A0VDD was converted	1323	1365	1407	LSB

- a) The specification does not include the quantization error.  
b) 'Power on' refers to  
- setting ADCAnGPS = 1  
c) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.
  3.  $AIDD_n + 1.72\text{mA} \times (\text{number of channels used with S/H})$

## 7.17.4 10bit A/D (for ADC channels without S/H functionality)

Table 7-15 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RESn		10	10	10	bit
Total conversion time	TCONn		1.5		10	μs
Overall error <sup>a</sup>	TOEn	Excluding quantization error	-	-	±2.0	LSB
Non-linearity error <sup>a</sup>	ILEn		-	-	±1.5	LSB
Differential linearity error <sup>a</sup>	DLEn		-	-	±1.0	LSB
Zero scale error <sup>a</sup>	ZSEn		-	-	±1.5	LSB
Full scale error <sup>a</sup>	FSEn		-	-	±1.5	LSB
Analog input voltage <sup>a</sup>	VAIN		AnVREFM		AnVREFP	V
Power on stabilization time <sup>b</sup>			-		1	μs
AnVDD current	AIDDn	ADAnBPC=0, with Diagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDDnPD	Power down	-	1	-	μA
AnVREFP current	AIREFn		-	500	-	μA
Conversion result by Diagnosis function <sup>c</sup>	TESHn	AnVDD was converted	1003		1023	LSB
	TESHLn3	2/3 AnVDD was converted	673	683	693	LSB
	TESHLn2	1/2 AnVDD was converted	504	512	520	LSB
	TESHLn1	1/3 AnVDD was converted	331	341	351	LSB
	TESLn	AGND was converted	0		20	LSB

a) The specification does not include the quantization error.

b) 'Power on' refers to  
- setting ADCAnGPS = 1

c) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.

### 7.17.5 10bit A/D (For channel ADCA010-5 when the S/H function is not used)

Table 7-16 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0SN		10	10	10	bit
Total conversion time	TCON0SN		1.5		10	μs
Overall error <sup>a</sup>	TOE0SN		-	-	±2.0	LSB
Non-linearity error <sup>a</sup>	ILE0SN		-	-	±1.5	LSB
Differential linearity error <sup>a</sup>	DLE0SN		-	-	±1.0	LSB
Zero scale error <sup>a</sup>	ZSE0SN		-	-	±1.5	LSB
Full scale error <sup>a</sup>	FSE0SN		-	-	±1.5	LSB
Analog input voltage <sup>a</sup>	VAIN0SN		AnVREFM		AnVREFP	V
Power on stabilization time <sup>b</sup>			-	-	1	μs
AnVDD current	AIDD0SN	ADAnBPC=0, with Diagnosis function	-	4.0	6.3	mA
		ADAnBPC=0, w/o Diagnosis function	-	5.2	8.1	mA
		ADAnBPC=1, with Diagnosis function	-	4.6	7.4	mA
		ADAnBPC=1, w/o Diagnosis function	-	6.2	9.2	mA
	AIDD0SNPD	Power down	-	1	-	μA
AnVREFP current	AIREF0SN		-	500	-	μA
Conversion result by Diagnosis function <sup>c</sup>	TESH0SN	AnVDD was converted	1003	-	1023	LSB
	TESHL0SN3	2/3 AnVDD was converted	673	683	693	LSB
	TESHL0SN2	1/2 AnVDD was converted	504	512	520	LSB
	TESHL0SN1	1/3 AnVDD was converted	331	341	351	LSB
	TESL0SN	AGND was converted	0	-	20	LSB

a) The specification does not include the quantization error.

b) 'Power on' refers to  
- setting ADCAnGPS = 1

c) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.
  3.  $AIDDn + 1.72mA \times (\text{number of channels used with S/H})$

## 7.17.6 10bit A/D (When channel S/H function is used)

Table 7-17 10 bit A/D

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Resolution	RES0S		10	10	10	bit
Total conversion time	TCON0S		1.84	-	12.2	μs
Sample & Hold time			50	-	-	μs
Overall error <sup>a</sup>	TOE0S		-	-	±2.5	LSB
Non-linearity error <sup>a</sup>	ILE0S		-	-	±2.0	LSB
Differential linearity error <sup>a</sup>	DLE0S		-	-	±1.5	LSB
Zero scale error <sup>a</sup>	ZSE0S		-	-	±2.0	LSB
Full scale error <sup>a</sup>	FSE0S		-	-	±2.0	LSB
Analog input voltage <sup>a</sup>	VAIN0S		0.2	-	A0VREFP-0.2	V
Power on stabilization time <sup>b</sup>			-	-	1	μs
AnVDD current	AIDD0S	ADAnBPC=1, with Diagnosis function	-	c	22.1	mA
		ADAnBPC=1, w/o Diagnosis function	-	c	24.0	mA
	AIDD0SPD	Power down	-	1	-	μA
AnVREFP current	AIREF0S		-	500	-	μA
Conversion result by Diagnosis function <sup>d</sup>	TESHL0S3	2/3 AnVDD was converted	672	683	694	LSB
	TESHL0S2	1/2 AnVDD was converted	503	512	521	LSB
	TESHL0S1	1/3 AnVDD was converted	330	341	352	LSB

a) The specification does not include the quantization error.

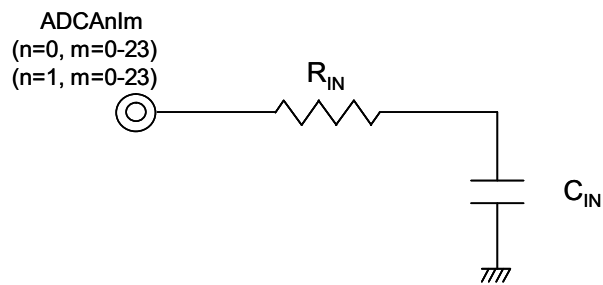
b) 'Power on' refers to  
- setting ADCAnGPS = 1

c) AIDDn x 1.72 x the number of used channels with Sample & Hold

d) The values given do not include influence of injected current

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.

### 7.17.7 Equivalent circuit



Terminals	Condition	$R_{IN}[k\Omega]$	$C_{IN}[pF]$	
ADCA010-ADCA015	When S&H is used	0.7	3.6	
	When S&H is not used	ADA0BPC=0	1.6	12.6
		ADA0BPC=1	1.5	7.1
ADCA016-ADCA0123	ADA0BPC=0	1.2	11.9	
	ADA0BPC=1	1.1	7.1	
ADCA110-ADCA1123	ADA0BPC=0	1.2	11.9	
	ADA0BPC=1	1.1	7.1	

**Caution** These specifications are not tested in outgoing inspection. Therefore  $R_{IN}$  and  $C_{IN}$  values are not guaranteed and are reference values only. Additionally these values are specified as maximum values.

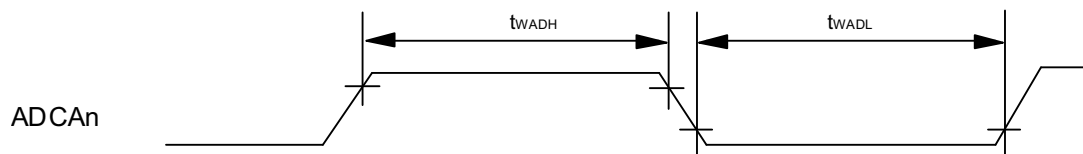
### 7.17.8 ADTRG timing

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
ADCAnTRGm input High level width	tWADH	with digital noise filter	a	-	-	ns
		without digital noise filter	b	-	-	ns
ADCAnTRGm input Low level width	tWADL	with digital noise filter	a	-	-	ns
		without digital noise filter	b	-	-	ns

- a)  $2, 3, 4$  or  $5 \times T_{\text{samp}} + 20$  ( $T_{\text{samp}}$  shows sampling period specified in noise filter).  
More than 1 PCLK width of ADC macro must be kept regarding DNF pass through pulse width.
- b)  $1 \times t_{\text{SYNC}} + 20$  ( $t_{\text{SYNC}}$ : 1 PCLK of ADC macro)

- Notes**
1. n: Number of macro instances. Refer to the User Manual for the detailed specification.
  2. m: Number of channels. Refer to the User Manual for the detailed specification.



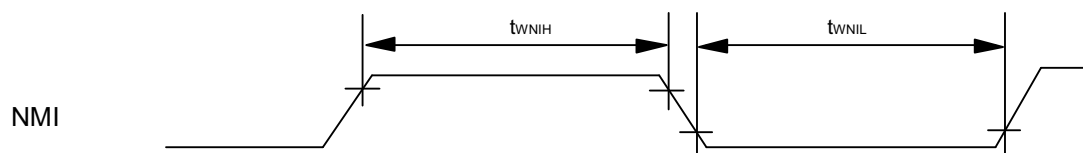


## 7.18 Key Return

Table 7-18

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
KRn input High level width	$t_{WKRH}$		300	-	-	ns
KRn input Low level width	$t_{WKRL}$		300	-	-	ns

**Note** n: Number of instances. Refer to the User Manual for the detailed specification.



## Chapter 8 Memory specification

### 8.1 Code flash specification

Table 8-1 Code flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes <sup>a)</sup>	CWRT	Data retention 20 years	-	-	100	times
Programming Temperature	tPRG	(A) grade products	-40	-	85	°C
		(A1) grade products	-40	-	110	°C

a) Please contact RENESAS sales office regarding specification other than the above.

### 8.2 Data flash specification

Table 8-2 Data flash

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
Number of Re-Writes <sup>a)</sup>	DWRT1	Data retention 20 years	-	-	1000	times
	DWRT2	Data retention 15 years	-	-	5000	times
	DWRT3	Data retention 5 years	-	-	15000	times
Programming Temperature	tPRG	(A) grade products	-40	-	85	°C
		(A1) grade products	-40	-	110	°C

a) Please contact RENESAS sales office regarding specification other than the above.

### 8.3 Serial write operation specification

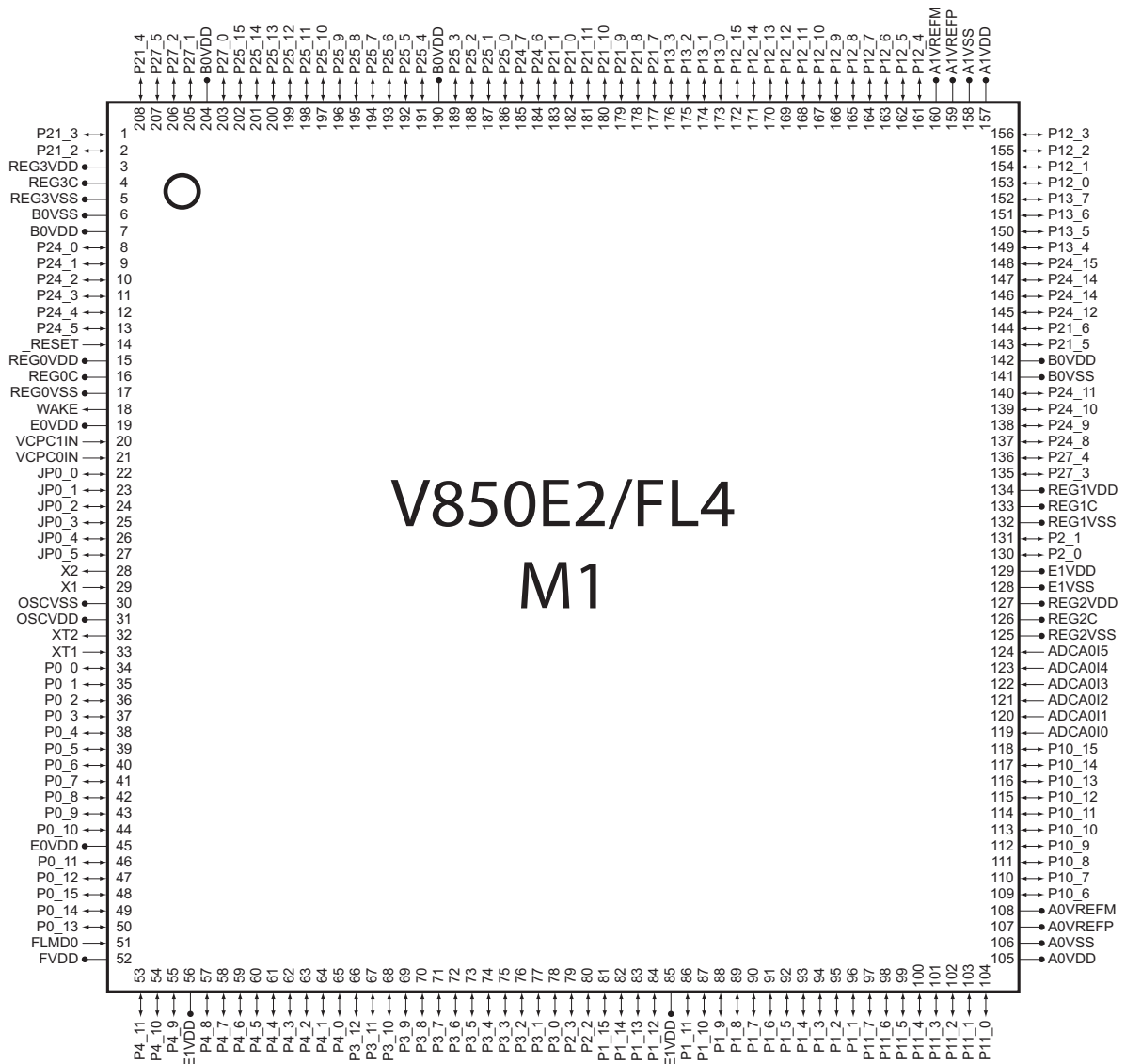
#### Serial write operation

Parameter	Symbol	Condition	Ratings			Unit
			Min	Typ	Max	
FLMD0 setup time	tDR		1	-	-	ms
RESET release	tPR		2	-	-	ms
FLMD0 pulse input start	tRP		-	100	-	ms
FLMD0 low/high level width	tPW		10	-	100	μs
FLMD0 raise time	tR		-	-	20	ns
FLMD0 fall time	tF		-	-	20	ns
Programming time		per 128 bit	-	-	50	μs
Erase time		per 4KB	-	-	54	ms

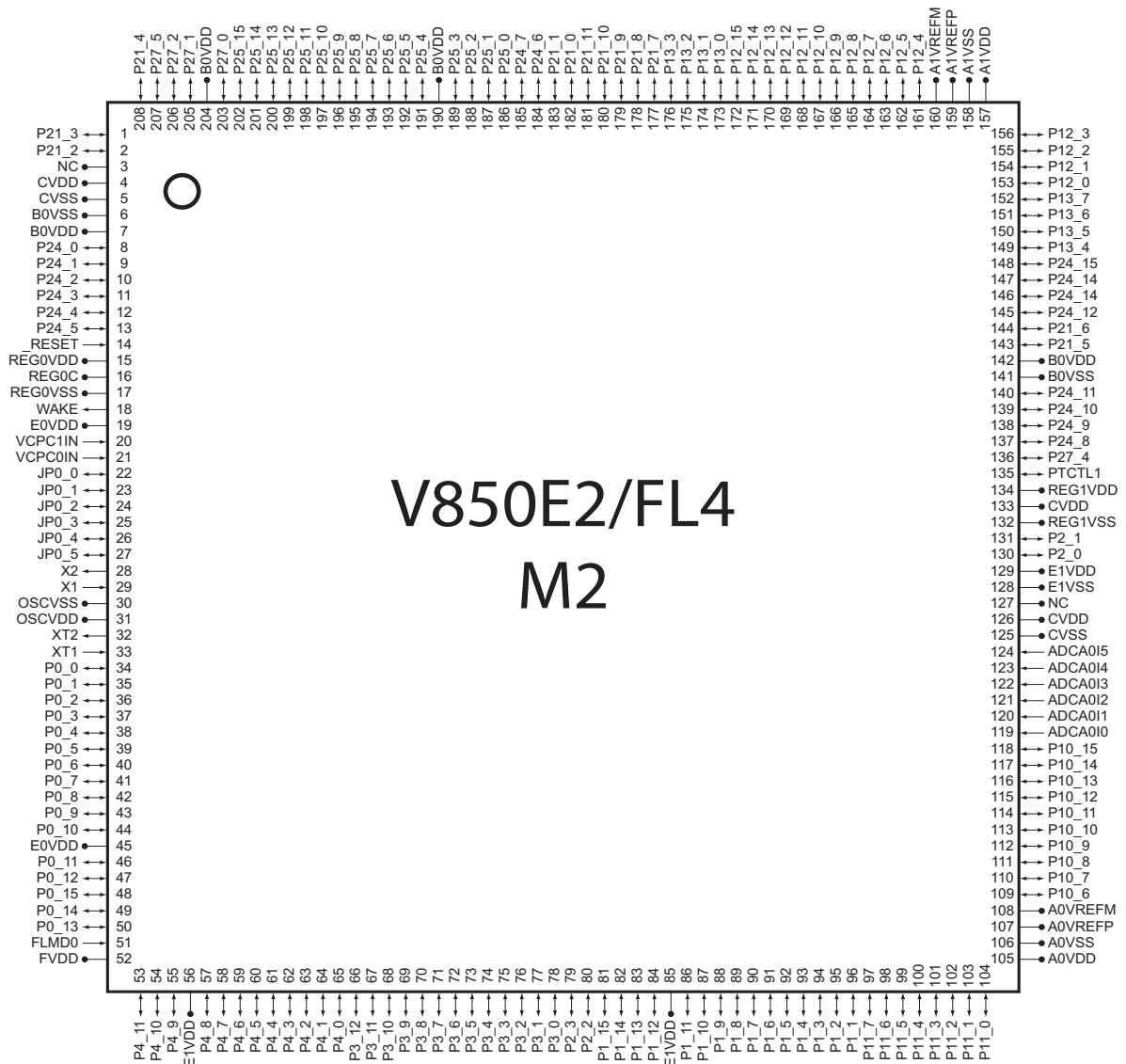
# Chapter 9 Pinning and package specification

## 9.1 Pinning specification

### (1) M1 Product

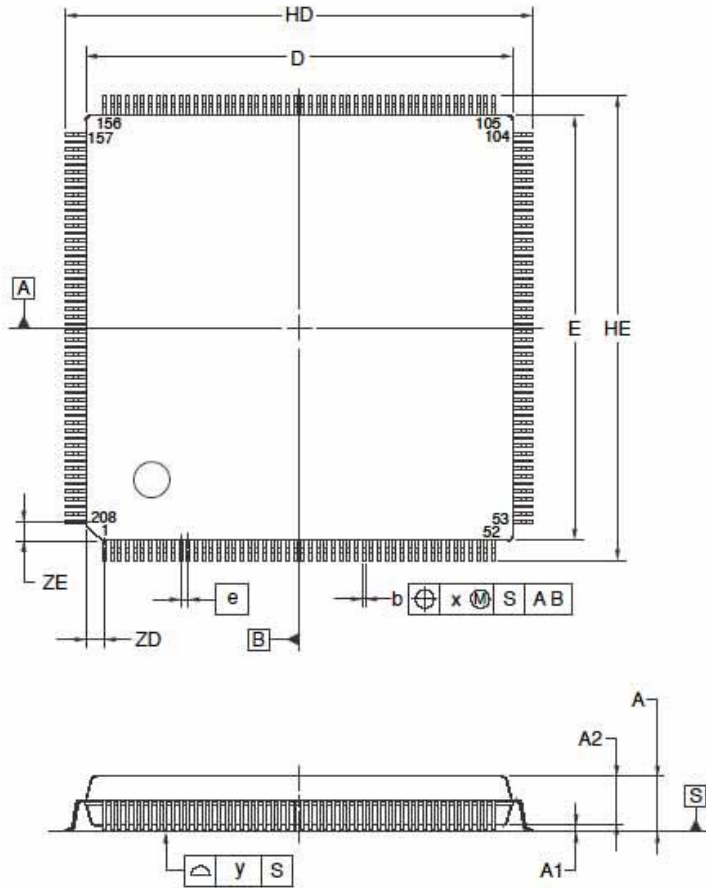


(2) M2 Product



## 9.2 Package specification

208-PIN PLASTIC QFP (FINE PITCH) (28x28)



(UNIT:mm)

ITEM	DIMENSIONS
D	28.00±0.20
E	28.00±0.20
HD	30.60±0.20
HE	30.60±0.20
A	3.80 MAX.
A1	0.40±0.10
A2	3.20±0.10
[A3]	0.25
b	0.20 <sup>+0.07</sup> <sub>-0.02</sub>
c	0.125 <sup>+0.075</sup> <sub>-0.025</sub>
L	0.50
Lp	0.60±0.15
L1	1.325 <sup>+0.175</sup> <sub>-0.225</sub>
θ	3° <sup>+</sup> <sub>-3°</sub>
[e]	0.50
x	0.10
y	0.10
ZD	1.25
ZE	1.25

P208GD-50-FAD

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## Chapter 10 Definition of terms

The following sections describe the meaning of several terms used in this document.

### 10.1 How to Read A/D Converter Characteristics Table

This section describes the meanings of the terms peculiar to the A/D converter.

#### (1) Resolution

The minimum analog input voltage that can be identified, i.e. the ratio of the analog input voltage to 1 digital output is called 1 LSB (Least Significant Bit). The ratio of 1 LSB to the full scale is expressed as %FSR (Full Scale Range). %FSR is the ratio, in percentage, of the range in which an analog input voltage can be converted, and is expressed as follows regardless of the resolution.

$$\begin{aligned} 1\%FSR &= (\text{Maximum value of analog input voltage that can be converted} - \\ &\quad \text{Minimum value of analog input voltage that can be converted})/100 \\ &= (AV_{REFP} - AV_{REFM})/100 \end{aligned}$$

1 LSB is as follows at a resolution of 10 bits:

$$\begin{aligned} 1 \text{ LSB} &= 1/2^{10} \\ &= 1/1,024 \\ &= 0.098\%FSR \end{aligned}$$

1 LSB is as follows at a resolution of 12 bits:

$$\begin{aligned} 1 \text{ LSB} &= 1/2^{12} \\ &= 1/4,096 \\ &= 0.024\%FSR \end{aligned}$$

The accuracy is determined by the total error, regardless of the resolution.

**(2) Total error**

This is the maximum value of the difference between the actually measured value and the theoretical value.

It is the total of the zero-scale error, full-scale error, linearity error, and a combination of these errors.

The total error shown in the characteristics table does not include the quantization error.

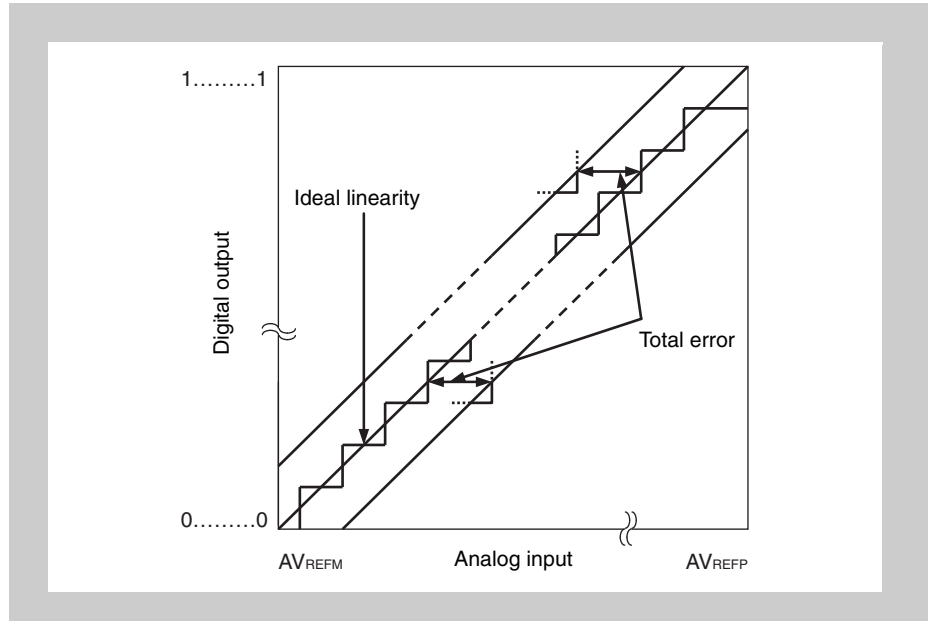


Figure 10-1 Total error

**(3) Quantization error**

This is the error of  $\pm 1/2$  LSB that always occurs when an analog value is converted into a digital value. Because the A/D converter converts an analog input voltage in a range of  $\pm 1/2$  LSB into the same digital code, the quantization error is unavoidable.

Note that this error is not included in the total error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

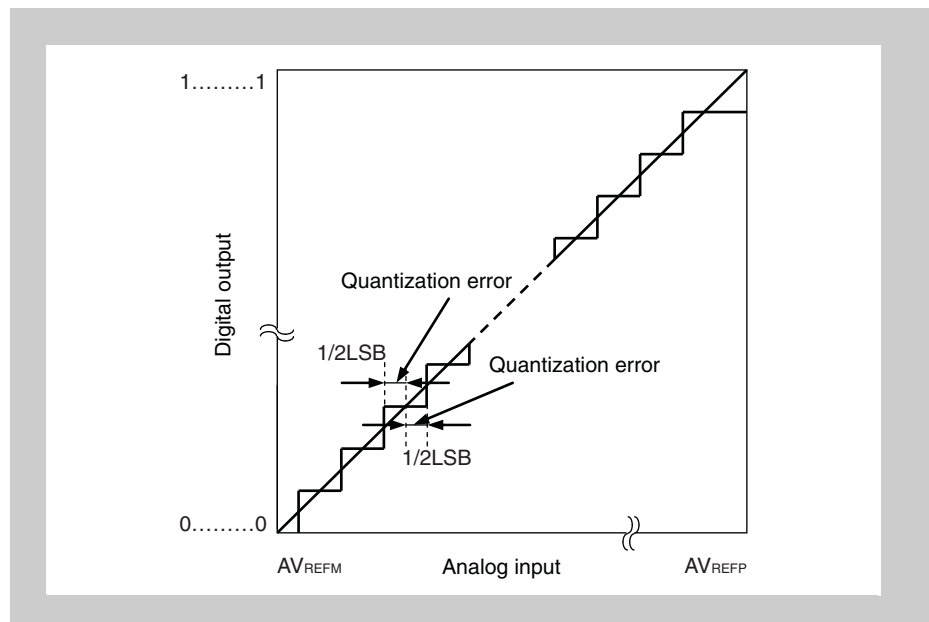


Figure 10-2 Quantization error



**(4) Zero-scale error**

This is the difference between the actually measured value of the analog input voltage and the theoretical value (1/2 LSB) when the digital output changes from 0...000 to 0...001.

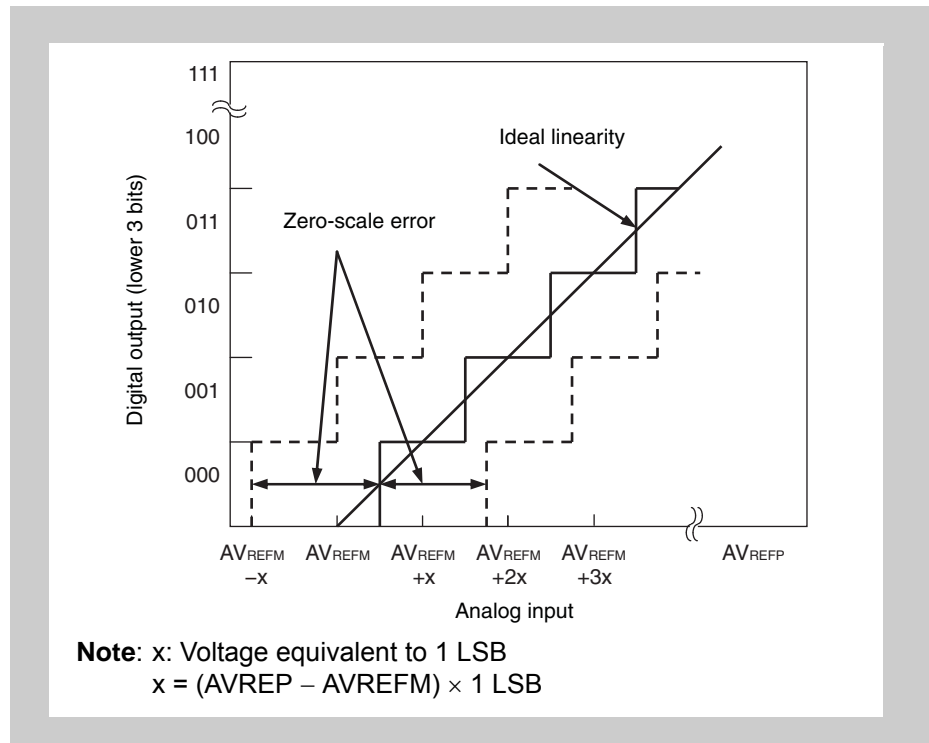


Figure 10-3 Zero-scale error

**(5) Full-scale error**

This is the difference between the actually measured value of the analog input voltage and the theoretical value (full scale - 3/2 LSB) when the digital output changes from 1...110 to 1...111.

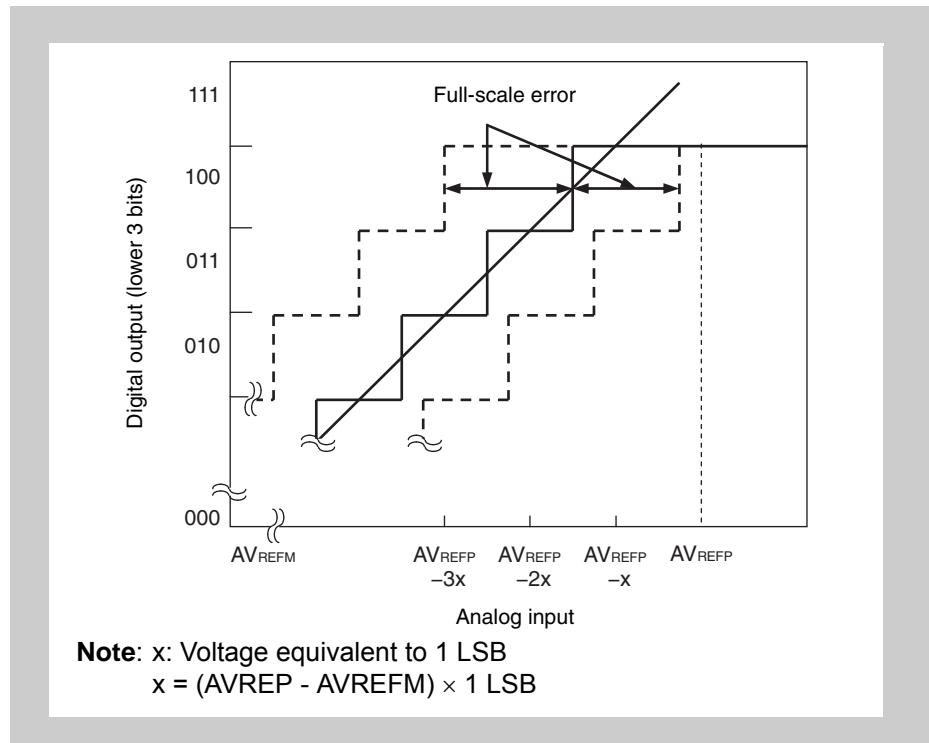


Figure 10-4 Full-scale error

**(6) Differential linearity error**

Ideally, the width at which a specific code is output is 1 LSB. The differential linearity error is the difference between the actually measured value of the width at which a specific code is output and the ideal value.

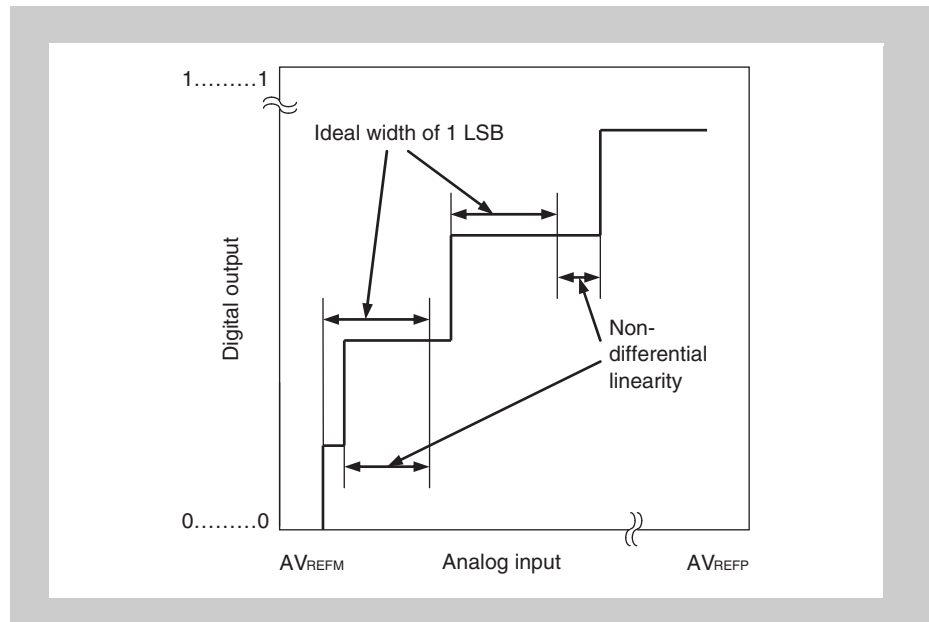


Figure 10-5 Differential linearity error

**(7) Integral linearity error**

This indicates the degree to which the conversion characteristic shifts from the ideal linearity, and indicates the maximum value of the difference between the actually measured value and the ideal linearity where the zero-scale error and full-scale error are 0.

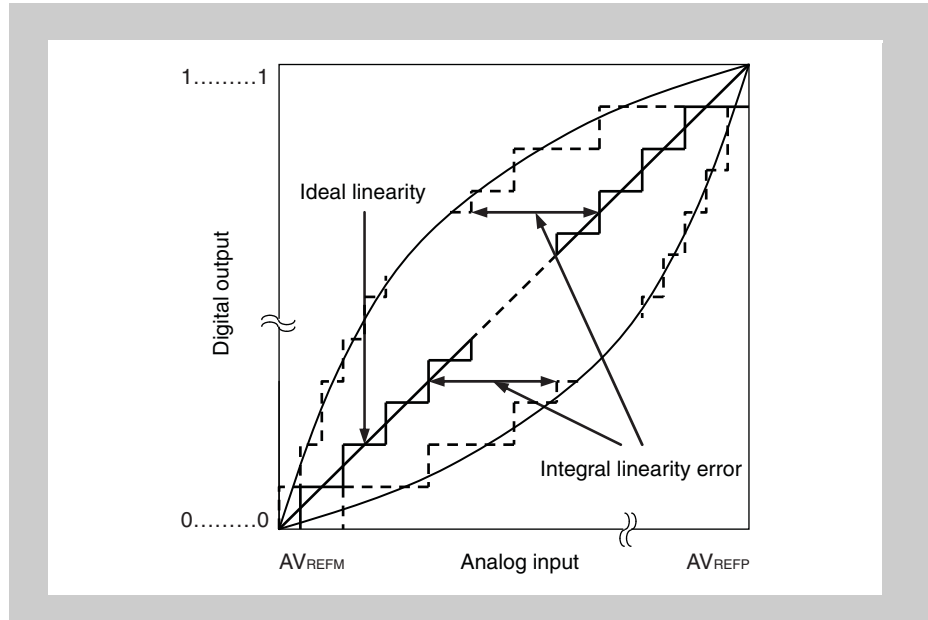


Figure 10-6 Integral linearity error

**(8) Conversion time**

This is the time from when an analog voltage is input until digital output is produced.

The conversion time in the characteristics table includes sampling time.

**(9) Sampling time**

This is the time during which the analog switch is on to input the analog voltage to the sample & hold circuit.

**(10) A/D start time**

This is the time from the A/D conversion trigger to the start of A/D conversion.

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## Revision History

Version	Date	Document number	Description
1.0	2013-05-24	R01DS0142ED0100	Initial version Document was EASE-DS-0027-1.3 Changes: - RIVS ISO0/ISO1 regulator value was 1.8V/ $\mu$ s is 5600V/s - Added FLMD0 / FLMD1 resistor values