

## EL5420T

### 12MHz Rail-to-Rail Input-Output Operational Amplifier

FN6838  
Rev 1.00  
September 8, 2015

The EL5420T is a low power, high voltage rail-to-rail input-output amplifier. The EL5420T contains four amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability and is unity gain stable.

The maximum operating voltage range is from 4.5V to 19V. It can be configured for single or dual supply operation, and typically consumes only 500 $\mu$ A per amplifier. The EL5420T has an output short circuit capability of  $\pm$ 200mA and a continuous output current capability of  $\pm$ 70mA.

The EL5420T features a slew rate of 12V/ $\mu$ s. Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of 12MHz (-3dB). This enables the amplifiers to offer maximum dynamic range at any supply voltage. These features make the EL5420T an ideal amplifier solution for use in TFT-LCD panels as a  $V_{COM}$  or static gamma buffer, and in high speed filtering and signal conditioning applications. Other applications include battery power and portable devices, especially where low power consumption is important.

The EL5420T is available in a 14 Ld TSSOP package, 14 Ld SOIC package, and a space saving thermally enhanced 16 Ld QFN package. All feature a standard operational amplifier pin out. The devices operate over an ambient temperature range of -40°C to +85°C.

### Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
EL5420TILZ* (No longer available or supported)	5420TIL Z	16 Ld QFN	MDP0046
EL5420TIRZ*	5420TIR Z	14 Ld TSSOP	MDP0044
EL5420TISZ*(No longer available or supported)	5420TIS Z	14 Ld SOIC	MDP0027

\*Add "-T7" or "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

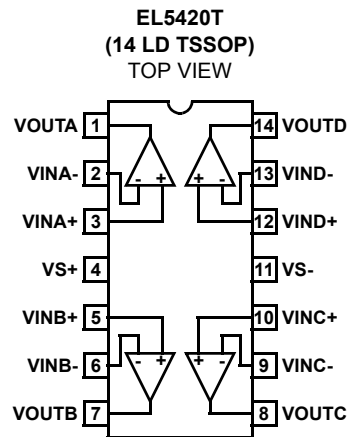
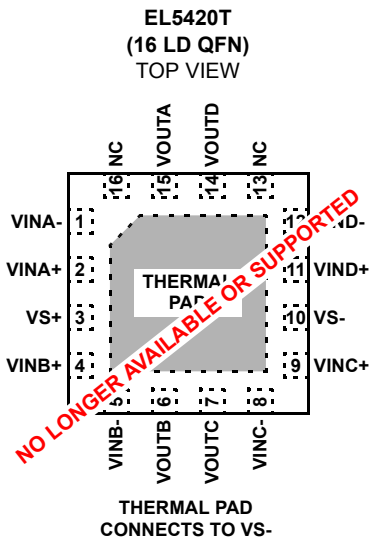
### Features

- 12MHz (-3dB) Bandwidth
- 4.5V to 19V Maximum Supply Voltage Range
- 12V/ $\mu$ s Slew Rate
- 500 $\mu$ A Supply Current (per Amplifier)
- $\pm$ 70mA Continuous Output Current
- $\pm$ 200mA Output Short Circuit Current
- Unity-gain Stable
- Beyond the Rails Input Capability
- Rail-to-rail Output Swing
- Built-in Thermal Protection
- -40°C to +85°C Ambient Temperature Range
- Pb-free (RoHS compliant)

### Applications

- TFT-LCD Panels
- $V_{COM}$  Amplifiers
- Static Gamma Buffers
- Electronics Notebooks
- Electronics Games
- Touch-screen Displays
- Personal Communication Devices
- Personal Digital Assistants (PDA)
- Portable Instrumentation
- Sampling ADC Amplifiers
- Wireless LANs
- Office Automation
- Active Filters
- ADC/DAC Buffer

**Pinouts**



**Absolute Maximum Ratings** ( $T_A = +25^{\circ}\text{C}$ )

Supply Voltage between $V_{S+}$ and $V_{S-}$ .....	+19.8V
Input Voltage Range ( $V_{INx+}$ , $V_{INx-}$ ) .....	$V_{S-} - 0.5\text{V}$ , $V_{S+} + 0.5\text{V}$
Input Differential Voltage ( $V_{INx+} - V_{INx-}$ ) .....	$(V_{S+} + 0.5\text{V}) - (V_{S-} - 0.5\text{V})$
Maximum Continuous Output Current .....	$\pm 70\text{mA}$
ESD Rating	
Human Body Model .....	3000V

**Thermal Information**

Thermal Resistance Junction-to-Ambient (Typical)	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )
16 Ld QFN (Note 1) .....	47
14 Ld SOIC (Note 2) .....	88
14 Ld TSSOP (Note 2) .....	100
Thermal Resistance Junction-to-Case (Typical)	$\theta_{JC}$ ( $^{\circ}\text{C}/\text{W}$ )
16 Ld QFN (Note 3) .....	9
Storage Temperature .....	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Ambient Operating Temperature .....	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Maximum Junction Temperature .....	$+150^{\circ}\text{C}$
Power Dissipation Curves .....	See Figures 30 and 31
Pb-free Reflow Profile .....	see link below
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**Electrical Specifications**  $V_{S+} = +5\text{V}$ ,  $V_{S-} = -5\text{V}$ ,  $R_L = 10\text{k}\Omega$  to  $0\text{V}$ ,  $T_A = +25^{\circ}\text{C}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 0\text{V}$		3	13	mV
$TCV_{OS}$	Average Offset Voltage Drift (Note 4)	14 LD TSSOP, SOIC package		7		$\mu\text{V}/^{\circ}\text{C}$
		16 LD QFN package		2		$\mu\text{V}/^{\circ}\text{C}$
$I_B$	Input Bias Current	$V_{CM} = 0\text{V}$		2	50	nA
$R_{IN}$	Input Impedance			1		$\text{G}\Omega$
$C_{IN}$	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For $V_{INx}$ from $-5.5\text{V}$ to $+5.5\text{V}$	50	75		dB
$A_{VOL}$	Open Loop Gain	$-4.5\text{V} \leq V_{OUTx} \leq +4.5\text{V}$	75	105		dB
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OL}$	Output Swing Low	$I_L = -5\text{mA}$		-4.94	-4.85	V
$V_{OH}$	Output Swing High	$I_L = +5\text{mA}$	4.85	4.94		V
$I_{SC}$	Short Circuit Current	$V_{CM} = 0\text{V}$ , Source: $V_{OUTx}$ short to $V_{S-}$ , Sink: $V_{OUTx}$ short to $V_{S+}$		$\pm 200$		mA
$I_{OUT}$	Output Current			$\pm 70$		mA
<b>POWER SUPPLY PERFORMANCE</b>						
$(V_{S+}) - (V_{S-})$	Supply Voltage Range		4.5		19	V
$I_S$	Supply Current (Per Amplifier)	$V_{CM} = 0\text{V}$ , No load		500	750	$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	Supply is moved from $\pm 2.25\text{V}$ to $\pm 9.5\text{V}$	60	75		dB
<b>DYNAMIC PERFORMANCE</b>						
SR	Slew Rate (Note 5)	$-4.0\text{V} \leq V_{OUTx} \leq +4.0\text{V}$ , 20% to 80%		12		$\text{V}/\mu\text{s}$

**Electrical Specifications**  $V_{S+} = +5V$ ,  $V_{S-} = -5V$ ,  $R_L = 10k\Omega$  to  $0V$ ,  $T_A = +25^\circ C$ , unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$t_s$	Settling to +0.1% (Note 6)	$A_V = +1$ , $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$ , $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ $R_L = 10k\Omega$ , $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ $R_L = 10k\Omega$ , $C_L = 8pF$		50		°
CS	Channel Separation	$f = 5MHz$		75		dB

**Electrical Specifications**  $V_{S+} = +5V$ ,  $V_{S-} = 0V$ ,  $R_L = 10k\Omega$  to  $2.5V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 2.5V$		3	13	mV
$TCV_{OS}$	Average Offset Voltage Drift (Note 4)	14 LD TSSOP, SOIC package		7		$\mu V/^\circ C$
		16 LD QFN package		2		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 2.5V$		2	50	nA
$R_{IN}$	Input Impedance			1		$G\Omega$
$C_{IN}$	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	For $V_{INx}$ from -0.5V to +5.5V	45	70		dB
$A_{VOL}$	Open Loop Gain	$0.5V \leq V_{OUTx} \leq +4.5V$	75	105		dB
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OL}$	Output Swing Low	$I_L = -2.5mA$		30	150	mV
$V_{OH}$	Output Swing High	$I_L = +2.5mA$	4.85	4.97		V
$I_{SC}$	Short Circuit Current	$V_{CM} = 2.5V$ , Source: $V_{OUTx}$ short to $V_{S-}$ , Sink: $V_{OUTx}$ short to $V_{S+}$		$\pm 125$		mA
$I_{OUT}$	Output Current			$\pm 70$		mA
<b>POWER SUPPLY PERFORMANCE</b>						
$(V_{S+}) - (V_{S-})$	Supply Voltage Range		4.5		19	V
$I_S$	Supply Current (Per Amplifier)	$V_{CM} = 2.5V$ , No load		500	750	$\mu A$
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
<b>DYNAMIC PERFORMANCE</b>						
SR	Slew Rate (Note 5)	$1V \leq V_{OUTx} \leq 4V$ , 20% to 80%		12		$V/\mu s$
$t_s$	Settling to +0.1% (Note 6)	$A_V = +1$ , $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$ , $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ $R_L = 10k\Omega$ , $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ $R_L = 10k\Omega$ , $C_L = 8pF$		50		°
CS	Channel Separation	$f = 5MHz$		75		dB

**Electrical Specifications**  $V_{S+} = +18V$ ,  $V_{S-} = 0V$ ,  $R_L = 10k\Omega$  to  $9V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{OS}$	Input Offset Voltage	$V_{CM} = 9V$		4	15	mV
$TCV_{OS}$	Average Offset Voltage Drift (Note 4)	14 LD TSSOP, SOIC package		7		$\mu V/^\circ C$
		16 LD QFN package		2		$\mu V/^\circ C$
$I_B$	Input Bias Current	$V_{CM} = 9V$		2	50	nA
$R_{IN}$	Input Impedance			1		$G\Omega$
$C_{IN}$	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+18.5	V
CMRR	Common-Mode Rejection Ratio	For $V_{INx}$ from -0.5V to +18.5V	53	78		dB
$A_{VOL}$	Open Loop Gain	$0.5V \leq V_{OUTx} \leq 17.5V$	75	90		dB
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OL}$	Output Swing Low	$I_L = -9mA$		100	150	mV
$V_{OH}$	Output Swing High	$I_L = +9mA$	17.85	17.90		V
$I_{SC}$	Short Circuit Current	$V_{CM} = 9V$ , Source: $V_{OUTx}$ short to $V_{S-}$ , Sink: $V_{OUTx}$ short to $V_{S+}$		$\pm 200$		mA
$I_{OUT}$	Output Current			$\pm 70$		mA
<b>POWER SUPPLY PERFORMANCE</b>						
$(V_{S+}) - (V_{S-})$	Supply Voltage Range		4.5		19	V
$I_S$	Supply Current (Per Amplifier)	$V_{CM} = 9V$ , No load		550	750	$\mu A$
PSRR	Power Supply Rejection Ratio	Supply is moved from 4.5V to 19V	60	75		dB
<b>DYNAMIC PERFORMANCE</b>						
SR	Slew Rate (Note 5)	$1V \leq V_{OUTx} \leq 17V$ , 20% to 80%		12		$V/\mu s$
$t_s$	Settling to +0.1% (Note 6)	$A_V = +1$ , $V_{OUTx} = 2V$ step, $R_L = 10k\Omega$ , $C_L = 8pF$		500		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$ , $C_L = 8pF$		12		MHz
GBWP	Gain-Bandwidth Product	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ , $R_L = 10k\Omega$ , $C_L = 8pF$		8		MHz
PM	Phase Margin	$A_V = -50$ , $R_F = 5k\Omega$ , $R_G = 100\Omega$ , $R_L = 10k\Omega$ , $C_L = 8pF$		50		$^\circ$
CS	Channel Separation	$f = 5MHz$		75		dB

## NOTES:

- Measured over  $-40^\circ C$  to  $+85^\circ C$  ambient operating temperature range. See the typical  $TCV_{OS}$  production distribution shown in the "Typical Performance Curves" on page 6
- Typical slew rate is an average of the slew rates measured on the rising (20%-80%) and the falling (80%-20%) edges of the output signal.
- Settling time measured as the time from when the output level crosses the final value on rising/falling edge to when the output level settles within a  $\pm 0.1\%$  error band. The range of the error band is determined by: Final Value(V)  $\pm$  [Full Scale(V) \* 0.1%]

### Typical Performance Curves

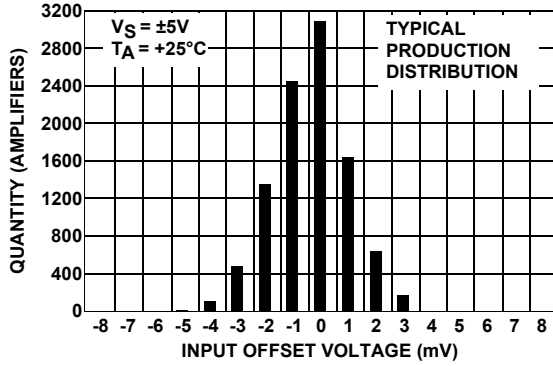


FIGURE 1. INPUT OFFSET VOLTAGE DISTRIBUTION

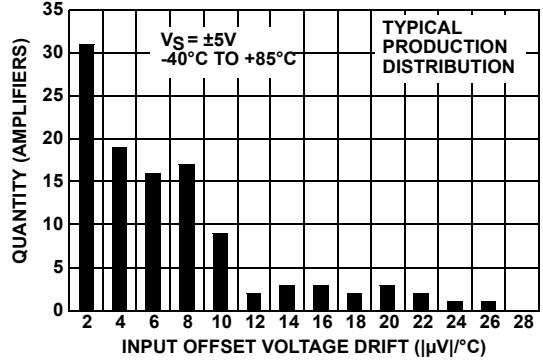


FIGURE 2. INPUT OFFSET VOLTAGE DRIFT (TSSOP, SOIC)

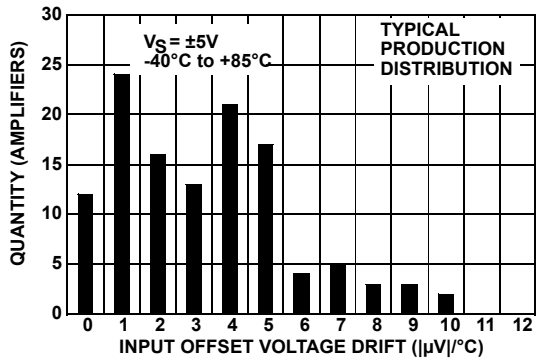


FIGURE 3. INPUT OFFSET VOLTAGE DRIFT (QFN)

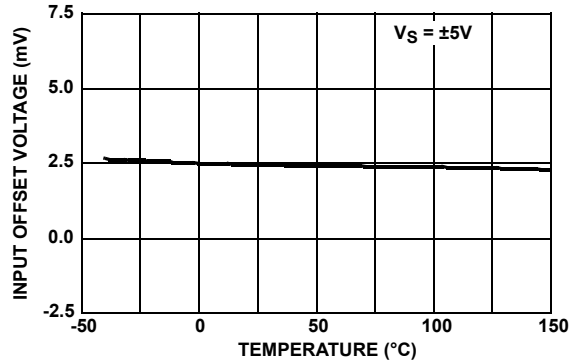


FIGURE 4. INPUT OFFSET VOLTAGE vs TEMPERATURE

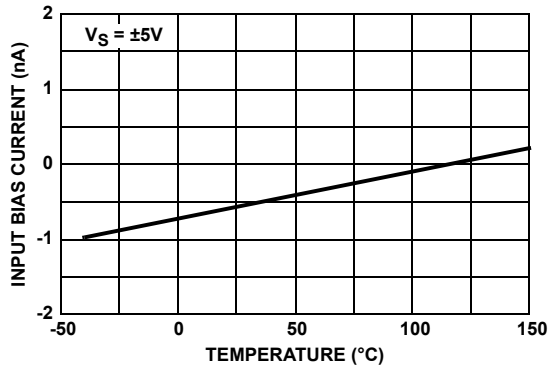


FIGURE 5. INPUT BIAS CURRENT vs TEMPERATURE

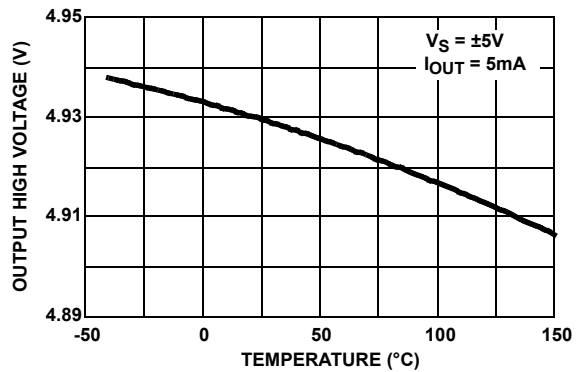


FIGURE 6. OUTPUT HIGH VOLTAGE vs TEMPERATURE

**Typical Performance Curves** (Continued)

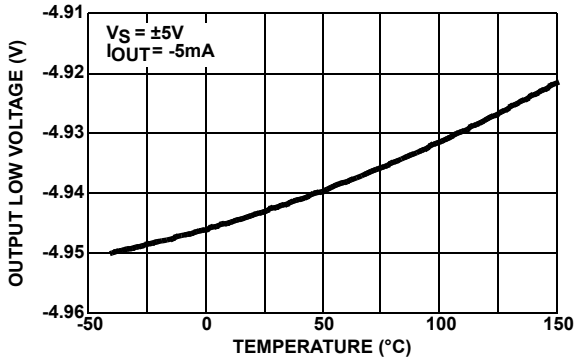


FIGURE 7. OUTPUT LOW VOLTAGE vs TEMPERATURE

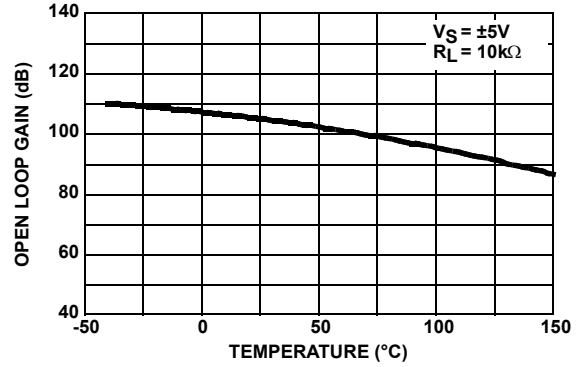


FIGURE 8. OPEN-LOOP GAIN vs TEMPERATURE

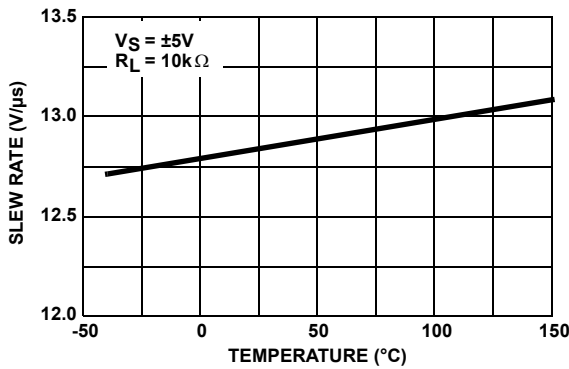


FIGURE 9. SLEW RATE vs TEMPERATURE

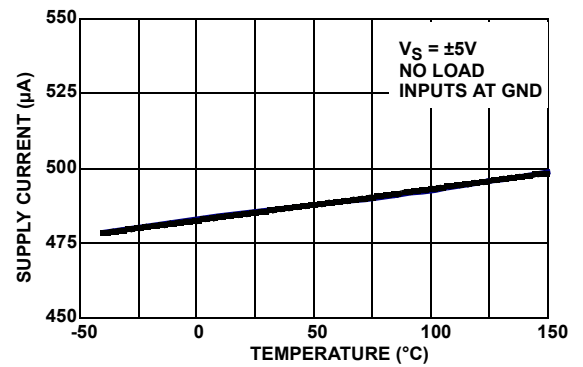


FIGURE 10. SUPPLY CURRENT PER AMPLIFIER vs TEMPERATURE

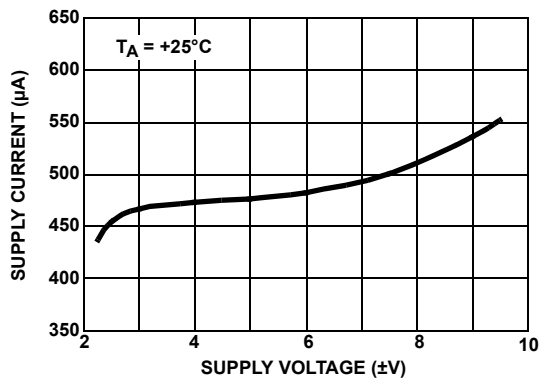


FIGURE 11. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

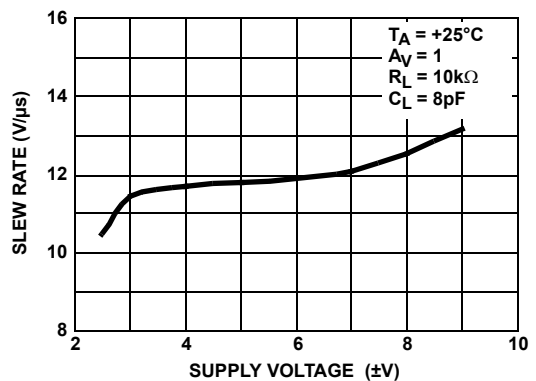


FIGURE 12. SLEW RATE vs SUPPLY VOLTAGE

**Typical Performance Curves** (Continued)

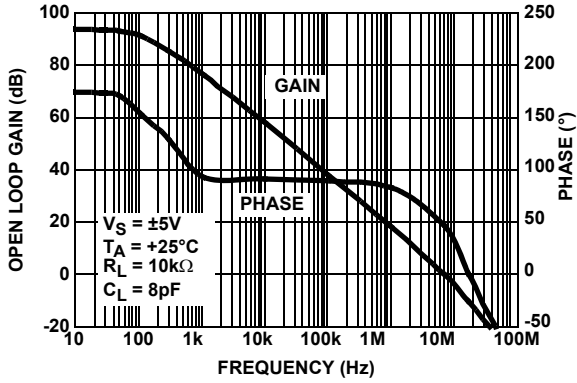


FIGURE 13. OPEN LOOP GAIN AND PHASE vs FREQUENCY

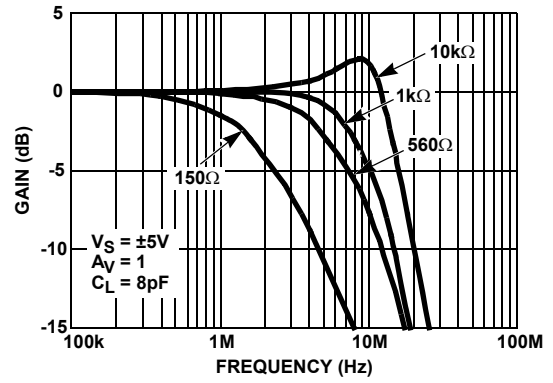


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS  $R_L$

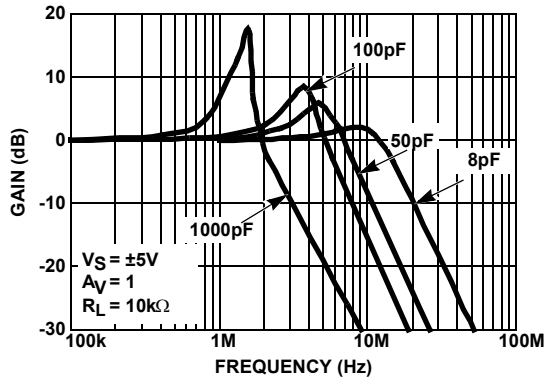


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS  $C_L$

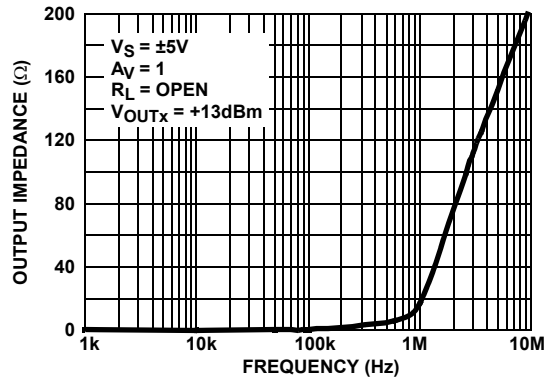


FIGURE 16. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

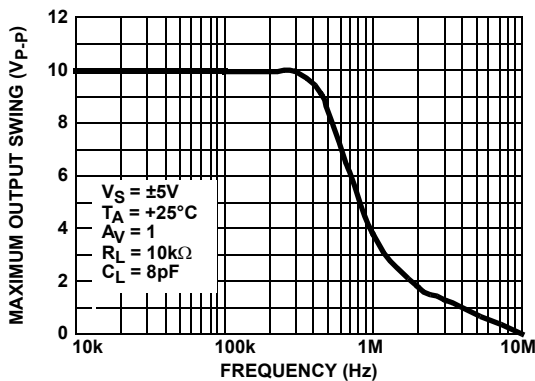


FIGURE 17. MAXIMUM OUTPUT SWING vs FREQUENCY

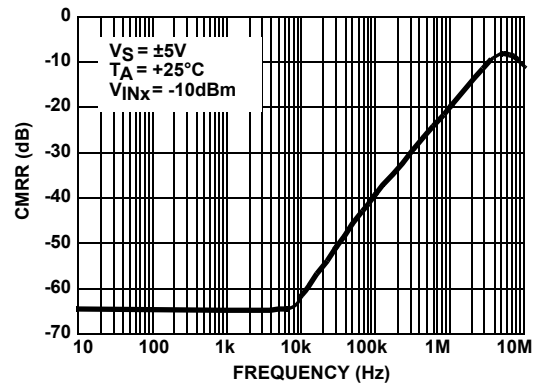


FIGURE 18. CMRR vs FREQUENCY



**Typical Performance Curves** (Continued)

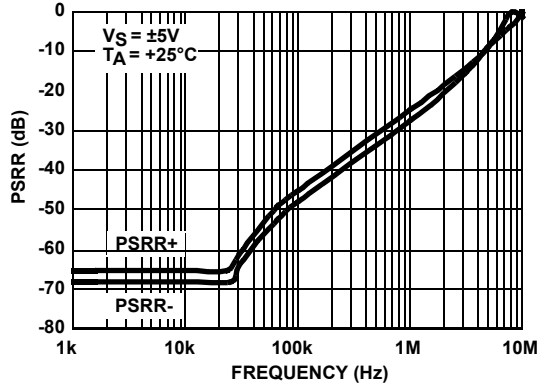


FIGURE 19. PSRR vs FREQUENCY

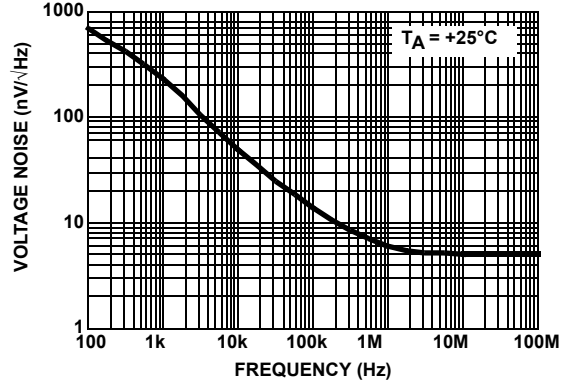


FIGURE 20. INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

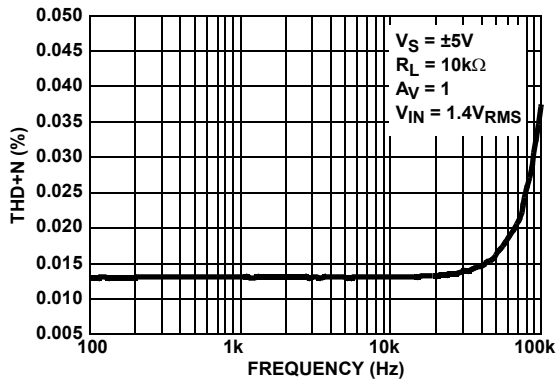


FIGURE 21. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

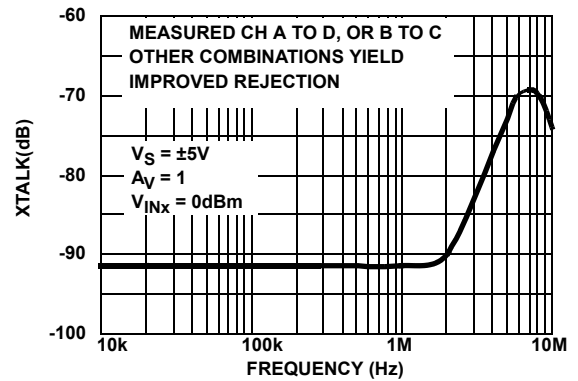


FIGURE 22. CHANNEL SEPARATION vs FREQUENCY RESPONSE

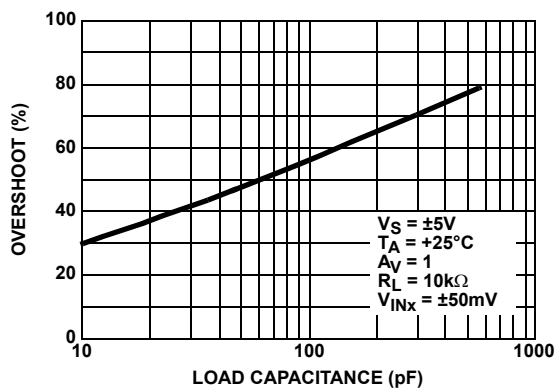


FIGURE 23. SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

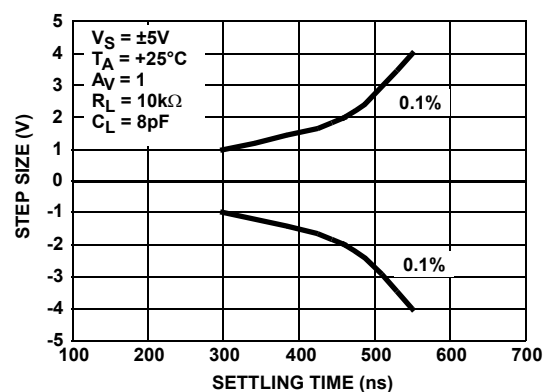


FIGURE 24. STEP SIZE vs SETTLING TIME

**Typical Performance Curves** (Continued)

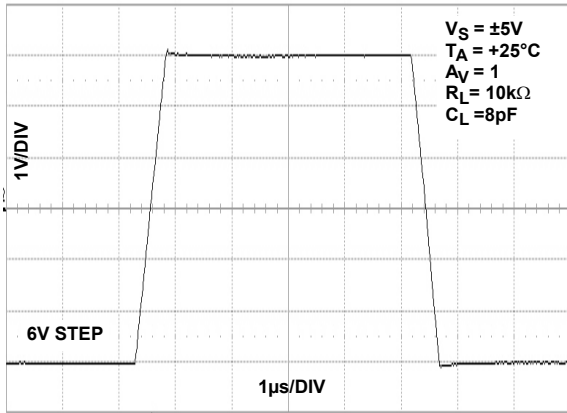


FIGURE 25. LARGE SIGNAL TRANSIENT RESPONSE

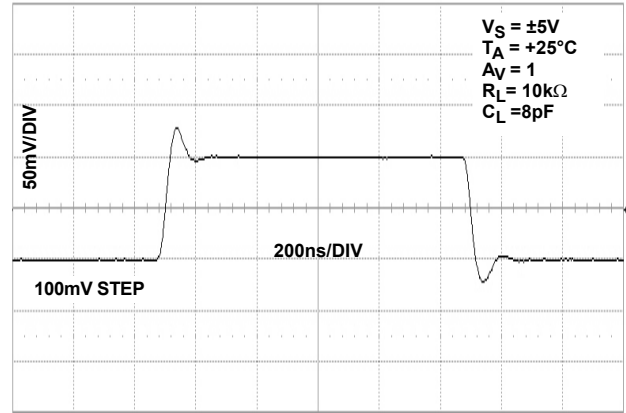


FIGURE 26. SMALL SIGNAL TRANSIENT RESPONSE

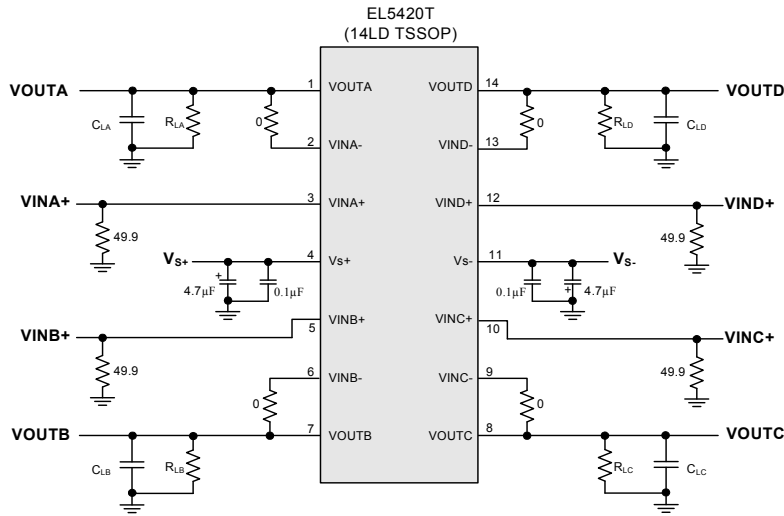


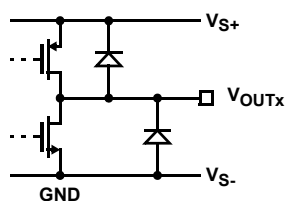
FIGURE 27. BASIC TEST CIRCUIT

**Pin Descriptions**

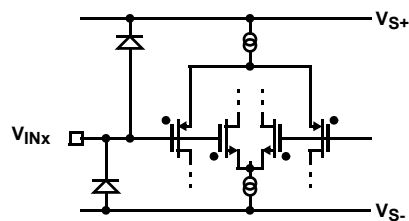
EL5420T		PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
14 LD TSSOP, 14 LD SOIC	16 LD QFN			
1	15	VOUTA	Amplifier A Output	(Reference Circuit 1)
2	1	VINA-	Amplifier A Inverting Input	(Reference Circuit 2)
3	2	VINA+	Amplifier A Non-Inverting Input	(Reference Circuit 2)
4	3	VS+	Positive Power Supply	
5	4	VINB+	Amplifier B Non-Inverting Input	(Reference Circuit 2)
6	5	VINB-	Amplifier B Inverting Input	(Reference Circuit 2)
7	6	VOUTB	Amplifier B Output	(Reference Circuit 1)
8	7	VOUTC	Amplifier C Output	(Reference Circuit 1)
9	8	VINC-	Amplifier C Inverting Input	(Reference Circuit 2)

**Pin Descriptions** (Continued)

EL5420T		PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
14 LD TSSOP, 14 LD SOIC	16 LD QFN			
10	9	VINC+	Amplifier C Non-Inverting Input	(Reference Circuit 2)
11	10	VS-	Negative Power Supply	
12	11	VIND+	Amplifier D Non-Inverting Input	(Reference Circuit 2)
13	12	VIND-	Amplifier D Inverting Input	(Reference Circuit 2)
14	14	VOUTD	Amplifier D Output	(Reference Circuit 1)
	13, 16	NC	No Connect	
	pad	Thermal Pad	Functions as a heat sink. Connects to most negative potential, VS-	



CIRCUIT 1



CIRCUIT 2

## Applications Information

### Product Description

The EL5420T is a high voltage rail-to-rail input-output amplifier with low power consumption. The EL5420T contains four amplifiers. Each amplifier exhibits beyond the rail input capability, rail-to-rail output capability, and is unity gain stable.

The EL5420T features a slew rate of  $12\text{V}/\mu\text{s}$ . Also, the device provides common mode input capability beyond the supply rails, rail-to-rail output capability, and a bandwidth of  $12\text{MHz}$  ( $-3\text{dB}$ ). This enables the amplifiers to offer maximum dynamic range at any supply voltage.

### Operating Voltage, Input and Output Capability

The EL5420T can operate on a single supply or dual supply configuration. The EL5420T operating voltage ranges from a minimum of  $4.5\text{V}$  to a maximum of  $19\text{V}$ . This range allows for a standard  $5\text{V}$  (or  $\pm 2.5\text{V}$ ) supply voltage to dip to  $-10\%$ , or a standard  $18\text{V}$  (or  $\pm 9\text{V}$ ) to rise by  $+5.5\%$  without affecting performance or reliability.

The input common-mode voltage range of the EL5420T extends  $500\text{mV}$  beyond the supply rails. Also, the EL5420T is immune to phase reversal. However, if the common mode input voltage exceeds the supply voltage by more than  $0.5\text{V}$ , electrostatic protection diodes in the input stage of the device begin to conduct. Even though phase reversal will not occur, to maintain optimal reliability it is suggested to avoid input overvoltage conditions. Figure 28 shows the input voltage driven  $500\text{mV}$  beyond the supply rails and the device output swinging between the supply rails.

The EL5420T output typically swings to within  $50\text{mV}$  of positive and negative supply rails with load currents of  $\pm 5\text{mA}$ . Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 29 shows the input and output waveforms for the device in a unity-gain configuration. Operation is from  $\pm 5\text{V}$  supply with a  $10\text{k}\Omega$  load connected to GND. The input is a  $10\text{V}_{\text{P-P}}$  sinusoid and the output voltage is approximately  $9.9\text{V}_{\text{P-P}}$ .

Refer to the “Electrical Specifications” Table beginning on page 3 for specific device parameters. Parameter variations with operating voltage, loading and/or temperature are shown in the “Typical Performance Curves” on page 6.

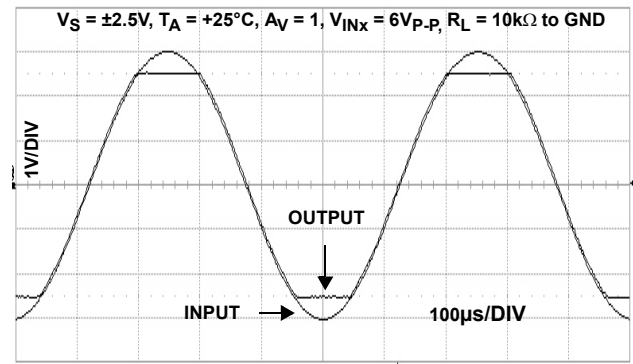


FIGURE 28. OPERATION WITH BEYOND-THE-RAILS INPUT

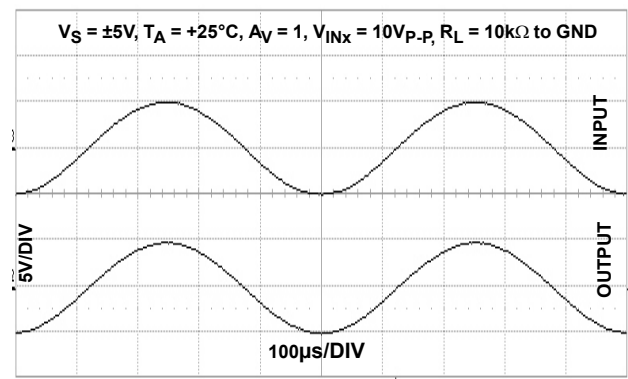


FIGURE 29. OPERATION WITH RAIL-TO-RAIL INPUT AND

### Output Current

The EL5420T is capable of output short circuit currents of  $200\text{mA}$  (source and sink), and the device has built-in protection circuitry which limits the short circuit current to  $\pm 200\text{mA}$  (typical).

To maintain maximum reliability the continuous output current should never exceed  $\pm 70\text{mA}$ . This  $\pm 70\text{mA}$  limit is determined by the characteristics of the internal metal interconnects. Also, see “Power Dissipation” on page 13 for detailed information on ensuring proper device operation and reliability for temperature and load conditions.

### Unused Amplifiers

It is recommended that any unused amplifiers be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground.

### Thermal Shutdown

The EL5420T has a built-in thermal protection which ensures safe operation and prevents internal damage to the device due to overheating. When the die temperature reaches  $+165^\circ\text{C}$  (typical) the device automatically shuts OFF the outputs by putting them in a high impedance state. When the die cools by  $15^\circ\text{C}$  (typical) the device automatically turns

ON the outputs by putting them in a low impedance (normal) operating state.

**Driving Capacitive Loads**

As load capacitance increases, the -3dB bandwidth will decrease and peaking can occur. Depending on the application, it may be necessary to reduce peaking and to improve device stability. To improve device stability a snubber circuit or a series resistor may be added to the output of the EL5420T.

A snubber is a shunt load consisting of a resistor in series with a capacitor. An optimized snubber can improve the phase margin and the stability of the EL5420T. The advantage of a snubber circuit is that it does not draw any DC load current or reduce the gain.

Another method to reduce peaking is to add a series output resistor (typically between 1Ω to 10Ω). Depending on the capacitive loading, a small value resistor may be the most appropriate choice to minimize any reduction in gain.

**Power Dissipation**

With the high-output drive capability of the EL5420T amplifiers, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. It is important to calculate the maximum power dissipation of the EL5420T in the application. Proper load conditions will ensure that the EL5420T junction temperature stays within a safe operating region.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \tag{EQ. 1}$$

where:

- $T_{JMAX}$  = Maximum junction temperature
- $T_{AMAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $P_{DMAX}$  = Maximum power dissipation allowed

The total power dissipation produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power dissipation in the IC due to the loads, or:

$$P_{DMAX} = \sum i[V_S \times I_{SMAX} + (V_{S+} - V_{OUT}^i) \times I_{LOAD}^i] \tag{EQ. 2}$$

when sourcing, and:

$$P_{DMAX} = \sum i[V_S \times I_{SMAX} + (V_{OUT}^i - V_{S-}) \times I_{LOAD}^i] \tag{EQ. 3}$$

when sinking,

where:

- $i = 1$  to 4  
(1, 2, 3, 4 corresponds to Channel A, B, C, D respectively)
- $V_S$  = Total supply voltage ( $V_{S+} - V_{S-}$ )
- $V_{S+}$  = Positive supply voltage
- $V_{S-}$  = Negative supply voltage
- $I_{SMAX}$  = Maximum supply current per amplifier  
( $I_{SMAX} = \text{EL5420T quiescent current} \div 4$ )
- $V_{OUT}$  = Output voltage
- $I_{LOAD}$  = Load current

Device overheating can be avoided by calculating the minimum resistive load condition,  $R_{LOAD}$ , resulting in the highest power dissipation. To find  $R_{LOAD}$  set the two  $P_{DMAX}$  equations equal to each other and solve for  $V_{OUT}/I_{LOAD}$ . Reference the package power dissipation curves, Figures 30 and 31, for further information.

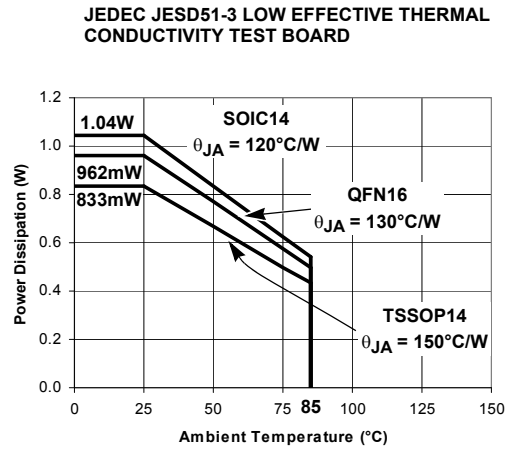


FIGURE 30. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

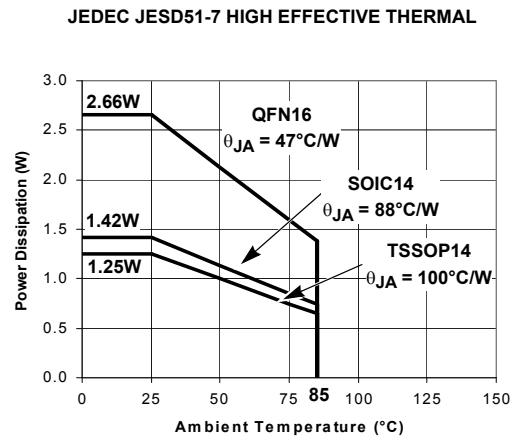


FIGURE 31. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

### **Power Supply Bypassing and Printed Circuit Board Layout**

The EL5420T can provide gain at high frequency, so good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, trace lengths should be as short as possible and the power supply pins must be well bypassed to reduce any risk of oscillation.

For normal single supply operation (the  $V_{S-}$  pin is connected to ground) a 4.7 $\mu$ F capacitor should be placed from  $V_{S+}$  to ground, then a parallel 0.1 $\mu$ F capacitor should be connected as

close to the amplifier as possible. One 4.7 $\mu$ F capacitor may be used for multiple devices. For dual supply operation the same capacitor combination should be placed at each supply pin to ground.

For the QFN package, with exposed thermal pad, the pad should be connected to the lowest potential,  $V_{S-}$ , to optimize thermal and operating performance. PCB vias should be placed below the device's exposed thermal pad to transfer heat to the  $V_{S-}$  plane and away from the device.

### **Revision History**

DATE	REVISION	CHANGE
September 8, 2015	FN6838.1	Updated Ordering Information Table on page 1. Added About Intersil section.
September 25, 2009	FN6838.0	Initial Release

### **About Intersil**

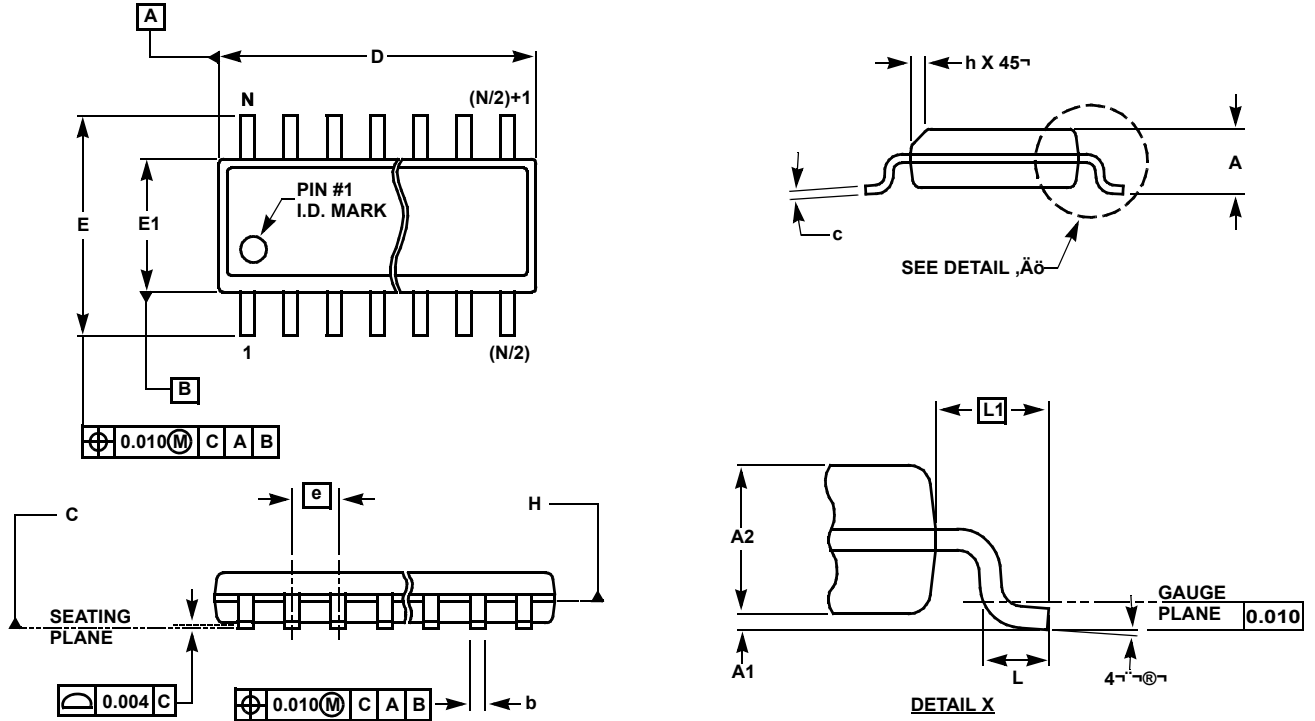
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**Small Outline Package Family (SO)**



**MDP0027**

**SMALL OUTLINE PACKAGE FAMILY (SO)**

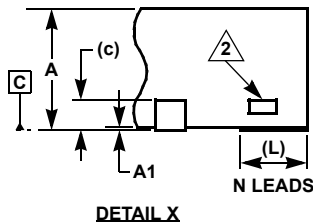
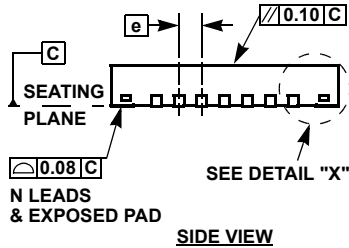
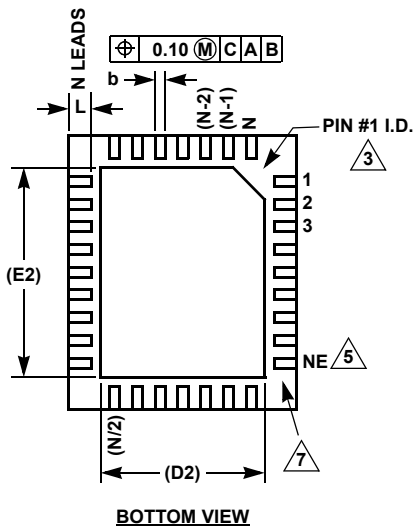
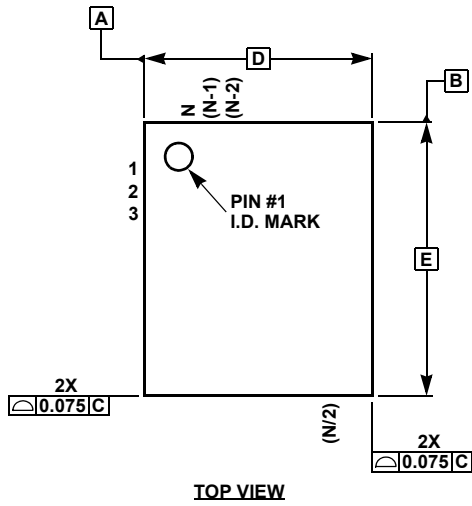
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**QFN (Quad Flat No-Lead) Package Family**



**MDP0046**

**QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY  
(COMPLIANT TO JEDEC MO-220)**

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLERANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

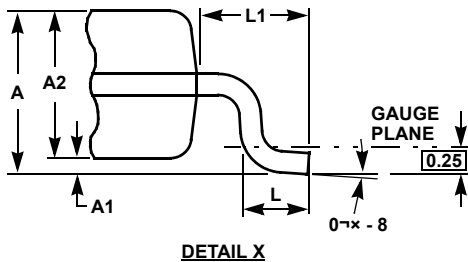
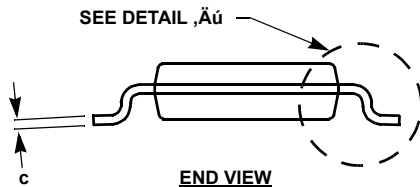
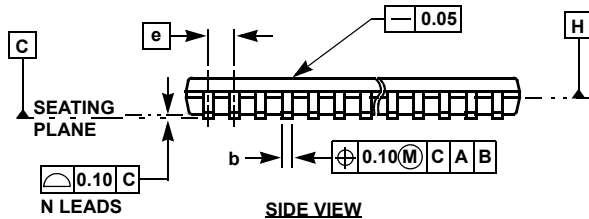
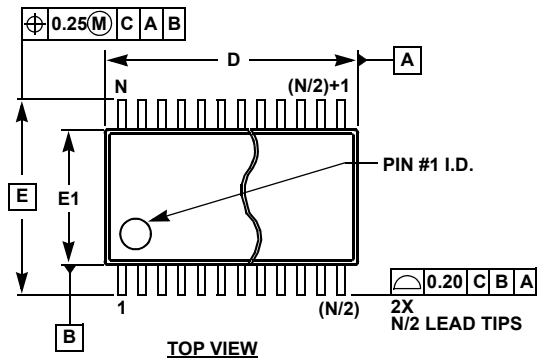
Rev 11 2/07

**NOTES:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y-direction).
6. ND is the number of terminals on the "D" side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.



**Thin Shrink Small Outline Package Family (TSSOP)**



**MDP0044**

**THIN SHRINK SMALL OUTLINE PACKAGE FAMILY**

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

**NOTES:**

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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