

## Description

The F0452C is an integrated dual-path RF front-end consisting of an RF switch and two gain stages with 6dB gain control used in the analog front-end receiver of an Active Antenna System (AAS). The F0452C supports frequencies from 2.3GHz to 2.7GHz.

The F0452C provides 34dB gain with +23dBm OIP3, +15dBm output P1dB, and 1.6dB noise figure (NF) at 2.6GHz. Gain is reduced 6dB in a single step with a maximum gain settling time of 31ns. The device uses a single 3.3V supply and 130mA of  $I_{DD}$ .

The F0452C is offered in a  $6 \times 6 \times 0.75$  mm, 32-pin LGA package with  $50\Omega$  input and output amplifier impedances for ease of integration into the signal path.

## Competitive Advantage

- High integration
- Low noise and high linearity
- On-chip matching and bias
- Extremely low current consumption

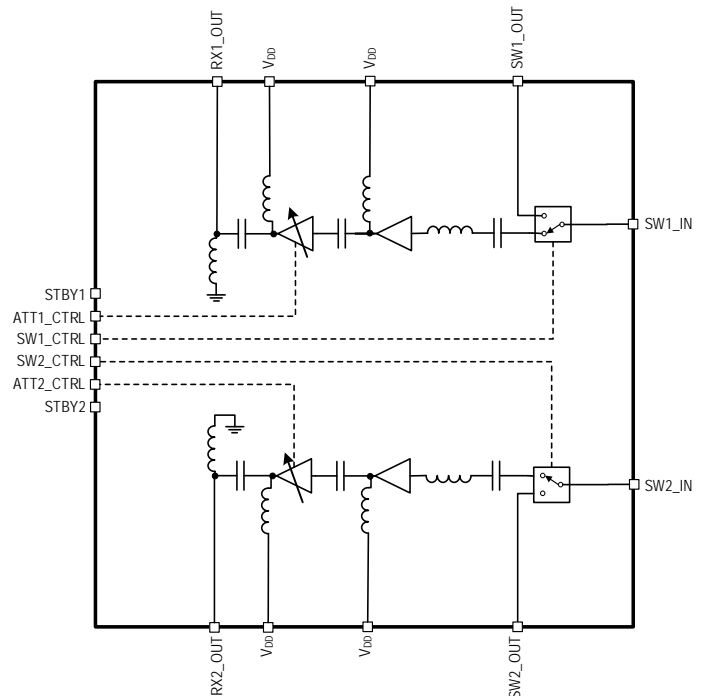
## Typical Applications

- Multi-mode, multi-carrier receivers
- AAS Rx Front-End
- 4.5G (LTE Advanced)
- 5G NR band n40 and n41

## Features

- Gain at 2.6GHz
  - 34dB typical in High Gain Mode
  - 28dB typical in Low Gain Mode
- 1.6dB NF at 2.6GHz
- +23dBm OIP3 at 2.6GHz
- OP1dB at 2.6GHz
  - +15dBm in High Gain Mode
  - +14dBm in Low Gain Mode
- $50\Omega$  single-ended input / output amplifier impedances
- $I_{DD} = 130\text{mA}$
- Independent Standby Mode for power savings
- Supply voltage: +3.15V to +3.45V
- $6 \times 6$  mm, 32-LGA package
- $-40^\circ\text{C}$  to  $+105^\circ\text{C}$  exposed pad operating temperature range

## Block Diagram



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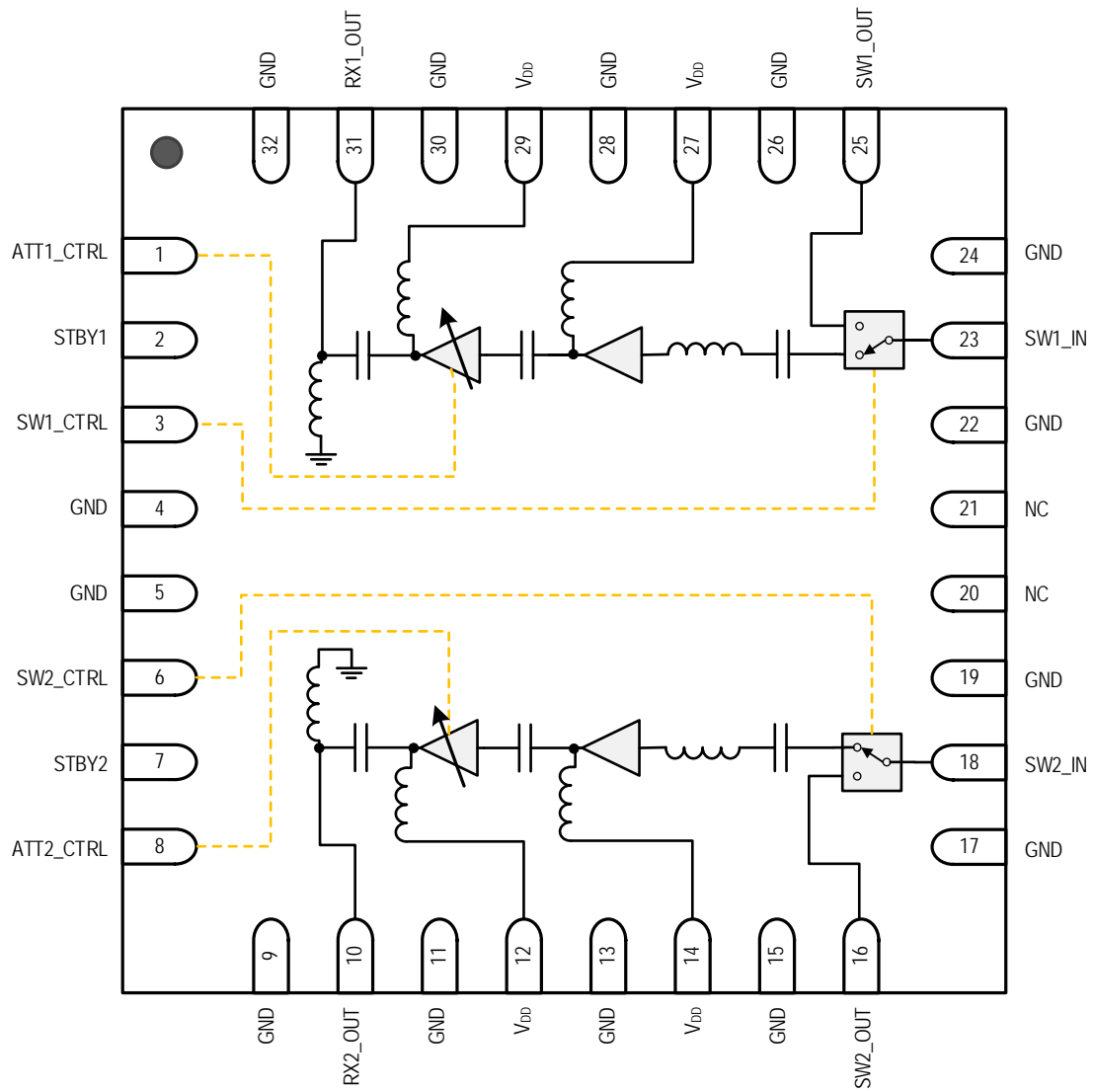
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# Pin Assignments

Figure 1. Pin Assignments for 6 × 6 × 0.75 mm 32-LGA – Top View



## Pin Descriptions

Table 1. Pin Descriptions

| Number  | Name      | Description  |
|---|-----------|--|
| 1   | ATT1_CTRL | 1-bit 6dB gain control for path 1. (Low /open = no attenuation; High = 6dB attenuation). A 500kΩ pull-down resistor is connected between this input and GND.   |
| 2   | STBY1     | Standby (Low/open = path 1 power ON; High = path 1 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.   |
| 3   | SW1_CTRL  | RF SWITCH 1 control (Low /open = select main RX PATH 1; High = switch output). SW1_CTRL also puts path 1 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.  |
| 4, 5, 9, 11, 13, 15, 17, 19, 22, 24, 26, 28, 30, 32 | GND       | Ground these pins.   |
| 6   | SW2_CTRL  | RF SWITCH 2 control (Low /open = select main RX PATH 2; High = switch output). SW2_CTRL also puts path 2 into Standby Mode for minimum current consumption. A 500kΩ pull-down resistor is connected between this input and GND.  |
| 7   | STBY2     | Standby (Low /open = path 2 power ON; High = path 2 power OFF). A 500kΩ pull-down resistor is connected between this input and GND.  |
| 8   | ATT2_CTRL | 1-bit 6dB gain control for path 2. (Low /open = no attenuation; High = 6dB attenuation). A 500kΩ pull-down resistor connects between this input and GND.   |
| 10  | RX2_OUT   | RF output path 2 matched to 50Ω. Use external DC block as close to the pin as possible.  |
| 12, 14, 27, 29                                      | VDD       | Power supply. Bypass to GND with capacitors shown in the F0452C Application Circuit as close as possible to the pins.  |
| 16  | SW2_OUT   | RF2 switch output matched to 50Ω. Use external 50Ω terminating resistor with proper power rating as required for the application.  |
| 18  | SW2_IN    | RF2 switch input matched to 50Ω. Use an external DC block as close to the pin as possible.   |
| 23  | SW1_IN    | RF1 switch input matched to 50Ω. Use an external DC block as close to the pin as possible.   |
| 25  | SW1_OUT   | RF1 switch output matched to 50Ω. Use an external 50Ω terminating resistor with proper power rating as required for the application.   |
| 31  | RX1_OUT   | RF output path 1 matched to 50Ω. Use an external DC block as close to the pin as possible.   |
| 20, 21  | NC        | These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.  |
| —   | EPAD      | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance. |

## Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter   | Symbol              | Minimum | Maximum                | Units |
|---|---------------------|---------|------------------------|-------|
| V <sub>DD</sub> to GND  | V <sub>DD</sub>     | -0.3    | +3.6                   | V     |
| STBY1, STBY2, ATT1_CTRL, ATT2_CTRL, SW1_CTRL, SW2_CTRL to GND   | V <sub>CTRL</sub>   | -0.3    | V <sub>DD</sub> + 0.25 | V     |
| SW1_IN, SW2_IN, RX1_OUT, RX2_OUT, SW1_OUT, SW2_OUT to GND<br>Externally Applied DC Voltage  | V <sub>SW</sub>     | -50     | 50                     | mV    |
| TX Mode CW Average Input Power +7.5dB PAR at SW1_IN, SW2_IN Ports,<br>10s, 89% Duty Cycle<br>50Ω, T <sub>EPAD</sub> = 105°C [a], V <sub>DD</sub> = +3.3V              | P <sub>ABS_TX</sub> | +31     | +33 [b]                | dBm   |
| RX Mode Average Input Power +7.5dB PAR at SW1_IN, SW2_IN Ports,<br>1 Hour Single Event, 50% Duty Cycle<br>50Ω, T <sub>EPAD</sub> = 105°C [a], V <sub>DD</sub> = +3.3V | P <sub>ABS_RX</sub> |         | +8                     | dBm   |
| Storage Temperature Range   | T <sub>ST</sub>     | -65     | +150                   | °C    |
| Lead Temperature (soldering, 10s)   | T <sub>LEAD</sub>   |         | +260                   | °C    |
| Electrostatic Discharge – HBM<br>(JEDEC/ESDA JS-001-2012)   | V <sub>ESDHBM</sub> |         | 1500<br>(Class 1C)     | V     |
| Electrostatic Discharge – CDM<br>(JEDEC JS-002-2014)<br>ALL pins except pins 16, 18, 23, 25   | V <sub>ESDCDM</sub> |         | 500<br>(Class C2A)     | V     |
| Electrostatic Discharge – CDM<br>(JEDEC JS-002-2014)<br>Pins 16, 18, 23, 25   | V <sub>ESDCDM</sub> |         | 125<br>(Class C0B)     | V     |

[a] T<sub>EPAD</sub> = temperature of the exposed paddle.

[b] RF input exposures greater than +31dBm and up to +33dBm for multiple extended periods will affect device reliability and lifetime if the maximum recommended input junction temperature is exceeded.

## Recommended Operating Conditions

Table 3. Recommended Operating Conditions

| Parameter  | Symbol        | Condition      | Minimum | Typical | Maximum            | Units |
|--|---------------|----------------|---------|---------|--------------------|-------|
| Power Supply Voltage   | $V_{DD}$      |                | 3.15    | 3.3     | 3.45               | V     |
| Operating Temperature Range  | $T_{EPAD}$    | Exposed Paddle | -40     |         | +105               | °C    |
| RF Frequency Range   | $f_{RF}$      |                | 2.3     |         | 2.7                | GHz   |
| TX Mode CW Average Input Power, +7.5dB PAR, Full Life Time <sup>[a]</sup><br>50Ω, $V_{DD} = +3.3V$ | $P_{MAX\_TX}$ | 89% Duty Cycle |         |         | +30 <sup>[b]</sup> | dBm   |
| RX Mode CW Average Input Power, +7.5dB PAR, Full Life Time <sup>[a]</sup><br>50Ω, $V_{DD} = +3.3V$ | $P_{MAX\_RX}$ | 89% Duty Cycle |         |         | -25                | dBm   |
| Port Impedance (SW1_IN, SW2_IN, RX1_OUT, RX2_OUT)  | $Z_{RF}$      |                |         | 50      |                    | Ω     |
| Junction Temperature   | $T_J$         |                |         |         | +125               | °C    |

[a] Assumes device environmental temperature cycling within the specified exposed pad operating temperature range of -40°C and 105°C and a maximum junction temperature of 125°C.

[b] Operation beyond the maximum recommended operating input power level should be limited and have reduced exposed pad temperatures to maintain device reliability per foundry guidelines. Electrical characteristics and lifetime are not guaranteed for RF input power levels beyond what is specified in this table.

## Electrical Characteristics

Table 4. Electrical Characteristics

See F0452C Application Circuit. Specifications apply when operated as an RX RF amplifier with  $V_{DD} = +3.3V$ ,  $T_{EPAD} = +25^{\circ}C$ ,  $STBYX = Low$ , RX output power = -10dBm,  $Z_S = Z_L = 50\Omega$ , and EVKit trace and connector losses are de-embedded unless otherwise noted.

| Parameter                                    | Symbol            | Condition   | Minimum                    | Typical   | Maximum                    | Units   |
|--|-------------------|---|----------------------------|-----------|----------------------------|---------|
| Logic Input High Threshold                   | $V_{IH}$          |   | <b>1.17</b> <sup>[a]</sup> |           | Lower of ( $V_{DD}$ , 3.3) | V       |
| Logic Input Low Threshold                    | $V_{IL}$          |   | -0.3                       |           | <b>0.55</b>                | V       |
| Logic Current                                | $I_{IH}, I_{IL}$  | For each control pin  | <b>-10</b>                 |           | <b>10</b>                  | $\mu A$ |
| DC Current                                   | $I_{DD}$          | 2 paths in RX Mode  |                            | 130       | <b>180</b>                 | mA      |
|  |                   | 1 path in RX Mode<br>1 path in TX Mode  |                            | 70        | <b>100</b>                 |         |
|  |                   | 1 path in RX Mode<br>1 path in Standby Mode   |                            | 67        |                            |         |
|  |                   | 1 path in TX Mode<br>1 path in Standby Mode   |                            | 5         |                            |         |
|  |                   | 2 paths in Standby Mode   |                            | 5         |                            |         |
| Gain Step                                    | $G_{STEP}$        |   |                            | 6         |                            | dB      |
| Gain Step Absolute Error                     | $G_{STEP\_ERR}$   | Relative to maximum gain, over-voltage, and temperature   |                            | $\pm 0.5$ |                            | dB      |
| Relative Phase Gain Step                     | $G_{STEP\_PH}$    |   |                            | 28        |                            | deg     |
| Gain Step Settling Time <sup>[b]</sup>       | $G_{STEP\_SET}$   | 50% control logic to RF output within $\pm 0.1$ dB of final value                                       |                            | 20        | 31                         | ns      |
| Gain Step Phase Settling Time <sup>[b]</sup> | $G_{STEP\_PHSET}$ | 50% control logic to RF output within $\pm 1$ degree of final value                                     |                            | 16        | 30                         | ns      |
| Power ON Switching Time <sup>[b]</sup>       | $SW_{ON}$         | To RX Mode from TX Mode<br>50% control logic to RF output settled to within $\pm 0.1$ dB of final value |                            |           | 1                          | $\mu s$ |
| Power OFF Switching Time <sup>[b]</sup>      | $SW_{OFF}$        | To TX Mode from RX Mode<br>50% control logic to RF input settled within $\pm 0.1$ dB of final value     |                            |           | 0.5                        | $\mu s$ |



| Parameter                                 | Symbol              | Condition   | Minimum | Typical | Maximum | Units   |
|---|---------------------|---|---------|---------|---------|---------|
| Power ON from Standby Mode <sup>[b]</sup> | $SW_{ON\_STANDBY}$  | To RX Mode from Standby Mode<br>50% STBYx to RF output settled within $\pm 0.1$ dB of final value |         |         | 1       | $\mu$ s |
| Power OFF to Standby Mode <sup>[b]</sup>  | $SW_{OFF\_STANDBY}$ | To Standby Mode from RX Mode<br>50% STBYx to gain below -25dB from maximum gain                   |         |         | 1       | $\mu$ s |

[a] Items in the "Minimum"/"Maximum" columns in ***bold italics*** are confirmed by test. Items in the "Minimum"/"Maximum" columns not in bold italics are confirmed by design characterization.

[b]  $f_{RF} = 2.6$ GHz. Assumes the control signal is clean and no external RC circuitry is required on the pin. Adding RC circuitry increases switching time. Timing tests performed with a control logic signal of +3.3V and a rise/fall time  $\leq 30$ ns.

Table 5. Electrical Characteristics – RX Path in RX Mode Cascaded Performance  
 See the F0452C Application Circuit. Specifications apply when operated as an RX RF amplifier with  $V_{DD} = +3.3V$ ,  $f_{RF} = 2.6GHz$ ,  $T_{EPAD} = +25^{\circ}C$ ,  $STBYx = Low$ , RX output power =  $-10dBm$ ,  $Z_S = Z_L = 50\Omega$ , and EVKit trace and connector losses are de-embedded unless otherwise noted.

| Parameter  | Symbol               | Condition   | Minimum   | Typical           | Maximum   | Units |
|--|----------------------|---|-----------|-------------------|-----------|-------|
| Input Return Loss  | RL <sub>IN</sub>     | Measured at SW1_IN, SW2_IN, High/Low Gain Mode, $f_{RF} = 2.4GHz$   |           | 16 <sup>[a]</sup> |           | dB    |
|  |                      | Measured at SW1_IN, SW2_IN, High/Low Gain Mode, $f_{RF} = 2.6GHz$   |           | 20                |           |       |
|  |                      | Measured at SW1_IN, SW2_IN, High/Low Gain Mode, $f_{RF} = 2.3GHz$ to $2.7GHz$   | 6         |                   |           |       |
| Output Return Loss   | RL <sub>OUT</sub>    | Measured at RX1_OUT, RX2_OUT, High/Low Gain Modes, $f_{RF} = 2.3GHz$ to $2.7GHz$  | 7         |                   |           | dB    |
| Reverse Isolation, RX1_OUT to SW1_IN, or RX2_OUT to SW2_IN | ISO <sub>REV</sub>   | $f_{RF} = 2.3GHz$ to $2.7GHz$   | 50        | 58                |           | dB    |
| Gain   | G <sub>HG</sub>      | High Gain Mode  | <b>32</b> | 34                | <b>37</b> | dB    |
|  | G <sub>HG_TEMP</sub> | $T_{EPAD} = -40^{\circ}C$ to $105^{\circ}C$   | 31        |                   | 38        |       |
| Gain Attenuated  | G <sub>LG</sub>      | Low Gain Mode   | 25.5      | 28                | 31.5      | dB    |
| Gain Ripple  | G <sub>RIPPLE</sub>  | $f_{RF} = 2.3GHz$ to $2.7GHz$<br>(Difference between maximum and minimum gain in each 100MHz subrange within the specified frequency range) |           | $\pm 0.75$        |           | dB    |
| Noise Figure   | NF                   | Measured at antenna port ideally matched to LNA   |           | 1.6               | 1.7       | dB    |
|  |                      | $T_{EPAD} = 105^{\circ}C$   |           |                   | 2.3       |       |
|  |                      | Low Gain Mode   |           | 1.5               |           |       |

[a] Items in the "Minimum"/"Maximum" columns in **bold italics** are confirmed by test. Items in the "Minimum"/"Maximum" columns NOT in bold italics are confirmed by design characterization.

Table 6. Electrical Characteristics – RX Path in RX Mode Cascaded Performance and TX Performance  
 See the F0452C Application Circuit. Specifications apply when operated as an RX RF amplifier with  $V_{DD} = +3.3V$ ,  $f_{RF} = 2.6GHz$ ,  $T_{EPAD} = +25^{\circ}C$ ,  $STBYx = Low$ , RX output power =  $-10dBm$ ,  $Z_S = Z_L = 50\Omega$ , and EVKit trace and connector losses are de-embedded unless otherwise noted.

| Parameter                          | Symbol             | Condition  | Minimum | Typical           | Maximum | Units |
|------------------------------------|--------------------|--|---------|-------------------|---------|-------|
| Output Third-Order Intercept Point | OIP3 <sub>1</sub>  | Pout = 0dBm/tone<br>5MHz tone separation   |         | 23 <sup>[a]</sup> |         | dBm   |
|                                    | OIP3 <sub>2</sub>  | Pout = 0dBm/tone<br>5MHz tone separation<br>$T_{EPAD} = -40^{\circ}C$ to $105^{\circ}C$  | 20      |                   |         |       |
|                                    | OIP3 <sub>3</sub>  | Pout = 0dBm/tone<br>5MHz tone separation<br>Low Gain Mode  |         | 23                |         |       |
|                                    | OIP3 <sub>4</sub>  | Pout = 0dBm/tone<br>5MHz tone separation<br>Low Gain Mode<br>$T_{EPAD} = -40^{\circ}C$ to $105^{\circ}C$   | 18      |                   |         |       |
| Output 1dB Compression             | OP1dB <sub>1</sub> | High Gain Mode <sup>[b]</sup>  |         | 15                |         | dBm   |
|                                    | OP1dB <sub>2</sub> | High Gain Mode<br>$T_{EPAD} = -40^{\circ}C$ to $105^{\circ}C$  | 11      |                   |         |       |
|                                    | OP1dB <sub>3</sub> | Low Gain Mode  |         | 14                |         |       |
|                                    | OP1dB <sub>4</sub> | Low Gain Mode<br>$T_{EPAD} = -40^{\circ}C$ to $105^{\circ}C$   | 10      |                   |         |       |
| Channel Isolation                  | ISO <sub>CH</sub>  | $RFISO_1 = \left( \frac{RX1\_OUT}{RX2\_OUT} \right)_{dB}$<br>with $-60 \leq SW1\_IN \leq -30dBm$<br><br>$RFISO_2 = \left( \frac{RX2\_OUT}{RX1\_OUT} \right)_{dB}$<br>with $-60 \leq SW2\_IN \leq -30dBm$ | 54      | 64                |         | dB    |
| RF Switch Isolation                | ISO <sub>SW</sub>  | TX Mode<br>Measured at SW_IN to<br>RX_OUT of the same channel  | 55      | 65                |         | dB    |

[a] Items in the "Minimum"/"Maximum" columns in **bold italics** are confirmed by test. Items in the "Minimum"/"Maximum" columns not in bold italics are confirmed by design characterization.

[b] In the OP1dB calculation formula, "G" denotes the gain of each part instance at the frequency of interest and appropriate HIGH / LOW gain state.

## Thermal Characteristics

Table 7. Thermal Characteristics

| Parameter  | Symbol             | Value | Units |
|--|--------------------|-------|-------|
| Junction-to-Ambient Thermal Resistance   | $\theta_{JA}$      | 31.2  | °C/W  |
| Junction-to-Case Thermal Resistance<br>(Case is defined as the exposed paddle) | $\theta_{JC\_BOT}$ | 3.4   | °C/W  |
| Moisture Sensitivity Rating (Per J-STD-020)                                    |                    | MSL3  |       |

## Typical Operating Conditions

Unless otherwise noted:

- $V_{DD} = +3.3V$
- $T_{EPAD} = 25^{\circ}C$
- $ZL = ZS = 50\Omega$  single-ended with matching networks
- $STBY1 = STBY2 =$  Low or open
- $SW\_CTRL =$  Low or open
- Gain Setting = High Gain Mode
- $P_{IN} \leq -30dBm$
- All temperatures are referenced to the exposed paddle
- Evaluation kit traces and connector losses are de-embedded

## Programming

Table 8. Gain Step Truth Table

| ATT1_CTRL, ATT2_CTRL | Attenuation Setting |
|----------------------|---------------------|
| Low or NC            | 0dB                 |
| High                 | 6dB                 |

Table 9. Standby and RF Switch Truth Table

In TX Mode, the amplifiers are Off but the bias will remain On for fast turn-on recovery time.

| STBY1, STBY2 | SW1_CTRL, SW2_CTRL | Mode    | Amplifier State |
|--------------|--------------------|---------|-----------------|
| Low or NC    | Low or NC          | RX      | On              |
| Low or NC    | High               | TX      | Off             |
| High         | High or Low or NC  | Standby | Off             |

# Typical Performance Characteristics

Figure 2. Rx Mode Gain (High Gain)

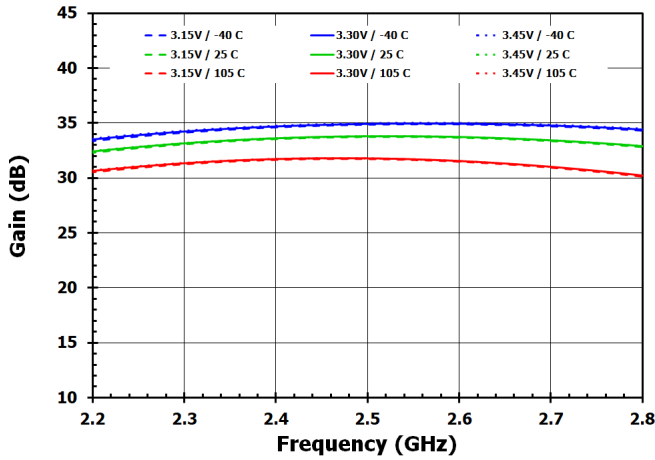


Figure 3. Rx Mode Gain (Low Gain)

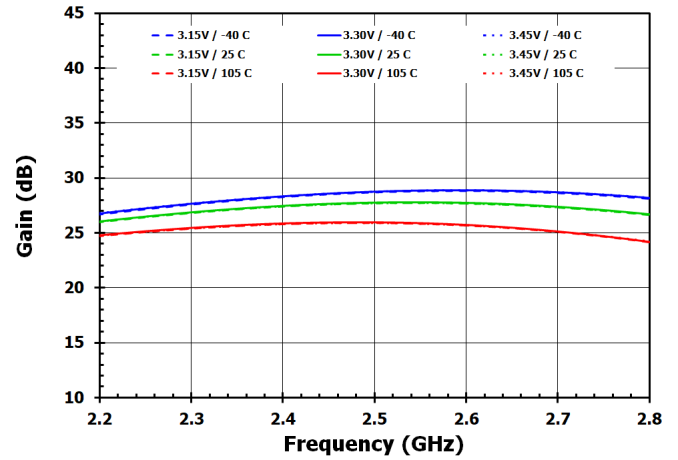


Figure 4. Rx Mode Reverse Isolation (High Gain)

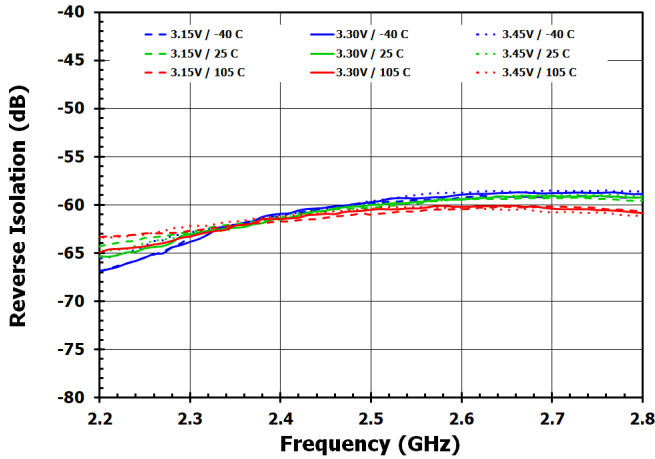


Figure 5. Rx Mode Reverse Isolation (Low Gain)

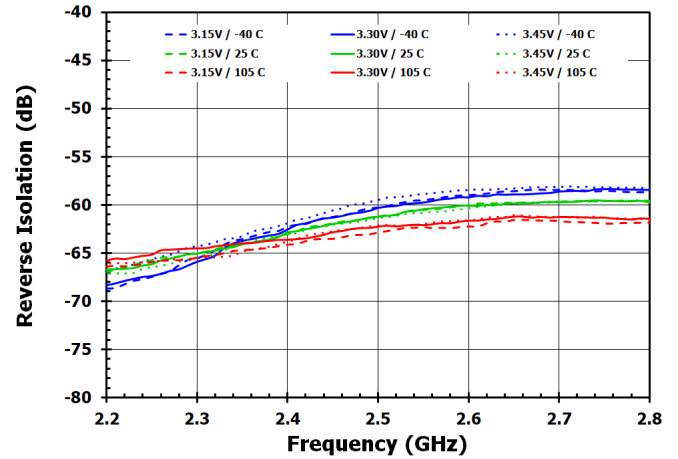


Figure 6. Rx Mode Input Return Loss (High Gain)

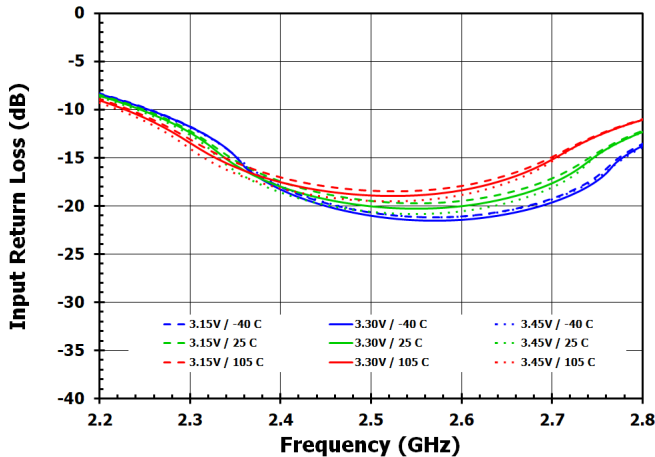


Figure 7. Rx Mode Input Return Loss (Low Gain)

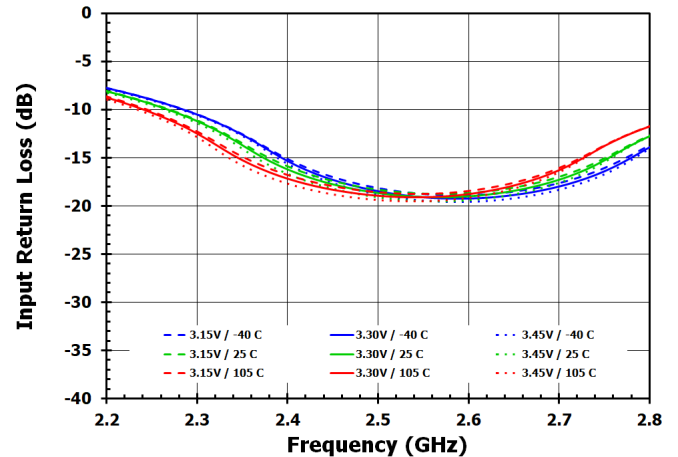


Figure 8. Rx Mode Output Return Loss (High Gain)

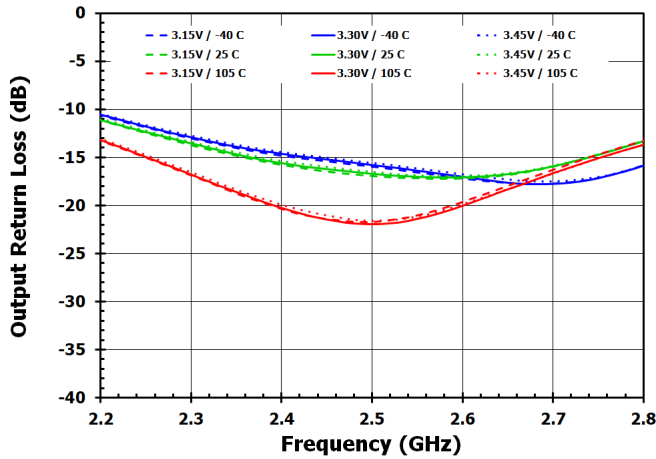


Figure 9. Rx Mode Output Return Loss (Low Gain)

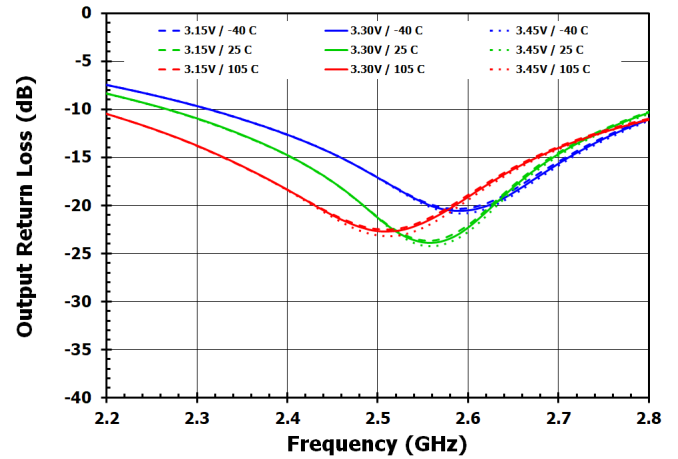


Figure 10. Rx Mode OP1dB (High Gain)

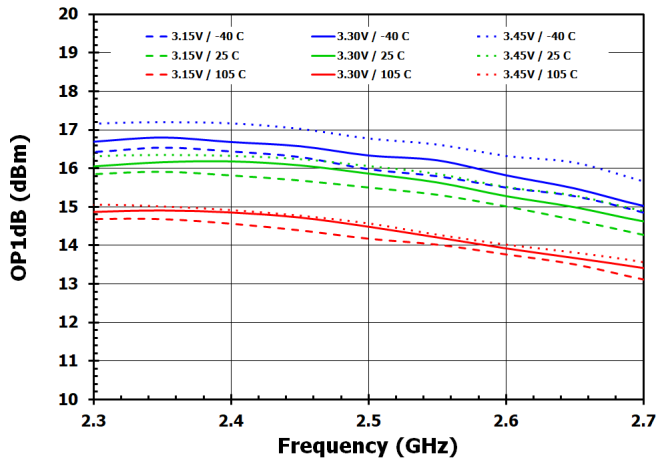


Figure 11. Rx Mode OP1dB (Low Gain)

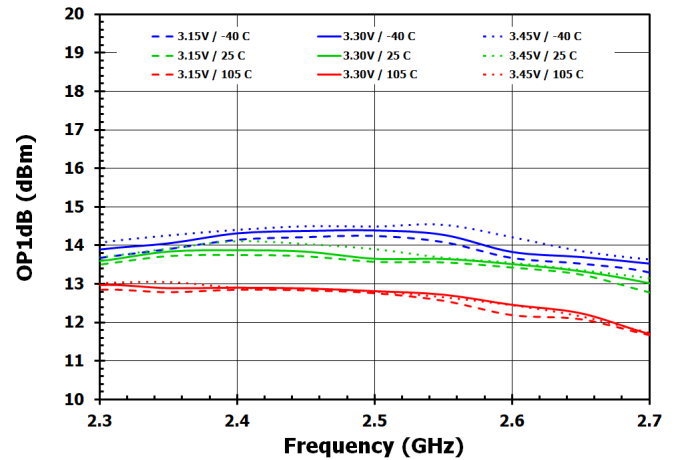


Figure 12. Rx Mode OIP3 (High Gain)

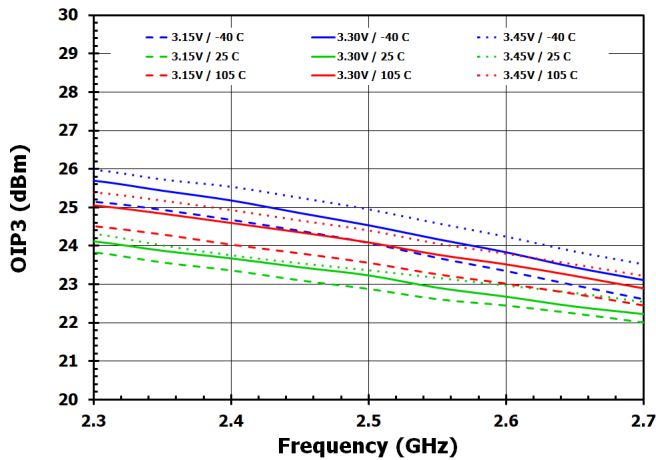


Figure 13. Rx Mode OIP3 (Low Gain)

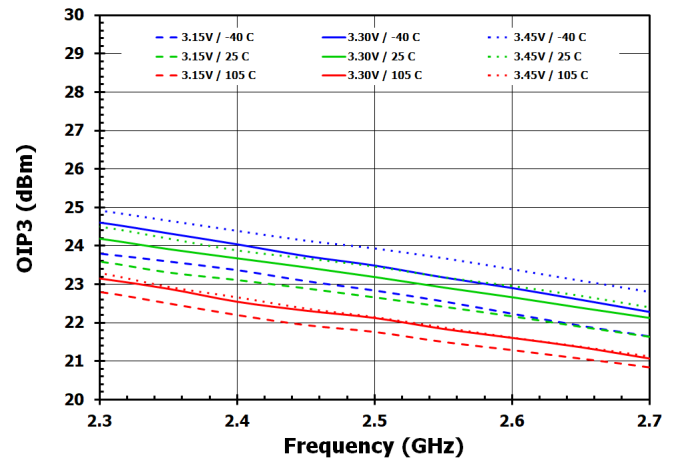


Figure 14. Rx Mode Noise Figure (High Gain)

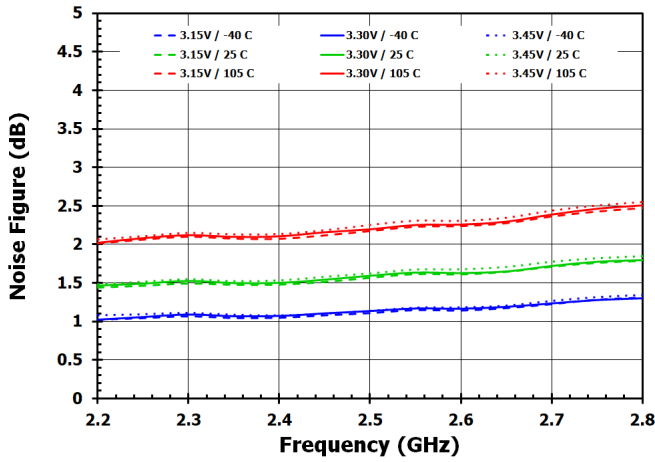


Figure 15. Rx Mode Noise Figure (Low Gain)

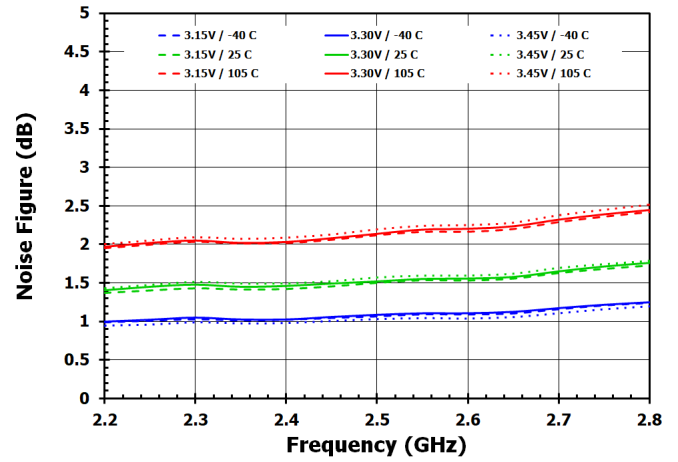


Figure 16. Tx Mode RF Switch Isolation

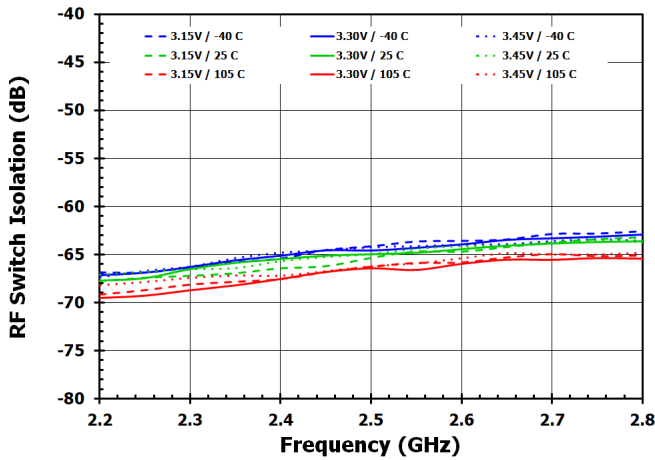


Figure 17. Rx Mode Channel Isolation

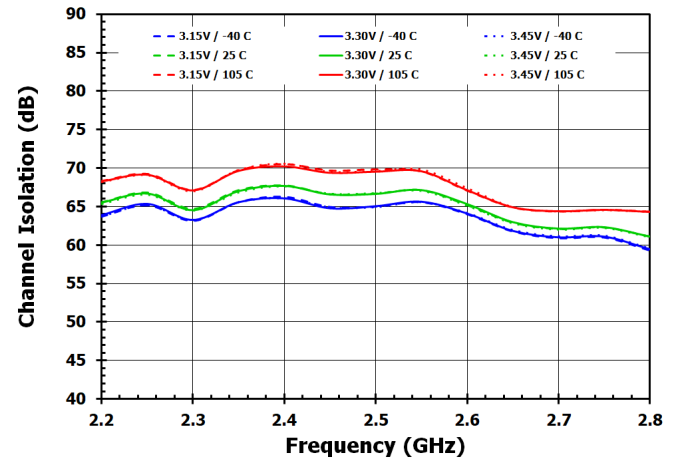


Figure 18. Stability Factor

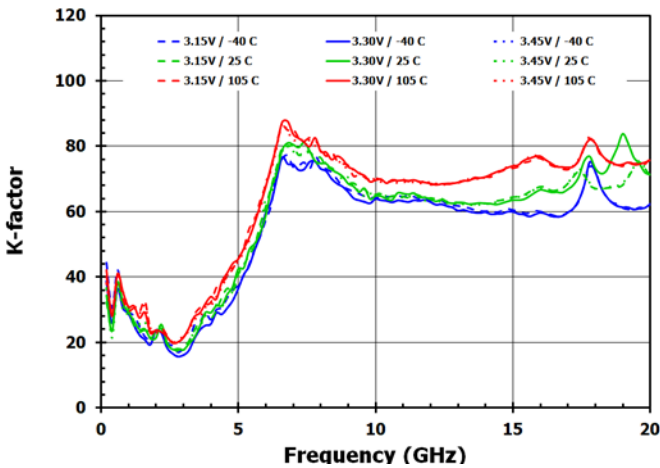


Figure 19. Gain Setting Time

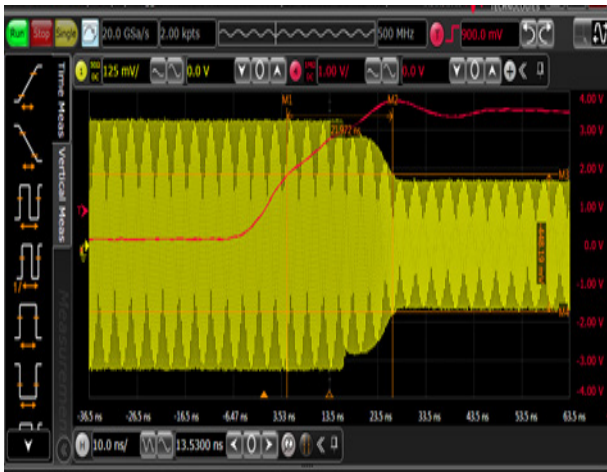


Figure 20. Gain Step Phase Settling Time



Figure 21. Power OFF Switching Time



Figure 22. Power ON Switching Time



Figure 23. Power OFF to Standby Mode

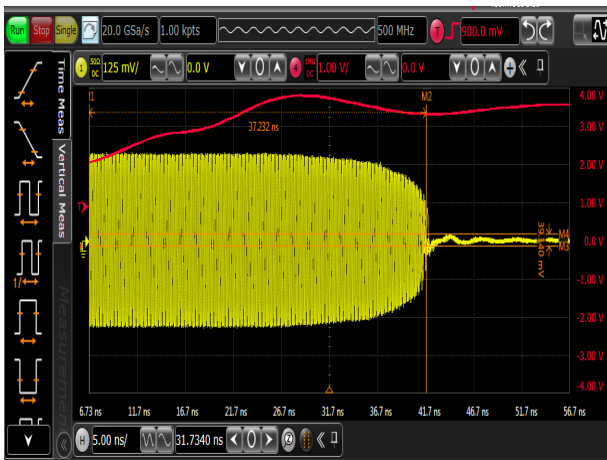
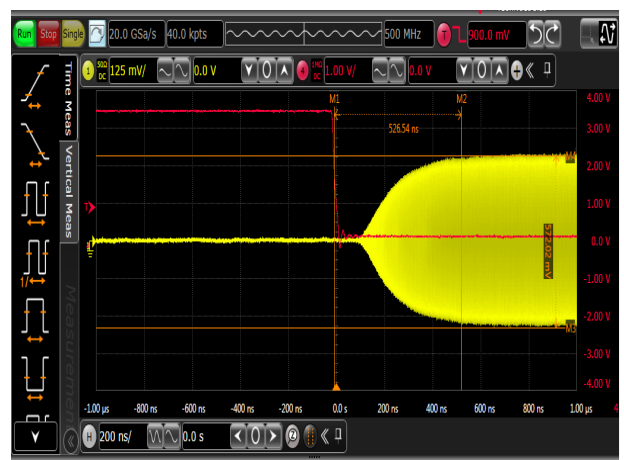


Figure 24. Power ON from Standby Mode





## Evaluation Kit Picture

Figure 26. Evaluation Kit: Top View

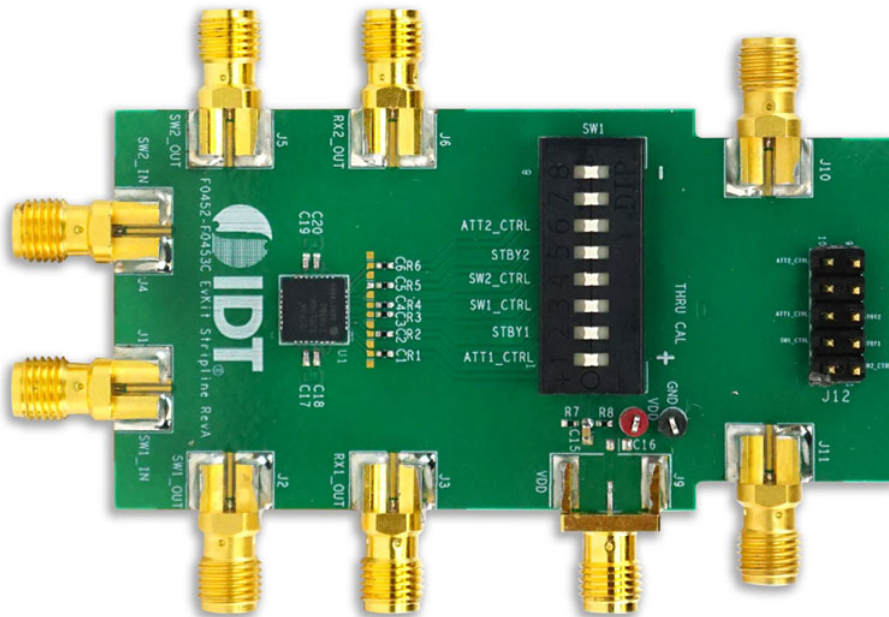
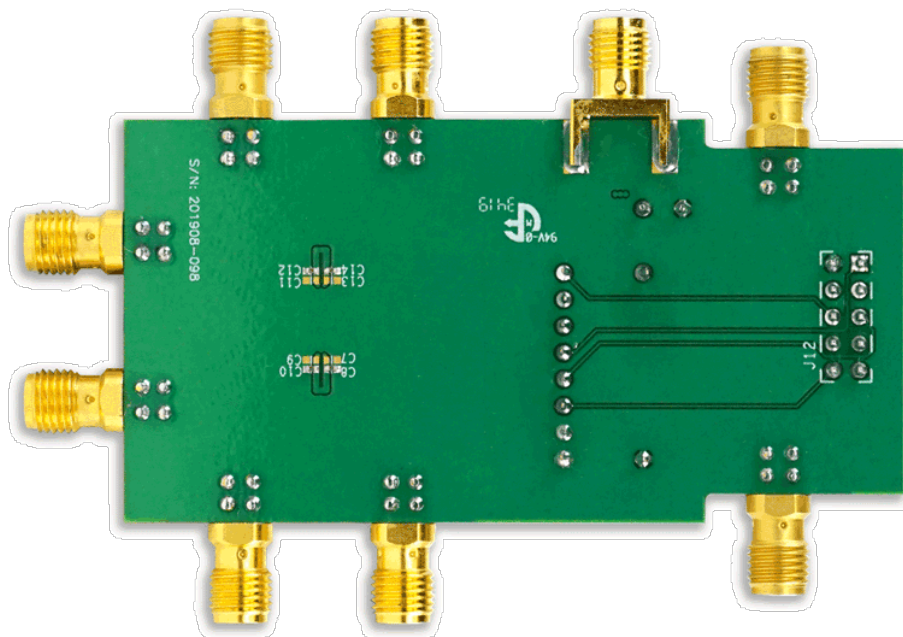


Figure 27. Evaluation Kit: Bottom View



# Evaluation Kit Circuit

Figure 28. Electrical Schematic

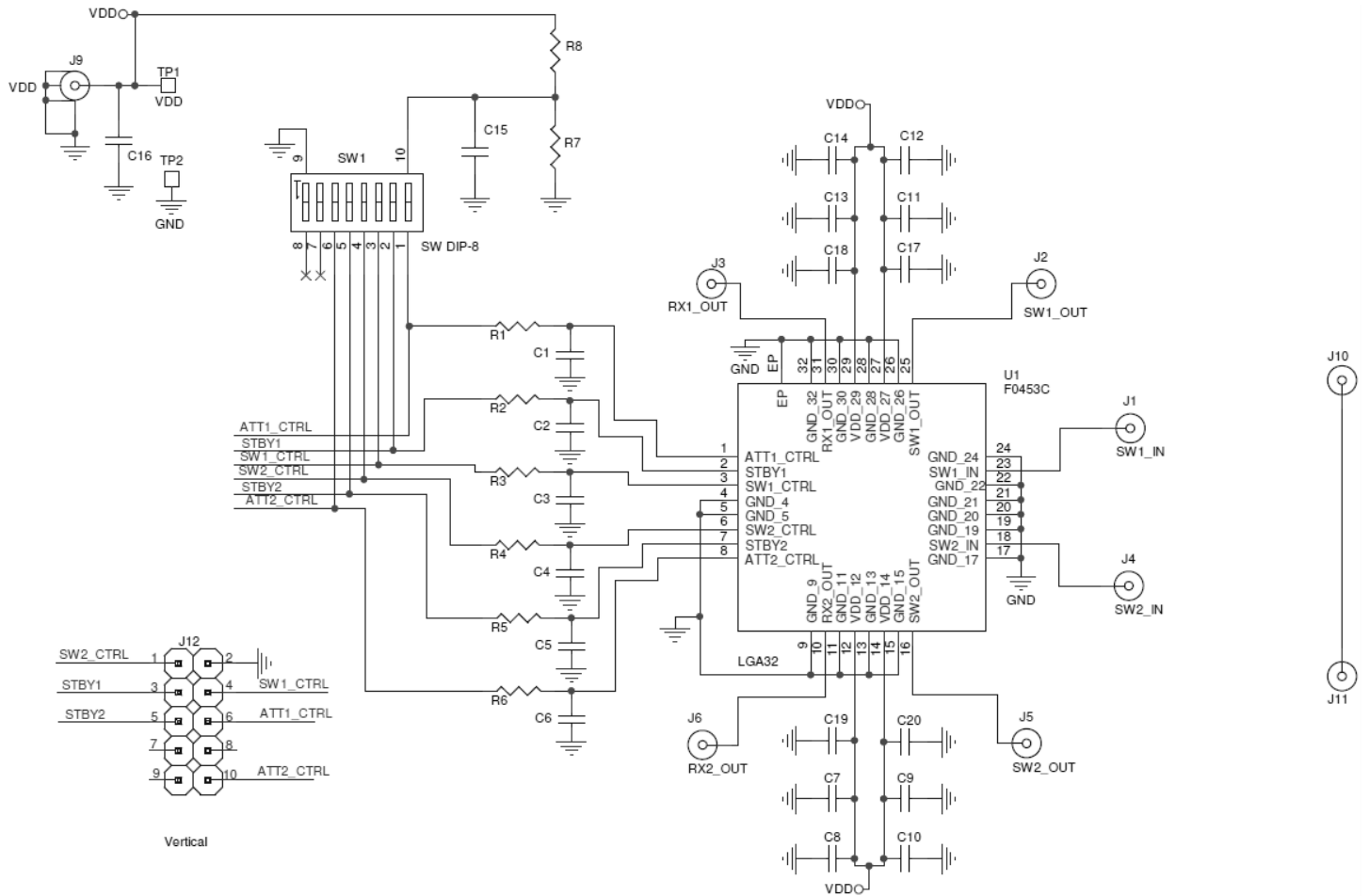


Table 10. Bill of Material (BOM)

| Part Reference                | Qty | Description   | Manufacturer Part #            | Manufacturer            |
|-------------------------------|-----|---|--------------------------------|-------------------------|
| C2,C3,C4,C5                   | DNI | 100pF ±5%, 50V, C0G Ceramic Capacitor (0402)          | GRM1555C1H101J                 | MURATA                  |
| C7,C9,C11,C13                 | DNI | 10nF ±5%, 50V, X7R Ceramic Capacitor (0402)           | GRM155R71H103J                 | MURATA                  |
| C8,C10,C12,C14                | 4   | 1µF ±10% 10V Ceramic Capacitor X5R 0402               | GRM155R61A105KE15D             | MURATA                  |
| C17,C18,C19,C20               | 4   | 8pF ±0.1pF 50V Ceramic Capacitor C0G,NP0 (0402)       | GJM1555C1H8R0B                 | MURATA                  |
| C15                           | 1   | 10nF ±5%, 50V, X7R Ceramic Capacitor (0603)           | GRM188R71H103K                 | MURATA                  |
| R1,R2,R3,R4,R5,R6             | 6   | 0Ω Resistors (0402)                                   | ERJ-2GE0R00X                   | PANASONIC               |
| R7                            | 1   | 1kΩ ±1%, 1/10W, Resistor (0402)                       | ERJ-2RKF1001X                  | PANASONIC               |
| R8                            | 1   | 1.3kΩ ±1%, 1/10W, Resistor (0402)                     | ERJ-2RKF1301X                  | PANASONIC               |
| J1,J2,J3,J4,J5,J6,<br>J10,J11 | 8   | SMA Edge Mount  | 142-0761-881                   | Cinch<br>Connectivity   |
| J12                           | 1   | CONN HEADER VERT 2X5 POS GOLD                         | 10-89-7100                     | 3M                      |
| J9                            | 1   | Edge Launch SMA(0.375 inch pitch ground, tab) (50Ohm) | 142-0701-851                   | Emerson<br>Johnson      |
| SW1                           | 1   | 8-pin DIP Switch (3 POS)                              | KAT1108E                       | IDE-Switch              |
| U1                            | 1   | Dual Path RF +LNA+DVGA 5x5 QFN                        | F0452C/F0453C LEG32K           | Renesas (IDT)           |
| PCB                           | 1   | Printed Circuit Board                                 | F0452C/F0453C Stripline Rev. B |                         |
| TEST POINT                    | DNI | BLACK/GND TP1   | 5001                           | Keystone<br>Electronics |
| TEST POINT                    | DNI | RED/VCC TP2   | 5000                           | Keystone<br>Electronics |
| C1,C6,C16                     | 3   | DNI   |                                |                         |

# Application Information

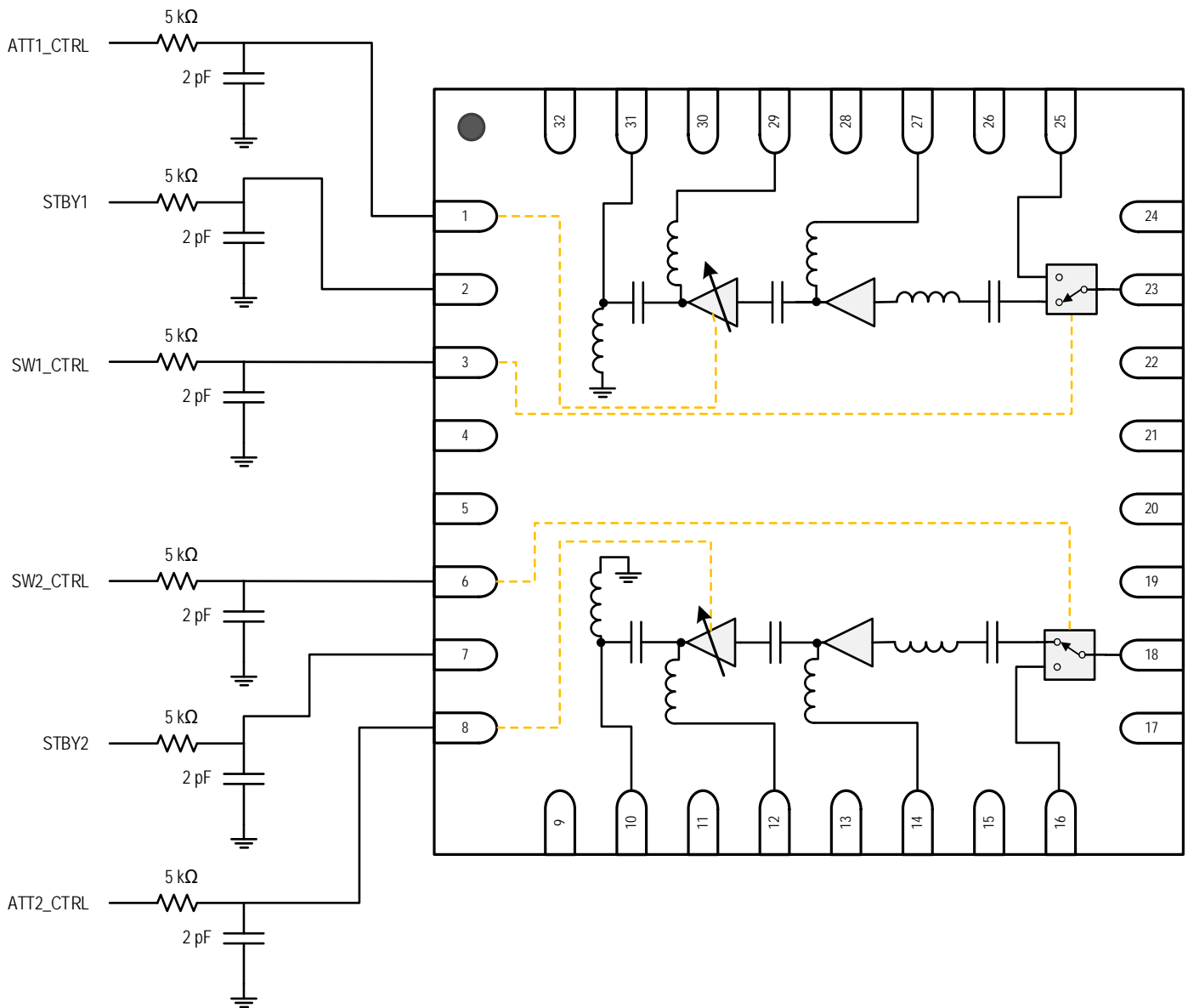
## Power Supplies

A common  $V_{DD}$  power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V / 20\mu s$ . In addition, all control pins should remain at  $0V (\pm 0.3V)$  while the supply voltage ramps up or while it returns to zero.

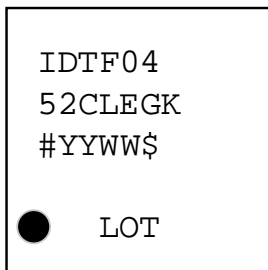
## Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 1, 2, 3, 6, 7, and 8 shown in Figure 29.

Figure 29. Control Pin Interface Schematic



## Marking Diagram



- Lines 1 and 2 indicate the part number
- Line 3 indicates the following:
  - “#” denotes stepping
  - “YY” is the last two digits of the year; “WW” is the work week number when the part was assembled.
  - “\$” denotes the mark code.
- Line 4 is the lot number

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

## Ordering Information

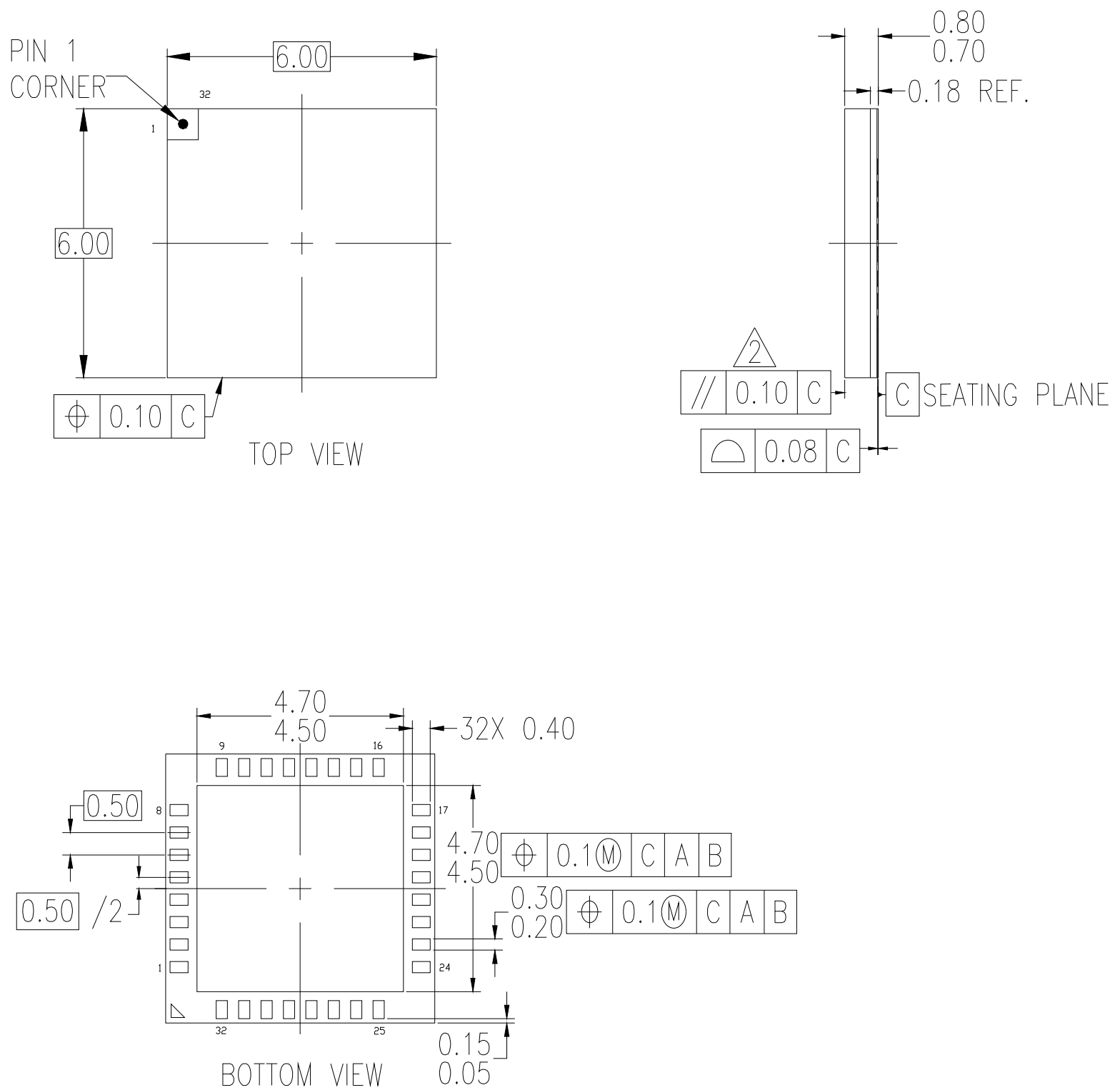
| Part Number | Package                                  | MSL Rating | Carrier Type | Temp. Range    |
|-------------|--|------------|--------------|----------------|
| F0452CLFGK  | 6 × 6 × 0.75 mm <a href="#">32-FCLGA</a> | MSL3       | Tray         | -40° to +105°C |
| F0452CLFGK8 | 6 × 6 × 0.75 mm <a href="#">32-FCLGA</a> | MSL3       | Reel         | -40° to +105°C |
| F0452CEVB   | Evaluation Board                         |            |              |                |

## Revision History

| Revision Date     | Description of Change   |
|-------------------|---|
| July 13, 2021     | <ul style="list-style-type: none"> <li>▪ Updated <math>V_{IL}</math> specification in Table 4.</li> <li>▪ Completed other minor changes.</li> </ul> |
| May 5, 2020       | Updated thickness package dimensions to match the POD dimensions.   |
| April 21, 2020    | <ul style="list-style-type: none"> <li>▪ Updated Orderable Part Number Information.</li> <li>▪ Added Application Section Information.</li> </ul>    |
| February 26, 2020 | Initial release.  |

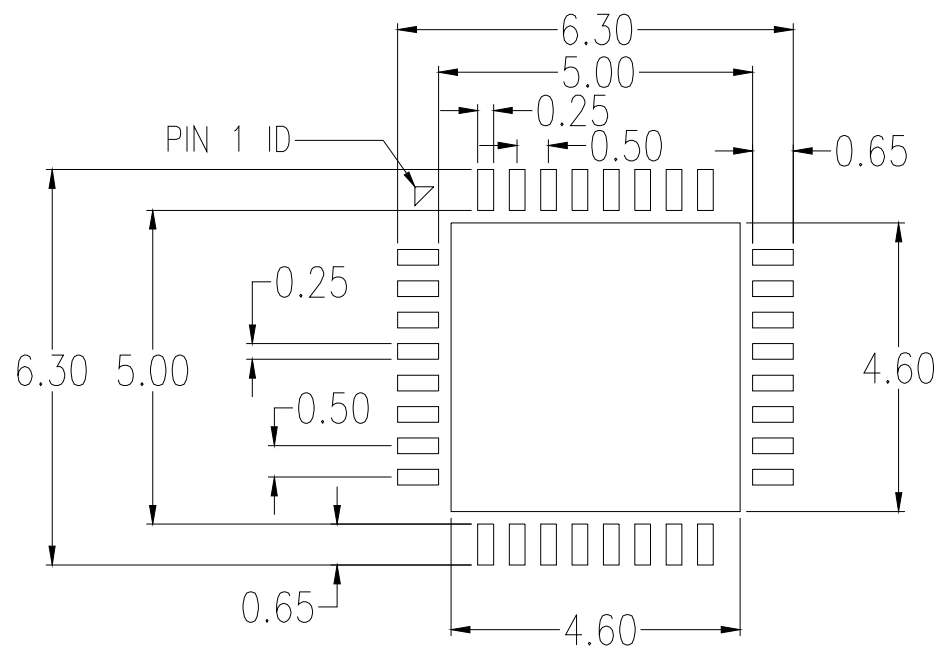
**32-FCLGA, Package Outline Drawing**

6.00 x 6.00 x 0.75 mm Body, 4.60 x 4.60 mm Epad, 0.5mm Pitch  
LFG32P1, PSC-4813-01, Rev 01, Page 1



NOTES:

1. ALL DIMENSIONS IN MM.
2. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| Package Revision History |         |                   |
|--------------------------|---------|-------------------|
| Date Created             | Rev No. | Description       |
| Apr 27, 2021             | Rev 01  | Update A1 to 0.18 |
| July 18, 2019            | Rev 00  | Initial Release   |

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