Description

The F2480 is a 400 to 3000 MHz RF Analog Variable Gain Amplifier (AVGA) that can be used in receivers, transmitters and other applications. Either the amplifier or voltage variable attenuator (VVA) can be configured as the first stage in the cascade.

The F2480 RF AVGA provides 12dB typical maximum cascade gain (no attenuation) with 4.3dB noise figure (amplifier as first stage) and 36dB gain adjustment designed to operate with a single +5V supply. Nominally, the amplifier offers +41.5dBm output IP3 using 106mA of I_{CC}.

This device is packaged in a 5 x 5 mm, 32-pin TQFN with 50Ω single-ended RF input and RF output impedances for ease of integration into the signal-path lineup.

Competitive Advantage

The F2480 RF AVGA provides very high-performance by combining a silicon VVA & a *Zero-Distortion*™ RF amplifier in a single, compact TQFN package. Because of the superb VVA IP3 performance over its full attenuation range, the VVA can be placed after the amplifier while yielding the desired cascaded OIP3 performance. Utilizing IDT's technology, the resultant RF AVGA provides +41.5dBm OIP3 performance at 900MHz. The device is internally matched so there is no need to optimize external matching elements.

Typical Applications

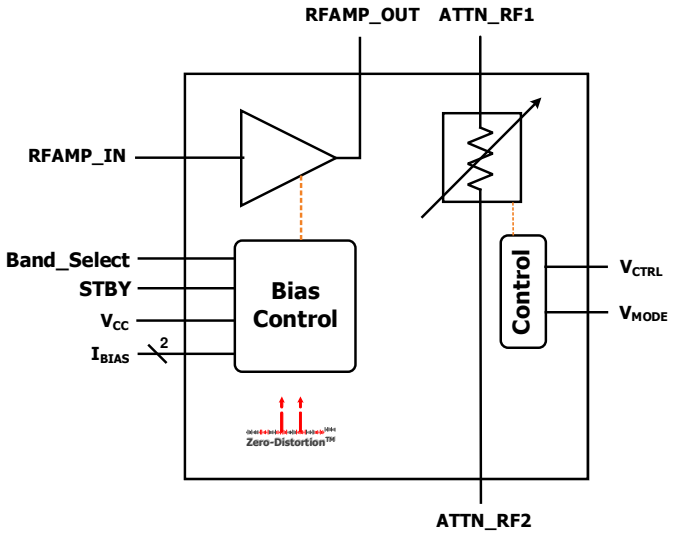
- Multi-mode, Multi-carrier Receivers
- PCS1900 Base Stations
- DCS1800 Base Stations
- WiMAX and LTE Base Stations
- UMTS/WCDMA 3G Base Stations
- PHS/PAS Base Stations
- Point to Point Infrastructure
- Public Safety Infrastructure
- Broadband Repeaters
- GPS Receivers
- Distributed Antenna Systems
- Cable Infrastructure
- Digital Radio

Features

- 400 to 3000 MHz (Amplifier Range)
- 50 to 6000 MHz (Attenuator Range)
- 12dB typical cascaded max gain
- 36dB continuous gain range
- Excellent linearity +41.5dBm OIP3
- Noise Figure 4.3dB
- I_{CC} = 106mA
- 1.2mA Amplifier Standby Current
- Bi-directional attenuator RF ports
- Positive amplifier gain slope vs. frequency to counteract system PCB loss.
- V_{MODE} pin allows either positive or negative attenuation control response
- Linear-in-dB attenuation characteristic
- 4 RF Port pinout supporting multiple lineup configurations
- 50Ω input and output impedances
- Broadband, Internally Matched
- 5 x 5 mm, 32-pin TQFN package

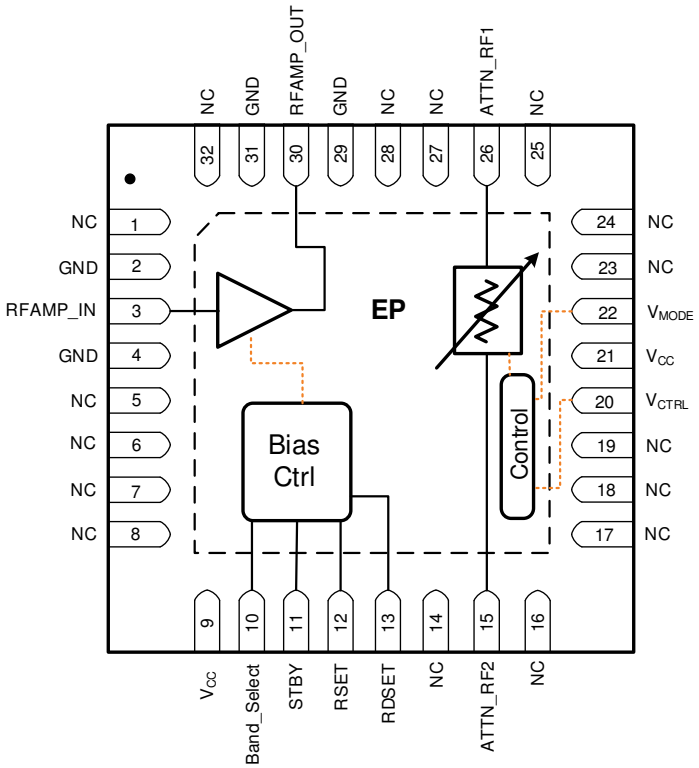
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 5 x 5 x 0.75 mm - TQFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 5, 6, 7, 8, 14, 16, 17, 18, 19, 23, 24, 25, 27, 28, 32	NC	No internal connection. These pins can be left unconnected, have voltage applied, or connected to ground (recommended).
2, 4, 29, 31	GND	Ground these pins. These pins are internally connected to the exposed paddle.
3	RFAMP_IN	Amplifier input internally matched to 50Ω. Must use external DC block.
9	V_{CC}	+5V Power Supply. Tie to V_{CC} and connect bypass capacitors as close to the pin as possible. See Typical Application Circuit for details.
10	Band_Select	Leave pin open circuited for low-band select and connect 0Ω resistor to GND for mid-band, high-band and wide-band applications. A pull-up resistor of approximately 1.5MΩ connects between this pin and $V_{CC.}$
11	STBY	Logic Low or Open on this pin enables the device. Logic High puts the device into Standby mode. A pull-down resistor of approximately 1MΩ connects between this pin and GND.
12	RSET	Connect external resistor to GND to optimize amplifier bias. Used in conjunction with pin 13.
13	RDSET	Connect external resistor to GND to optimize amplifier bias. Used in conjunction with pin 12.
15	ATTN_RF2	Attenuator RF Port 2. Matched to 50Ω. Use an external DC blocking capacitor as close to the device as possible.
20	V_{CTRL}	Attenuator control voltage. Apply a voltage in the range as specified in the General Specifications Table. See application section for details about V_{CTRL}. This pin has an internal pull down resistor.
21	V_{CC}	+5V Power Supply. Tie to V_{CC} and connect bypass capacitors as close to the pin as possible. See Typical Application Circuit for details.
22	V_{MODE}	Attenuator slope control. Set to logic LOW to enable negative attenuation slope (Attenuation low to high as voltage is increased). Set to logic HIGH to enable positive attenuation slope (Attenuation high to low as voltage is increased).
26	ATTN_RF1	Attenuator RF Port 1. Matched to 50Ω. Use an external DC blocking capacitor as close to the device as possible.
30	RFAMP_OUT	Amplifier output internally matched to 50Ω. Must use external DC block as close to the pin as possible.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F2480 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

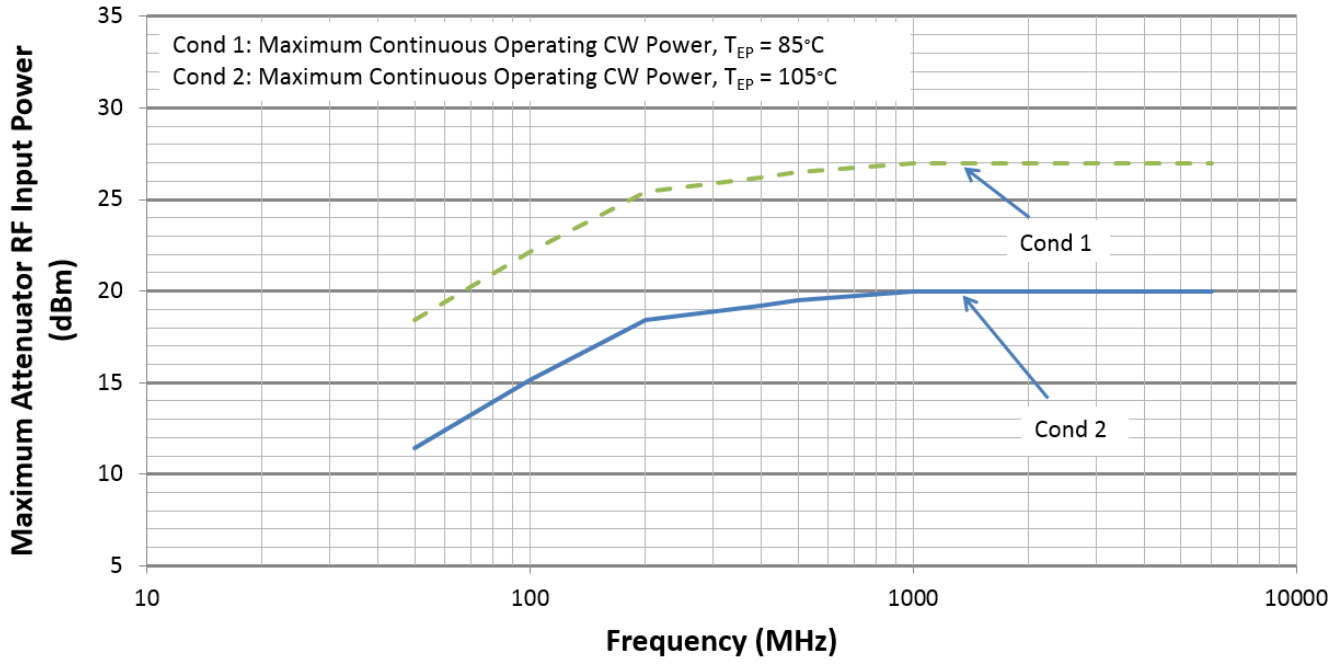
Parameter	Symbol	Minimum	Maximum	Units
V_{CC} to GND	V_{CC}	-0.3	5.5	V
STBY, Band_Select	V_{LOGIC}	-0.3	V_{CC} + 0.25	V
RSET	I_{RSET}		+1.5	mA
RDSET	I_{RDSET}		+0.8	mA
RFAMP_IN externally applied DC voltage	$V_{RFAMPin}$	+1.4	+3.6	V
RFAMP_OUT externally applied DC voltage	$V_{RFAMPout}$	V_{CC} - 0.15	V_{CC} + 0.15	V
V_{MODE} to GND	V_{MODE}	-0.3	Lower of (V_{CC}, 3.9)	V
V_{CTRL} to GND (V_{CC} = 0 to 5.25 V)	V_{CTRL}	-0.3	Lower of (V_{CC}, 4.0)	V
ATTEN_RF1, ATTEN_RF2	$V_{ATTENRF}$	-0.3	+0.3	V
RFAMP_IN RF Input Power applied for 24 hours maximum (V_{CC} applied, RF = 2GHz, T_A=+25°C)	P_{MAXAMP}		+22	dBm
ATTN_RF1 or ATTN_RF2 RF Input Power (@ 2GHz and +85°C)	$P_{MAXATTEN}$		+30	dBm
Continuous Power Dissipation	P_{diss}		1.5	W
Junction Temperature	T_j		+150	°C
Storage Temperature Range	T_{st}	-65	+150	°C
Lead Temperature (soldering, 10s)			+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2014)			Class 1C	
Electrostatic Discharge – CDM (JEDEC 22-C101F)			Class C3	

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage	V_{CC}	All V_{CC} Pins	4.75	5.00	5.25	V
Operating Temperature Range	T_{EP}	Exposed Paddle Temperature	-40		+105	°C
RF Frequency Range	f_{RF}	Amplifier	400		3000	MHz
		Attenuator	50		6000	
Amplifier RF Maximum Input Operating Power	$P_{max1, CW}$	T_{EP} = -40 to 105 °C			8	dBm
Attenuator RF Maximum Input Operating Power	$P_{max2, CW}$	ATTEN_RF1 or ATTEN_RF2			See Figure 3	dBm
RFAMP_IN Port Impedance	$Z_{RFAMPIN}$			50		Ω
RFAMP_OUT Port Impedance	$Z_{RFAMPOUT}$			50		Ω
ATTN_RF1 Port Impedance	$Z_{ATTNRF1}$			50		Ω
ATTN_RF2 Port Impedance	$Z_{ATTNRF2}$			50		Ω

Figure 3. Attenuator Maximum RF Input Power vs. Frequency



Electrical Characteristics

Table 4. General Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH_AMP}	STBY, Band_Select	***1.1*** [a]		V_{CC} [b]	V
Logic Input Low Threshold	V_{IL_AMP}	STBY, Band_Select	***-0.3***		***0.63***	V
V_{MODE} Logic	V_{IH_Mode}	V_{CC} > 3.9V	1.17		3.6	V
		3.15V ≤ V_{CC} ≤ 3.9V	1.17		V_{CC} – 0.3	
	V_{IL_Mode}		0		0.63	
V_{CTRL} Voltage	V_{CTRL}	3.9V < V_{CC} ≤ 5.25V	0		3.6	V
		3.15V ≤ V_{CC} ≤ 3.9V	0		V_{CC} – 0.3	
Logic Current	I_{STBY}		***-10***		***12***	µA
	I_{Band_Select}		***-10***		***10***	
	I_{MODE}		***-1***		***35***	
Control Current	I_{CTRL}	Pin 20	***-1***		***12***	µA
Supply Current	I_{CC}	Pin 21	***0.90***	1.17	***2.20***	mA
		Pin 9 – Low Band Bias		106		
		Pin 9 – Mid Band Bias		121	***170***	
		Pin 9 – High Band Bias		121		
		Pin 9 – Wide Band Bias		121		
		Pin 9 – Standby		0.8	***1.7***	
Startup Time from STBY		50% of STBY going low to Gain within ± 1dB		250		ns

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold/italics are guaranteed by design characterization.

Table 5. Stand Alone Amplifier Electrical Characteristics

Typical Application Circuit. See Table 8 band settings as noted (LB, MB, HB, WB), V_{CC} = +5.0V, T_{EP} = +25°C, f_{RF} = 2000MHz, P_{OUT} = 0dBm/tone for single tone and two tone tests, OIP3 tone delta = 1MHz, all RF source and RF load impedances = 50Ω, PCB board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input Return Loss	RL_{AMPIN}			16		dB
Output Return Loss	RL_{AMPOUT}			17		dB
Gain	G_{LB}	400MHz Low Band Bias		11.1		dB
		900MHz Low Band Bias	***12.1*** [a]	13.2	***14.2***	
	G_{MB}	2000MHz Mid Band Bias		14.1		
	G_{HB}	2700MHz High Band Bias	***13.0***	14.4	***15.5***	
	G_{WB}	400MHz Wide Band Bias		11.1		
		2700MHz Wide Band Bias		14.4		
Noise Figure	NF_{LB}	400MHz Low Band Bias		4.5		dB
		900MHz Low Band Bias		4.3		
	NF_{MB}	2000MHz Mid Band Bias		4.5		
	NF_{HB}	2700MHz High Band Bias		5.0		
	NF_{WB}	400MHz Wide Band Bias		4.5		
		2700MHz Wide Band Bias		5.0		
Output Third Order Intercept Point	$OIP3_{LB}$	400MHz Low Band Bias		37		dBm
		900MHz Low Band Bias	38 [b]	41.5		
	$OIP3_{MB}$	2000MHz Mid Band Bias		41		
	$OIP3_{HB}$	2700MHz High Band Bias		40		
	$OIP3_{WB}$	400MHz Wide Band Bias		35		
		2700MHz Wide Band Bias		39		
Output 1dB Compression	$OP1dB_{LB}$	400MHz Low Band Bias		19.5		dBm
		900MHz Low Band Bias		20.9		
	$OP1dB_{MB}$	2000MHz Mid Band Bias		19.7		
	$OP1dB_{HB}$	2700MHz High Band Bias		19.5		
	$OP1dB_{WB}$	400MHz Wide Band Bias		18.7		
		2700MHz Wide Band Bias		19.5		
Reverse Isolation	$RevISO_{LB}$	400MHz Low Band Bias		20.5		dB
		900MHz Low Band Bias		18.5		
	$RevISO_{MB}$	2000MHz Mid Band Bias		18		
	$RevISO_{HB}$	2700MHz High Band Bias		18		
	$RevISO_{WB}$	400MHz Low Band Bias		20.5		
		2700MHz High Band Bias		18		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold/italics are guaranteed by design characterization.

Table 6. Stand Alone Voltage Variable Attenuator Electrical Characteristics

Typical Application Circuit. V_{CC} = +5V, T_{EP} = +25°C, signals applied to ATTEN_RF1 input, f_{RF} = 2000MHz, minimum attenuation, P_{IN} = 0dBm for small signal parameters, P_{IN} = +20dBm / tone for single tone and two tone linearity tests, two tone delta frequency = 50MHz, all RF source and RF load impedances = 50Ω, PCB board traces and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss	A_{min}	50MHz [a]		1.0		dB
		700MHz		1.2		
		2000MHz		1.4	***1.9***	
		2700MHz		1.5		
		6000MHz		2.7		
Maximum Attenuation	A_{max}	50MHz [a]		29		dB
		700MHz		35.6		
		2000MHz	33.2	35.5		
		2700MHz		35.4		
		6000MHz		37		
Relative Insertion Phase Relative to Insertion Loss	$\Phi_{\Delta MAX}$	At 35dB attenuation		27		deg
	$\Phi_{\Delta MID}$	At 18dB attenuation		10		
Minimum ATTEN_RF1 Return Loss Over Control Voltage Range	S11	50MHz [a]		16		dB
		700MHz		17		
		2000MHz		17		
		2700MHz		17		
		6000MHz		15		
Minimum ATTEN_RF2 Return Loss Over Control Voltage Range	S22	50MHz [a]		14		dB
		700MHz		15		
		2000MHz		16		
		2700MHz		17		
		6000MHz		13		
Input IP3	IIP3			65		dBm
	$IIP3_{ATTEN}$	All attenuation settings	44	47		dBm
Minimum Output IP3	$OIP3_{MIN}$	Maximum attenuation		35		dBm
Input IP2 (f_1+ f_2)	IIP2	P_{IN} + IM2 [dBc]		95		dBm
	$IIP2_{MIN}$	All attenuation settings		87		
Input IH2	HD2	P_{IN} + H2 [dBc]		90		dBm
Input IH3	HD3	P_{IN} + H3 [dBc]/2		54		dBm
Input 1dB Compression [b]	IP1dB			34.4		dBm
Settling Time	$T_{SETTL0.1dB}$	Any 1dB step in the 0dB to 33dB range. 50% V_{CTRL} to RF settled to within ± 0.1dB		15		µs

a. Set blocking capacitors C2 and C9 to 0.01µF to achieve best return loss performance at 50MHz.

b. The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Amplifier - Junction to Ambient Thermal Resistance.	θ_{JA-AMP}	40	°C/W
Attenuator - Junction to Ambient Thermal Resistance.	$\theta_{JA-ATTN}$	80	°C/W
Amplifier - Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\_BOT\_AMP}$	4	°C/W
Attenuator - Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\_BOT\_ATTN}$	5	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted:

- V_{CC} = +5.0V
- T_{EP} = +25°C (T_{EP} is defined as the exposed paddle temperature).
- Amplifier components configured for operation per Table 8 for each indicated band.
- P_{OUT} = 0dBm/tone for all amplifier linearity tests.
- 1MHz tone spacing for all amplifier linearity tests.
- P_{IN} = +20dBm/tone applied to ATTEN_RF1 for all attenuator linearity tests.
- 50MHz tone spacing for all attenuator linearity tests.
- V_{CTRL} setting = minimum attenuation setting.
- STBY = Logic HIGH (or open).
- Band Select = GND.
- V_{MODE} = Logic LOW = Negative Slope.
- Evaluation kit trace and connector losses are fully de-embedded.
- S-parameters for the amplifier and attenuator have external RF caps replaced by 0Ω resistors for purposes of displaying broadband results.
- Since the Wide Band and Mid Band settings are the same in Table 8, the Mid Band results will be the same curves as those displayed in the Amplifier Wide Band section.

Typical Performance Characteristics – Attenuator [1]

Figure 4. Attenuation vs. V_{CTRL} over Frequency and V_{MODE}

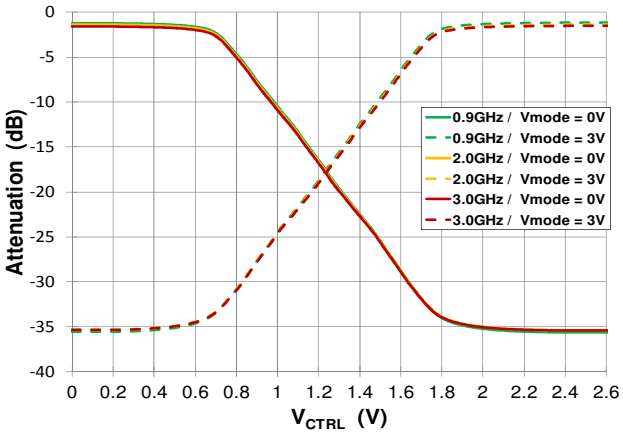


Figure 5. Attenuation vs. Frequency over V_{CTRL}

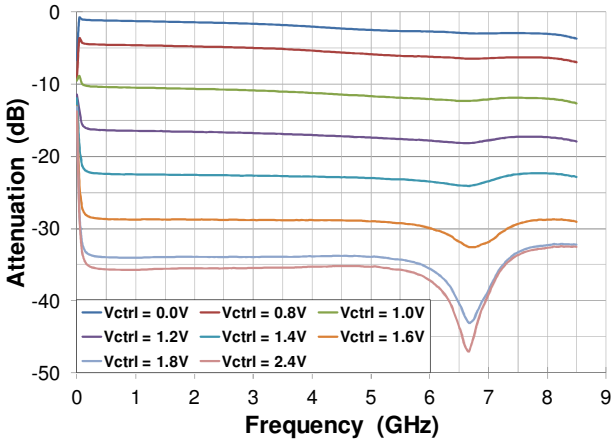


Figure 6. Min. and Max. Attenuation vs. Frequency over Temperature

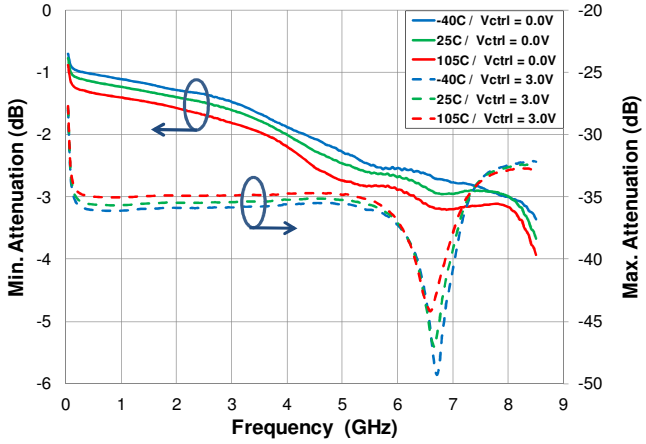
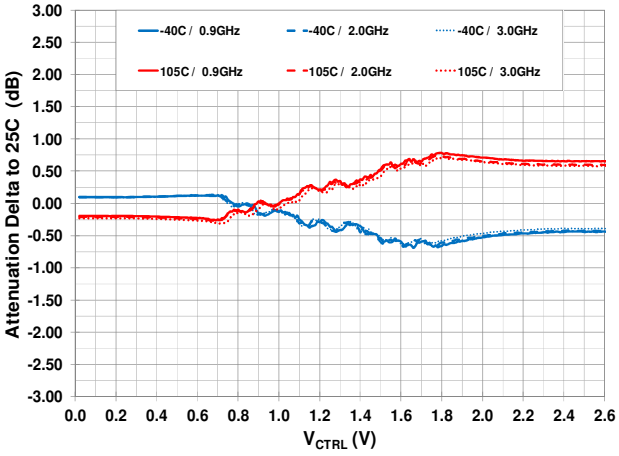


Figure 7. Attenuation Delta to +25 C vs. V_{CTRL} over Frequency and Temperature



Typical Performance Characteristics – Attenuator [2]

Figure 8. Attenuation vs. V_{CTRL} over Frequency

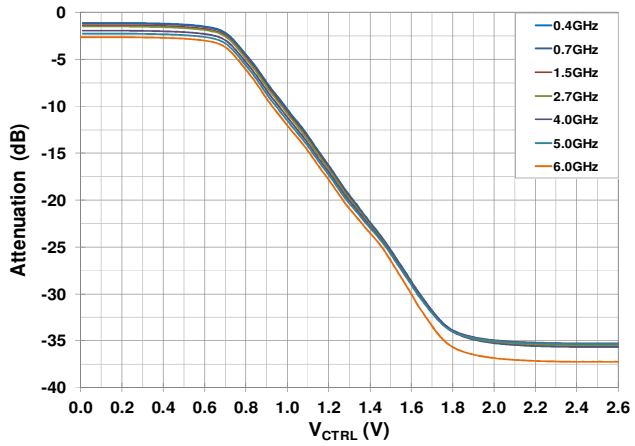


Figure 9. Attenuation Slope vs. V_{CTRL} over Frequency

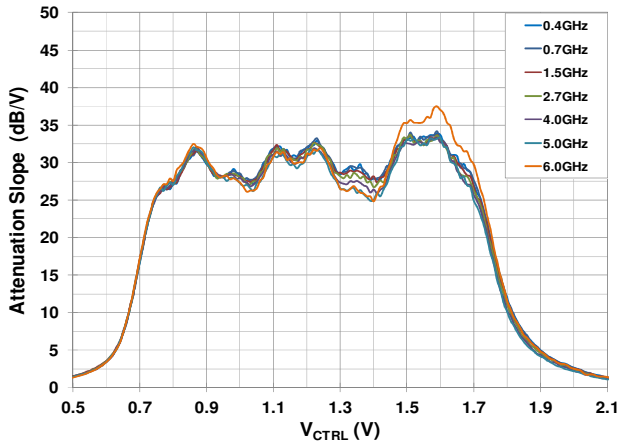


Figure 10. Return Loss (ATTEN_RF1 port) vs. V_{CTRL} over Frequency

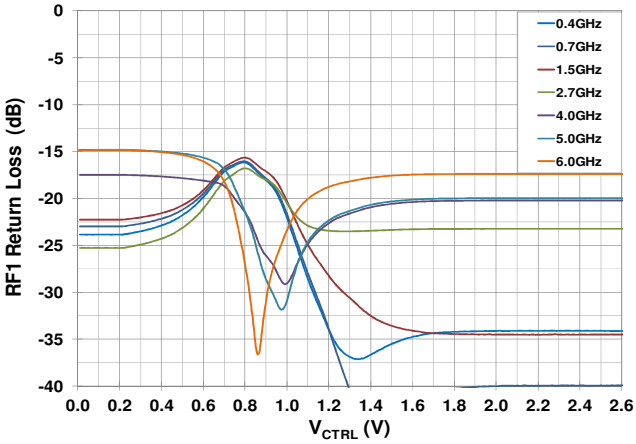


Figure 11. Return Loss (ATTEN_RF2 port) vs. V_{CTRL} over Frequency

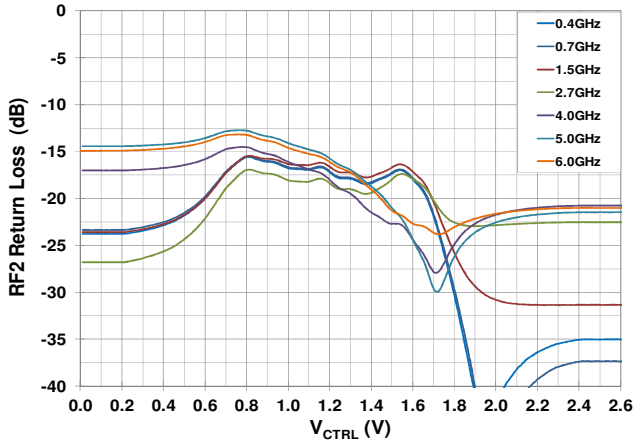


Figure 12. Insertion Phase Change vs. V_{CTRL} over Frequency

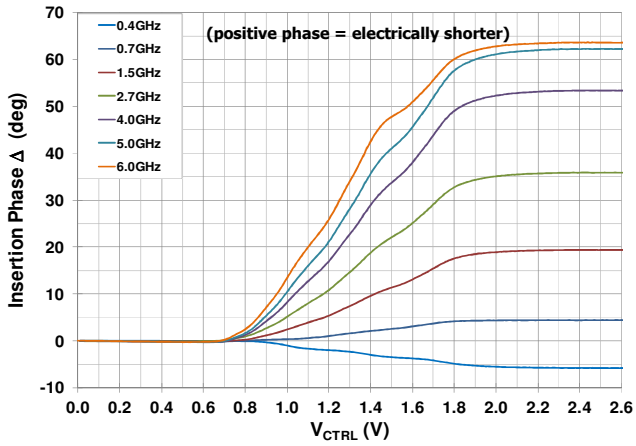
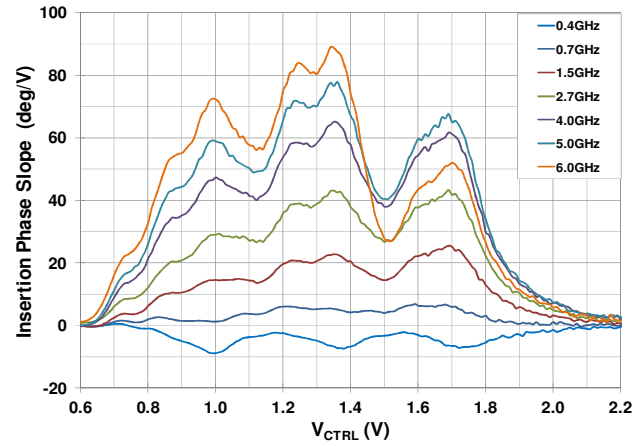


Figure 13. Insertion Phase Slope vs. V_{CTRL} over Frequency



Typical Performance Characteristics – Attenuator [3]

Figure 14. Attenuation Response vs. V_{CTRL} over Frequency and Temperature

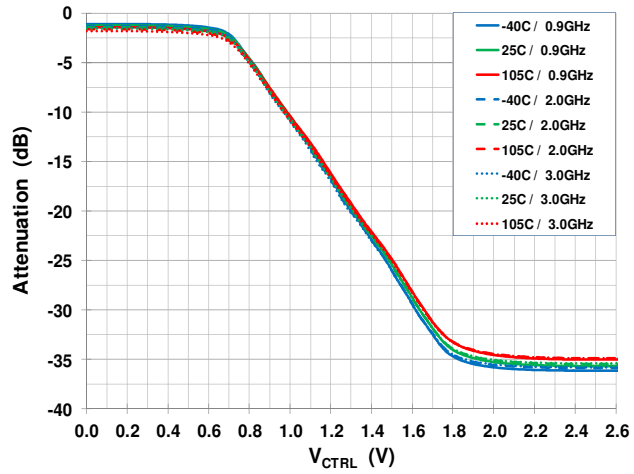


Figure 15. Attenuation Slope vs. V_{CTRL} over Frequency and Temperature

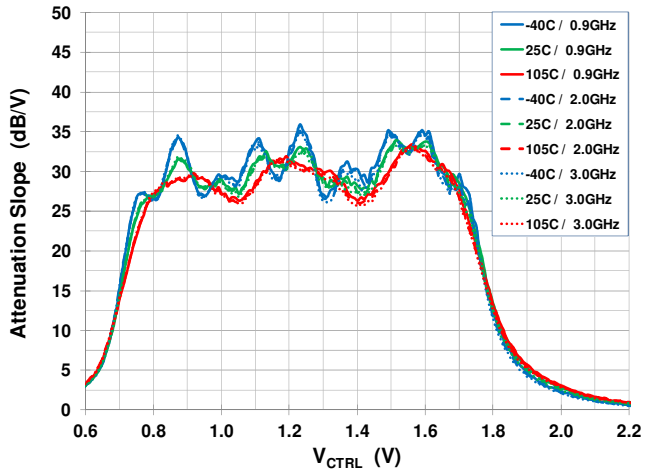


Figure 16. Return Loss (ATTEN_RF1) vs. V_{CTRL} over Frequency and Temperature

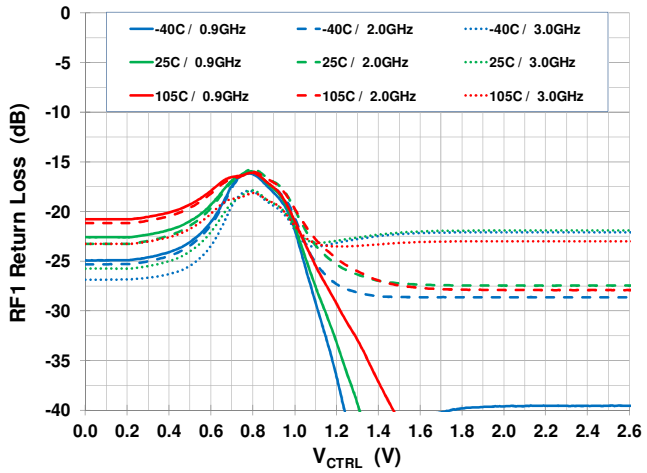


Figure 17. Return Loss (ATTEN_RF2) vs. V_{CTRL}, over Frequency and Temperature

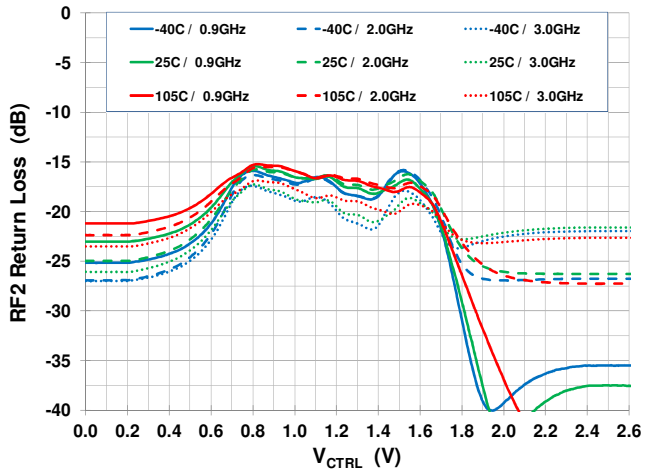


Figure 18. Insertion Phase Change vs. V_{CTRL} over Frequency and Temperature

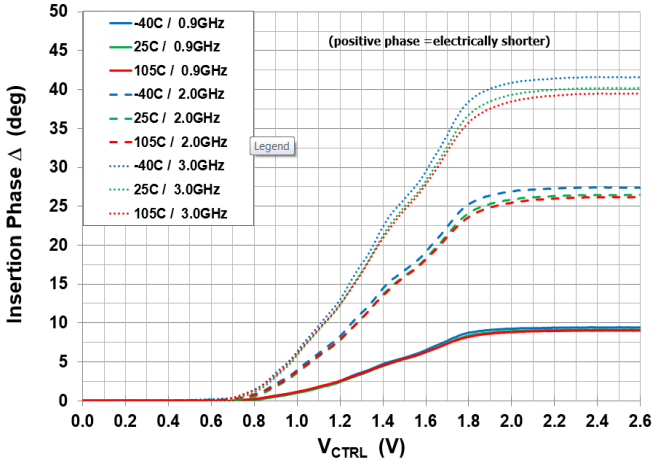
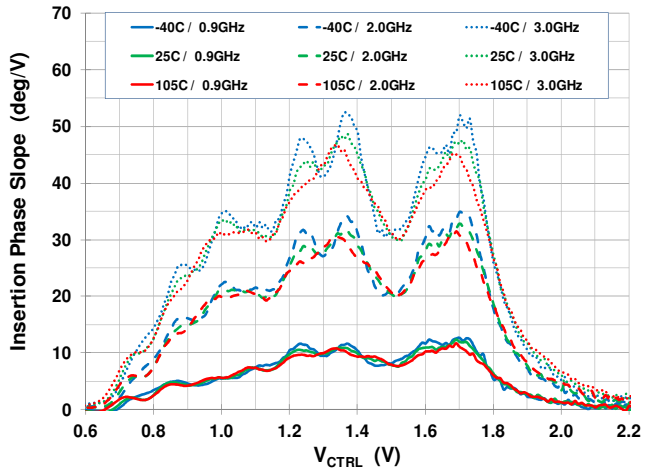


Figure 19. Insertion Phase Slope vs. V_{CTRL} over Frequency and Temperature



Typical Performance Characteristics – Attenuator [4]

Figure 20. Return Loss (ATTEN_RF1 port) vs. Attenuation over Frequency

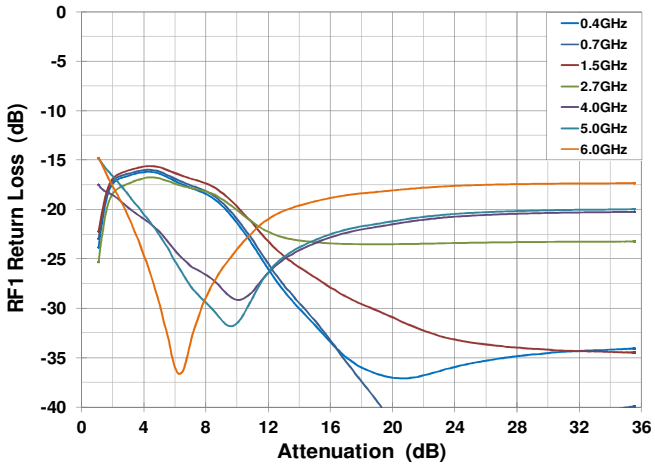


Figure 21. Return Loss (ATTEN_RF1 port) vs. Attenuation over Freq & Temp

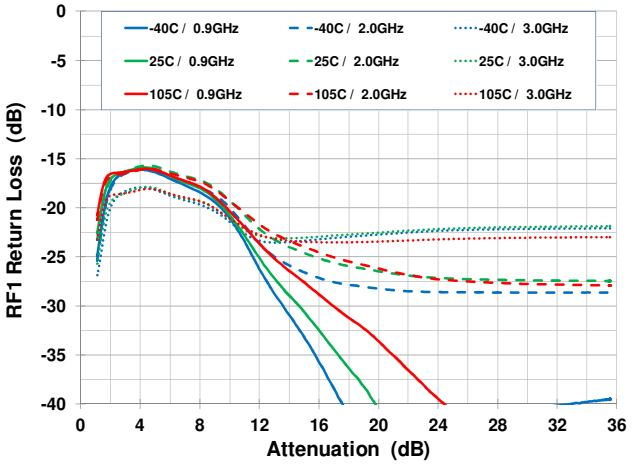


Figure 22. Return Loss (ATTEN_RF2 port) vs. Attenuation over Frequency

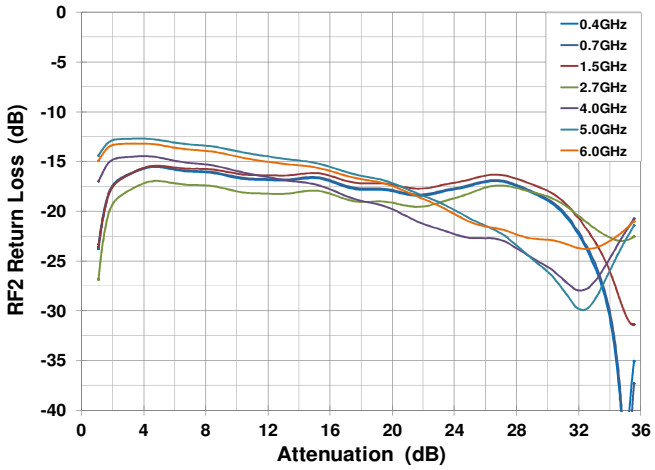


Figure 23. Return Loss (ATTEN_RF2 port) vs. Attenuation over Freq & Temp

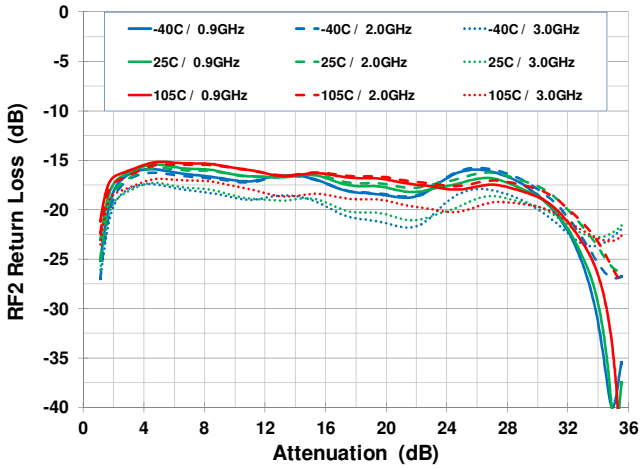


Figure 24. Insertion Phase Change vs. Attenuation over Frequency

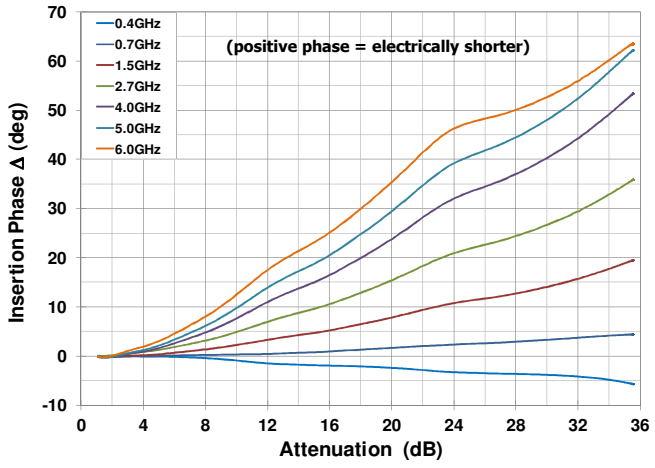
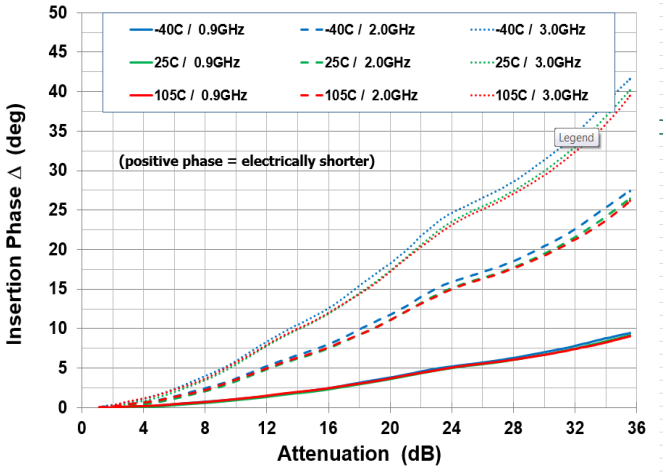


Figure 25. Insertion Phase Change vs. Attenuation over Freq & Temp



Typical Performance Characteristics – Attenuator [5]

Figure 26. Min. and Max. Attenuation vs. Frequency

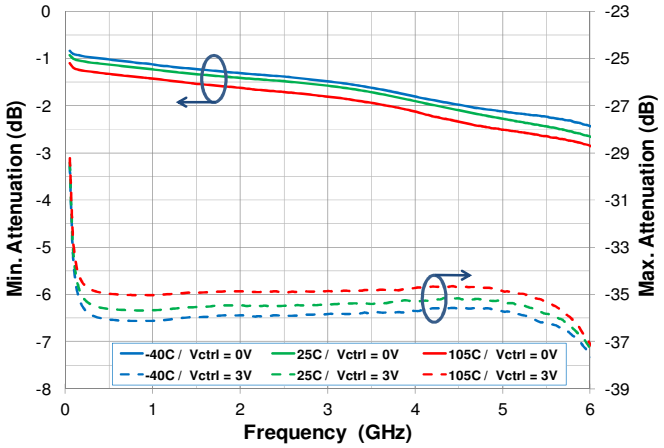


Figure 27. Min. and Max. Attenuation Slope vs. Frequency

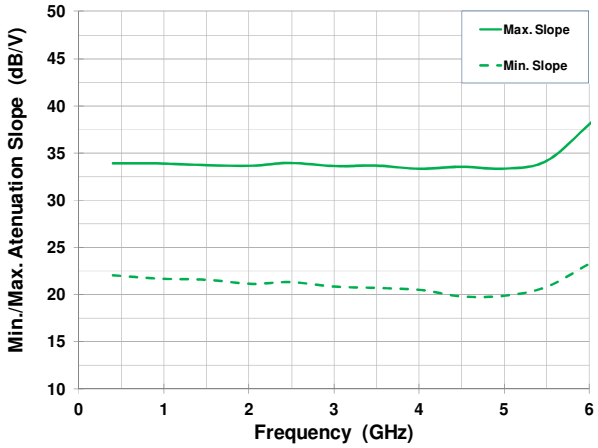


Figure 28. Worst-Case Return Loss (ATTEN_RF1 port) vs. Frequency over Temp

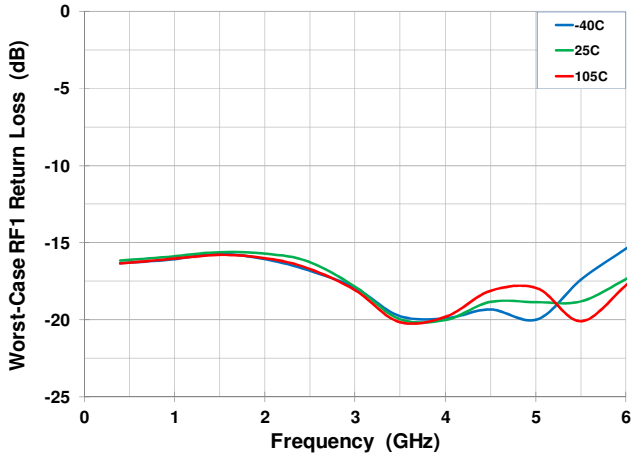


Figure 29. Worst-Case Return Loss (ATTEN_RF2 port) vs. Frequency over Temp

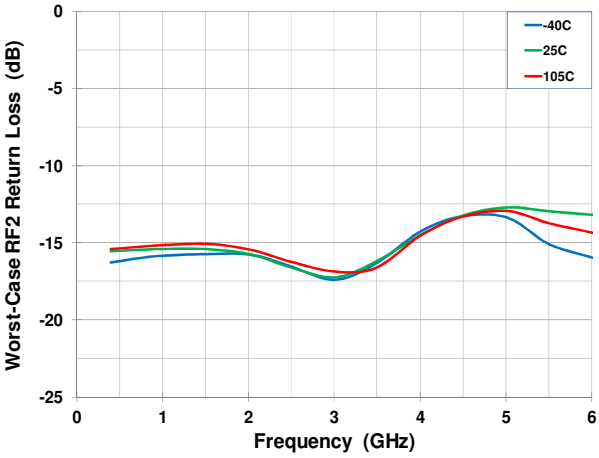
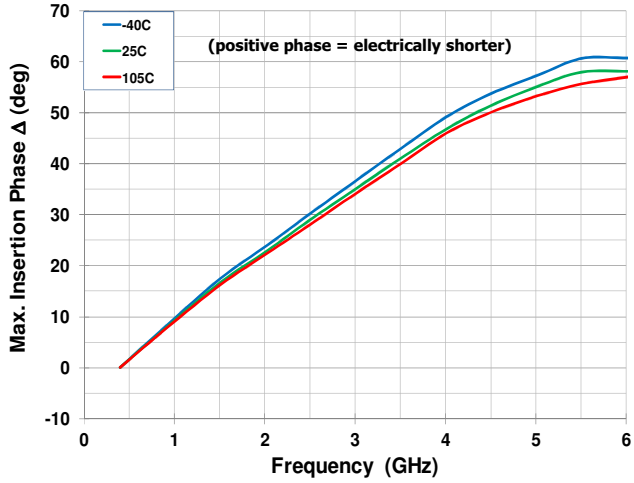


Figure 30. Max. Insertion Phase Change vs. Frequency over Temp



Typical Performance Characteristics – 2 GHz Attenuator [6]

Figure 31. Input IP3 vs. V_{CTRL} over V_{MODE} and Temperature

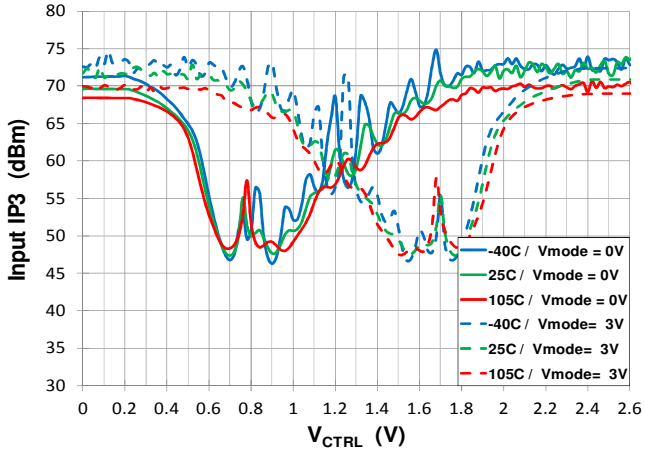


Figure 32. Output IP3 vs. V_{CTRL} over V_{MODE} and Temperature

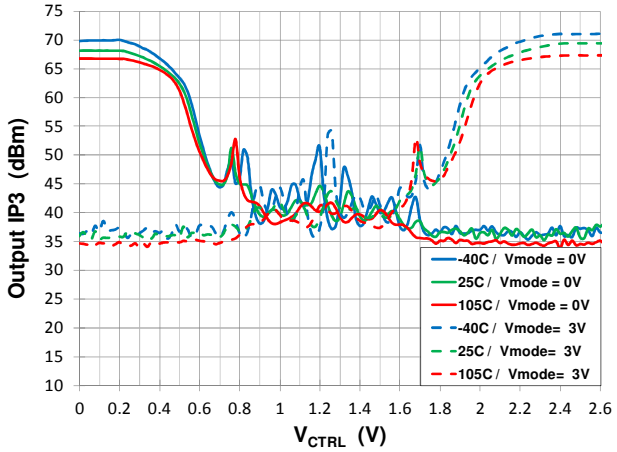


Figure 33. Input IP2 vs. V_{CTRL} over V_{MODE} and Temperature

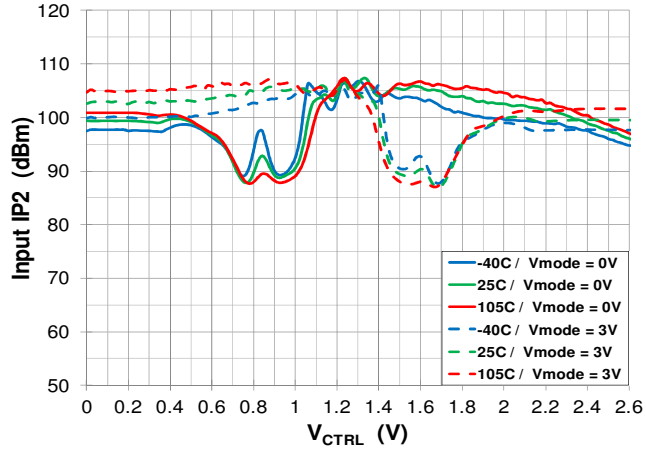


Figure 34. Output IP2 vs. V_{CTRL} over V_{MODE} and Temperature

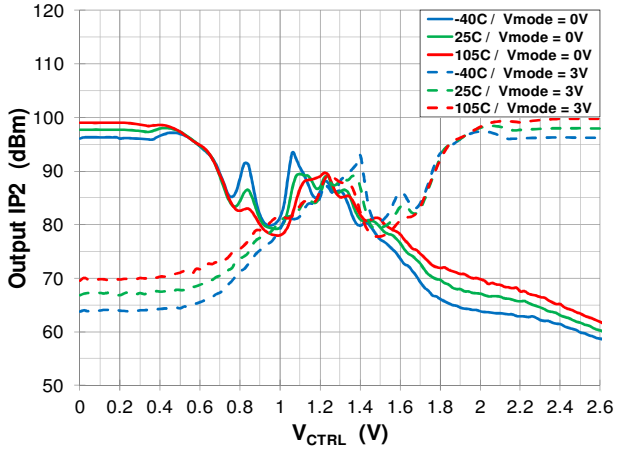


Figure 35. 2nd Harmonic Input Intercept Point vs. V_{CTRL} over V_{MODE} and Temperature

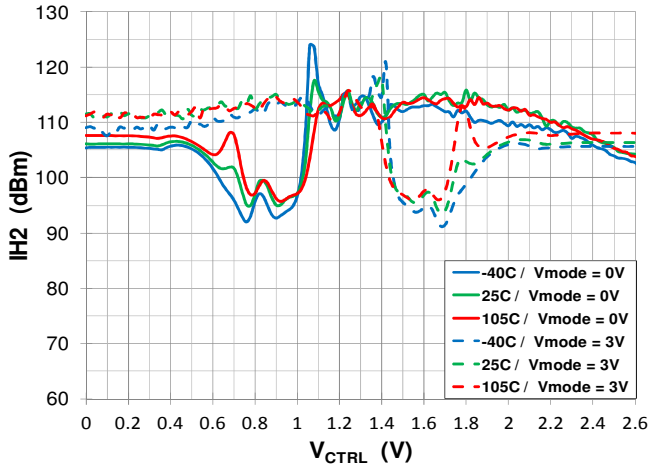
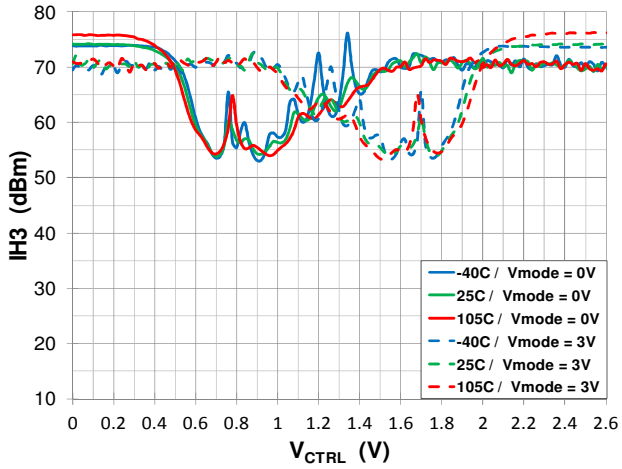


Figure 36. 3rd Harmonic Input Intercept Point vs. V_{CTRL} over V_{MODE} and Temperature



Typical Performance Characteristics – 2 GHz Attenuator [7]

Figure 37. Input IP3 vs. V_{CTRL} over RF Port and Temperature

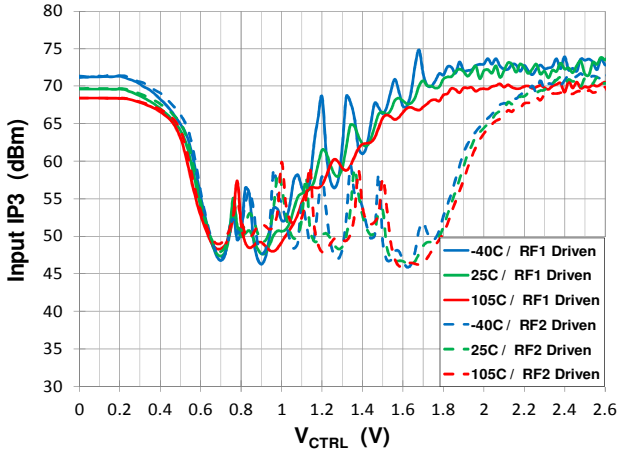


Figure 38. Output IP3 vs. V_{CTRL} over RF Port and Temperature

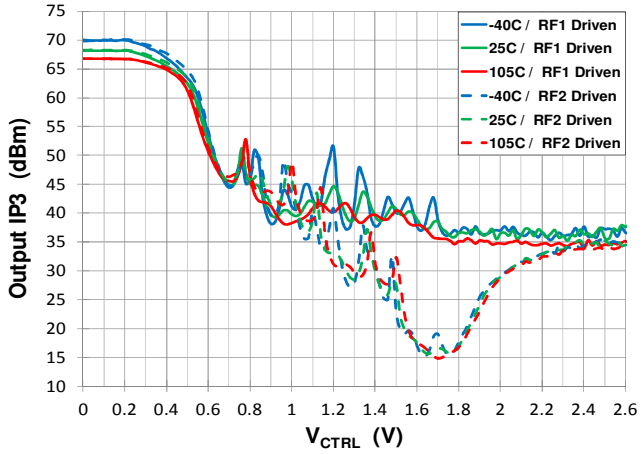


Figure 39. Input IP2 vs. V_{CTRL} over RF Port and Temperature

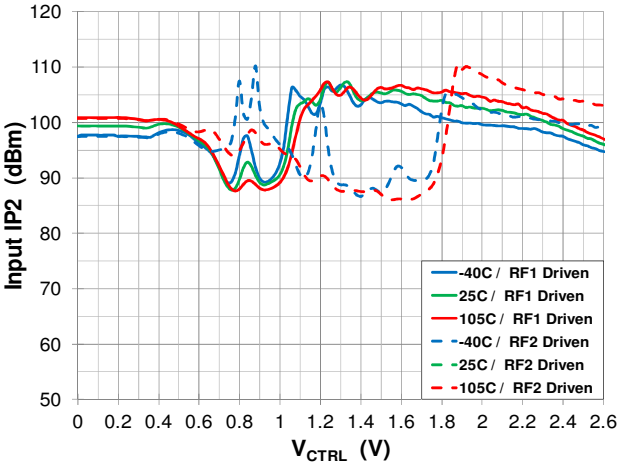


Figure 40. Output IP2 vs. V_{CTRL} over RF Port and Temperature

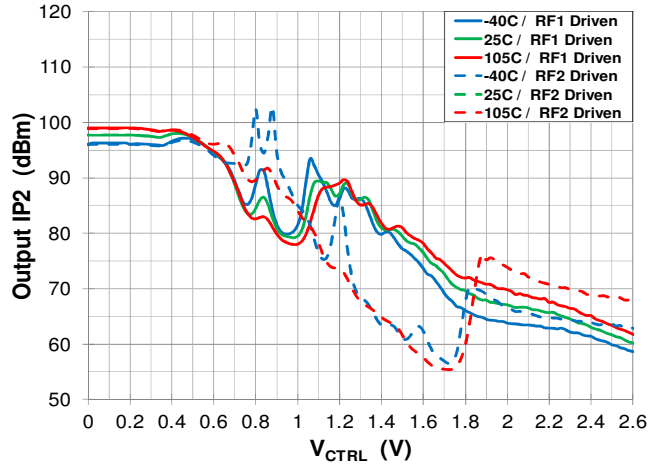


Figure 41. 2nd Harm Input Intercept Point vs. V_{CTRL} over RF Port and Temp

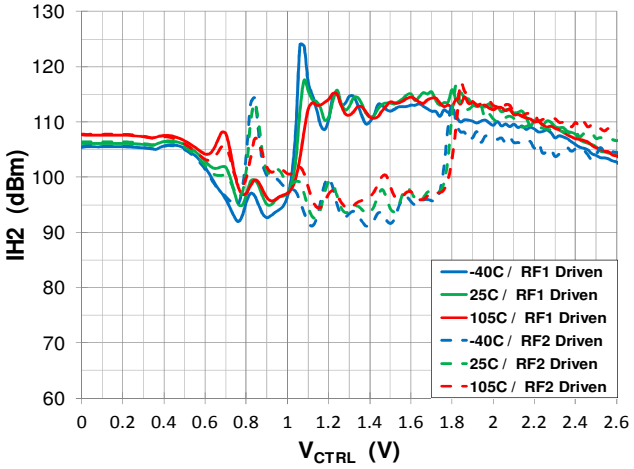
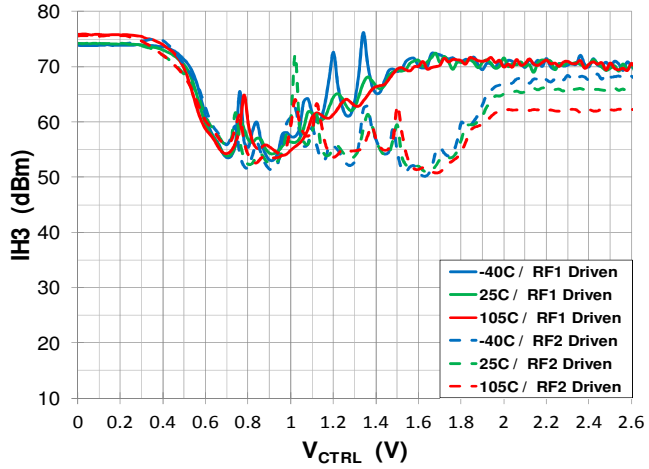


Figure 42. 3rd Harm Input Intercept Point vs. V_{CTRL} over RF Port and Temp



Typical Performance Characteristics – 2 GHz Attenuator [8]

Figure 43. Input IP3 vs. Attenuation over Temperature

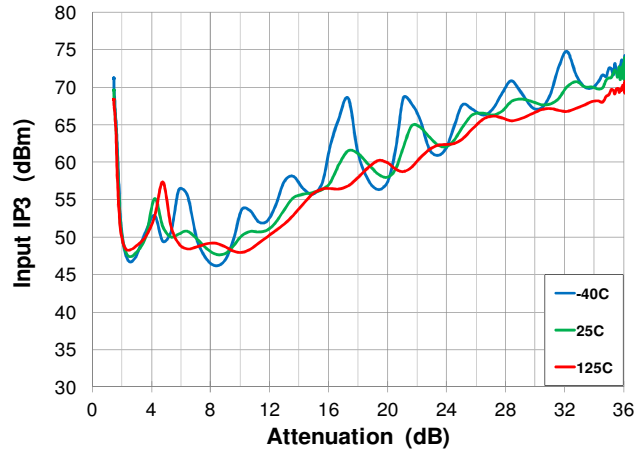


Figure 44. Output IP3 vs. Attenuation over Temperature

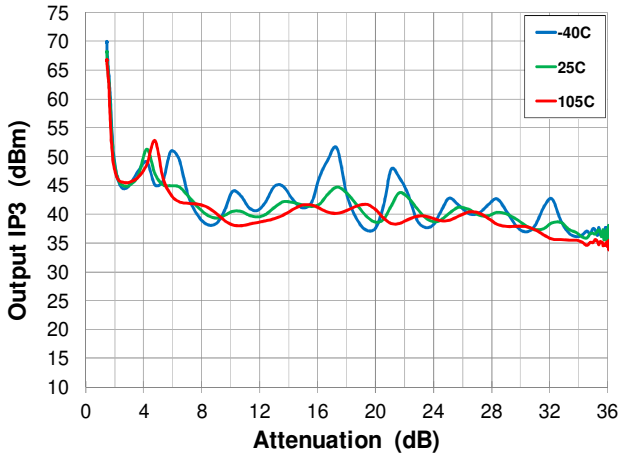


Figure 45. Input IP2 vs. Attenuation over Temperature

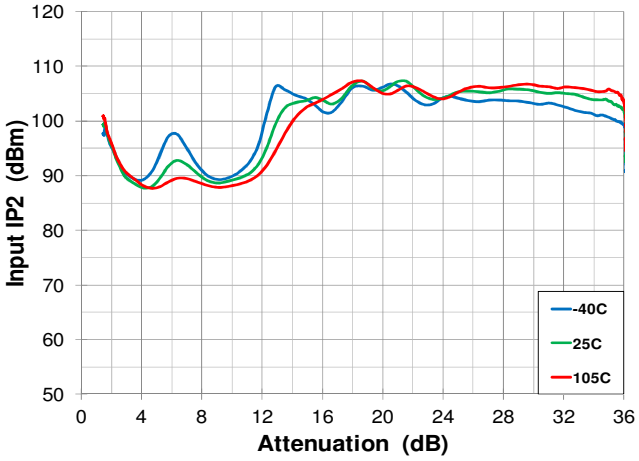


Figure 46. Output IP2 vs. Attenuation over Temperature

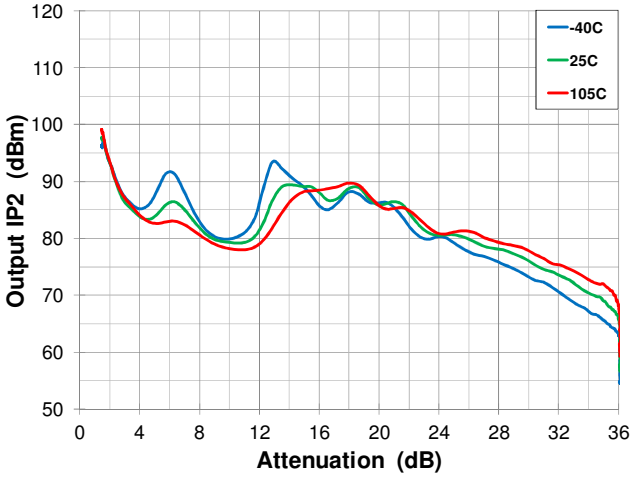


Figure 47. 2nd Harm Input Intercept Point vs. Attenuation over Temperature

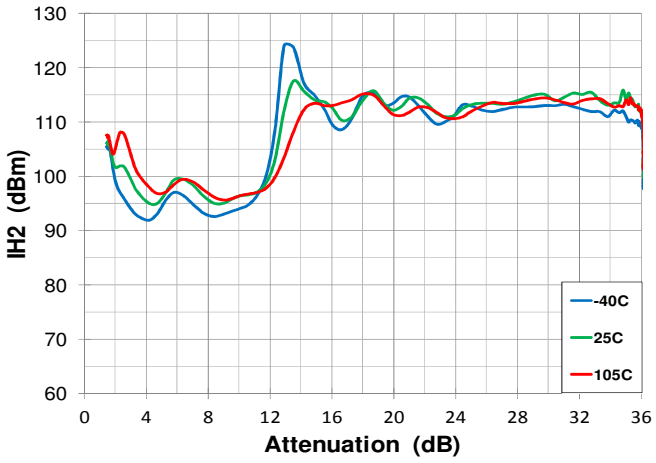
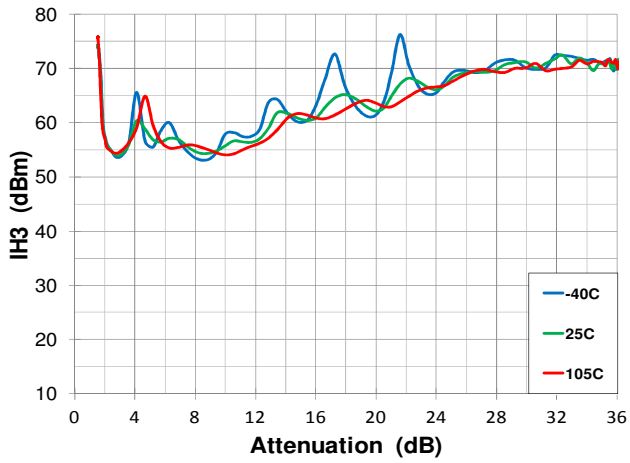


Figure 48. 3rd Harm Input Intercept Point vs. Attenuation over Temperature



Typical Performance Characteristics – 2 GHz Attenuator [9]

Figure 49. Input IP3 vs. Attenuation over RF Port and Temperature

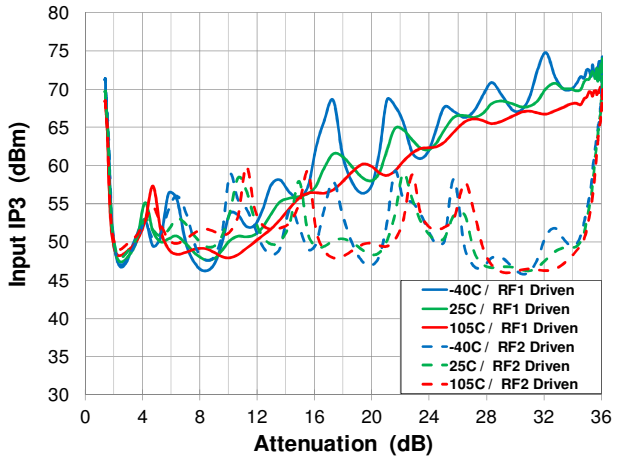


Figure 50. Output IP3 vs. Attenuation over RF Port and Temperature

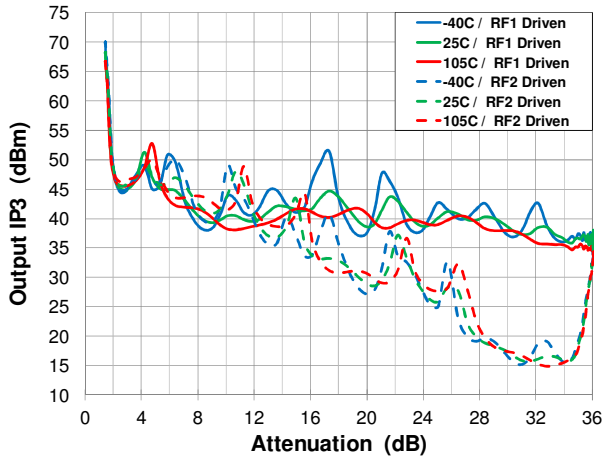


Figure 51. Input IP2 vs. Attenuation over RF Port and Temperature

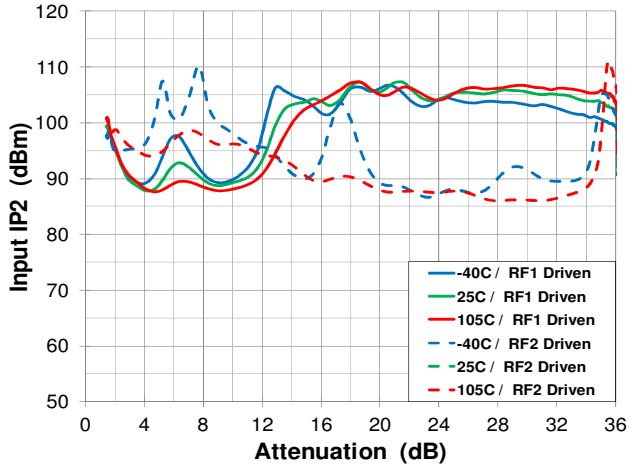


Figure 52. Output IP2 vs. Attenuation over RF Port and Temperature

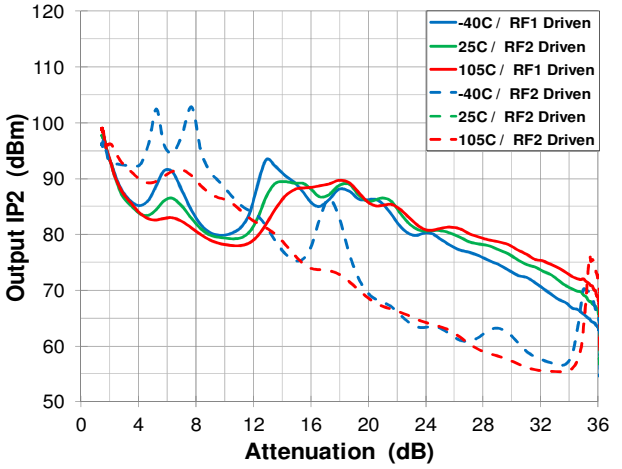


Figure 53. 2nd Harm Input Intercept Point vs. Attenuation over RF Port and Temp

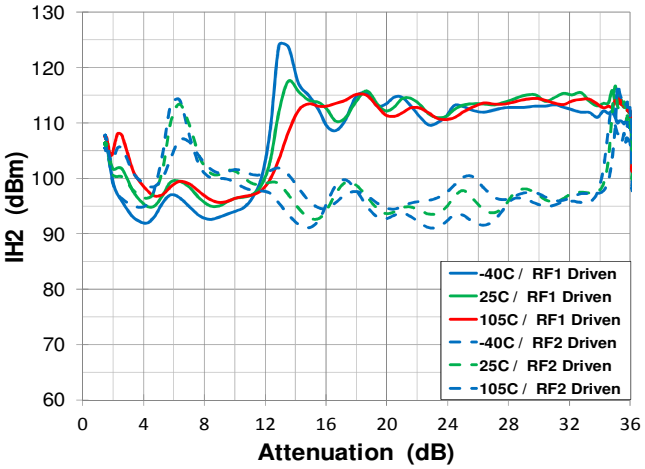
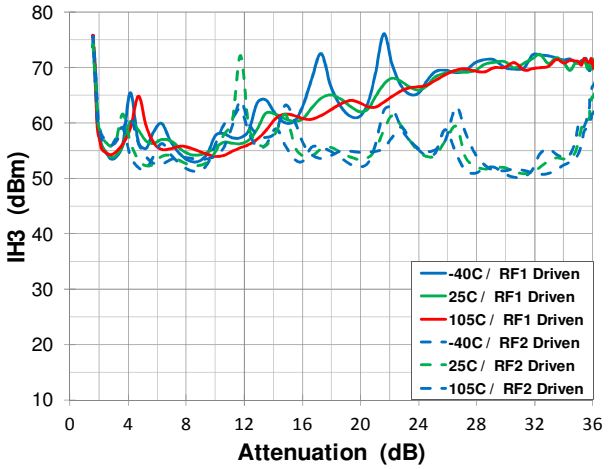


Figure 54. 3rd Harm Input Intercept Point vs. Attenuation over RF Port and Temp



Typical Performance Characteristics – Amplifier – Wide Band Mode [1]

Figure 55. Gain vs. Frequency over Temperature and Voltage – WB mode

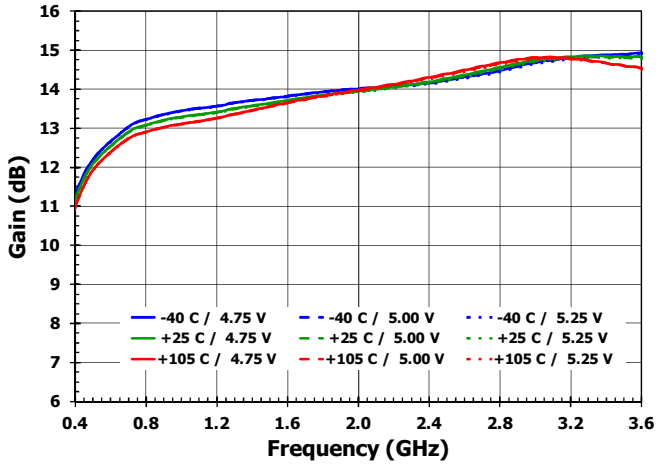


Figure 56. Reverse Isolation vs. Frequency over Temperature and Voltage – WB Mode

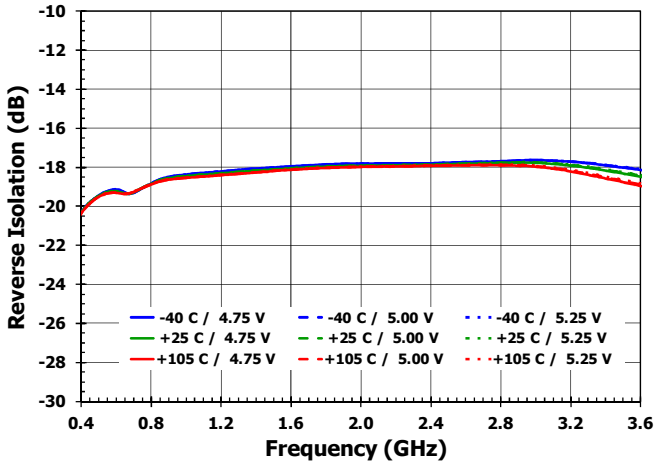


Figure 57. Input Match vs. Frequency over Temperature and Voltage – WB Mode

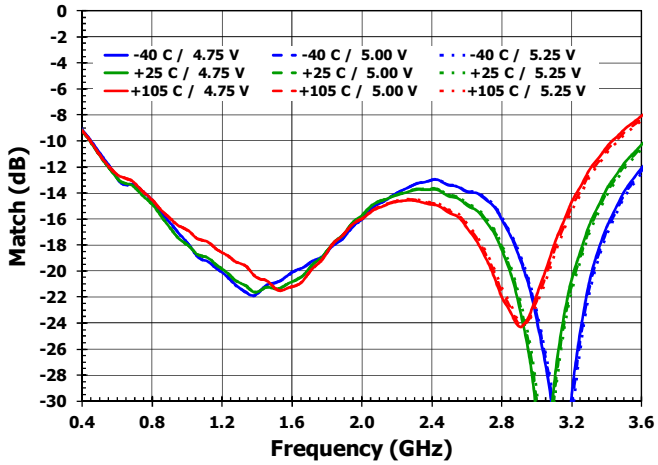


Figure 58. Output Match vs. Frequency over Temperature and Voltage – WB Mode

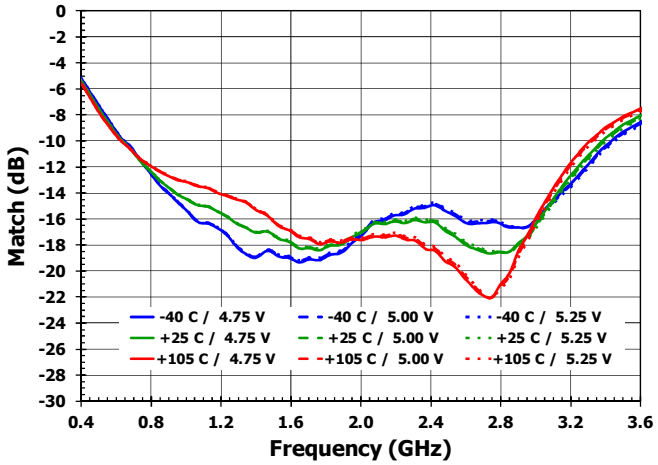


Figure 59. 2nd Harmonic vs. Fundamental Freq over Temp and Voltage – WB Mode

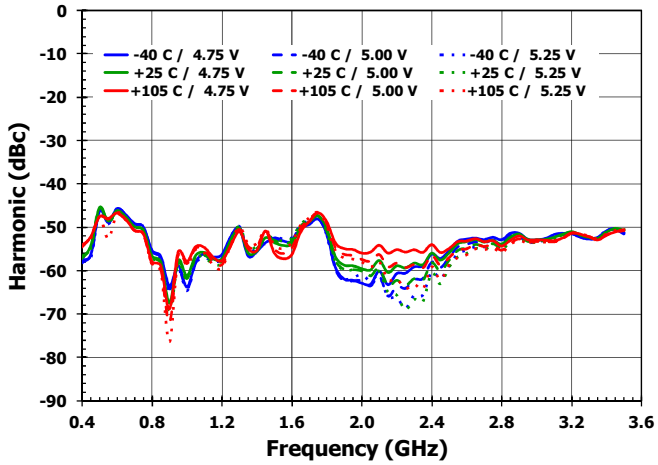
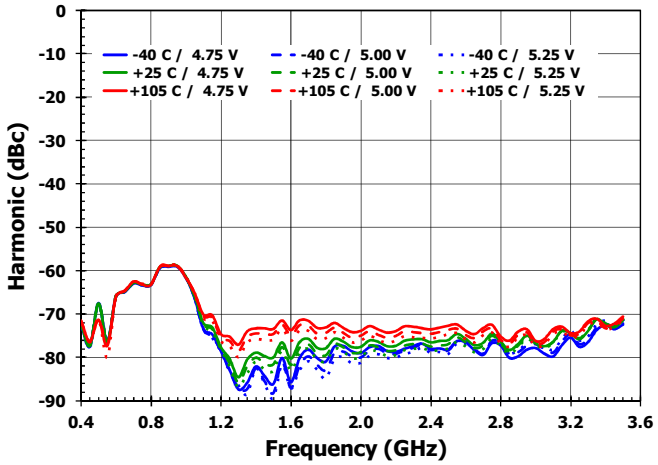


Figure 60. 3rd Harmonic vs. Fundamental Freq over Temp and Voltage – WB Mode



Typical Performance Characteristics – Amplifier – Wide Band Mode [2]

Figure 61. Output IP3 vs. Frequency over Temperature and Voltage – WB Mode

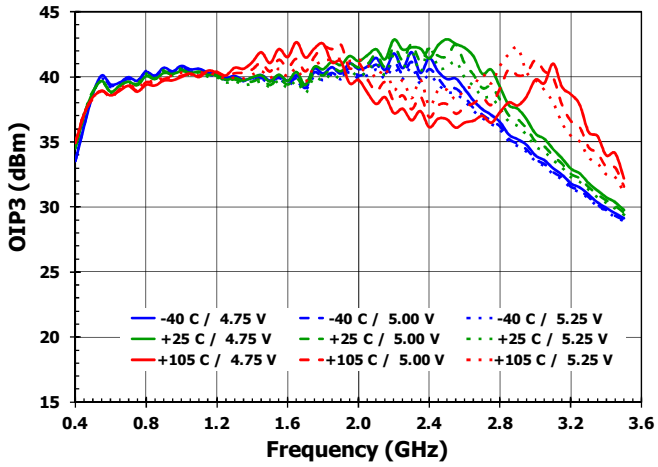


Figure 62. Output IP2H vs. Frequency over Temperature and Voltage – WB Mode

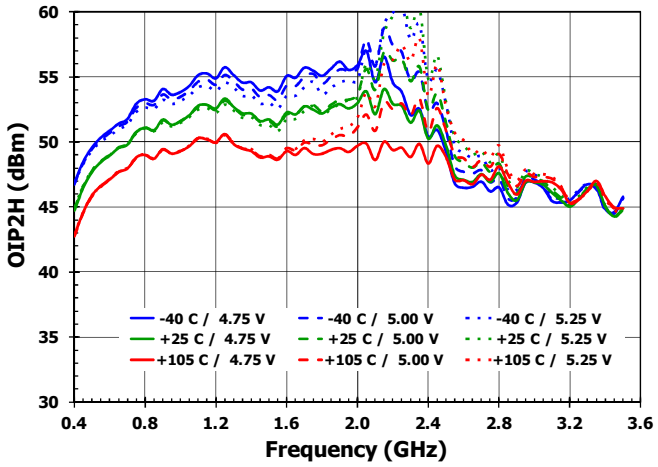


Figure 63. Output P1dB vs. Frequency over Temperature and Voltage – WB Mode

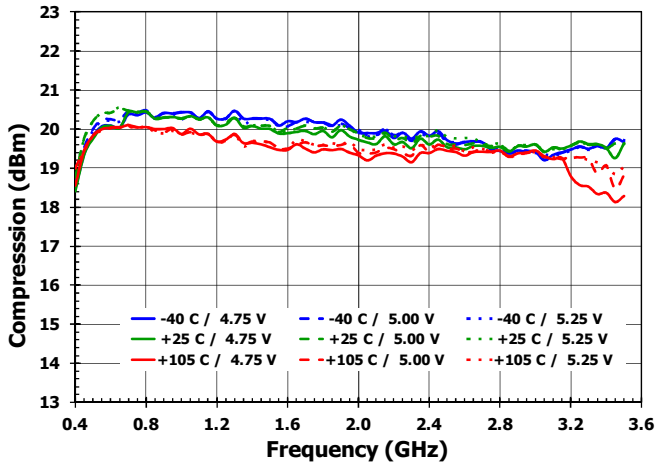
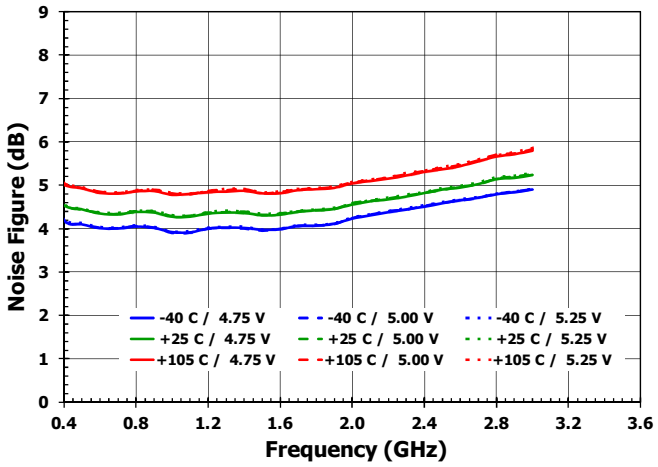


Figure 64. Noise Figure vs. Frequency over Temperature and Voltage – WB Mode



Typical Performance Characteristics – Amplifier – Low Band Mode [1]

Figure 65. Gain vs. Frequency over Temperature and Voltage – LB mode

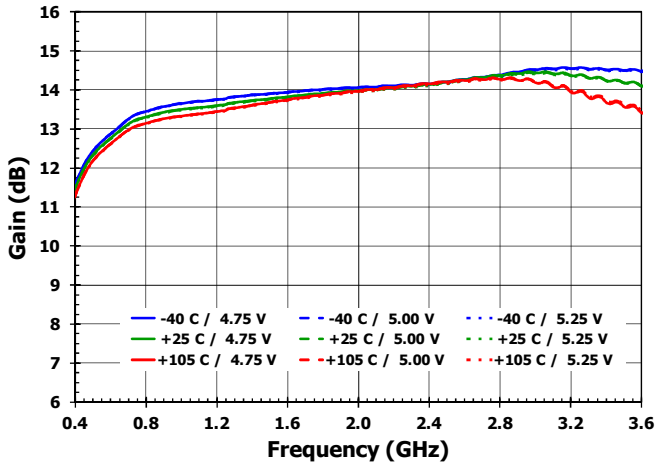


Figure 66. Reverse Isolation vs. Frequency over Temperature and Voltage – LB Mode

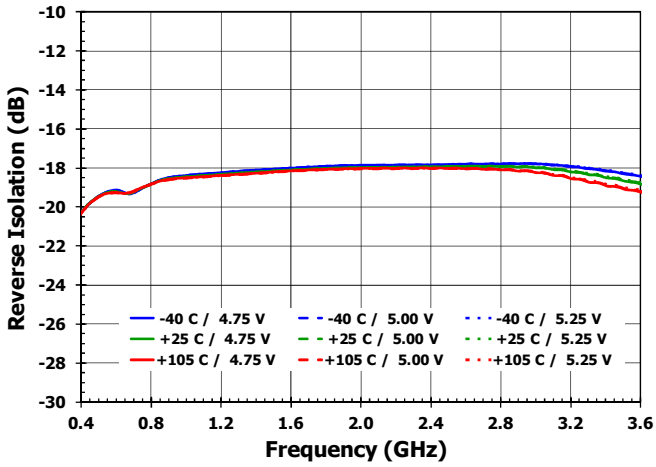


Figure 67. Input Match vs. Frequency over Temperature and Voltage – LB Mode

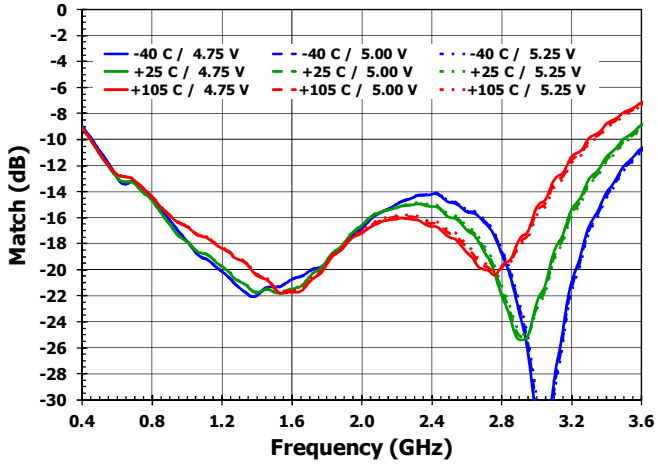


Figure 68. Output Match vs. Frequency over Temperature and Voltage – LB Mode

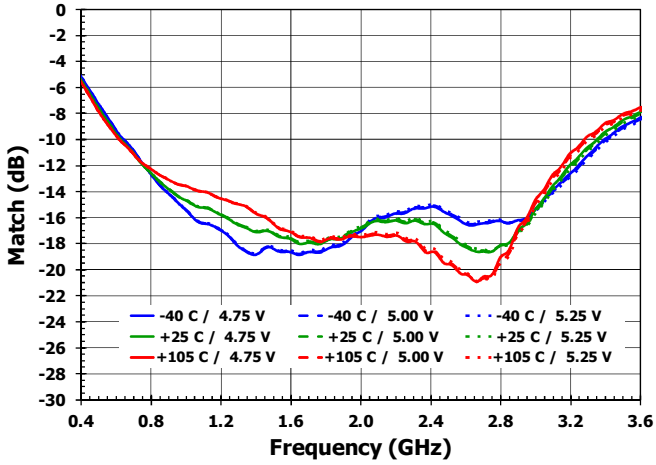


Figure 69. 2nd Harmonic vs. Fundamental Freq over Temp and Voltage – LB Mode

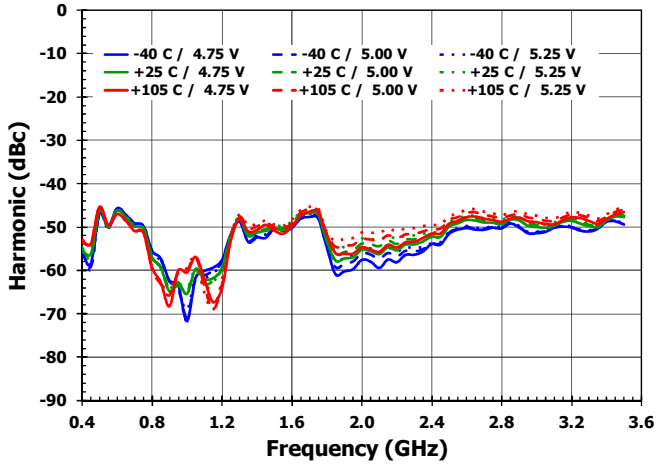
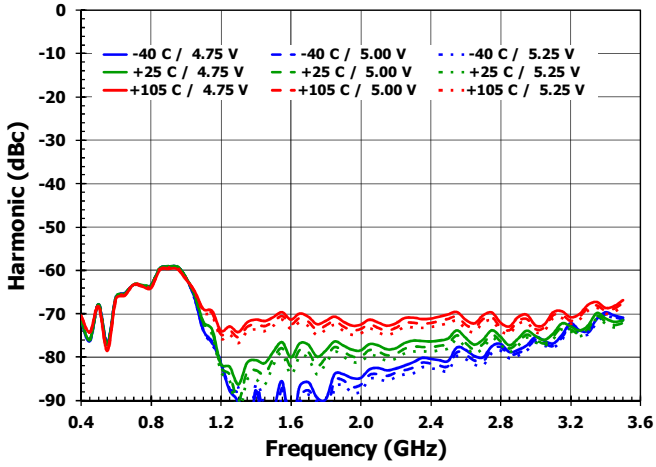


Figure 70. 3rd Harmonic vs. Fundamental Freq over Temp and Voltage – LB Mode



Typical Performance Characteristics – Amplifier – Low Band Mode [2]

Figure 71. Output IP3 vs. Frequency over Temperature and Voltage – LB Mode

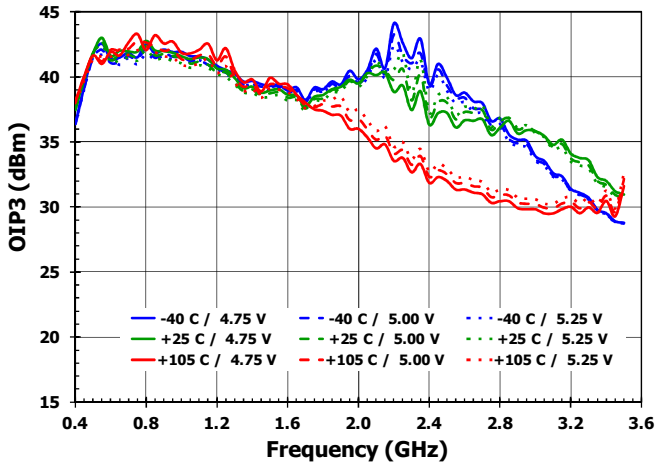


Figure 72. Output IP2H vs. Frequency over Temperature and Voltage – LB Mode

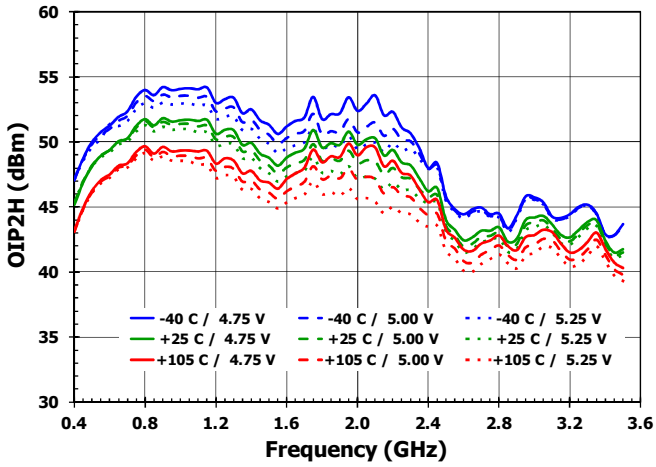
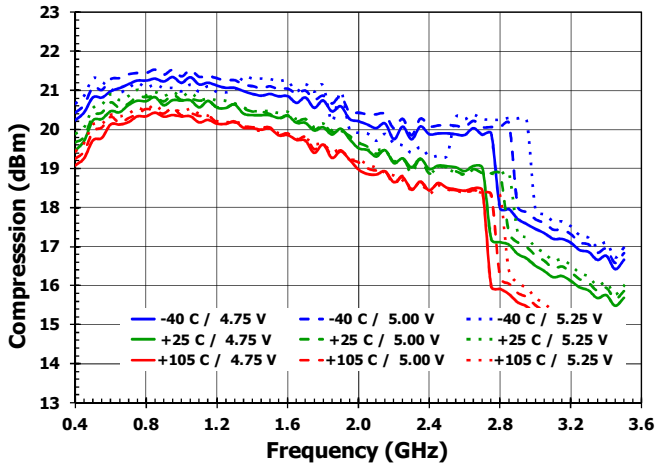


Figure 73. Output P1dB vs. Frequency over Temperature and Voltage – LB Mode



Typical Performance Characteristics – Amplifier – High Band Mode [1]

Figure 74. Gain vs. Frequency over Temperature and Voltage – HB mode

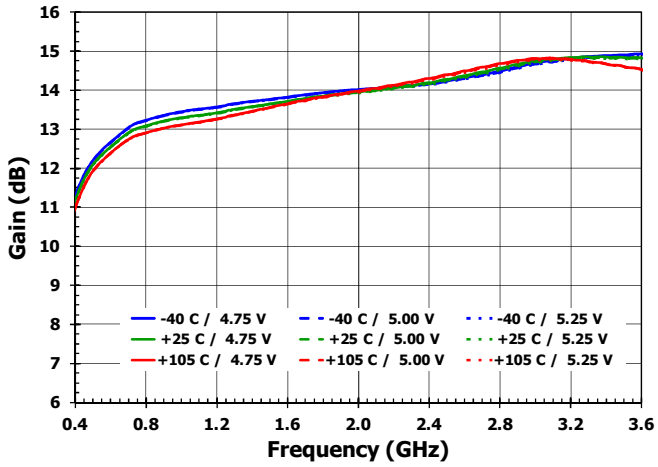


Figure 75. Reverse Isolation vs. Frequency over Temperature and Voltage – HB Mode

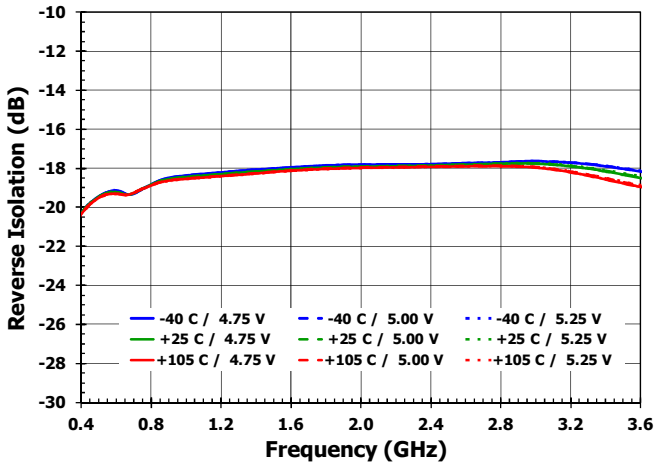


Figure 76. Input Match vs. Frequency over Temperature and Voltage – HB Mode

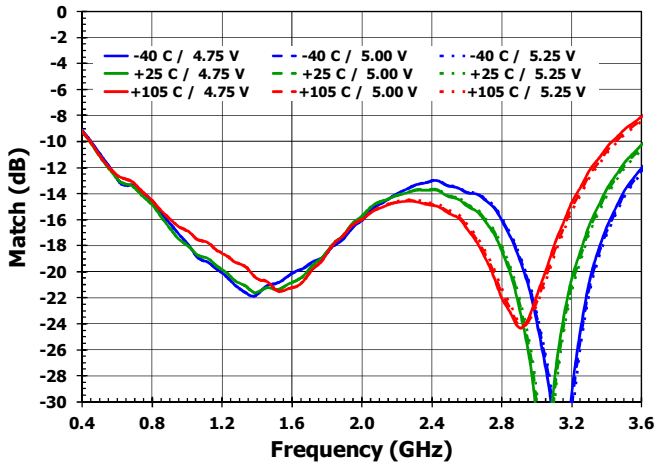


Figure 77. Output Match vs. Frequency over Temperature and Voltage – HB Mode

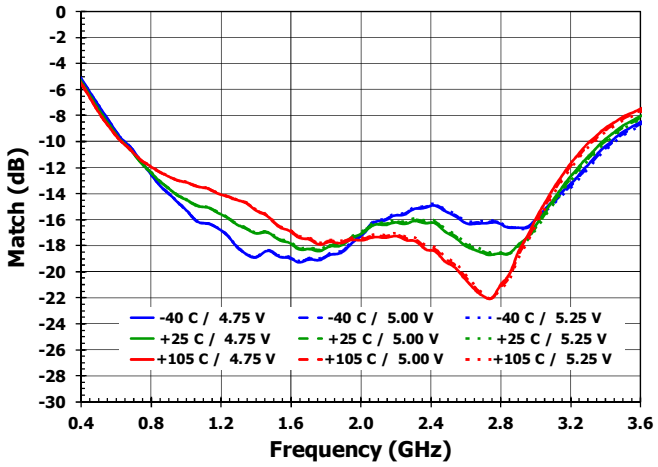


Figure 78. 2nd Harmonic vs. Fundamental Freq over Temp and Voltage – HB Mode

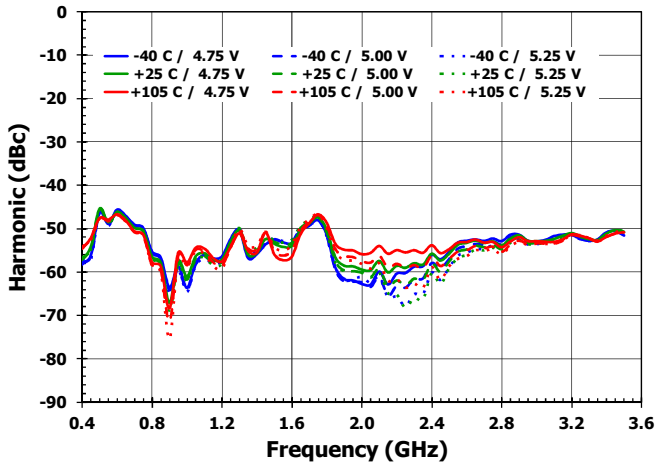
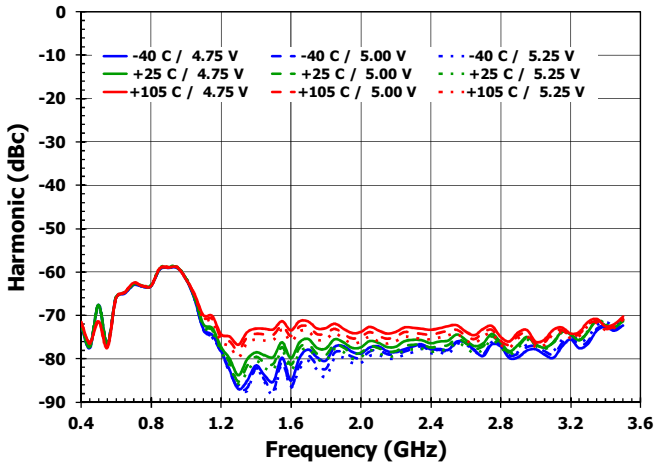


Figure 79. 3rd Harmonic vs. Fundamental Freq over Temp and Voltage – HB Mode



Typical Performance Characteristics – Amplifier – High Band Mode [2]

Figure 80. Output IP3 vs. Frequency over Temperature and Voltage – HB Mode

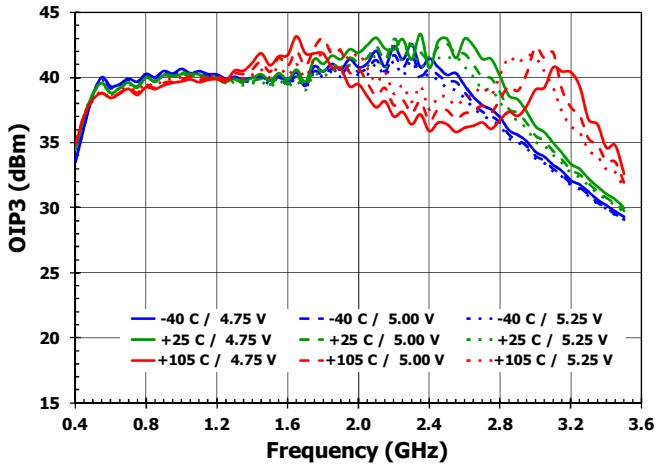


Figure 81. Output IP2H vs. Frequency over Temperature and Voltage – HB Mode

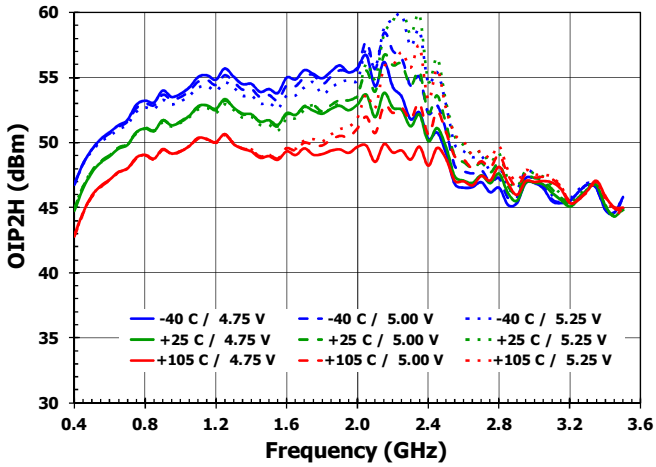
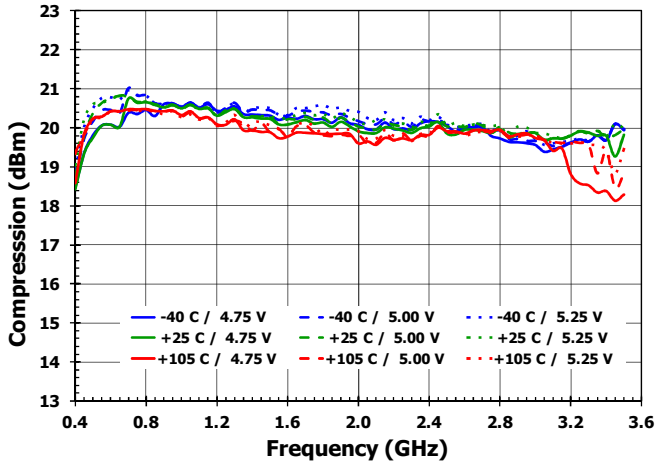


Figure 82. Output P1dB vs. Frequency over Temperature and Voltage – HB Mode



Device Usage

Table 8. Suggested Components for Optimum Linearity Performance of the Amplifier

Band	Frequency Range (MHz)	Band_Select Pin 10	RSET Pin 12 to GND (kΩ)	RDSET Pin 13 to GND (kΩ)	C1 (pF)	Icc (mA)
Low Band	400 – 1100	LB (Open)	2.1	9.1	9	106
Mid Band	1100 – 2200	HB (GND)	2.4	60.4	9	121
High Band	2200 – 3000	HB (GND)	2.4	90.9	6	121
Wide Band	400 – 3000	HB (GND)	2.4	60.4	9	121

Note: Mid Band and Wide Band use the same setting and component values.

Table 9. Control Pins Usage for the TX VGA

Pin Description	Pin	Input Level	Function
Band_Select	10	Logic LOW	Improves higher frequency performance
		Logic HIGH or Open Circuit	Improves lower frequency performance
STBY	11	Logic LOW or Open Circuit	Amplifier Powered On
		Logic HIGH	Amplifier Power Savings Mode
V_{MODE}	22	Logic LOW	Negative Attenuation Slope V_{CTRL} = 0.0 V results in insertion loss V_{CTRL} = 2.8 V results in maximum attenuation
		Logic HIGH	Positve Attenuation Slope V_{CTRL} = 2.8 V results in insertion loss V_{CTRL} = 0.0 V results in maximum attenuation

Application Information

The F2480 has been optimized for use in high performance RF applications from 400 to 3000 MHz.

STBY

The STBY control pin allows for power saving when the device is not in use. Setting the STBY pin as a logic low or by leaving the pin open will produce a full current operation mode. The STBY pin has an internal 1 MΩ resistor to ground. Applying logic high to this pin will put the part in the power savings mode.

Band_Select

The Band_Select control pin can be used to boost the current in the device. This is typical done in the High Band and Wide Band frequency applications by grounding the Band_Select pin. Internally there is a 1.5 MΩ pull-up resistor to set this pin high if no connection is made to it.

RSET and RDSET

RSET (pin 12) and RDSET (pin 13) use external resistors to ground to set the DC current in the device and to optimize the linearity performance of the amplifier stage. The resistor values in Table 8 can be used as a guide for the RF band of interest. By decreasing the resistor value to ground on the RSET pin will increase the DC current in the amplifier stage. The maximum operating DC current through RSET should never be higher than 1.5mA at T_{EP}= 105 ºC. The resistor to ground on RDSET is used to optimize the linearity performance in conjunction with the resistor on RSET.

Application Information (Cont.)

Amplifier Stability

The standalone amplifier is not unconditionally stable. Set RS = 5Ω and R1 = 500Ω to makes the circuit unconditionally stable. By increasing RS from the EVKIT value of 0Ω to 5Ω decreases the small signal gain by approx. 0.5dB and increases the NF by approx. 0.5dB. By changing R1 from an open to 500Ω decreases the small signal gain by approx. 0.5dB and decreases the OIP3 and OP1dB by approx. 0.5dB.

ATTEN_RF1 and ATTEN_RF2 Ports

The attenuator stage is bi-directional thus allowing ATTEN_RF1 or ATTEN_RF2 to be used as the RF input. As displayed in the Typical Operating Conditions curves, ATTEN_RF1 shows enhanced linearity. V_{CC} must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

Attenuator Default Start-up

The V_{CTRL} pin has an internal pull-down resistor while V_{MODE} does not have an internal pull-up or pull-down resistor and thus needs to be set externally. If V_{MODE} is set to a logic LOW and V_{CTRL} = 0V, the part will power up in the insertion loss state. If V_{MODE} is set to a logic HIGH and V_{CTRL} = 0V the part will power up in the maximum attenuation state. It is recommended that the user tie V_{MODE} to either ground or logic HIGH. Ensure the V_{MODE} and V_{CTRL} pin voltages meet the dependencies to V_{CC} as noted in the General Specifications Table during power up or under operation.

V_{CTRL}

The V_{CTRL} pin is used to control the attenuation of the attenuator stage. With V_{MODE} set to a logic LOW (HIGH), this places the device in a negative (positive) slope mode where increasing (decreasing) the V_{CTRL} voltage produces an increasing (a decreasing) attenuation from min attenuation (max attenuation) to max attenuation (min attenuation) respectively. See the General Specifications Table for the allowed control voltage range and its dependence on V_{CC}. Apply V_{CC} before applying voltage to the V_{CTRL} pin to prevent damage to the on-chip pull-up ESD diode. If this sequencing is not possible, then set resistor R6 to 1kΩ to limit the current into the V_{CTRL} pin.

V_{MODE}

The V_{MODE} pin is used to set the attenuation vs. V_{CTRL} slope. With V_{MODE} set to logic LOW (HIGH) this will set the attenuation slope to be negative (positive). A negative (positive) slope is defined as increasing (decreasing) attenuation with increasing (decreasing) V_{CTRL} voltage. The EVKit provides an on-board jumper to manually set the V_{MODE}. Installing a jumper on header J4 from V_{MODE} to GND (V_{IH}) to set the device for a negative (positive) slope. Resistors R2 and R3 on the evaluation board form a voltage divider to establish a compatible logic HIGH level using the V_{CC} supply as a source. The V_{MODE} does not have an internal pull-up or pull-down resistor so it must be set externally.

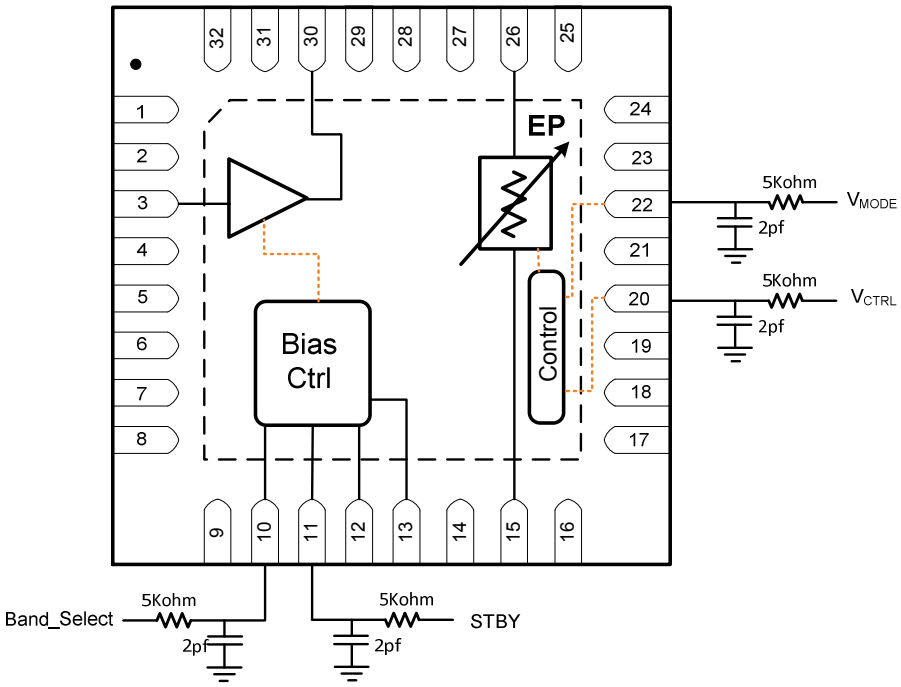
Power Supplies

A common 5V power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (± 0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 10, 11, 20, and 22 as shown below. Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, values will need to be adjusted accordingly so as to not load the control line.

Figure 83. Control Pin Components for Signal Integrity



Evaluation Kit Picture

Figure 84. Top View

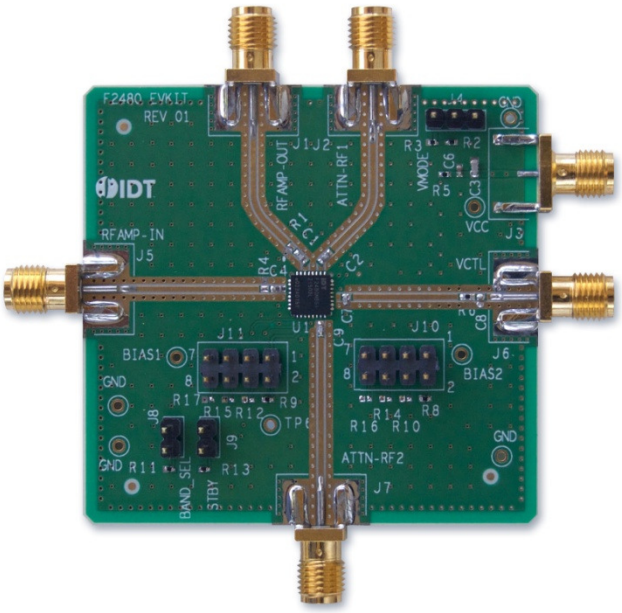
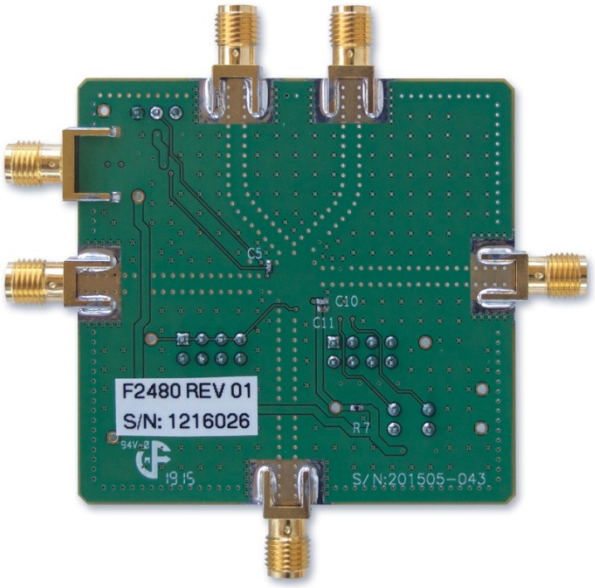
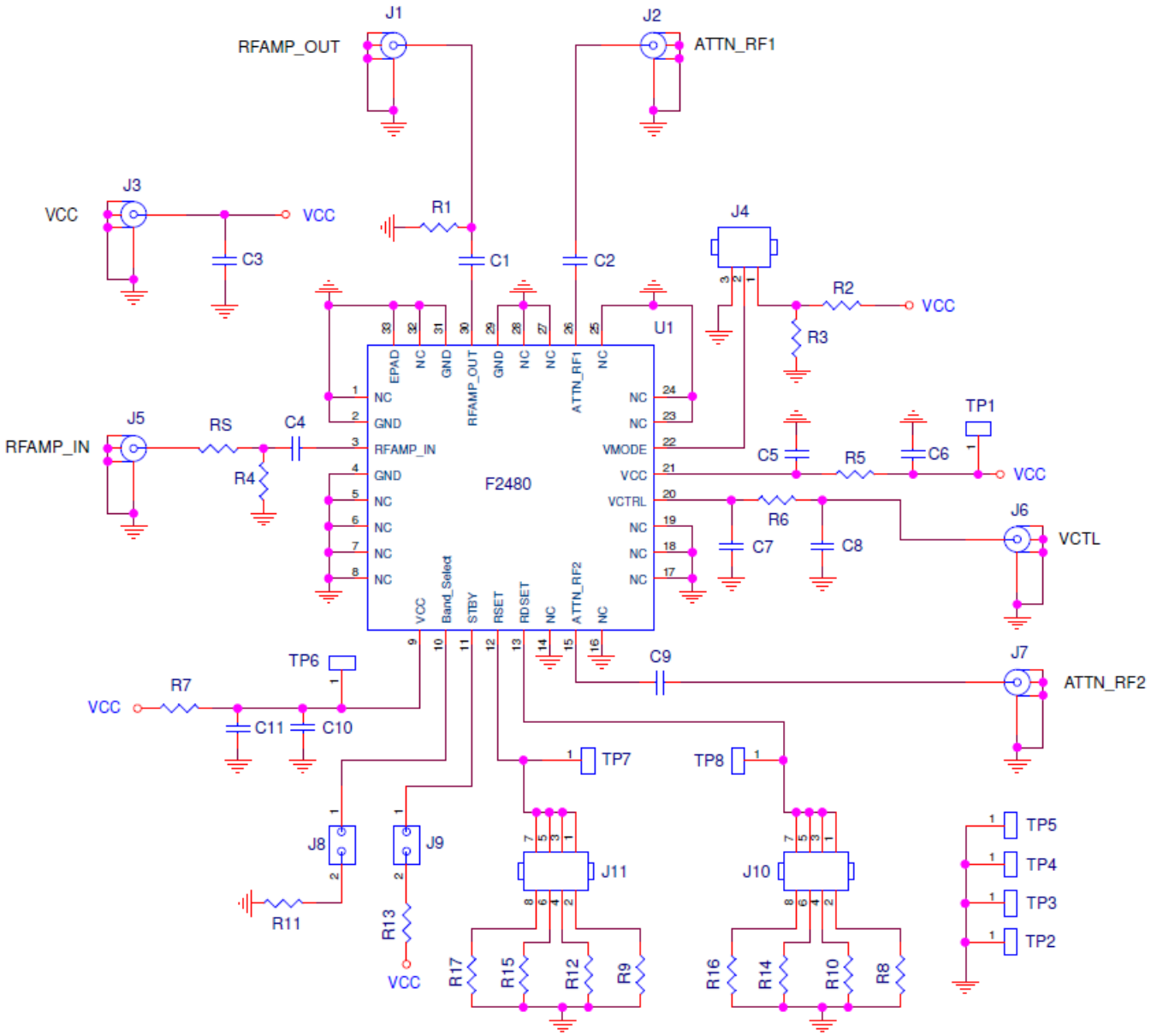


Figure 85. Bottom View



Evaluation Kit / Applications Circuit

Figure 86. Electrical Schematic



Note: RS and R1 are used to produce unconditional stability for the amplifier and are not included in the performance stated in this datasheet. See applications information section above.

Table 10. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	9pF ±0.25pF, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H9R0C	Murata
C2, C9	2	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C3	1	10µF ±20%, 6.3V, X5R Ceramic Capacitor (0603)	GRM188R60J106M	Murata
C4	1	47pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H470J	Murata
C5, C7, C10	3	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C6, C8	2	10nF ±5%, 50V, X7R Ceramic Capacitor (0603)	GRM188R71H103J	Murata
C11	1	0.1µF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
RS [a]	1	0Ω ±1%, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
R1 [a]	0	Not Installed		
R2, R3	2	100kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
R4	0	Not Installed		
R5, R6, R7, R11, R13	5	0Ω ±1%, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
R8	1	60.4kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF6042X	Panasonic
R9	1	2.4kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2401X	Panasonic
R10, R12	0	Not Installed, Alternate 1 Bias Resistor (0402)		
R14, R15	0	Not Installed, Alternate 2 Bias Resistor (0402)		
R16, R17	0	Not Installed, Alternate 3 Bias Resistor (0402)		
TP1 – TP5	5	Test Point	5021	Keystone Electronics
J1, J2, J3, J5, J6, J7	6	SMA End-Launch (small)	142-0711-821	Emerson Johnson
J4	1	CONN HEADER VERT SGL 3 POS GOLD	961103-6404-AR	3M
J8, J9	2	CONN HEADERS VERT SGL 2 POS GOLD	961102-6404-AR	3M
J10, J11	2	2 x 4 HEADER VERT	67997-108HLF	FCI
U1	1	RF Amplifier / VVA	F2480NBGI	IDT
	1	Printed Circuit Board	F2480 PCB	IDT

a. The data included in this datasheet does not include these as stability resistors. For the amplifier to be unconditionally stable RS and R1 must be installed. See the Applications Section for more details.

Evaluation Kit Operation

Below is a basic setup procedure for configuring and testing the F2480 EVKit.

Pre-Configure EVKit:

The section is a guide to setup the EVKit for testing. Remove the J8 header shunt if the application is for low band operation. All other operating bands require the J8 shunt to be installed. Remove any shorting shunt from header J9 which will allow the part to be in the operating mode when powered up. Verify that there is a shunt between pins 1, 2 of J11 and pins 1, 2 of J10. These pins configure the PCB to use the installed bias resistors to support Mid Band and Wide Band (see Table 8). Alternate resistors can be installed on the unpopulated resistor slots on J11 and J10 to support the other operating bands (see Additional EVKit Information section). If a negative (positive) attenuator control slope is desired, connect a shunt between pins 1 and 2 (2 and 3) of header J4.

Power Supply Setup:

Without making any connections to the EVKit, setup one fixed power supply for 5V with a current limit of 160mA and one variable supply set to 0V with a current limit of 10mA. Disable both power supplies.

RF Test Setup:

Set up the RF test set to the desired frequency and power ranges within the specified operating limits noted in this datasheet.
Disable the output power of all the RF sources.

Connect EVKit to Test setup:

With the RF sources and power supplies disabled connect the fixed 5V power supply to connector J3, the variable supply to J6 and the RF connections to the desired RF ports. Terminate any unused RF ports (J1, J2, J5, J7) into 50Ω.

Powering Up the EVkit:

Enable the 5V supply and observe a DC current of approx. 120mA.
Enable the variable supply.
Enable the RF sources. Verify that the DC current stays about 120mA to verify that the amplifier is not being over driven by RF input power.
If the J4 connection is set for a negative (positive) attenuation slope then increasing the variable supply with produce increased (decreased) attenuation for the attenuator path (J2 to J7).

Powering Down the EVkit:

Disable the RF power being applied to the device.
Adjust the variable supply down to 0V and disable it.
Disable the 5V supply.
Disconnect EVKit from the RF test stand.

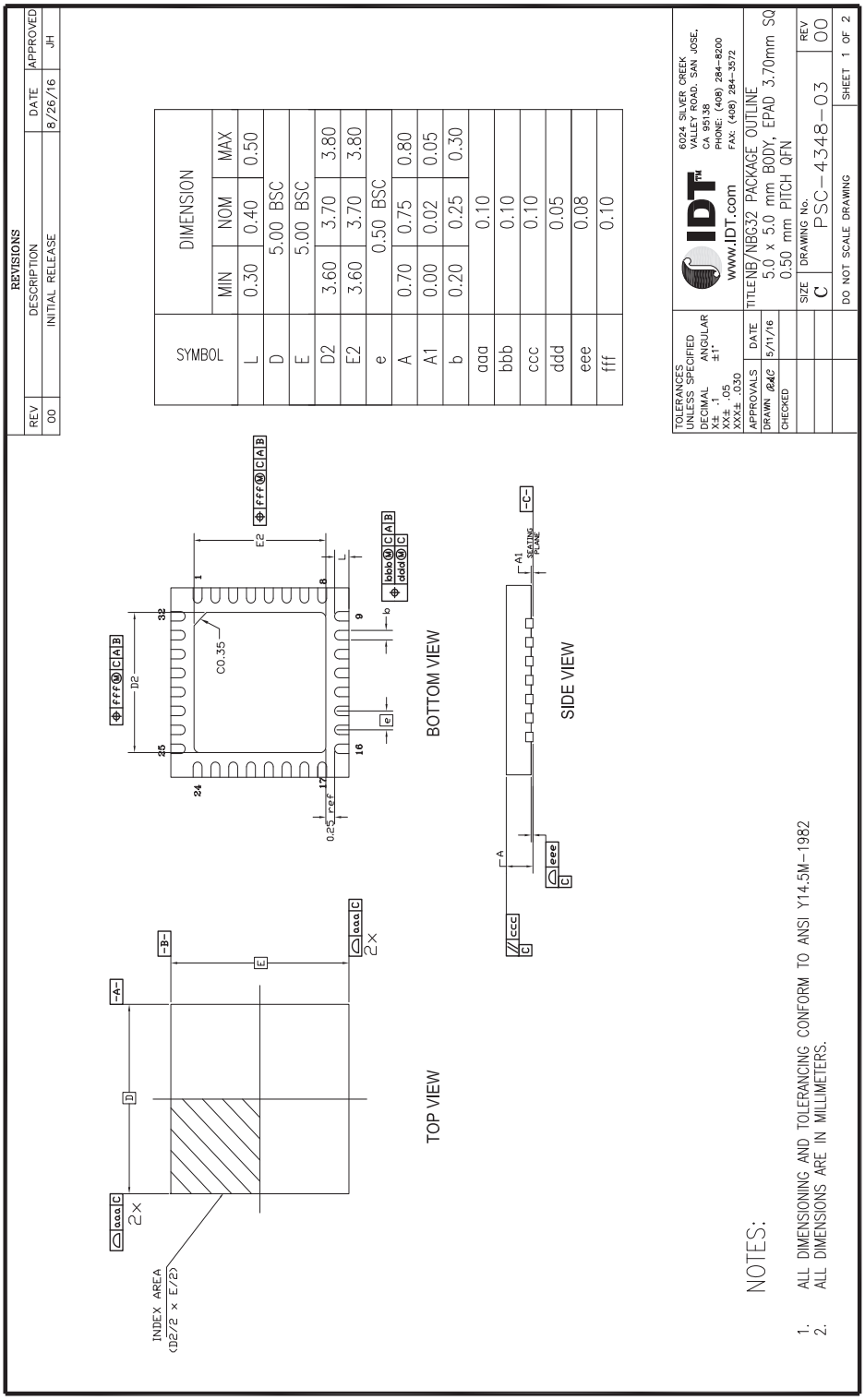
Additional EVKIT Information

EVKit modification to support additional Table 8 bias settings:

The standard EVKit is setup for only one RSET / RDSET bias setting (pins 12/ 13 on the F2480) noted in Table 8.
Additional Table 8 values (R12/R10, R15/R14, R17/ R16) can be installed on the board to allow for different jumper settings. Never have two shunts installed at the same time on header J11 since this may produce excessive bias current and damage the part. As the resistance to ground decreases on pin 12 of the device, the DC current will increase. The DC current of the EVKIT should never exceed 250mA.

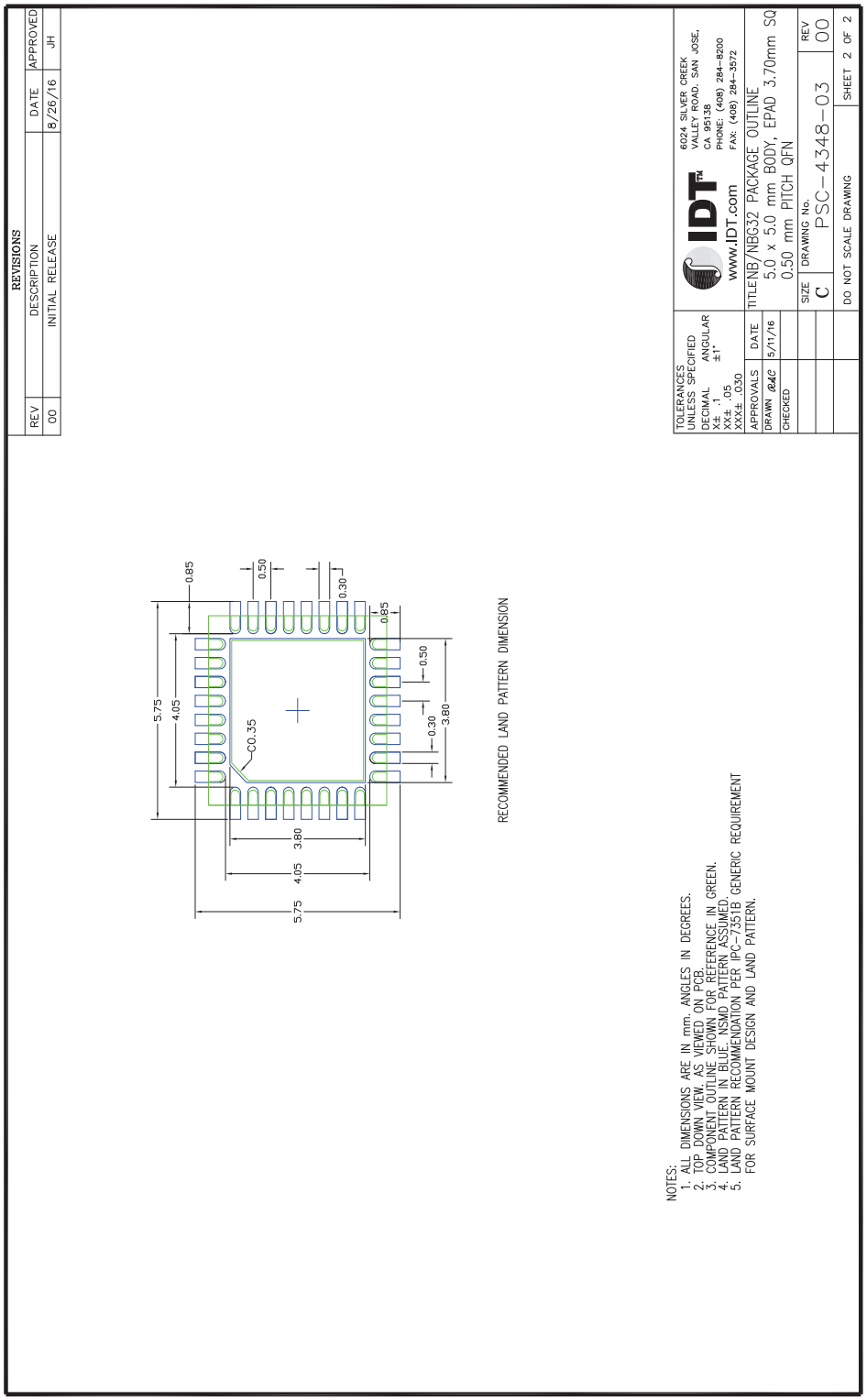
Package Drawings

Figure 87. Package Outline Drawing (5 x 5 x 0.75 mm 32-pin TQFN), NBG32



Recommended Land Pattern

Figure 88. Recommended Land Pattern



Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2480NBGI	5 x 5 x 0.75 mm 32-TQFN	1	Tray	-40 to +105 °C
F2480NBGI8	5 x 5 x 0.75 mm 32-TQFN	1	Tape and Reel	-40 to +105 °C
F2480EVBI	Evaluation Board			

Marking Diagram

Line 1 - Company.
Line 2 - Product Number.
Line 3 - “Z” the initial alpha characters are the ASM Test Step.
Line 3 - “1503” is two digits for the year and week that the part was assembled (2015, Week 3).
Line 3 - “L” or last alpha characters are the Assembler Code.
Line 4 - Near Dot – Lot Code.

Revision History

Revision Date	Description of Change
March 23, 2017	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.