Description

The F2955 is a high reliability, low insertion loss, 50Ω SP5T absorptive RF switch designed for a multitude of RF applications, including wireless communications. This device covers a broad frequency range from 50MHz to 8000MHz. In addition to providing low insertion loss, the F2955 also delivers excellent linearity and isolation performance while providing a 50Ω termination to the unused RF input ports. The F2955 also includes a patent-pending constant impedance ($K_{|Z|}$™) feature. $K_{|Z|}$ improves system hot switching ruggedness, minimizes LO pulling in VCOs, and reduces phase and amplitude variations in distribution networks. It is also ideal for dynamic switching/selection between two or more amplifiers while avoiding damage to upstream/downstream sensitive devices, such as power amplifiers (PAs) and analog-to-digital converters (ADCs).

The F2955 uses a single positive supply voltage supporting three logic control pins using either 3.3V or 1.8V control logic. Connecting a negative voltage to pin 20 disables the internal negative voltage generator and becomes the negative supply.

Competitive Advantage

The F2955 provides constant impedance in all RF ports during transitions, improving a system's hot-switching ruggedness. The device also supports high-power handling and high isolation, particularly important for DPD receiver use.

- Constant impedance $K_{|Z|}$ during switching transition
- RFX to RFC isolation = 49dB at 4GHz
- Insertion loss = 1.1dB at 4GHz
- IIP3: +60.5dBm at 4GHz
- Extended temperature: -40°C to +105°C

Typical Applications

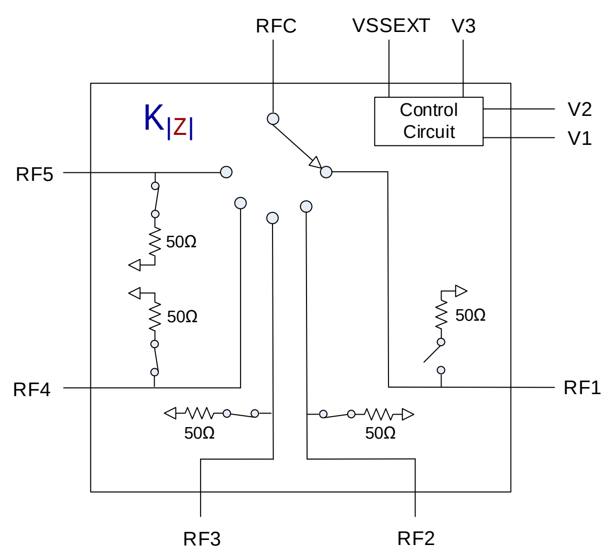
- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 Systems
- Digital Pre-distortion
- Point-to-Point Infrastructure
- Public Safety Infrastructure
- Military Systems, JTRS Radios
- Cable Infrastructure
- Test / ATE Equipment

Features

- Five symmetric, absorptive RF ports
- High isolation: 49dB at 4000MHz
- Low insertion loss: 1.1dB at 4000MHz
- High linearity:
  - IIP2 of 114dBm at 2000MHz
  - IIP3 of 60.5dBm at 4000MHz
- High operating power handling:
  - 33dBm CW on selected RF port
  - 27dBm on terminated ports
- Single 2.7V to 5.5V supply voltage
- External negative supply option
- 3.3V and 1.8V compatible control logic
- Operating temperature: -40°C to +105°C
- 4 × 4 mm 24-QFN package
- Pin compatible with competitors

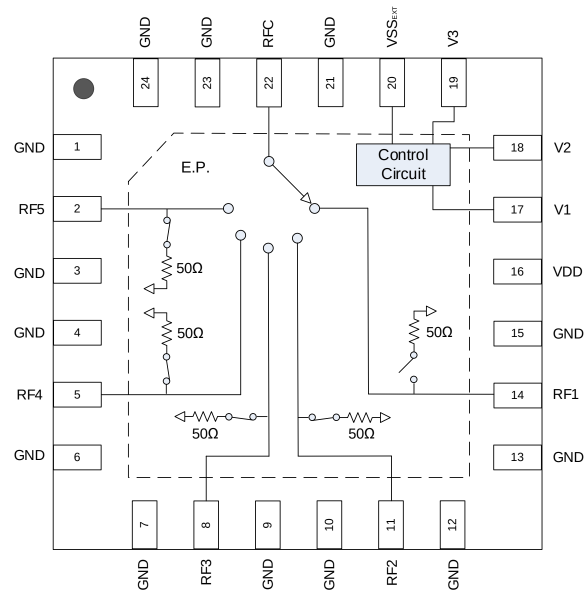
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4 x 4 x 0.75 mm 24-QFN – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 3, 4, 6, 7, 9, 10, 12, 13, 15, 21, 23, 24	GND	Ground these pins as close to the device as possible.
2	RF5	RF5 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
5	RF4	RF5 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
8	RF3	RF5 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
11	RF2	RF5 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
14	RF1	RF5 Port. Matched to 50Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	V_{DD}	Power Supply. Bypass to GND with capacitors as shown in the “Typical Application Circuit” (Figure 39) as close as possible to the pin.
17	V1	Control pin to set the switch state. See Table 8.
18	V2	Control pin to set the switch state. See Table 8.
19	V3	Control pin to set the switch state. See Table 8.
20	VSS_{EXT}	External VSS negative voltage control. Connect to ground to enable on-chip negative voltage generator. To bypass and disable on chip generator connect this pin to an external VSS.
22	RFC	RF Common Port. Matched to 50Ω when one of the 5 RF ports is selected. If this pin is not 0V DC, then an external coupling capacitor must be used.
	EPAD	Exposed Paddle. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
V_{DD} to GND	V_{DD}	-0.3	+5.5	V
V1, V2, V3 to GND	V_{CNTL}	-0.3	Lower of (3.6,V_{DD}+0.3)	V
RF1, RF2, RF3, RF4, RF5, RFC to GND	V_{RF}	-0.3	+0.3	V
VSS_{EXT} to GND	VSS_{EXT}	-4.0	+0.3	V
Input Power for Any One Selected RF Through Port (V_{DD} applied at 2GHz and T_{EPAD} = +85°C)	$P_{MAXTHRU}$	-	37	dBm
Input Power for Any One Selected RF Terminated Port (V_{DD} applied at 2GHz and T_{EPAD} = +85°C)	$P_{MAXTERM}$	-	30	dBm
Input Power for RFC When in the All Off State (V_{DD} applied at 2GHz and T_{EPAD} = +85°C)	P_{MAXCOM}	-	33	dBm
Continuous Power Dissipation[a] (T_{EPAD} = +95°C Max)	P_{CONT}	-	3	W
Maximum Junction Temperature	T_{JMAX}	-	+125	°C
Storage Temperature Range	T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}	-	+260	°C
ESD Voltage – HBM (Per JESD22-A114)	V_{ESDHBM}	-	1500 (Class 1C)	V
ESD Voltage – CDM (Per JESD22-C101)	V_{ESDCDM}	-	1000 (Class C3)	V

[a] T_{EPAD} = Temperature of the exposed paddle

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

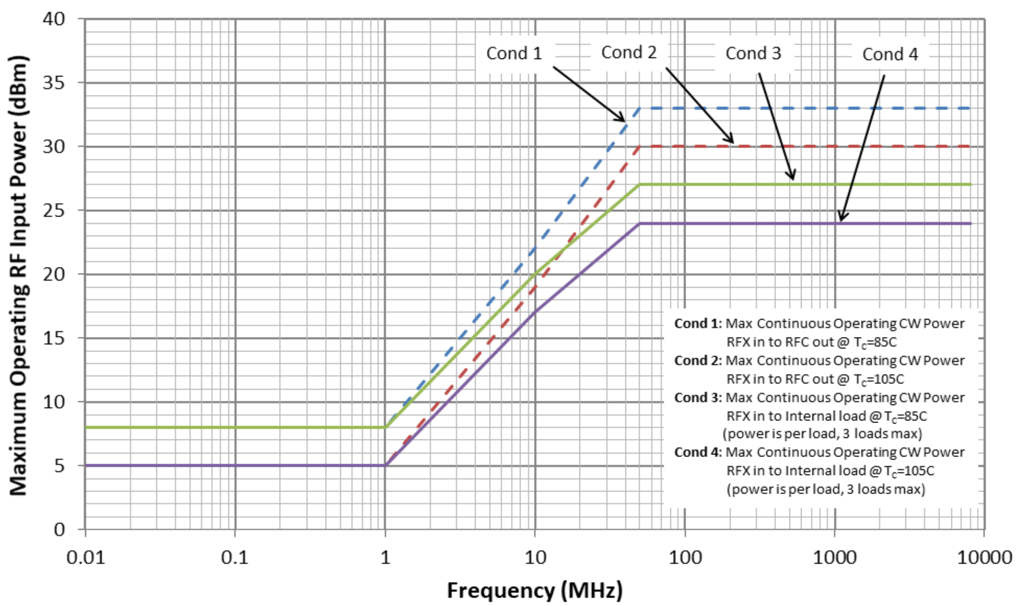
Parameter	Symbol	Condition		Minimum	Typical	Maximum	Unit
Power Supply Voltages	V_{DD}	Pin 20 grounded		2.7	-	5.25	V
		Pin 20 driven with VSS_{EXT}		2.7	-	5.25	
	VSS_{EXT}	Negative supply [a]		-3.6	-3.4	-3.2	
Operating Temperature Range	T_{EPAD}	Exposed paddle		-40	-	+105	°C
RF Frequency Range	f_{RF}	-		50	-	8000	MHz
RF Continuous Input CW Power [b]	P_{RF}	Selected ports		-	-	33	dBm
		Terminated ports [c]		-	-	27	
RF Continuous Input CW Power for Hot RF Switching [c]	P_{RFSW}	RFC as the input	Switch to RF1 through RF5	-	-	27	dBm
			Switched into or out of all off state	-	-	24	
		RF1 through RF5 as the inputs	Switched to RFC or into term[c]	-	-	27	
			Switch into or out of all off conditions	-	-	27	
RF1 through 5 Port Impedance	Z_{RFx}	-		-	50	-	Ω
RFC Port Impedance	Z_{RFC}	-		-	50	-	

[a] For normal operation, connect VSS_{EXT} (pin 20) = 0V to GND to enable the internal negative voltage generator. If VSS_{EXT} is applied to pin 20, the on-chip negative voltage generator is disabled, completely eliminating any generator spurious responses.

[b] Levels based on $T_{EPAD} \leq 85°C$. See Figure 3 for the power de-rating curve for higher case temperatures.

[c] In any of the insertion loss modes or when switching into any insertion loss mode, any 3 of the 4 remaining terminated port paths can be each exposed to the maximum stated power level during continuous or hot switching operation.

Figure 3. Maximum CW RF Input Operating Power vs. RF Frequency



Electrical Characteristics (1)

Table 4. Electrical Characteristics

Typical application circuit (Figure 39), Normal Mode (V_{DD} = 3.3V, VSS_{EXT} = 0V) or Bypass Mode (V_{DD} = 3.3V, VSS_{EXT} = -3.3V), T_{EPAD} = +25°C, f_{RF} = 2000MHz, input power = 0dBm, Z_S = Z_L = 50Ω, RFX = one of the five input ports, and PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}	-	***1.1*** [a]	-	Lower of (3.6, V_{DD})	V
Logic Input Low	V_{IL}	-	***-0.3***	-	***0.6***	V
Logic Current	I_{IH}, I_{IL}	For each control pin	***-2***	-	***+2***	µA
V_{DD} DC Current	I_{DD}	Normal Mode — 3.3V or 1.8V logic	-	290	***360***	µA
		Bypass Mode — 3.3V or 1.8V logic	-	270	***340***	
DC Current (VSS_{EXT})	I_{VSS}	VSS_{EXT} = -3.3V	-	-46	***-60***	µA
Insertion Loss RFX to RFC	IL	f_{RF} = 900MHz	-	0.93	***1.4***	dB
		f_{RF} = 2100MHz	-	1.1	***1.5***	
		f_{RF} = 2700MHz	-	1.2	***1.6***	
		2700MHz < f_{RF} ≤ 4000MHz	-	1.1	1.65	
		4000MHz < f_{RF} ≤ 8000MHz	-	2.3	-	
Insertion Loss Flatness	IL_{FLAT}	400MHz to 3800MHz Any 400MHz range	-	0.1	0.4	dB
Minimum Isolation RFX to RFC [b][c]	ISOC	400MHz ≤ f_{RF} ≤ 900MHz	57.5	62	-	dB
		900MHz < f_{RF} ≤ 2100MHz	51	55	-	
		2100MHz < f_{RF} ≤ 2700MHz	49.5	54	-	
		2700MHz < f_{RF} ≤ 4000MHz	45	49	-	
		4500MHz ≤ f_{RF} ≤ 5500MHz	43	44.8	-	
Minimum Isolation RFX to RFX [b][d]	ISOX	400MHz ≤ f_{RF} ≤ 900MHz	56.5	59	-	dB
		900MHz < f_{RF} ≤ 2100MHz	50	53	-	
		2100MHz < f_{RF} ≤ 2700MHz	48	51	-	
		2700MHz < f_{RF} ≤ 4000MHz	44.5	48	-	
		4500MHz ≤ f_{RF} ≤ 5500MHz	41	43	-	

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] With one path always active.

[c] Minimum value specified for RFC to RF1 through RF4 only. Specification does not apply to RF5.

[d] Each of the 4 inputs to any other input, 4 states only, RF5 removed.

Electrical Characteristics (2)

Table 5. Electrical Characteristics

Typical application circuit (Figure 39), Normal Mode (V_{DD}= 3.3V, VSS_{EXT} = 0V) or Bypass Mode (V_{DD} = 3.3V, VSS_{EXT} = -3.3V), T_{EPAD} = +25°C, f_{RF} = 2000MHz, input power = 0dBm, Z_S = Z_L = 50Ω, RFX = one of the five input ports, and PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Minimum RFC Return Loss [b]	RL_{RFC}	400MHz ≤ f_{RF} ≤ 900MHz	-	23	-	dB
		900MHz < f_{RF} ≤ 2100MHz	-	18	-	
		2100MHz < f_{RF} ≤ 2700MHz	-	16	-	
		2700MHz < f_{RF} ≤ 4000MHz	-	16	-	
		4500MHz ≤ f_{RF} ≤ 5500MHz	-	23	-	
Minimum RFX Return Loss [b] (Active Thru)	RL_{RFC_A}	400MHz ≤ f_{RF} ≤ 900MHz	-	23	-	dB
		900MHz < f_{RF} ≤ 2100MHz	-	16	-	
		2100MHz < f_{RF} ≤ 2700MHz	-	15	-	
		2700MHz < f_{RF} ≤ 4000MHz	-	14	-	
		4500MHz ≤ f_{RF} ≤ 5500MHz	-	17	-	
Minimum RFX Return Loss [b] (Terminated State)	RL_{RFX_T}	400MHz ≤ f_{RF} ≤ 900MHz	-	30	-	dB
		900MHz < f_{RF} ≤ 2100MHz	-	22	-	
		2100MHz < f_{RF} ≤ 2700MHz	-	20	-	
		2700MHz < f_{RF} ≤ 4000MHz	-	15	-	
		4500MHz ≤ f_{RF} ≤ 5500MHz	-	14	-	
Maximum RFX Port VSWR During Switching	$VSWR_T$	From RFX Active to RFX Terminated	-	1.7:1	-	
		From RFX Terminated to RFX Active	-	2:1	-	
Input 1dB Compression [c]	ICP_{1dB}	-	34 [a]	36.5	-	dBm
Input 0.1dB Compression [c]	$ICP_{0.1dB}$	-	28	35	-	dBm
Input IP2 (Insertion Loss State)	IIP2	f_{RF1} = 2000MHz, f_{RF2} = 2010MHz RF input = RFX, P_{IN} = +20dBm / tone f_{RF1} + f_{RF2} = 4010MHz	-	114	-	dBm
		f_{RF1} = 4900MHz, f_{RF2} = 4910MHz RF Input = RFX, P_{IN} = +20dBm / tone f_{RF1} + f_{RF2} = 9810MHz	-	106	-	
		f_{RF1} = 5500MHz, f_{RF2} = 5510MHz RF input = RFX, P_{IN} = +20dBm / tone f_{RF1} + f_{RF2} = 11010MHz	-	111	-	

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] With one path always active.

[c] The input 0.1dB and 1dB compression points are linearity figures of merit. Refer to the “Absolute Maximum Ratings” section 0 for the maximum RF input power and for maximum operating RF input power.

Electrical Characteristics (3)

Table 6. Electrical Characteristics

Typical application circuit (Figure 39), Normal Mode (V_{DD} = 3.3V, VSS_{EXT} = 0V) or Bypass Mode (V_{DD} = 3.3V, VSS_{EXT} = -3.3V), T_{EPAD} = +25°C, f_{RF} = 2000MHz, input power = 0dBm, Z_S = Z_L = 50Ω, RFX = one of the five input ports, and PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Unit
Input IP3	IIP3	Δf = 5MHz RF Input = RFX P_{IN} = +15dBm/tone	f_{RF} = 400MHz	45 [a]	60.5	-	dBm
			f_{RF} = 2000MHz	56	60	-	
			f_{RF} = 4000MHz	-	60.5	-	
			f_{RF} = 4900MHz	-	55	-	
			f_{RF} = 5500MHz	-	55	-	
Group Delay	GD	-		-	0.43	1	ns
Switching Time – Bypass (VSS_{EXT} = -3.3V) [b][c]	$t_{BP\text{-}ON1}$	50% CTRL to 90% maximum RF power		-	256	345	ns
	$t_{BP\text{-}ON2}$	50% CTRL to RF power settled to within ± 0.1dB of maximum power		-	285	-	
	$t_{BP\text{-}OFF}$	50% CTRL to 10% maximum RF power		-	256	345	
Switching Time –Normal (VSS_{EXT} = 0V) [b][c]	$t_{N\text{-}ON1}$	50% CTRL to 90% maximum RF power		-	245	-	ns
	$t_{N\text{-}ON2}$	50% CTRL to RF power settled to within ± 0.1dB of maximum power		-	295	-	
	$t_{N\text{-}ON3}$	50% CTRL to 99% RF maximum RF power		-	350	-	
	$t_{n\text{-}OFF1}$	50% CTRL to 10% maximum RF power		-	200	-	
	$t_{n\text{-}OFF2}$	50% CTRL to 1% maximum RF power		-	245	-	
Maximum Switching Rate [d]		Pin 20 = GND		-	25	-	kHz
		Pin 20 = VSS_{EXT} applied		-	290	-	
Maximum spurious level on any RF port [e]	$Spur_{MAX}$	RF ports terminated into 50Ω RFX connected to RFC		-	-120	-	dBm

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] f_{RF} = 1GHz.

[c] RFC to RFX. In and out of all-off state [000].

[d] Minimum time required between switching of states =1/ (Maximum Switching Rate).

[e] Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance	θ_{JA}	41	°C/W
Junction-to-Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC}	6.4	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL1	

Typical Operating Conditions (TOCs)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- V_{DD} = 3.3V.
- T_{EPAD} = +25ºC (Temperature of exposed paddle).
- f_{RF} = 2000MHz.
- RFX is the driven RF port, and RFC is the output port.
- P_{IN} = 10dBm for all small signal tests.
- P_{IN} = +15dBm / tone applied to selected RFX port for two-tone linearity tests.
- Two-tone frequency spacing = 5MHz.
- $Z_S = Z_L = 50\Omega$.
- All unused RF ports terminated into 50Ω.
- For insertion loss and isolation plots, RF trace and connector losses are de-embedded (see Figure 36 for the "EVKIT Trace and Connector Loss vs. Temperature" plot).
- Plots for isolation and insertion loss over temperature and voltage are for a typical path. For performance of a specific path, refer to the online S-Parameter file.

Typical Performance Characteristics

Figure 4. Insertion Loss vs. Frequency over Selected Switch

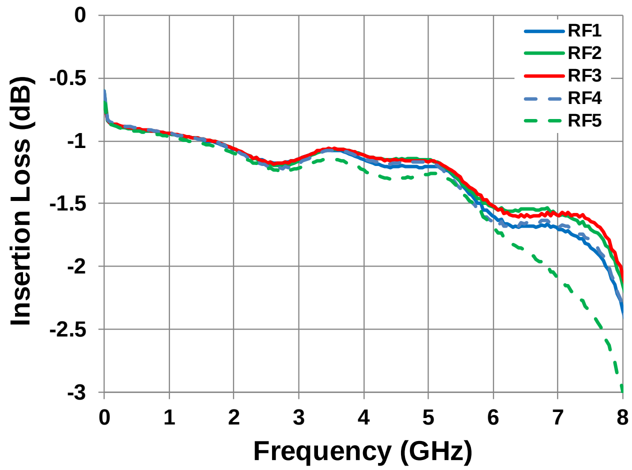


Figure 5. Insertion Loss vs. Frequency over Temperature

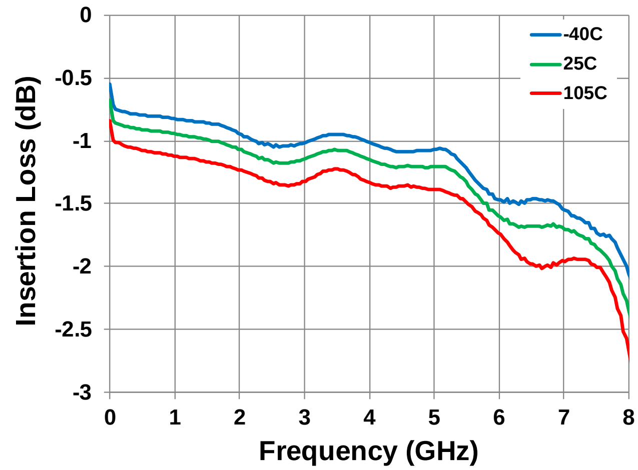


Figure 6. Insertion Loss vs. Frequency over Voltage

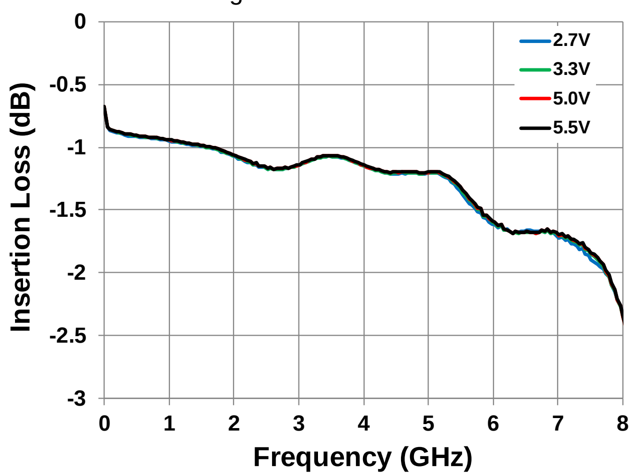


Figure 7. RFC to RFX Isolation vs. Frequency

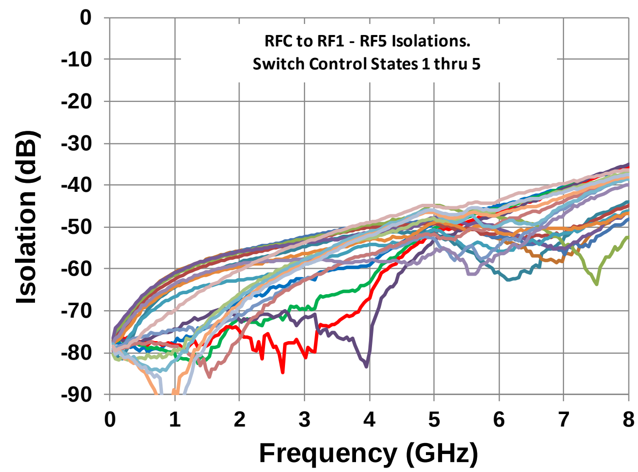


Figure 8. RFC to RFX Isolation vs. Frequency

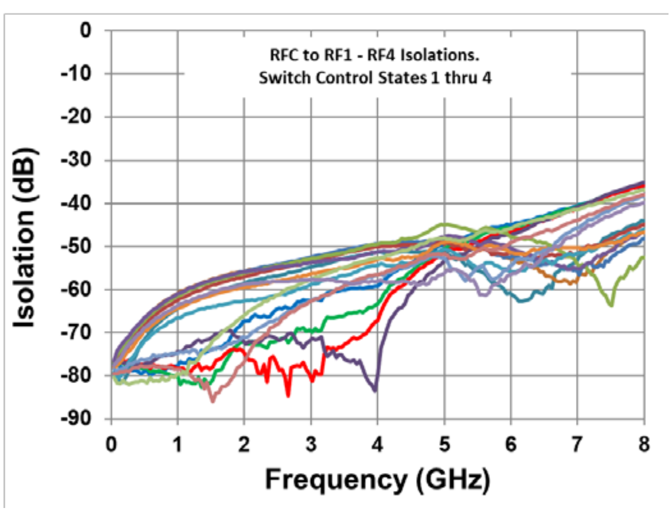


Figure 9. Typical RFC to RFX Isolation vs. Frequency over Temperature

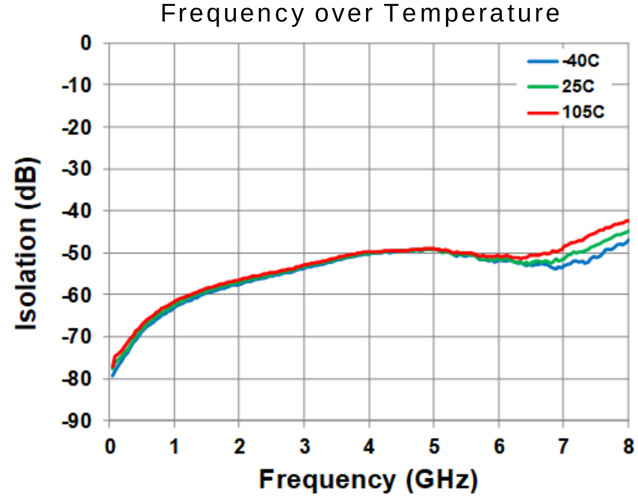


Figure 10. Typical RFC to RFX Isolation vs. Frequency over V_{DD}

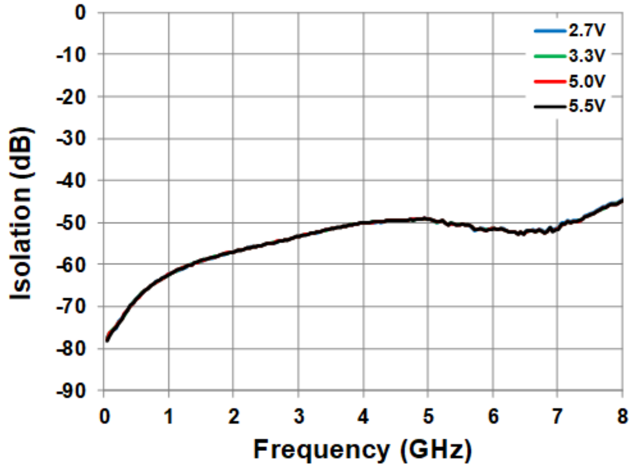


Figure 11. RFX to RFX Isolation vs. Frequency

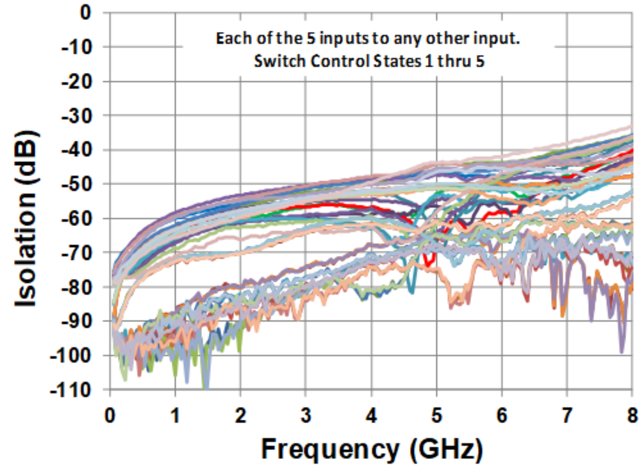


Figure 12. RFX to RFX Isolation vs. Frequency

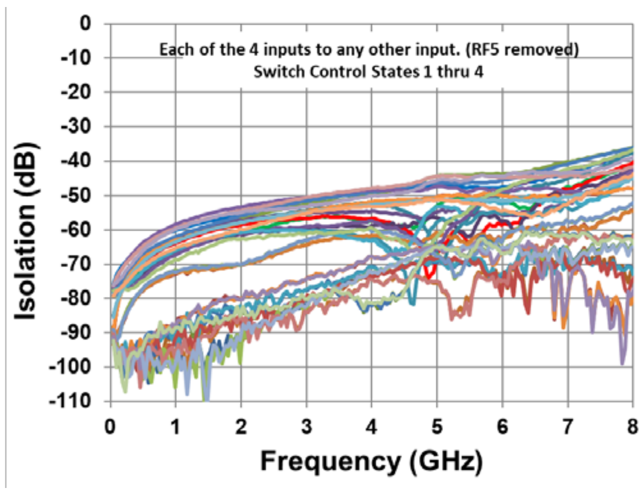


Figure 13. Typical RFX to RFX Isolation vs. Frequency over Temperature

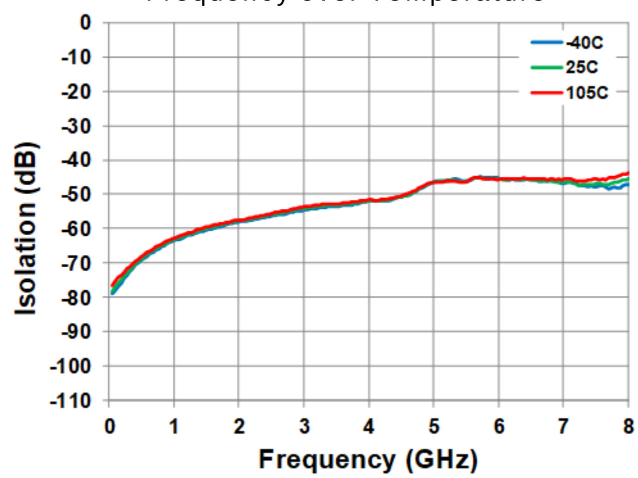


Figure 14. Typical RFX to RFX Isolation vs. Frequency over VDD

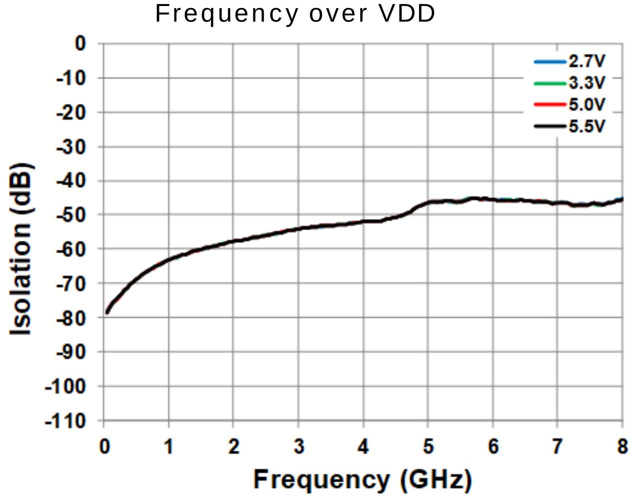


Figure 15. RFX Return Loss vs. Frequency over Switch Path [Selected State]

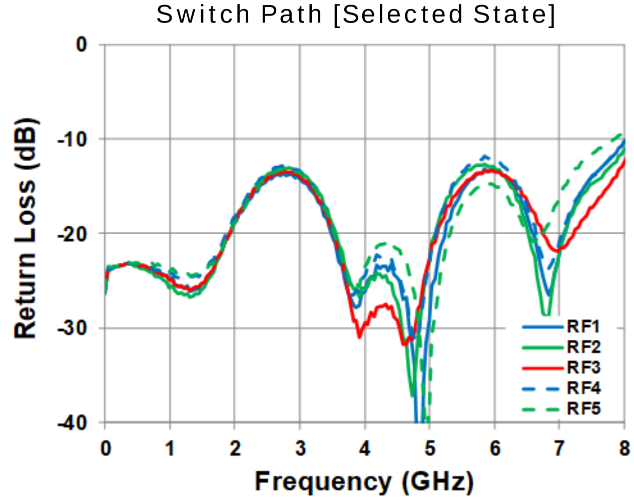


Figure 16. Typical RFX Return Loss vs. Freq. over Temp. [Selected State]

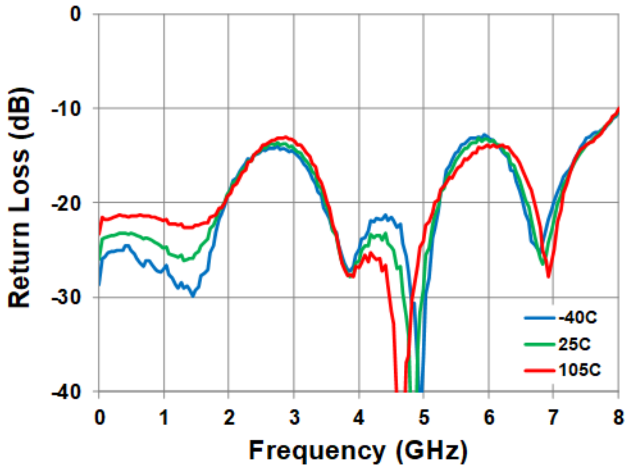


Figure 17. Typical RFX Return Loss vs. Frequency over V_{DD} [Selected State]

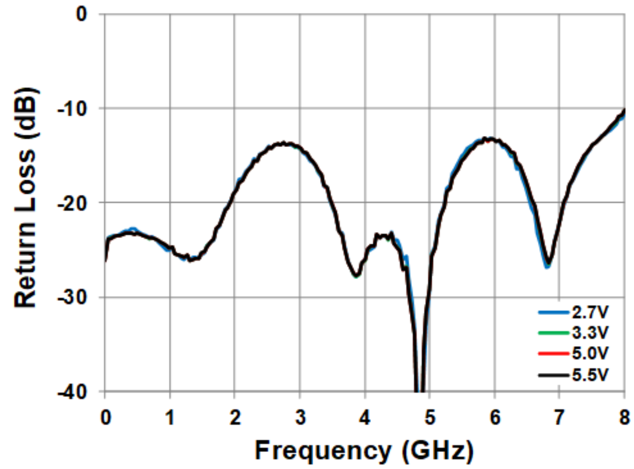


Figure 18. RFC Return Loss vs. Frequency over Switch Path [Selected State]

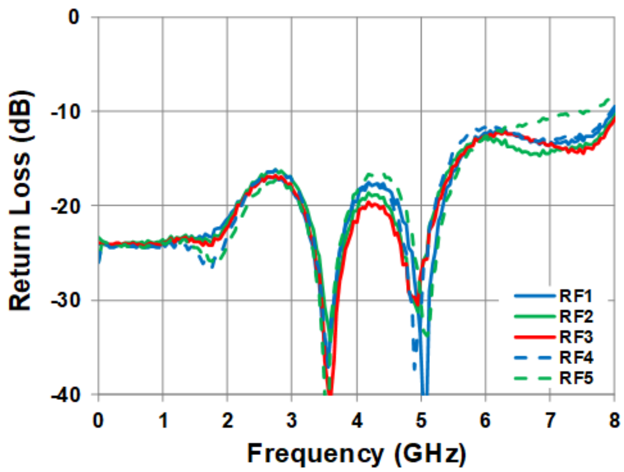


Figure 19. Typical RFC Return Loss vs. Freq. over Temp. [Selected State]

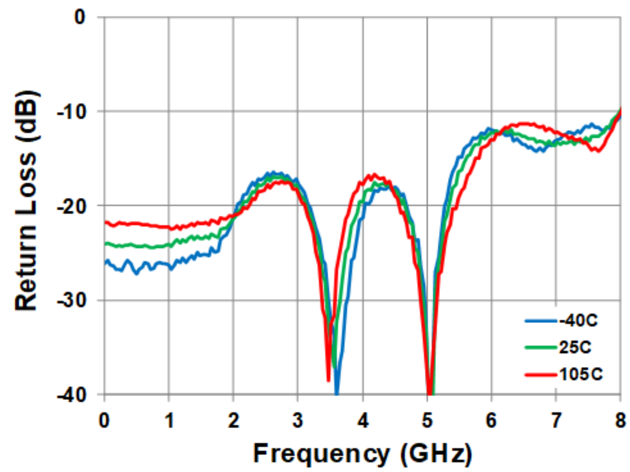


Figure 20. Typical RFC Return Loss vs. Freq. over V_{DD} [Selected State]

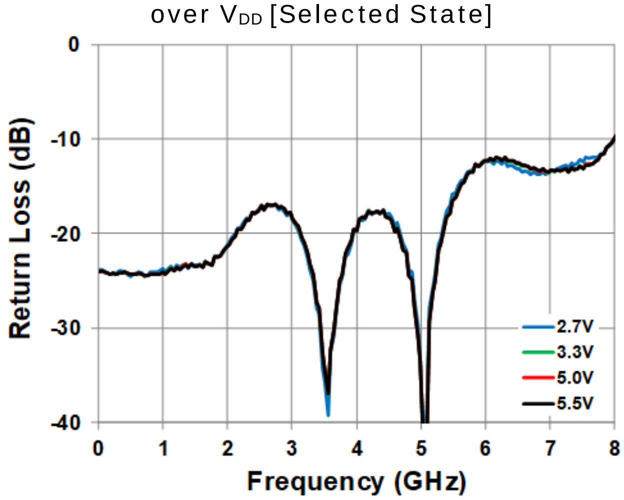


Figure 21. RFX Return Loss vs. Frequency over Switch Path [Terminated State]

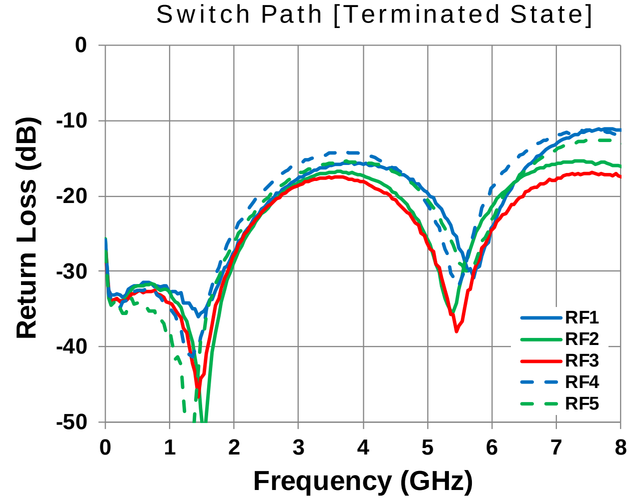


Figure 22. Typical RFX Return Loss vs. Freq. over Temp. [Terminated State]

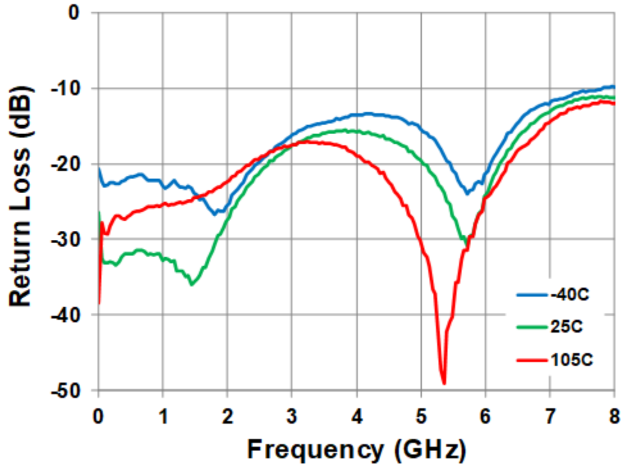


Figure 23. Typical RFX Return Loss vs. Freq. over V_{DD} [Terminated State]

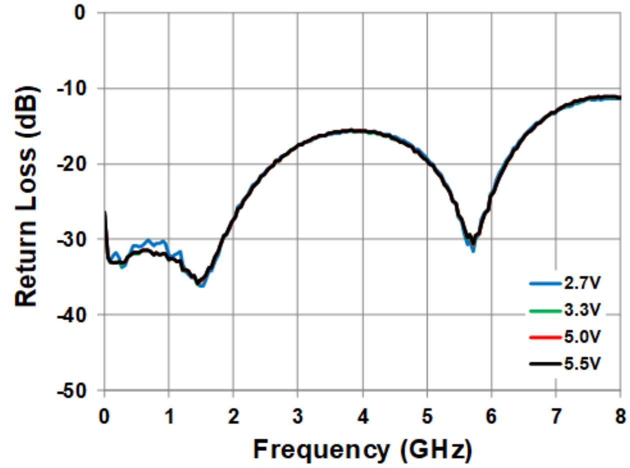


Figure 24. Return Loss (During Switching) vs. Time

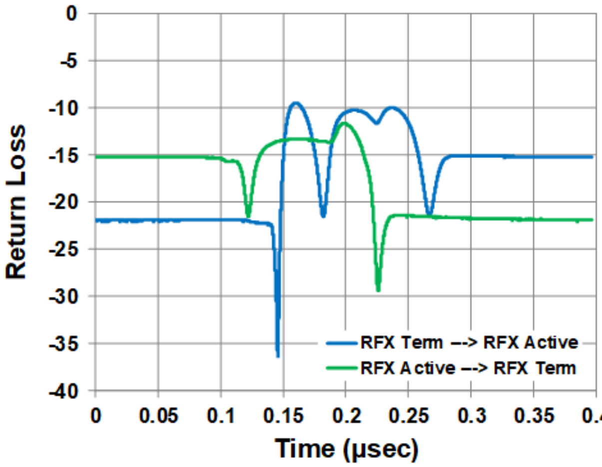


Figure 25. VSWR (During Switching) vs. Time

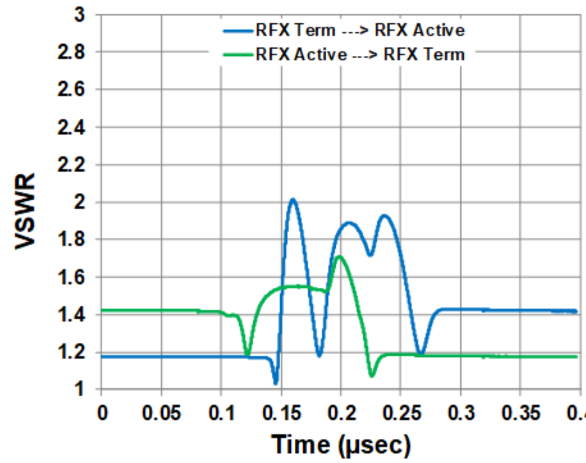


Figure 26. RFX Switching Time [RFX Terminated to RFX Active]

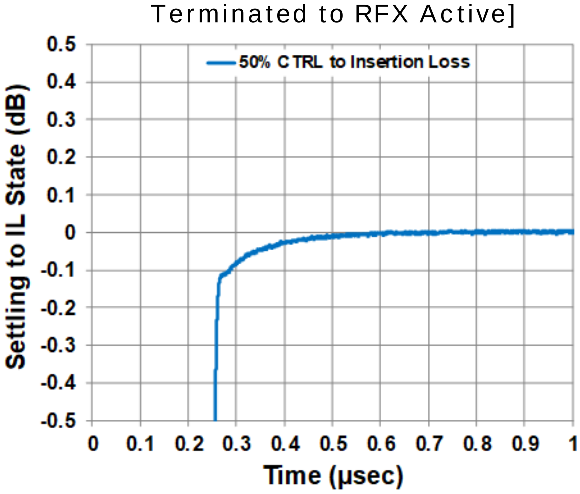


Figure 27. RFX Switching Time [RFX Active to RFX Terminated]

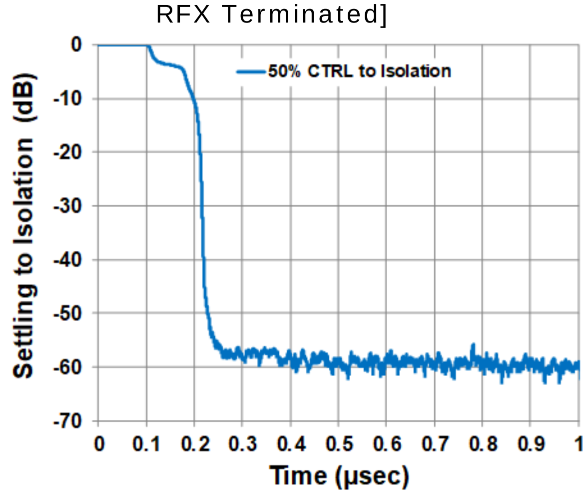


Figure 28. Switching Speed RFX to RFC All Off to On

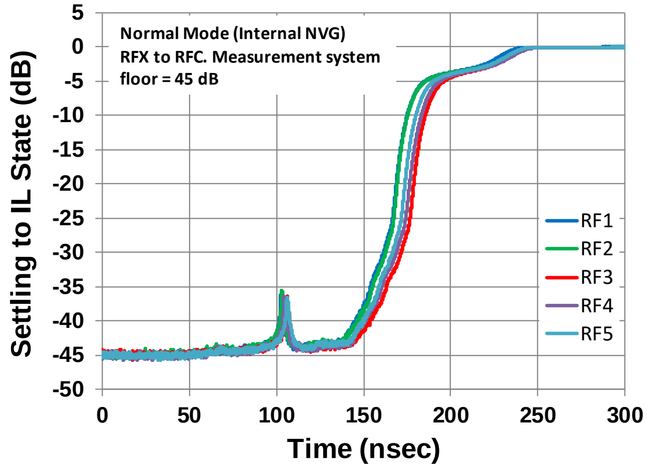


Figure 29. Switching Speed RFX to RFC On to All Off

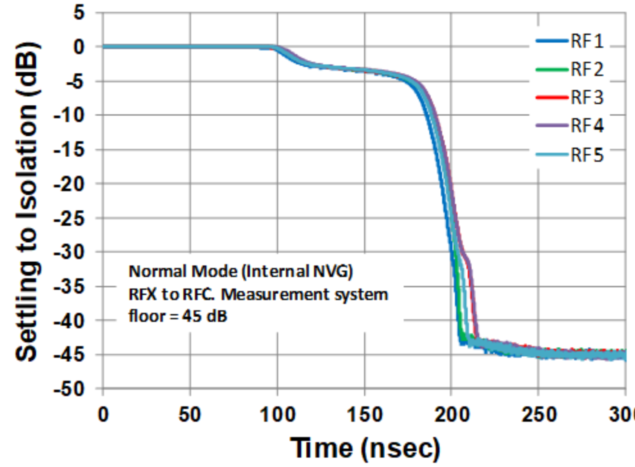


Figure 30. RFX IIP3 vs. Frequency over Switch Path [Selected State]

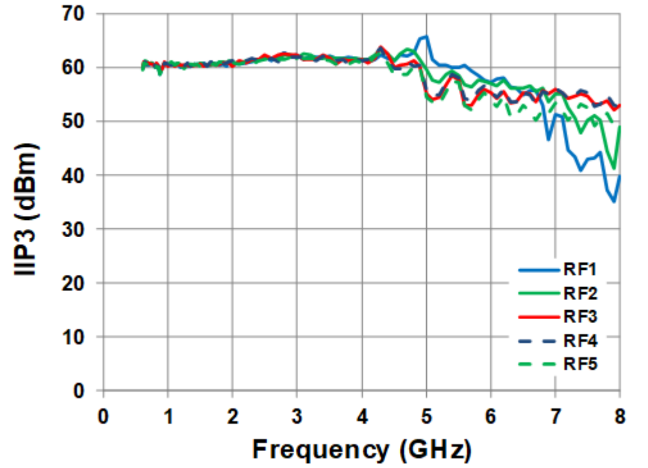


Figure 31. RF1 IIP3 vs. Frequency over Temperature and Voltage

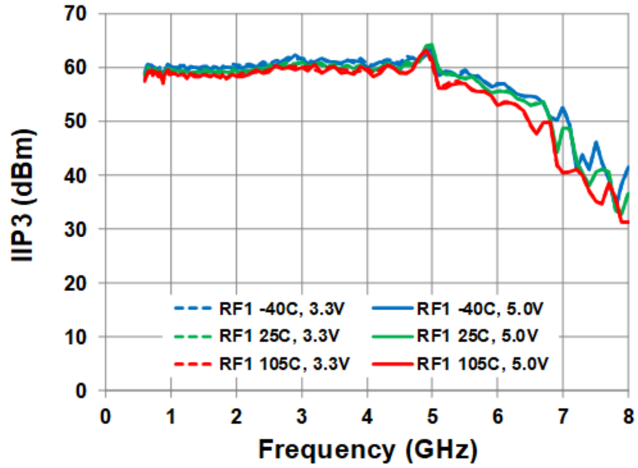


Figure 32. RF2 IIP3 vs. Frequency over Temperature and Voltage

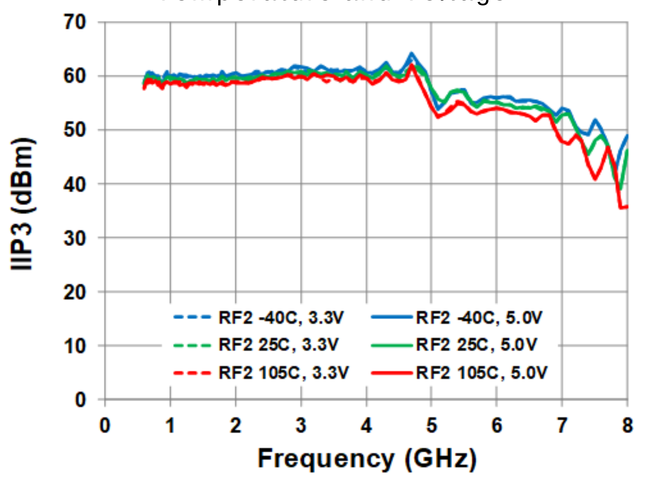


Figure 33. RF3 IIP3 vs. Frequency over Temperature and Voltage

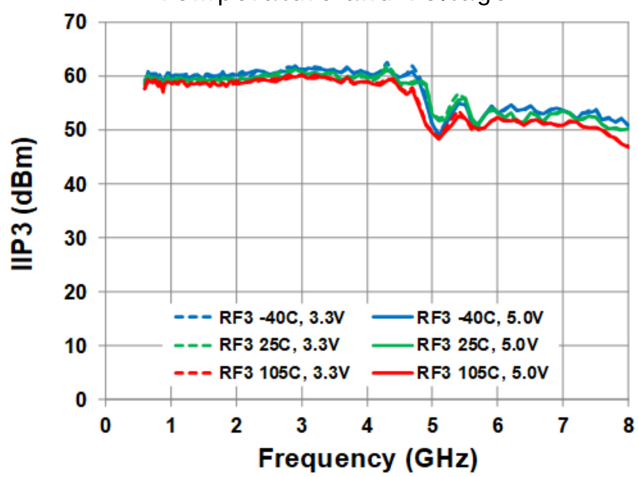


Figure 34. RF4 IIP3 vs. Frequency over Temperature and Voltage

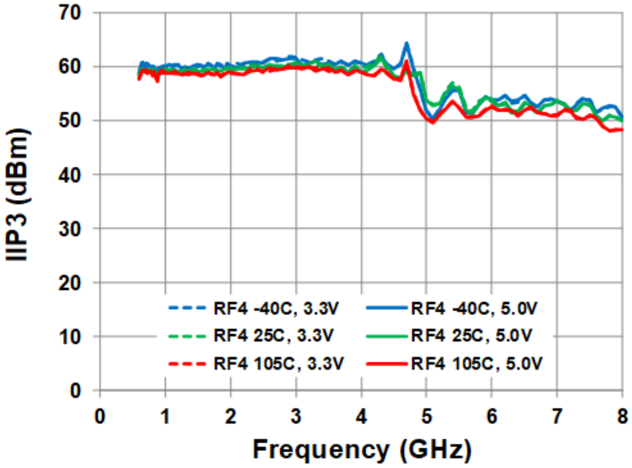


Figure 35. RF5 IIP3 vs. Frequency over Temperature and Voltage

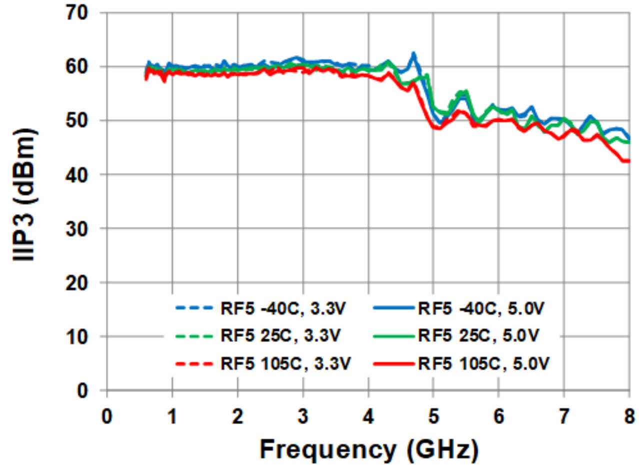
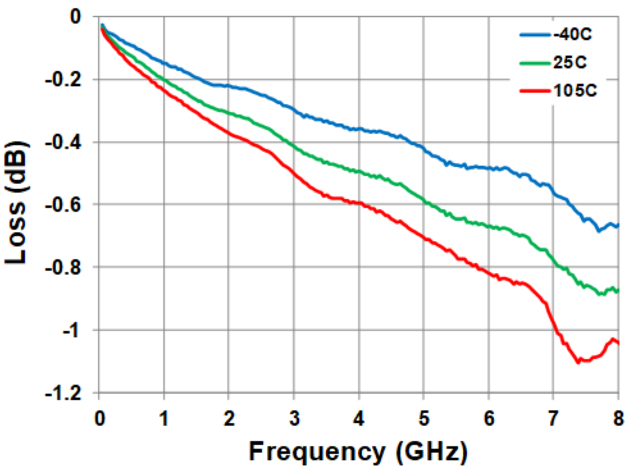


Figure 36. EVKIT Trace and Connector Loss vs. Temperature



Control Mode

To select the path of the F2915 use Table 8 to see the control voltage with either 1.8V or 3.3V logic.

Table 8. Switch Control Truth Table

Mode	V3	V2	V1
All Off	0	0	0
RF1 On	0	0	1
RF2 On	0	1	0
RF3 On	0	1	1
RF4 On	1	0	0
RF5 On	1	0	1
All Off	1	1	0
All Off	1	1	1

Evaluation Kit Picture

Figure 37. Top View

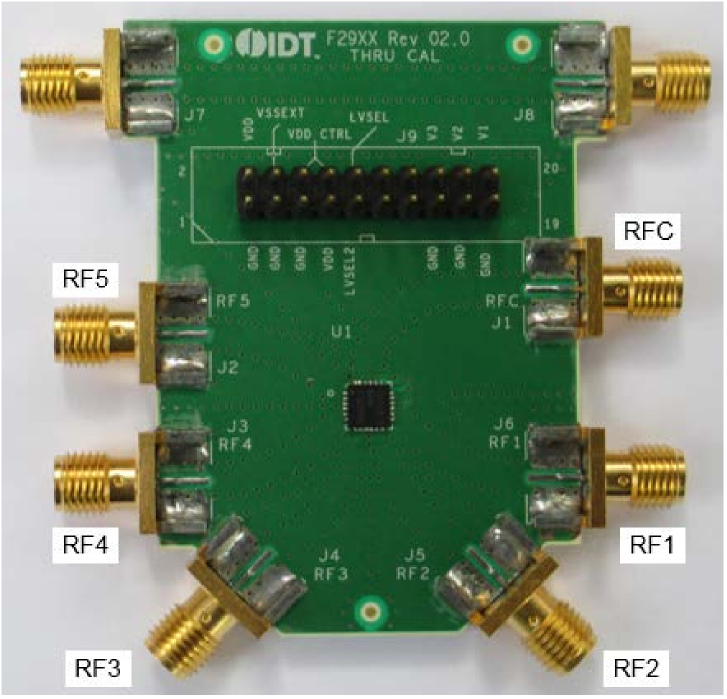
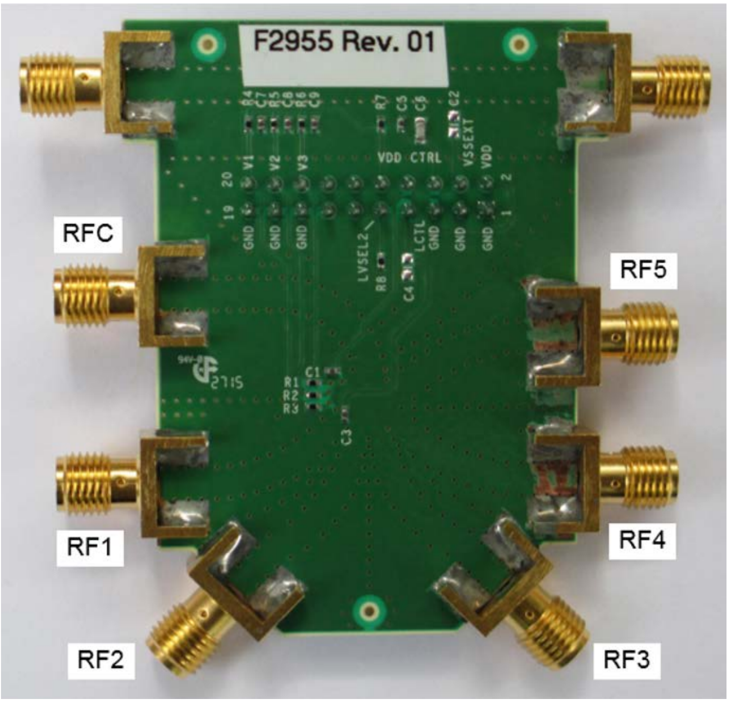


Figure 38. Bottom View



Evaluation Kit / Applications Circuit

Figure 39. Electrical Schematic

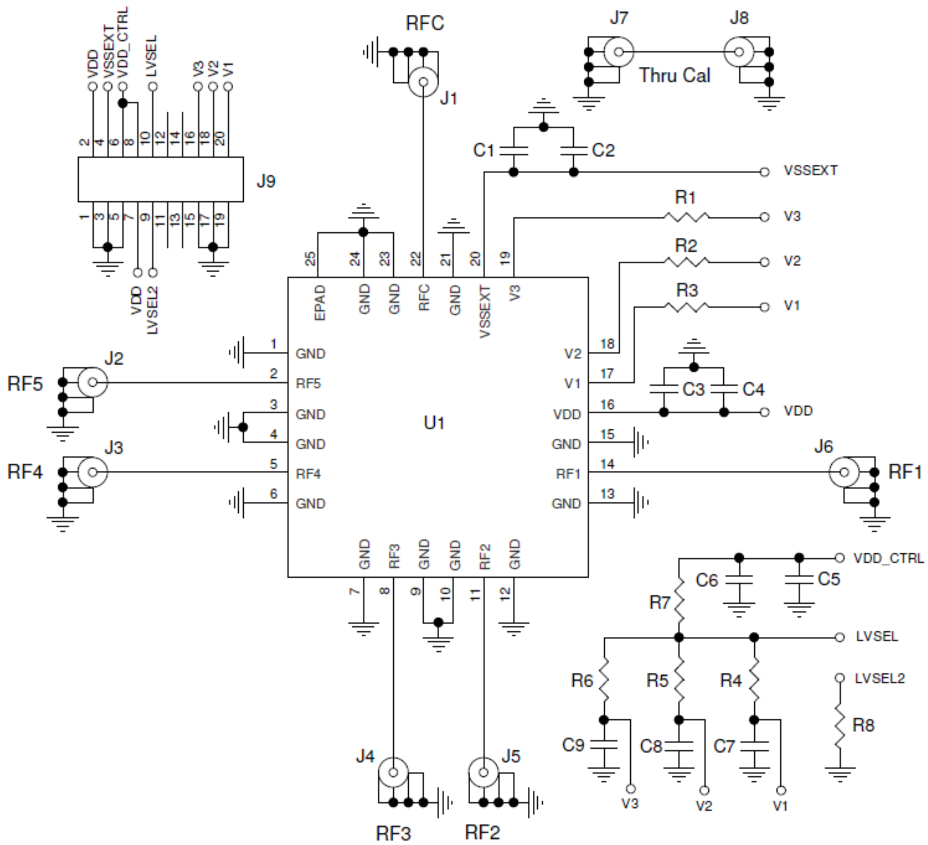


Table 9. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1, C3, C5, C7, C8, C9	6	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C2	0	Not Installed (0603)	-	-
C4	0	Not Installed (0603)	-	-
C6	1	1000pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H102J	Murata
R1, R2, R3	3	0Ω ±1%, 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
R4, R5, R6	3	100kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
R7	1	15kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1502X	Panasonic
R8	1	22kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2202X	Panasonic
J1-J8	8	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J9	1	CONN HEADER VERT DBL 10 X 2 POS GOLD	67997-120HLF	FCI
U1	1	SP5T Switch 4mm x 4mm QFN24-EP	F2955NBGK	Renesas (IDT)
	1	Printed Circuit Board	F29XX EVKIT Rev 02.0	Renesas (IDT)

Evaluation Kit (EVKit) Operation

External Supply Setup

1. Set up a VDD power supply in the voltage range of 2.7V to 5.5V and disable the power supply output.
2. If using the on-chip negative voltage generator, install a 2-pin shunt to short pins 3 (GND) and 4 (VSSEXT) of J9.
3. If an external negative voltage supply is to be used, set its voltage within the range of -3.6V to -3.2V and disable it. Also, ensure there are no jumper connections on pins 3 and 4 of J9.

Logic Control Setup

Using the EVKIT to Manually Set the Control Logic

1. On connector J9, connect a 2-pin shunt from pin 7 (VDD) to pin 8 (VDD_CTRL). This connection provides the VDD voltage supply to the Evaluation Board logic control pull-up network.
2. On connector J9 connect a 2-pin shunt from pin 9 (LVSEL2) to pin 10 (LVSEL). This connection enables R7 (15kΩ) and R8 (22kΩ) to form a voltage divider to set the proper logic control levels to support the full voltage range of VDD. Note that when using the on-board R7 / R8 voltage divider, the current draw from the VDD supply will be higher by approximately VDD/37kΩ.
3. Connector J9 has 3 logic input pins: V1 (pin 20), V2 (pin 18), and V3 (pin 16). See Table 8 for the logic truth table. With the pull-up network enabled (as noted above), if these pins are left open, a logic HIGH will be provided through pull-up resistors R4, R5, and R6. To set a logic LOW to V1, V2, and V3, connect 2-pin shunts from pin 16 to pin 15, pin 18 to pin 17 and pin 20 to pin 19, respectively.

Using the External Control Logic

Pins 6, 7, 8, 9, and 10 of J9 should have no connection. External logic controls can be applied to J9 pins 16 (V3), 18 (V2) and 20 (V1). See Table 8 for the logic truth table.

Turn On Procedure

1. Set up the supplies and Evaluation Board as noted in “External Supply Setup” and “Logic Control Setup” above.
2. Connect the preset disabled VDD power supply to pin 2 (VDD) and pin 1 (GND) of J9.
3. If the external negative voltage source is to be used, connect the disabled supply to pin 4 (VSSEXT) and pin 3 (GND) of J9. If using the on-chip negative supply, ensure that the 2-pin shunt is installed connecting pin 3 to pin 4.
4. Enable the VDD supply and then enable the VSSEXT supply (if used).
5. Set the desired logic setting using V1, V2, and V3 to achieve the desired path setting, see Table 8. Note that external control logic should not be applied without VDD being applied first.

Turn Off Procedure

1. If using external control logic, V1, V2, and V3 must be set to a logic LOW.
2. Disable any external VSSEXT supply.
3. Disable the VDD supply.

Application Information

Default Start-up

There are no internal pull-up or pull-down resistors on the control pins.

Logic Control

Control pins V1, V2, and V3 are used to set the state of the SP5T switch (See Table 8).

External V_{SS}

The F2955 is designed with an on-chip negative voltage generator. This on-chip generator is enabled by connecting pin 20 of the device to ground. To disable the on-chip generator, apply a negative voltage to pin 20 (VSS_{EXT}) of the device within the range stated in the "Recommended Operating Conditions" (Table 3).

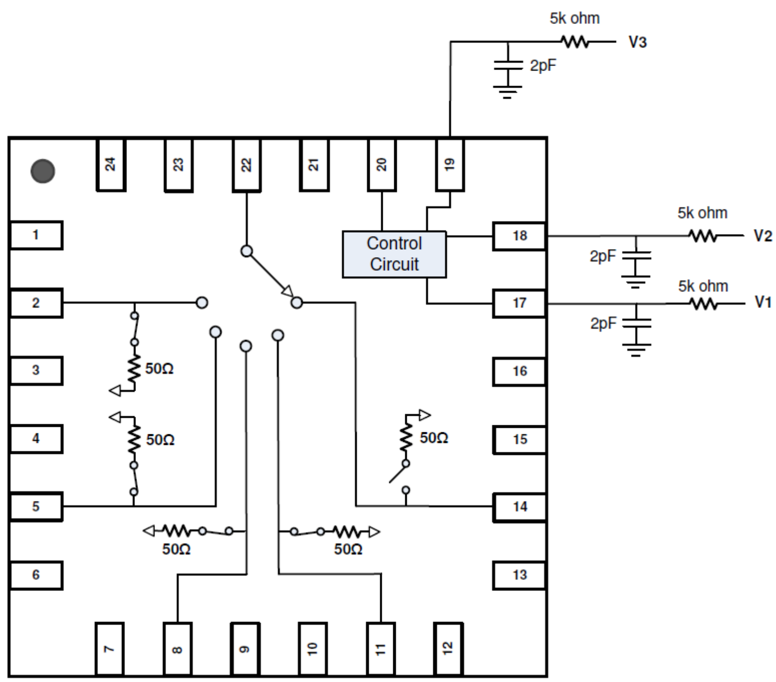
Power Supplies

A common VDD power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 17, 18, and 19 as shown below.

Figure 40. Control Pin Interface Schematic



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

Line 1 and 2 are the part number.
Line 3: “Z” is for the ASM Test Step.
Line 3: “1528” is the last two digits of the year plus the work week (YYWW).
Line 3: “UZL” denotes the Assembler Code.

Ordering Information

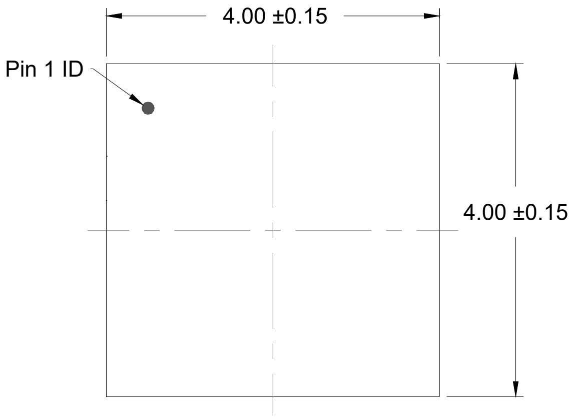
Part Number	Package	MSL Rating	Carrier Type	Temperature Range
F2955NBGK	4.0 × 4.0 × 0.75 mm 24-QFN	MSL1	Tray	-40°C to +105°C
F2955NBGK8	4.0 × 4.0 × 0.75 mm 24-QFN	MSL1	Reel	-40°C to +105°C
F2955EVBK	Evaluation Board			

Revision History

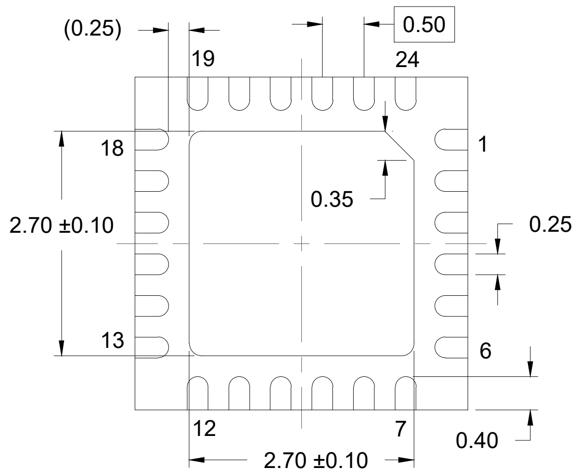
Date	Description of Change
November 1, 2023	▪ Updated Block Diagram ▪ Updated Package Outline Drawings section and added POD links in Ordering Information
February 7, 2023	Updated disclaimer and POD links.
June 25, 2020	▪ Rebranded the document as Renesas
February 21, 2019	▪ Corrected HBM ESD voltage in Table 2
October 11, 2018	▪ Changed maximum value for “Maximum Junction Temperature” in Table 2 ▪ Changed maximum value for “VDD to GND” in Table 2 ▪ Updated maximum value for “Power Supply Voltages” in Table 3
September 25, 2018	Initial release.

Package Outline Drawing

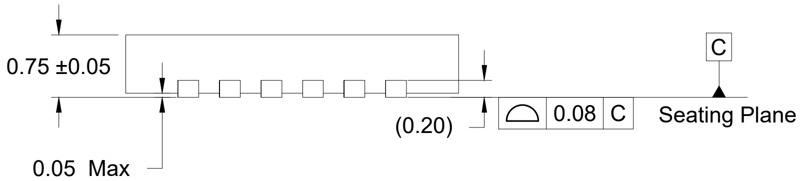
Package Code:NBG24P3
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.50 mm Pitch
PSC-4313-03, Revision: 02, Date Created: Jul 20, 2023



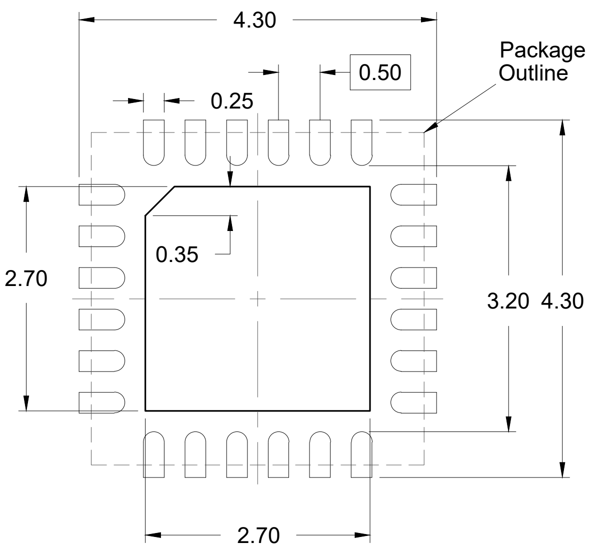
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

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