Description

The F2970 is a high reliability, low insertion loss, 75 Ω absorptive SP2T RF switch designed for a multitude of cable systems and other RF applications. This device covers a broad frequency range from 5 MHz to 3000 MHz. In addition to providing low insertion loss, the F2970 also delivers excellent linearity and isolation performance while providing a 75 Ω termination for the unselected port.

The F2970 uses a single positive supply voltage and supports 3.3 V logic.

Competitive Advantage

The F2970 provides broadband RF performance to support the CATV market along with high power handling, and high isolation.

- Low Insertion Loss
- High Isolation
- Excellent Linearity
- Extended Temperature: -40 °C to +105 °C

Typical Applications

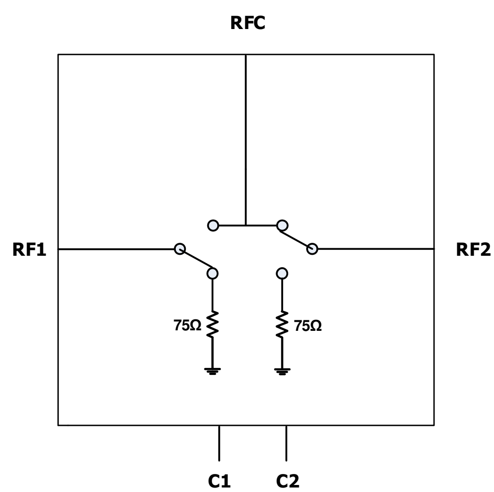
- CATV/Broadband Applications
  - ✓ Headend
  - ✓ Fiber/HFC Distribution Nodes
  - ✓ Distribution Amplifiers
  - ✓ Switch Matrix
  - ✓ DTV Tuner Input Select
  - ✓ DVR/PVR/Set-top box
- CATV Test Equipment

Features

- Low Insertion Loss:
  - ✓ 0.32 dB @ 1200 MHz
- High Isolation:
  - ✓ 70 dB @ 1200 MHz (RF1/RF2 to RFC)
- Excellent Linearity:
  - ✓ IIP3 of 63 dBm
- Selectable Logic Control
- Operating Temperature: -40 °C to +105 °C
- 4 mm x 4 mm 20-pin LQFN package

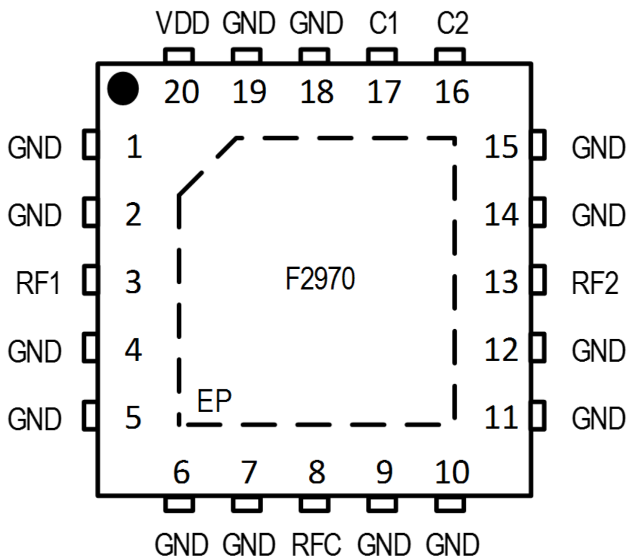
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4 mm x 4 mm x 0.75 mm 20-pin LQFN, NCG20 – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 18, 19	GND	Ground these pins as close to the device as possible.
3	RF1	RF1 Port. Matched to 75 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
8	RFC	RFC Port. Matched to 75 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
13	RF2	RF2 Port. Matched to 75 ohms. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	C2	Control pin to set switch state. See Table 8.
17	C1	Control pin to set switch state. See Table 8.
20	V_{DD}	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{DD} to GND		V_{DD}	-0.3	4.0	V
C1, C2 to GND		V_{logic}	-0.3	Lower of (V_{DD}+0.3, 3.9)	V
RF1, RF2, RFC to GND		V_{RF}	-0.3	+0.3	V
Maximum Input CW Power [a]	RF1 or RF2 as an input (Connected to RFC)	P_{ABS}		30	dBm
	RFC as an input (Connected to RF1 or RF2)			30	
	RF1 or RF2 as an input (Terminated states)			26	
Maximum Junction Temperature		T_{jmax}		140	°C
Storage Temperature Range		T_{ST}	-65	150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2000 (Class 2)	V
ElectroStatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		1500 (Class C3)	V

a. Levels based on: V_{DD} = 2.7 V to 3.6 V, 5 MHz $\leq F_{RF} \leq$ 3000 MHz, Tc = 105 °C, $Z_S = Z_L$ = 75 ohms.

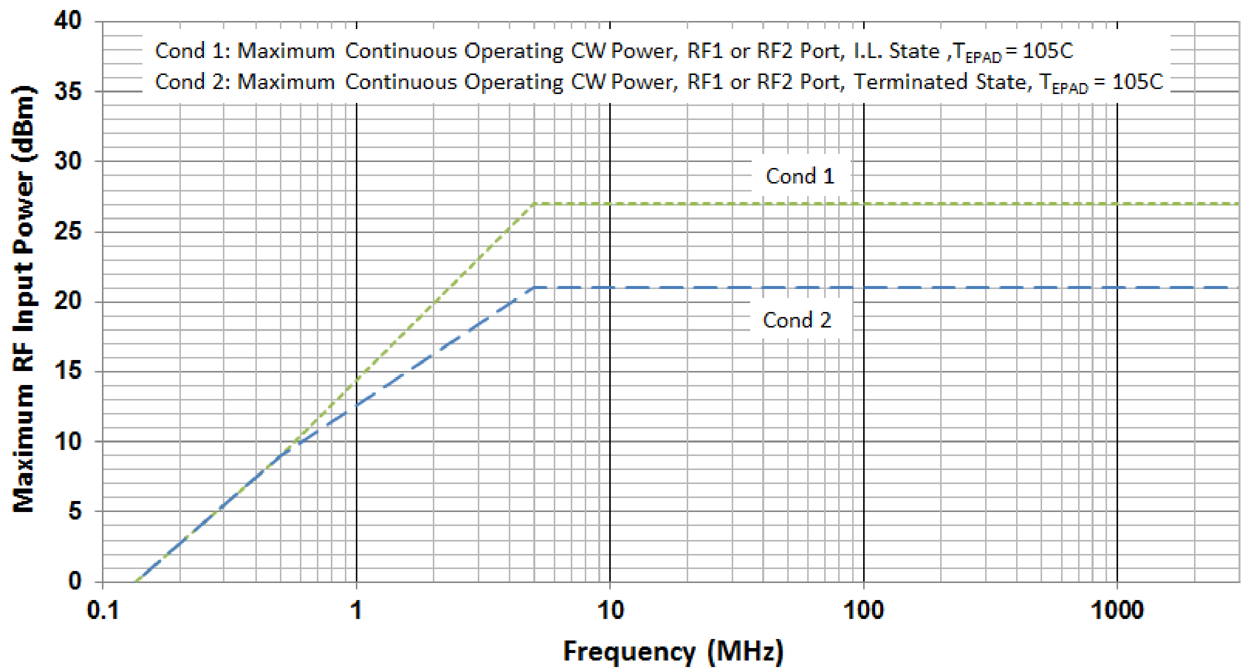
Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition		Min	Typ	Max	Units
Supply Voltage	V_{DD}			2.7		3.6	V
Operating Temp Range	T_{CASE}	Exposed Paddle Temperature		-40		+105	°C
RF Frequency Range	F_{RF}			5		3000	MHz
RF Continuous Input CW Power (Non-Switched) [a]	P_{RF}	RFC connected to RF1 or RF2	T_C = 85°C			27	dBm
			T_C = 105°C			27	
		RF1 / RF2 Input, Terminated State	T_C = 85°C			24	
			T_C = 105°C			21	
RF Continuous Input Power (RF Hot Switching CW) [a]	P_{RFSW}	RFC Input switching between RF1 and RF2	T_C = 85°C			21	dBm
			T_C = 105°C			21	
		RF1 or RF2 as input, switched between RFC and Term.	T_C = 85°C			17	
			T_C = 105°C			17	
RF1 Port Impedance	Z_{RF1}	Single ended			75		Ω
RF2 Port Impedance	Z_{RF2}	Single ended			75		
RFC Port Impedance	Z_{RFC}	Single ended			75		

a. Levels based on: V_{DD} = 2.7 V to 3.6 V, 5 MHz ≤ F_{RF} ≤ 3000 MHz, Z_S = Z_L = 75 ohms. See Figure 3 for power handling derating vs RF frequency.

Figure 3. Maximum RF Input Operating Power vs. RF Frequency



Electrical Characteristics

Table 4. Electrical Characteristics

Typical Application Circuit: V_{DD} = 3.0 V, T_C = +25 °C, F_{RF} = 1200 MHz, Driven Port = RF1 or RF2, Input Power = 0 dBm, Z_S = Z_L = 75 ohms. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold [c]	V_{IH}	2.7 V $\leq V_{DD} \leq$ 3.6 V	***0.7 x V_{DD}*** [a]		***V_{DD}***	V
Logic Input Low Threshold [c]	V_{IL}		-0.3 [b]		***0.3 x V_{DD}***	V
Logic Current	I_{IH}, I_{IL}	For each control pin		180	***500***	nA
V_{DD} DC Current [c]	I_{DD}	Logic Inputs at GND or V_{DD}		20	***30***	µA
Insertion Loss	IL	5 – 250 MHz		0.25		dB
		250 – 750 MHz		0.30		
		750 – 1000 MHz		0.30		
		1000 – 1200 MHz		0.32	***0.57***	
		1200 – 2000 MHz		0.32		
		2000 – 3000 MHz		0.35		
Isolation (RFC to RF1 / RF2)	ISO_{RFC}	5 – 250 MHz	79	84		dB
		250 – 750 MHz	69	74		
		750 – 1000 MHz	67	72		
		1000 – 1200 MHz	65	70		
		1200 – 2000 MHz	62	67		
		2000 – 3000 MHz		57		
Isolation (RF1 to RF2)	ISO_{R12}	5 – 250 MHz	79	84		dB
		250 – 750 MHz	69	74		
		750 – 1000 MHz	66	71		
		1000 – 1200 MHz	63	68		
		1200 – 2000 MHz	57	62		
		2000 – 3000 MHz		53		
RF1, RF2, RFC Return Loss (Insertion Loss State)	RL_{IL}	5 – 250 MHz		25		dB
		250 – 750 MHz		20		
		750 – 1000 MHz		18		
		1000 – 1200 MHz		18		
		1200 – 2000 MHz		18		
		2000 – 3000 MHz		18		

a. Items in min/max columns in ***bold italics*** are Guaranteed by Test.
b. Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
c. Increased I_{DD} current will result if logic low level is above ground and up to V_{IL} max. Similarly, increased I_{DD} current will result if logic high level is below V_{DD} and down to V_{IH} min.

Electrical Characteristics

Table 5. Electrical Characteristics

Typical Application Circuit: V_{DD} = 3.0 V, T_C = +25 °C, F_{RF} = 1200 MHz, Driven Port = RF1 or RF2, Input Power = 0 dBm, Z_S = Z_L = 75 ohms. PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
RF1, RF2 Return Loss (Terminated State)	RL_{TERM}	5 – 250 MHz			27		dB
		250 – 750 MHz			22		
		750 – 1000 MHz			20		
		1000 – 1200 MHz			20		
		1200 – 2000 MHz			20		
		2000 – 3000 MHz			17		
Input 1dB Compression [c]	ICP_{1dB}	5 – 250 MHz		29 [b]	31		dBm
		250 – 2000 MHz		30	32		
Input IP2 (Insertion Loss State)	IIP2	Pin = 13 dBm / tone (F1 + F2 Frequency)	F1 = 5 MHz F2 = 6 MHz		95		dBm
			F1 = 185 MHz F2 = 190 MHz		103		
			F1 = 895 MHz F2 = 900 MHz		129		
Input IP3 (Insertion Loss State)	IIP3	Pin = 13 dBm / tone	F1 = 5 MHz F2 = 6 MHz		63		dBm
			F1 = 185 MHz F2 = 190 MHz		63		
			F1 = 1790 MHz F2 = 1795 MHz		63		
CTB / CSO		77 & 110 channels P_{OUT} = 44 dBmV			-90		dBc
Non-RF Driven Spurious [d]	$Spur_{MAX}$	Out any RF port when externally terminated into 75 Ω			-128		dBm
Switching Time [e]	T_{SW}	50% control to 90% RF			2.7		µs
		50% control to 10% RF			2.7		
Maximum Switching Rate [f]	SW_{RATE}					25	kHz
Maximum Video Feed-through on RF Ports	VID_{FT}	Peak transient during switching measured with 20 ns risetime, 0 to 3.3 V control pulse	Rise		1.0		mV_{pp}
			Fall		1.5		

a. Items in min/max columns in ***bold italics*** are Guaranteed by Test.
b. Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
c. The input 1 dB compression point is a linearity figure of merit. Refer to the Recommended Operating Conditions section and Figure 3 for the maximum operating power levels.
d. Spurious due to on-chip negative voltage generator. Spurious fundamental = approx. 2.2 MHz.
e. F_{RF} = 1000 MHz.
f. Minimum time required between switching of states = 1/ (Maximum Switching Rate).

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance.	θ_{JA}	53	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC}	13.8	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

- V_{DD} = +3.0 V
- $Z_L = Z_S = 75\Omega$
- T_{CASE} = 25°C
- F_{RF} = 1200 MHz
- Small signal parameters measured with P_{IN} = 0 dBm
- Two tone parameters measured with P_{IN} = 13 dBm/tone
- Driven Port is RF1 or RF2
- All temperatures are referenced to the exposed paddle.
- Evaluation Kit traces and connector losses are de-embedded.

Typical Performance Characteristics [1]

Figure 4. Insertion Loss vs. Frequency over Temperature and V_{DD} [RF1]

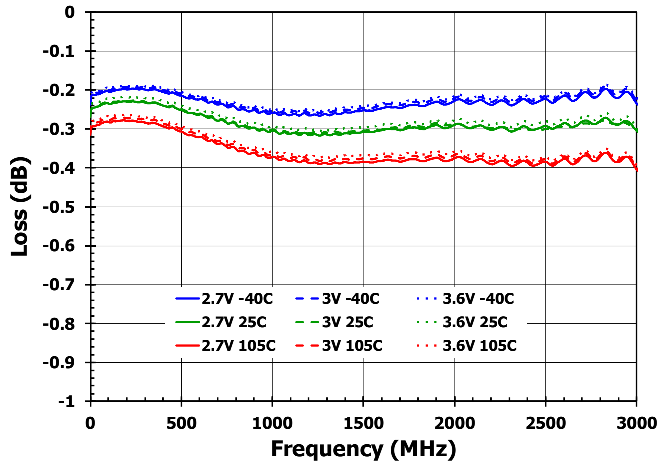


Figure 5. Insertion Loss vs. Frequency over Temperature and V_{DD} [RF2]

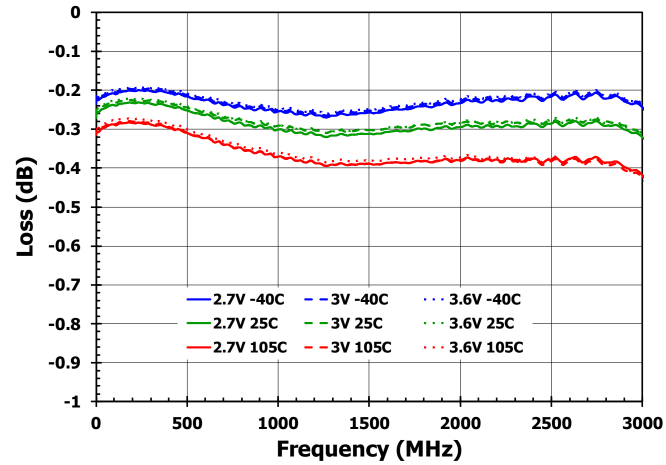


Figure 6. Isolation vs. Frequency over Temp and V_{DD} [RF1 to RF2, RF1 Selected]

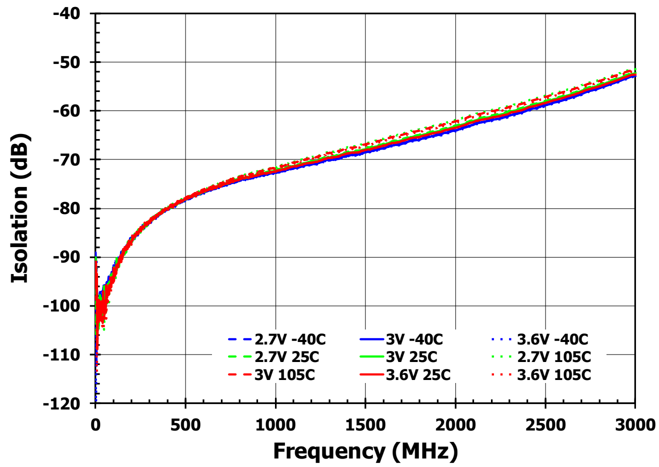


Figure 7. Isolation vs. Frequency over Temp and V_{DD} [RF2 to RF1, RF2 Selected]

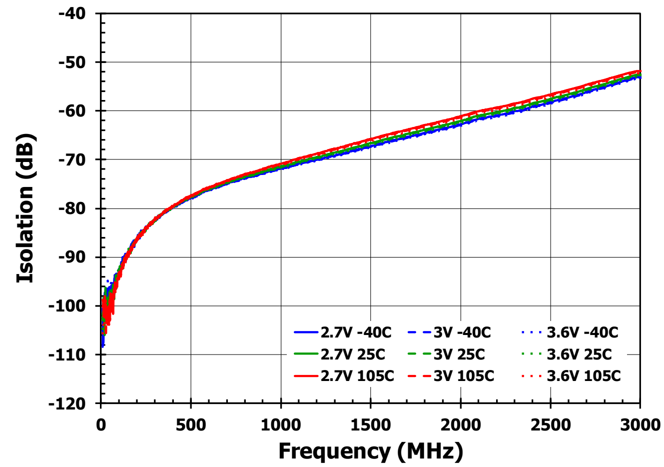


Figure 8. Isolation vs. Frequency over Temp and V_{DD} [RF2 to RFC, RF1 Selected]

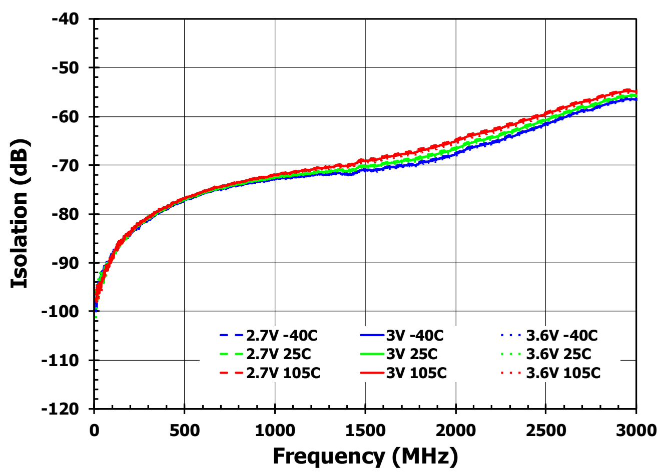
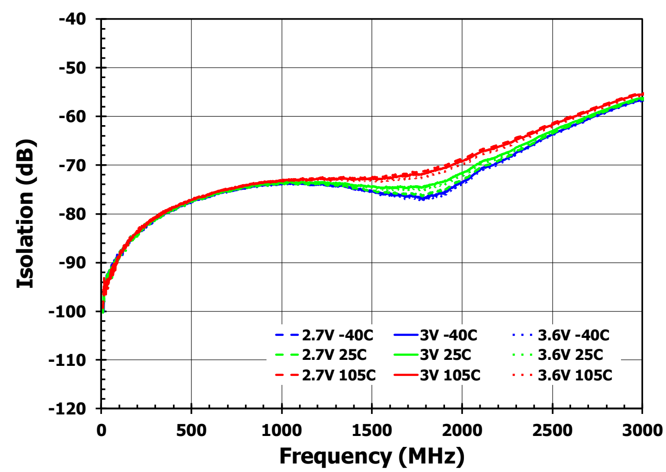


Figure 9. Isolation vs. Frequency over Temp and V_{DD} [RF1 to RFC, RF2 Selected]



Typical Performance Characteristics [2]

Figure 10. RF1 Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

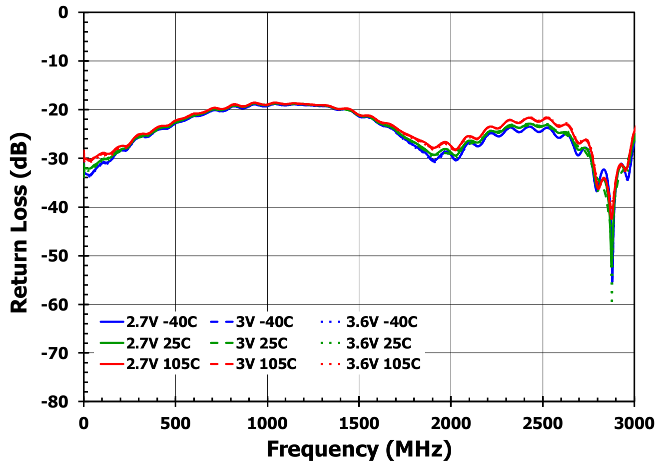


Figure 11. RF2 Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]

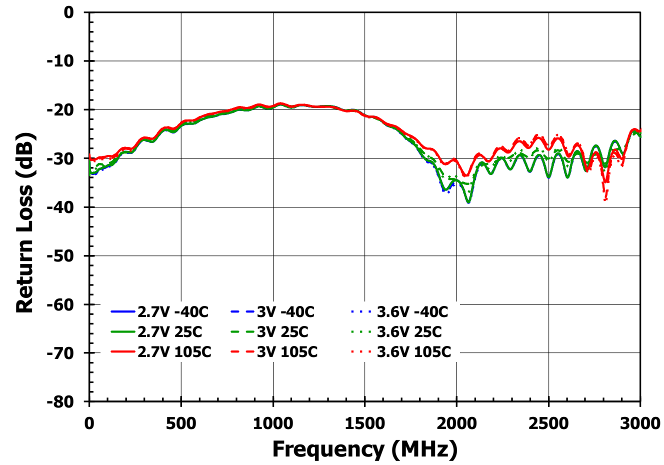


Figure 12. RF1 Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]

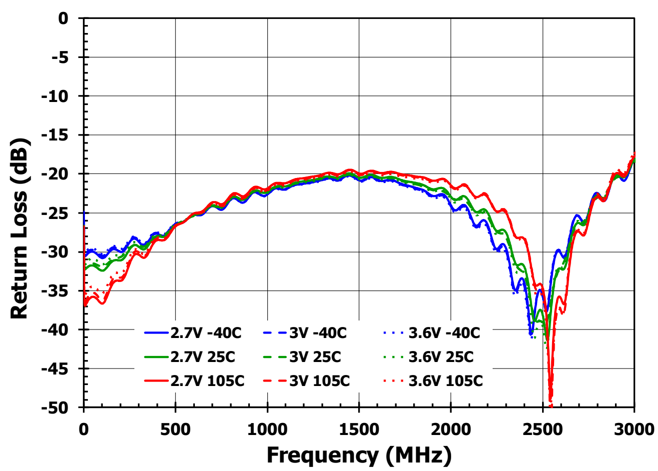


Figure 13. RF2 Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

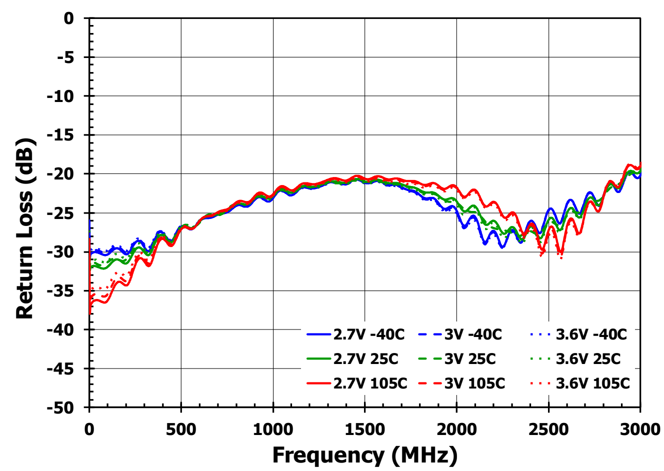


Figure 14. RFC Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

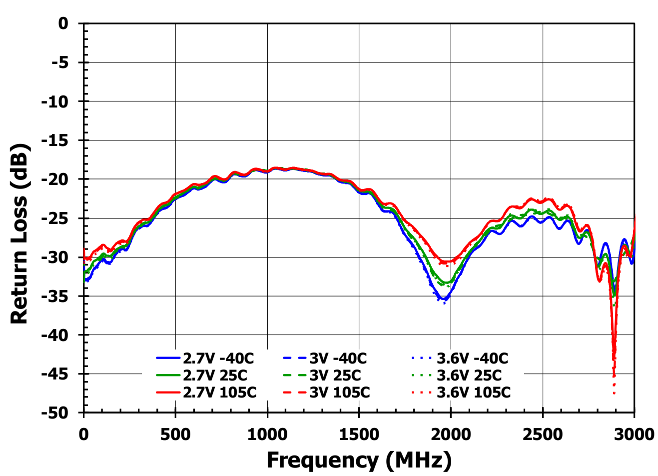
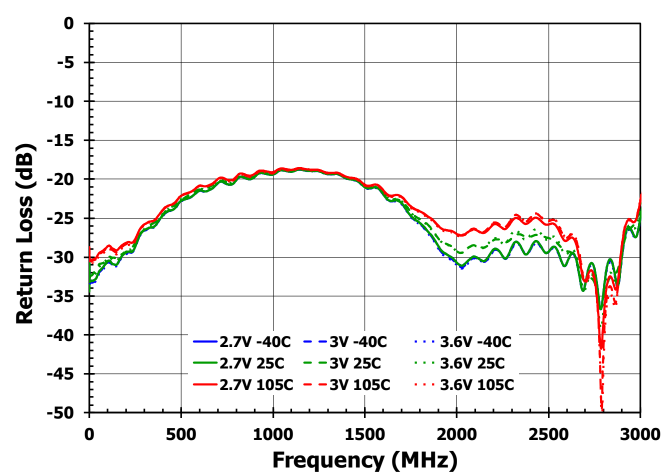


Figure 15. RFC Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]



Typical Performance Characteristics [3]

Figure 16. Evaluation Board Loss vs. Frequency over Temperature

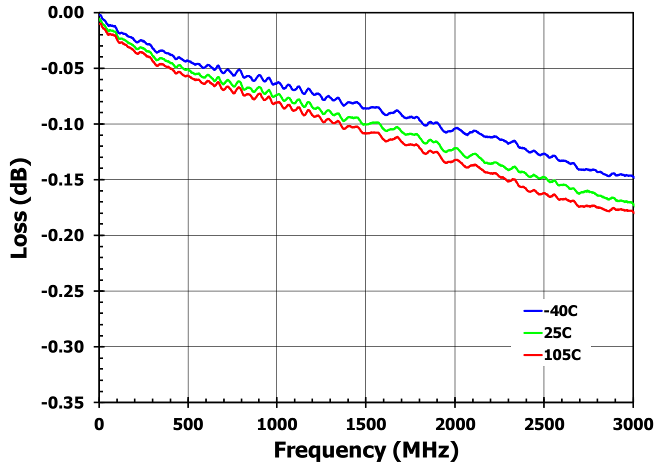


Figure 17. Eval Board Through Line Return Loss vs. Frequency over Temperature

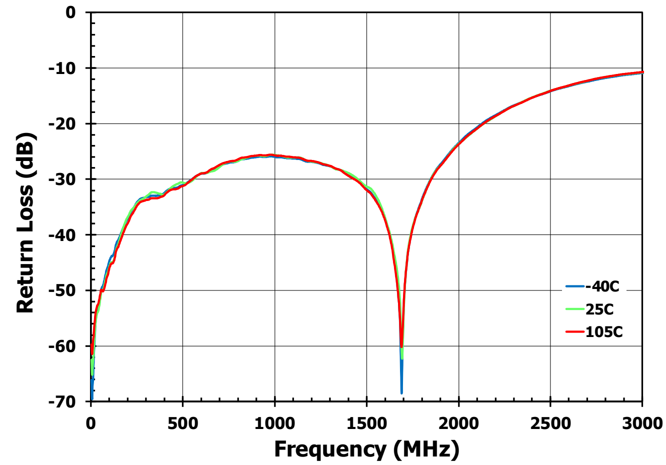


Figure 18. Switching Time Insertion Loss to Isolation

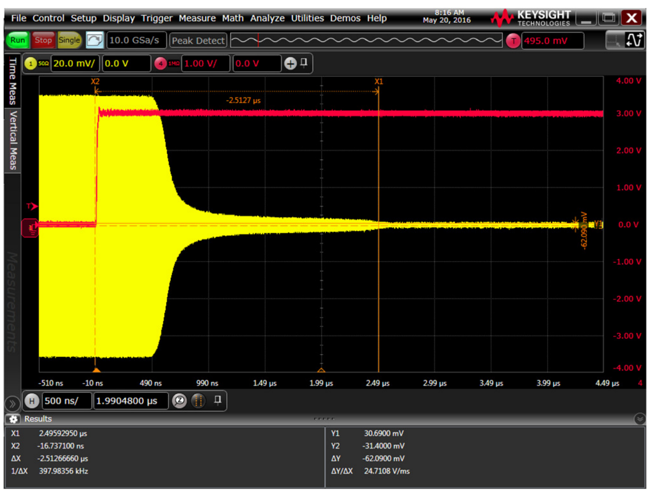


Figure 19. Switching Time Isolation to Insertion Loss

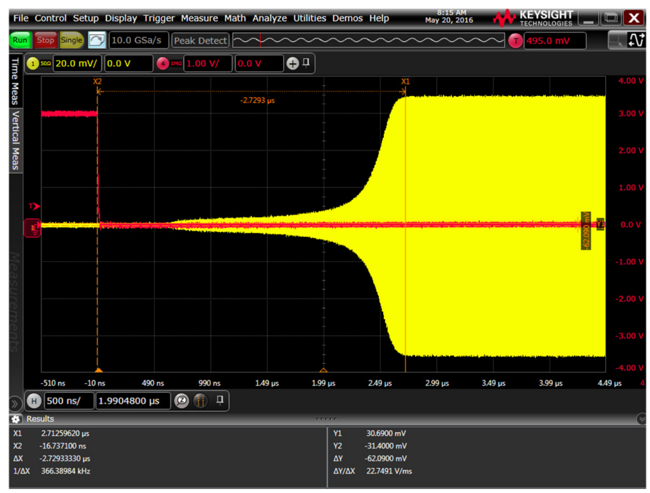


Figure 20. Idd vs. Control Voltage; VDD=2.7V (C1 set to GND and VDD)

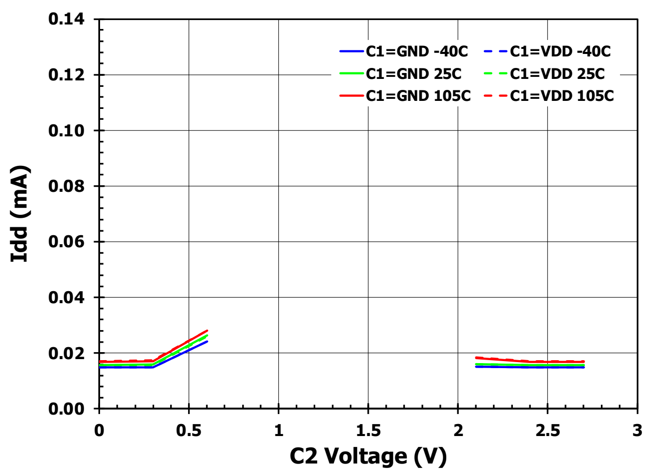
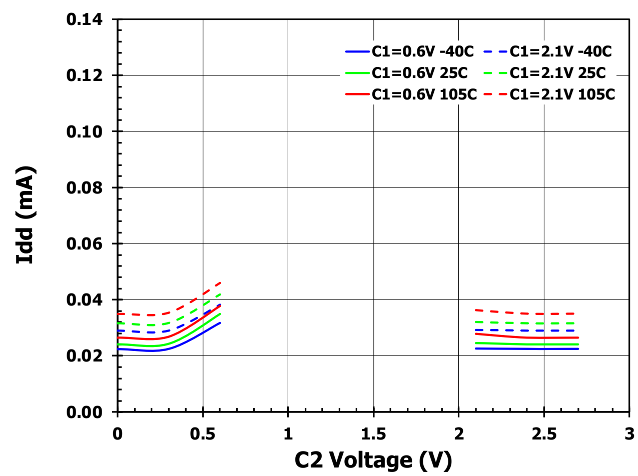


Figure 21. Idd vs. Control Voltage; VDD=2.7V (C1 set to 0.6V and 2.1V)



Typical Performance Characteristics [4]

Figure 22. Idd vs. Control Voltage; VDD=3.0V (C1 set to GND and VDD)

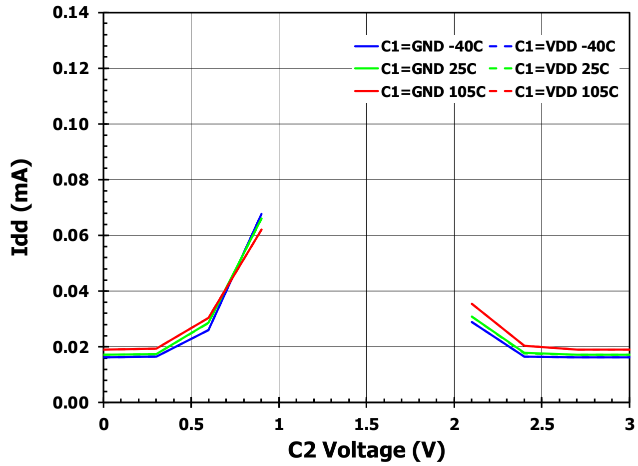


Figure 23. Idd vs. Control Voltage; VDD=3.0V (C1 set to 0.9V and 2.1V)

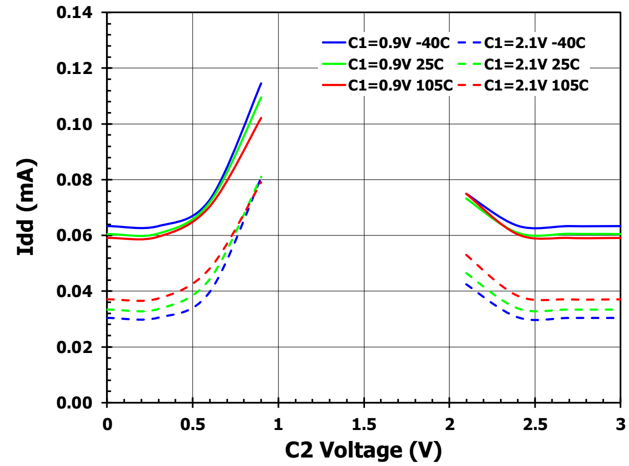


Figure 24. Idd vs. Control Voltage; VDD=3.6V (C1 set to GND and VDD)

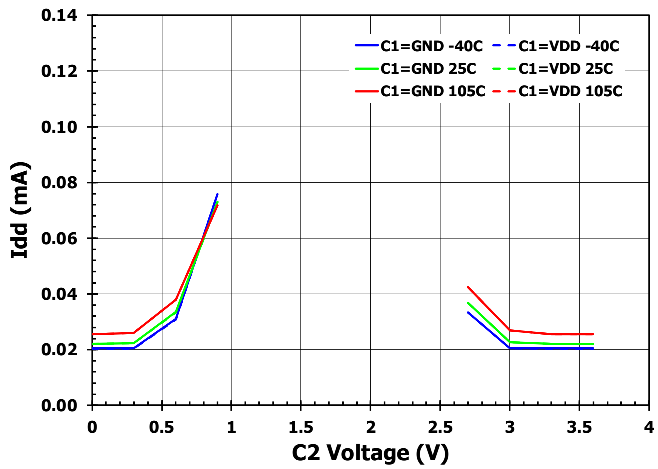
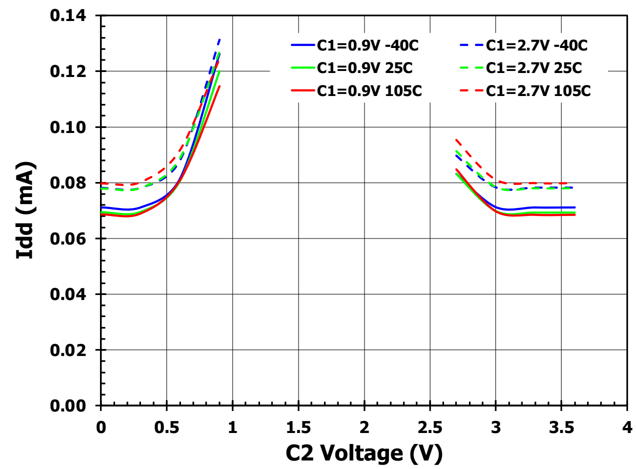


Figure 25. Idd vs. Control Voltage; VDD=3.6V (C1 set to 0.9V and 2.7V)



Evaluation Kit Picture

Figure 26. Top View

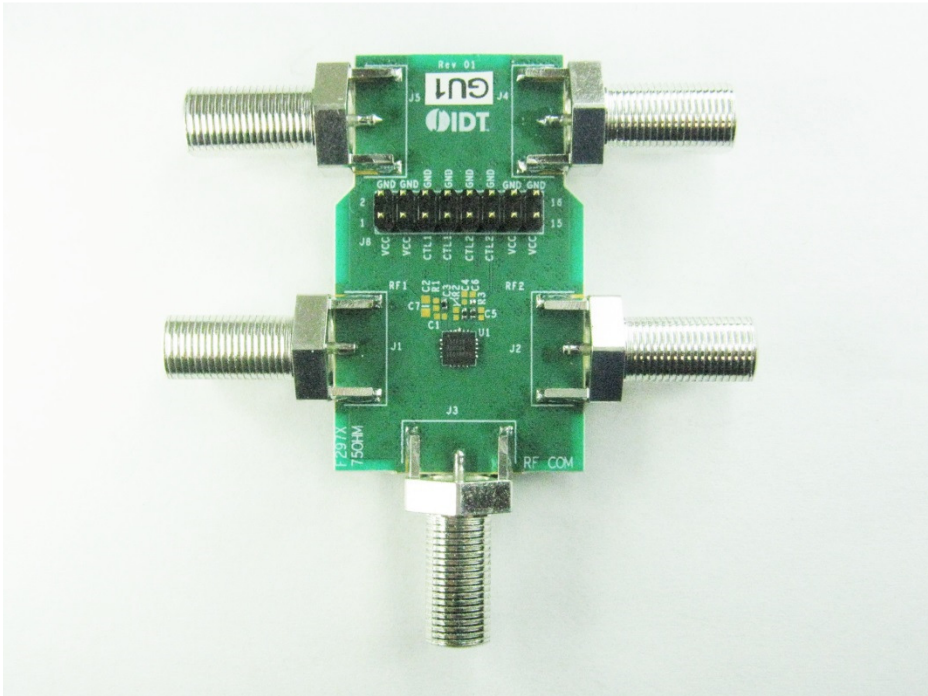
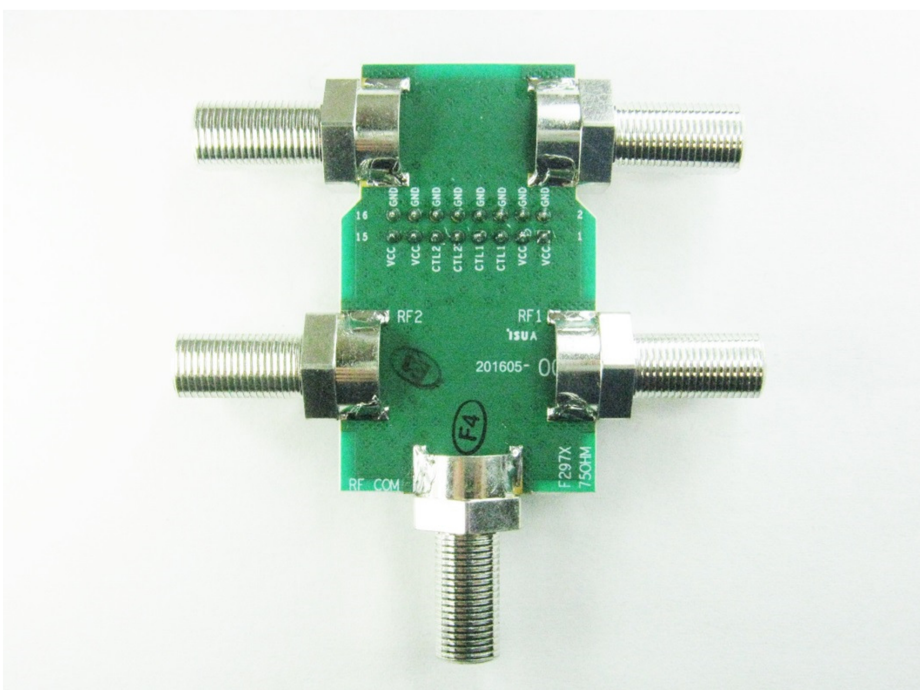


Figure 27. Bottom View



Evaluation Kit / Applications Circuit

Figure 28. Electrical Schematic

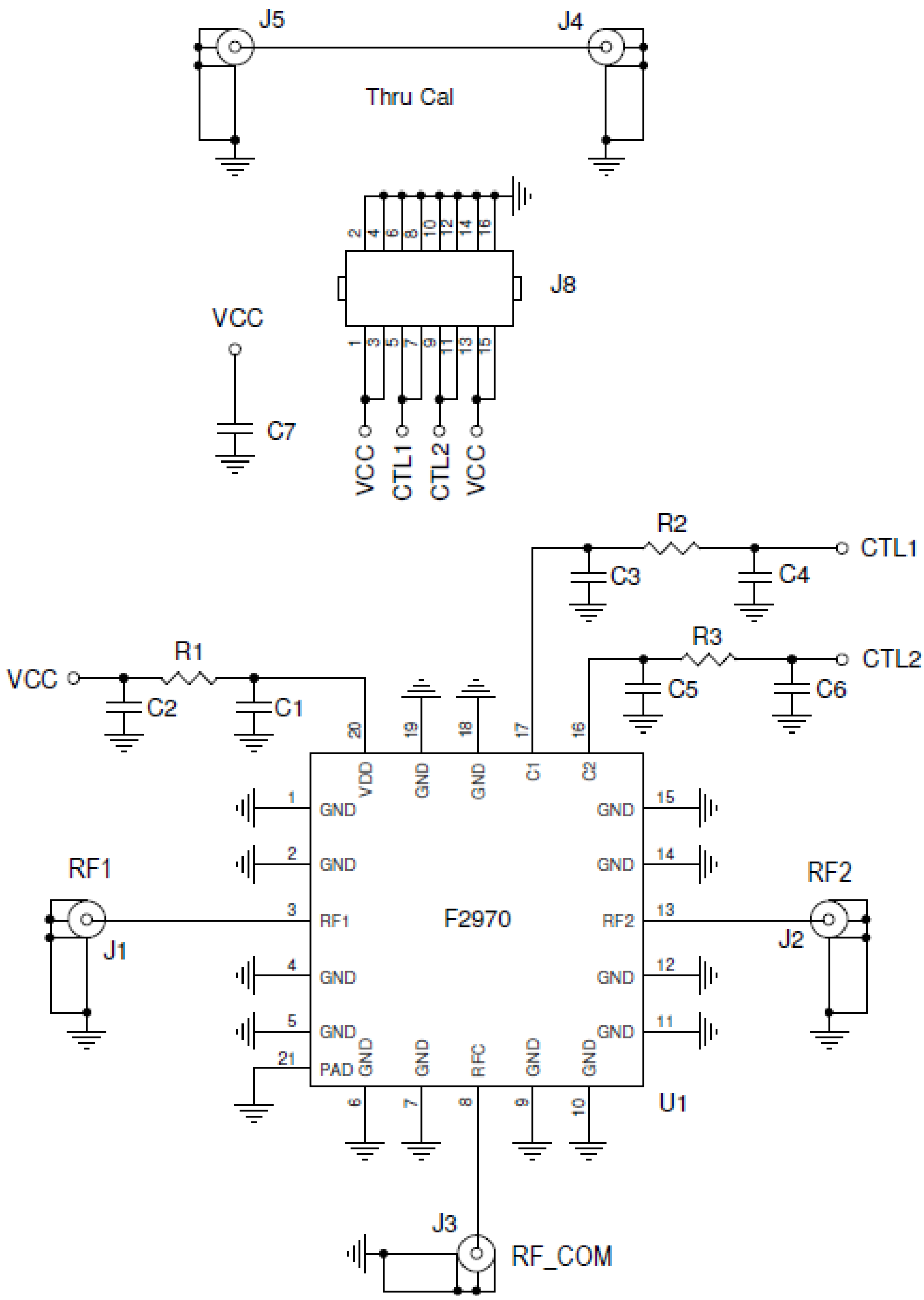


Table 7. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C6	6	Not Installed		
C7	1	1000 pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H102J	Murata
R1 – R3	3	0 ohm ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	Connector Type F	222181	Amphenol RF
J7	1	Conn Header Vert 8x2 Pos Gold	961216-6404-AR	3M
U1	1	SP2T Switch 4 mm x 4 mm LQFN	F2970NCGK	IDT
	1	Printed Circuit Board	F2970 EVKIT REV 01	IDT

Control Mode

Table 8 Switch Control Truth Table

C1	C2	RFC – RF1	RFC – RF2	75 Ohm Terminated Ports
0	0	ON	OFF	RF2
0	1	OFF	ON	RF1
1	0	OFF	ON	RF1
1	1	ON	OFF	RF2

Evaluation Kit Operation

Default Start-up

Control pins do not include internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

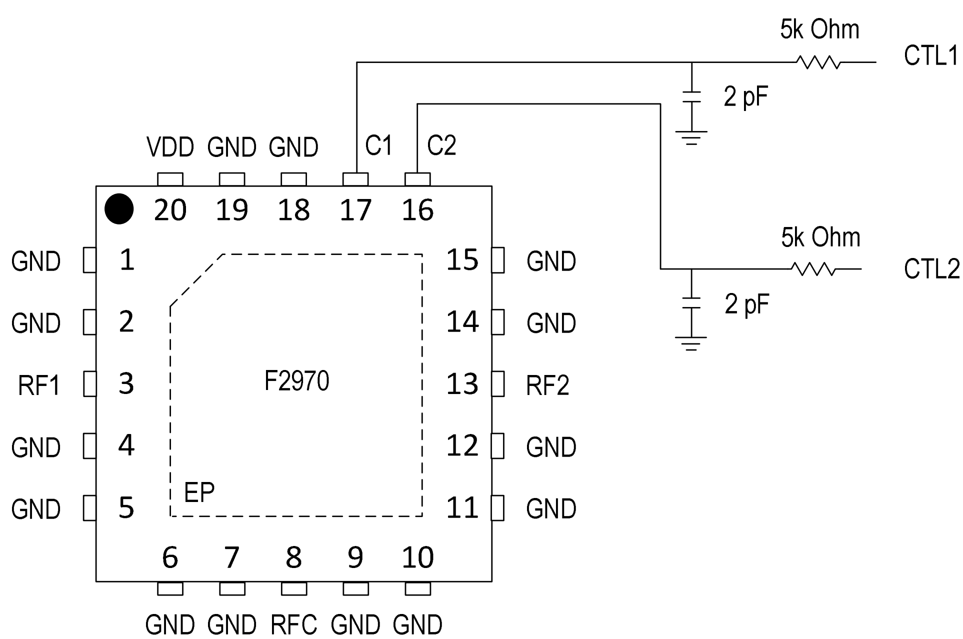
Power Supplies

A common V_{cc} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20 uS. In addition, all control pins should remain at 0V (+/- 0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 16 & 17 as shown below.

Figure 29. Control Pin Interface Schematic



External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.7 V to 3.6 V with the power supply output disabled.

Logic Control Setup

External logic control is applied to J8 CTL1 (pins 5 and 7) and CTL2 (pins 9 and 11). See Table 8 for the logic truth table.

Turn On Procedure

Setup the supplies and EVKIT as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V_{CC} supply.

Set the desired logic setting to achieve the desired configuration (see Table 8). Note that external control logic should not be applied without V_{CC} being present.

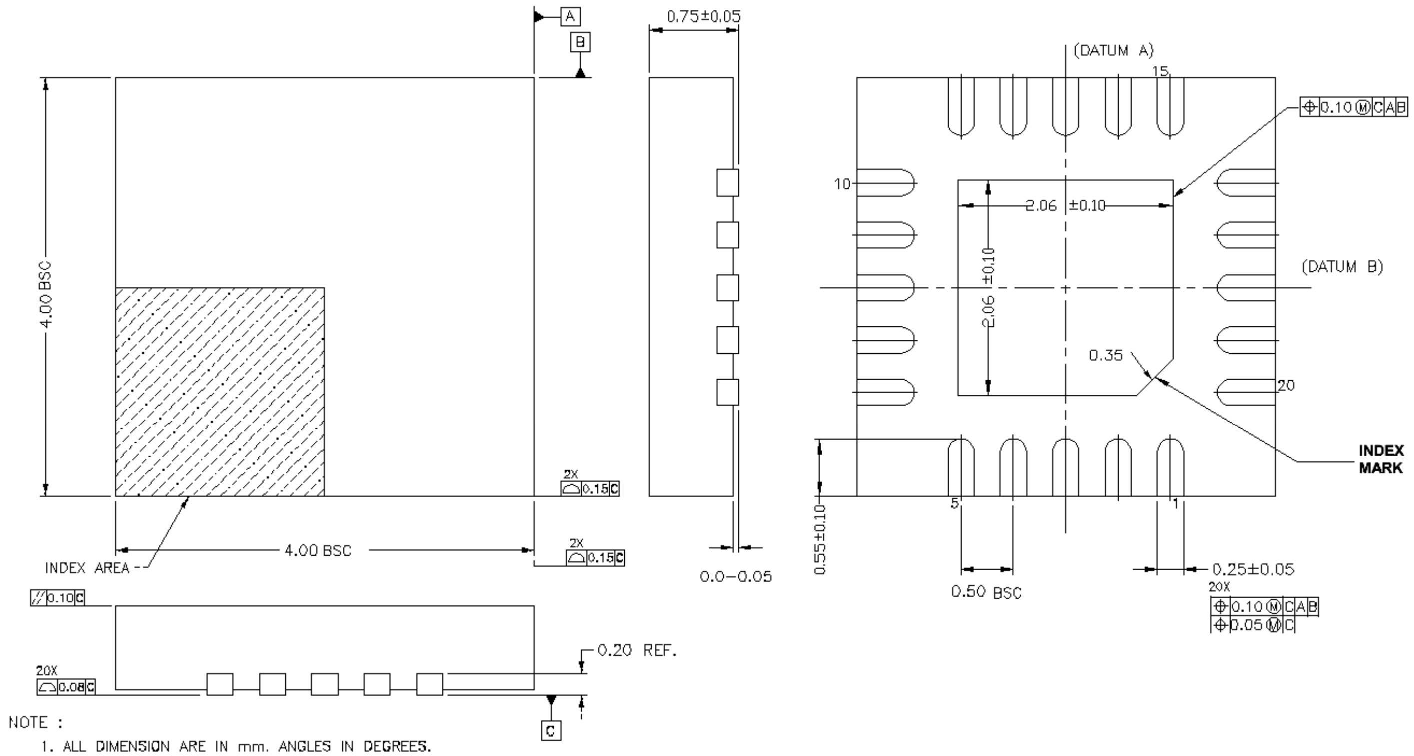
Turn Off Procedure

Set the logic control to a logic low.

Disable the V_{CC} supply.

Package Drawings

Figure 30. Package Outline Drawing



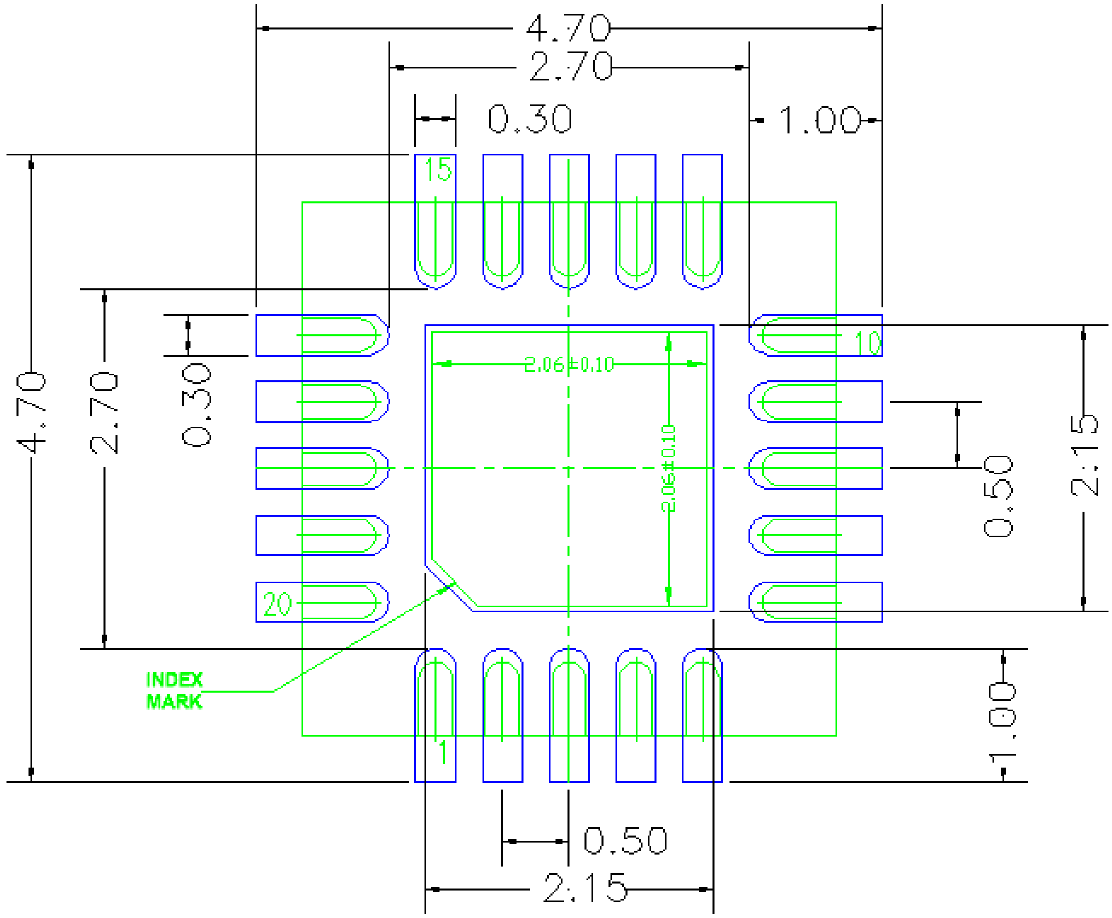
NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. REFER JEDEC MO-220.

TOLERANCES UNLESS SPECIFIED DECIMAL X± XX± XXX± ANGULAR ±1°	IDT™ www.IDT.com 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591			
APPROVALS	DATE	TITLE NCG20 PACKAGE OUTLINE 4.0 x 4.0 mm BODY 0.50 mm PITCH LQFN		
DRAWN XCB	10/09/12			
CHECKED				
		SIZE C	DRAWING No. PSC-4445	REV 02
		DO NOT SCALE DRAWING	SHEET 1 OF 2	

Recommended Land Pattern

Figure 31. Recommended Land Pattern



RECOMMENDED LAND PATTERN DIMENSION

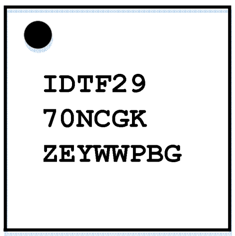
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2970NCGK	4.00 x 4.00 x 0.75 mm LQFN	MSL1	Bulk	-40° to +105°C
F2970NCGK8	4.00 x 4.00 x 0.75 mm LQFN	MSL1	Tape and Reel	-40° to +105°C
F2970EVBI	Evaluation Board			

Marking Diagram



1. Line 1 and 2 are the part number.
2. Line 3 - “ZE” are for die version.
3. Line 3 - “YWW” is last digit of the year plus work week.
4. Line 3 - “PBG” denotes the production process.

Revision History

Revision	Revision Date	Description of Change
O	2016-November-10	Initial Release

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Contact Information

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