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April 1st, 2010
Renesas Electronics Corporation

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H5N2001LD, H5N2001LS, H5N2001LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1339-0600

Rev.6.00

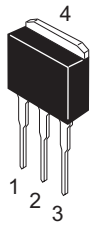
Jul 14, 2006

Features

- Low on-resistance
- Low leakage current
- High speed switching

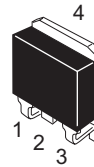
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



H5N2001LD

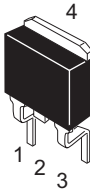
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(Package name: LDKPAK (S)-(1))



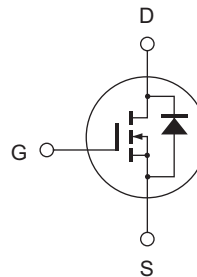
H5N2001LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDKPAK (S)-(2))



H5N2001LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	200	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	20	A
Drain peak current	I _{D (pulse)} ^{Note 1}	80	A
Body to drain diode reverse drain current	I _{DR}	20	A
Body to drain diode reverse drain peak current	I _{DR (pulse)} ^{Note 1}	80	A
Avalanche current	I _{AP} ^{Note 3}	20	A
Channel dissipation	P _{ch} ^{Note 2}	75	W
Channel to case Thermal Impedance	θ _{ch-c}	1.67	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_c = 25°C
 3. T_{ch} ≤ 150°C

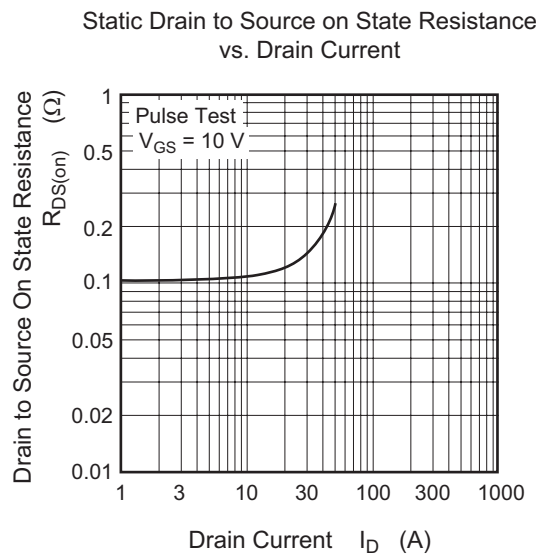
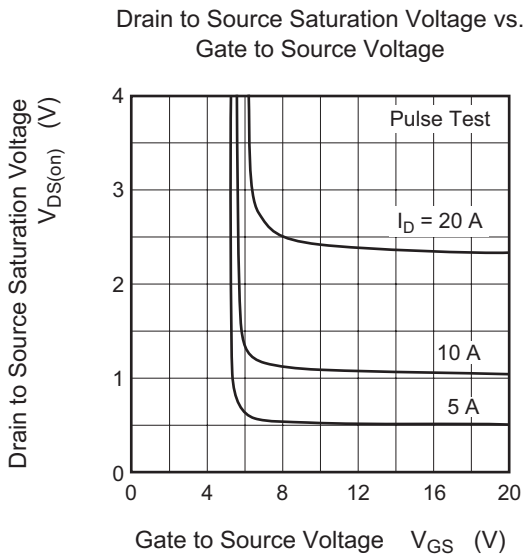
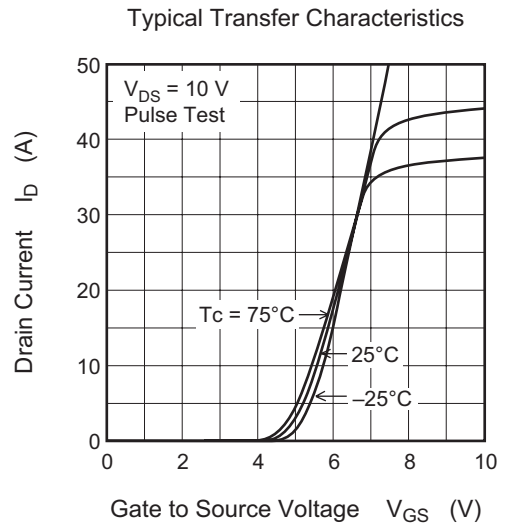
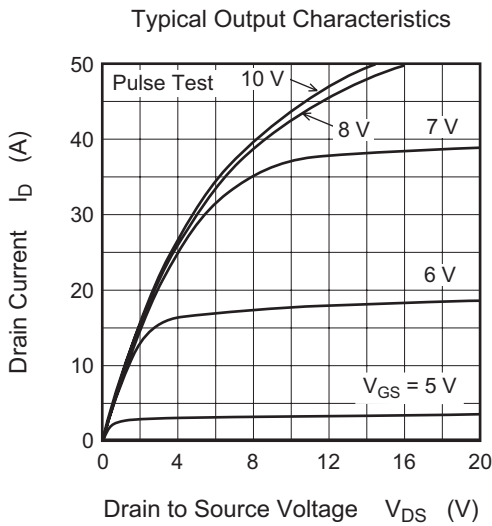
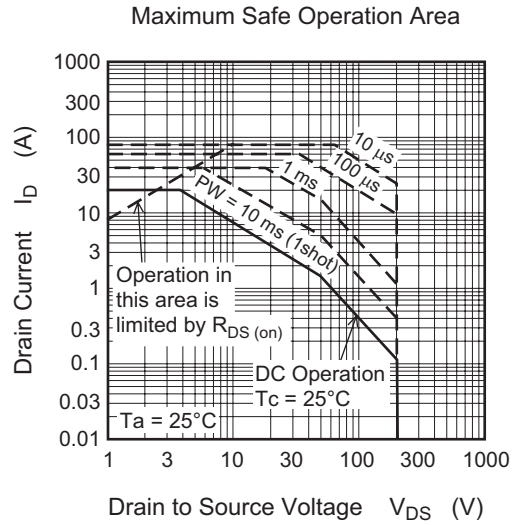
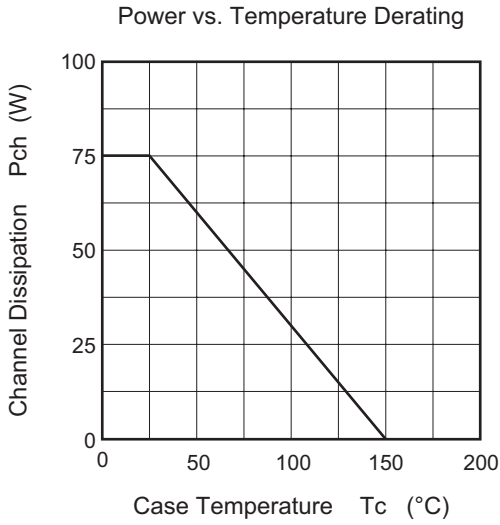
Electrical Characteristics

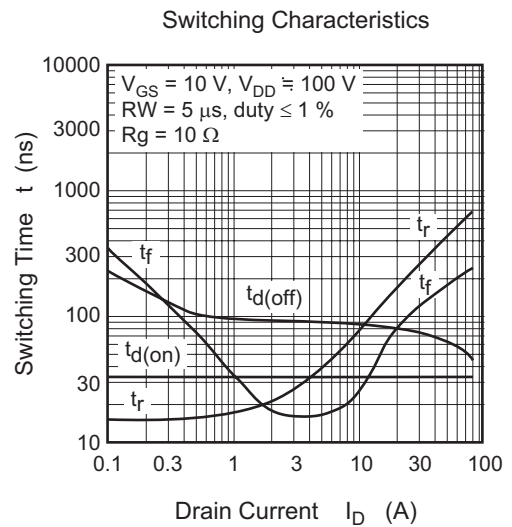
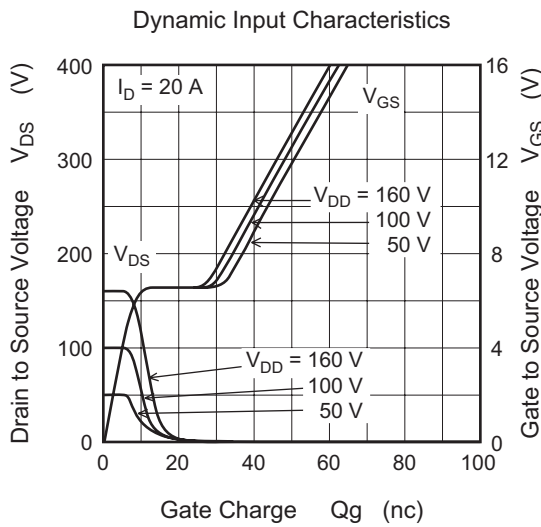
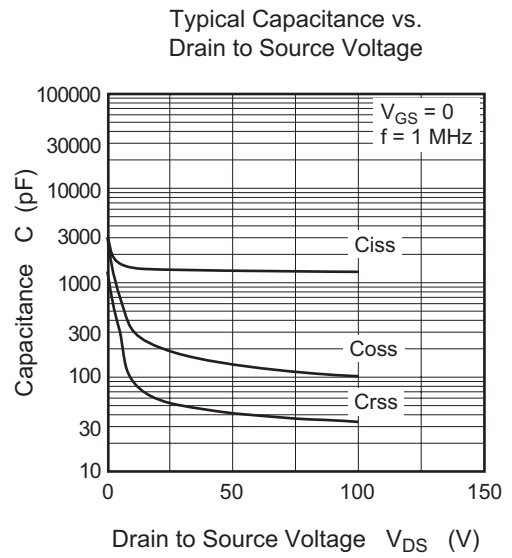
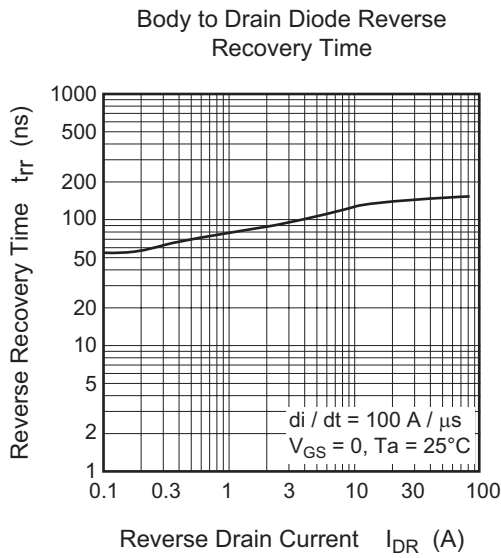
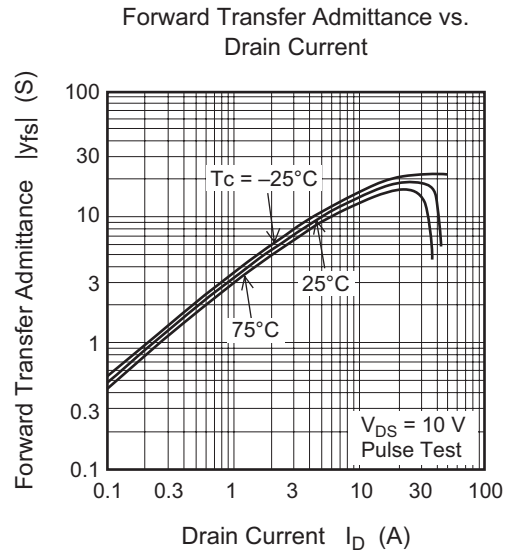
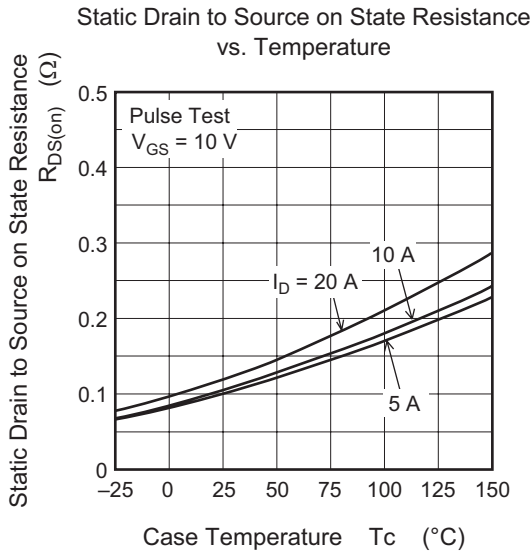
(Ta = 25°C)

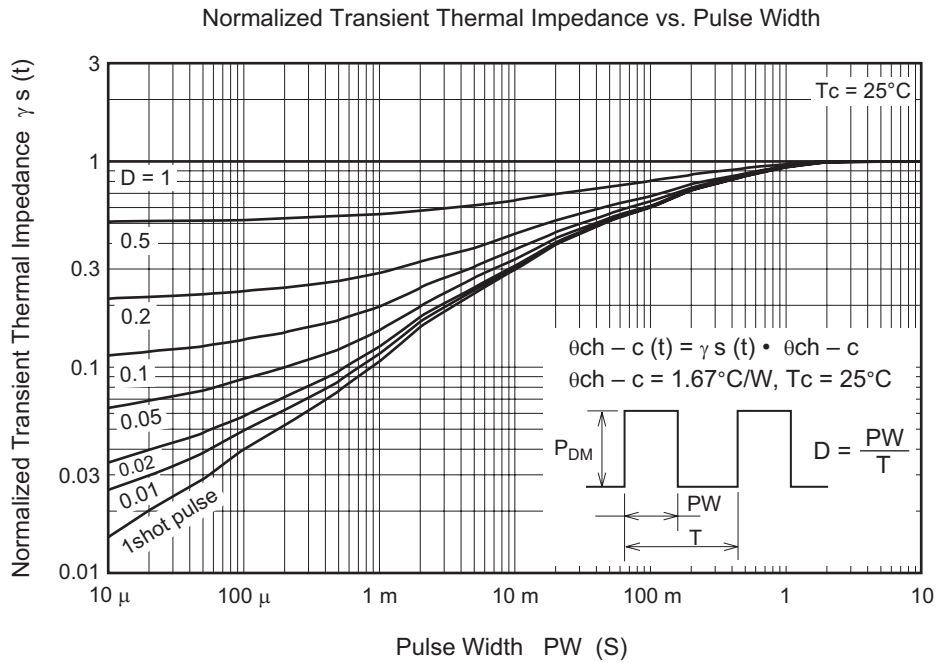
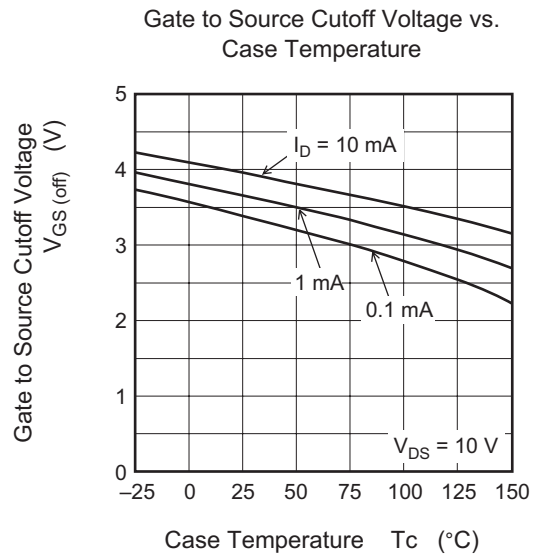
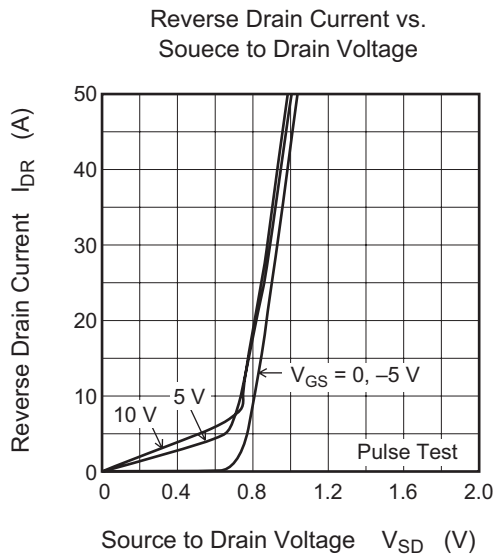
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	200	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±30 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	1	μA	V _{DS} = 200 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	3.0	—	4.5	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS (on)}	—	0.100	0.125	Ω	I _D = 10 A, V _{GS} = 10 V ^{Note 4}
Forward transfer admittance	y _{fs}	8	14	—	S	I _D = 10 A, V _{DS} = 10 V ^{Note 4}
Input capacitance	C _{iss}	—	1350	—	pF	V _{DS} = 25 V
Output capacitance	C _{oss}	—	180	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	55	—	pF	f = 1 MHz
Turn-on delay time	t _{d (on)}	—	35	—	ns	I _D = 10 A
Rise time	t _r	—	70	—	ns	R _L = 10 Ω
Turn-off delay time	t _{d (off)}	—	85	—	ns	V _{GS} = 10 V
Fall time	t _f	—	20	—	ns	R _g = 10 Ω
Total gate charge	Q _g	—	44	—	nC	V _{DD} = 160 V
Gate to source charge	Q _{gs}	—	8	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	22	—	nC	I _D = 20 A
Body to drain diode forward voltage	V _{DF}	—	0.9	1.4	V	I _F = 20 A, V _{GS} = 0 ^{Note 4}
Body to drain diode reverse recovery time	t _{rr}	—	140	—	ns	I _F = 20 A, V _{GS} = 0
Body to drain diode reverse recovery charge	Q _{rr}	—	0.7	—	μC	di _F /dt = 100 A/μs

- Note: 4. Pulse test

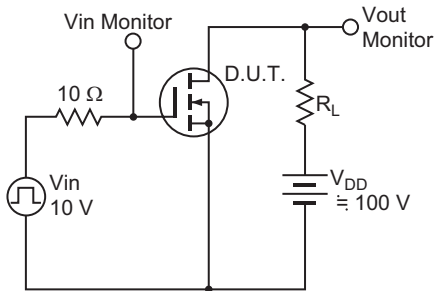
Main Characteristics



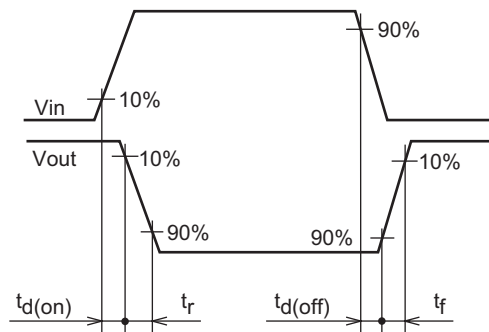




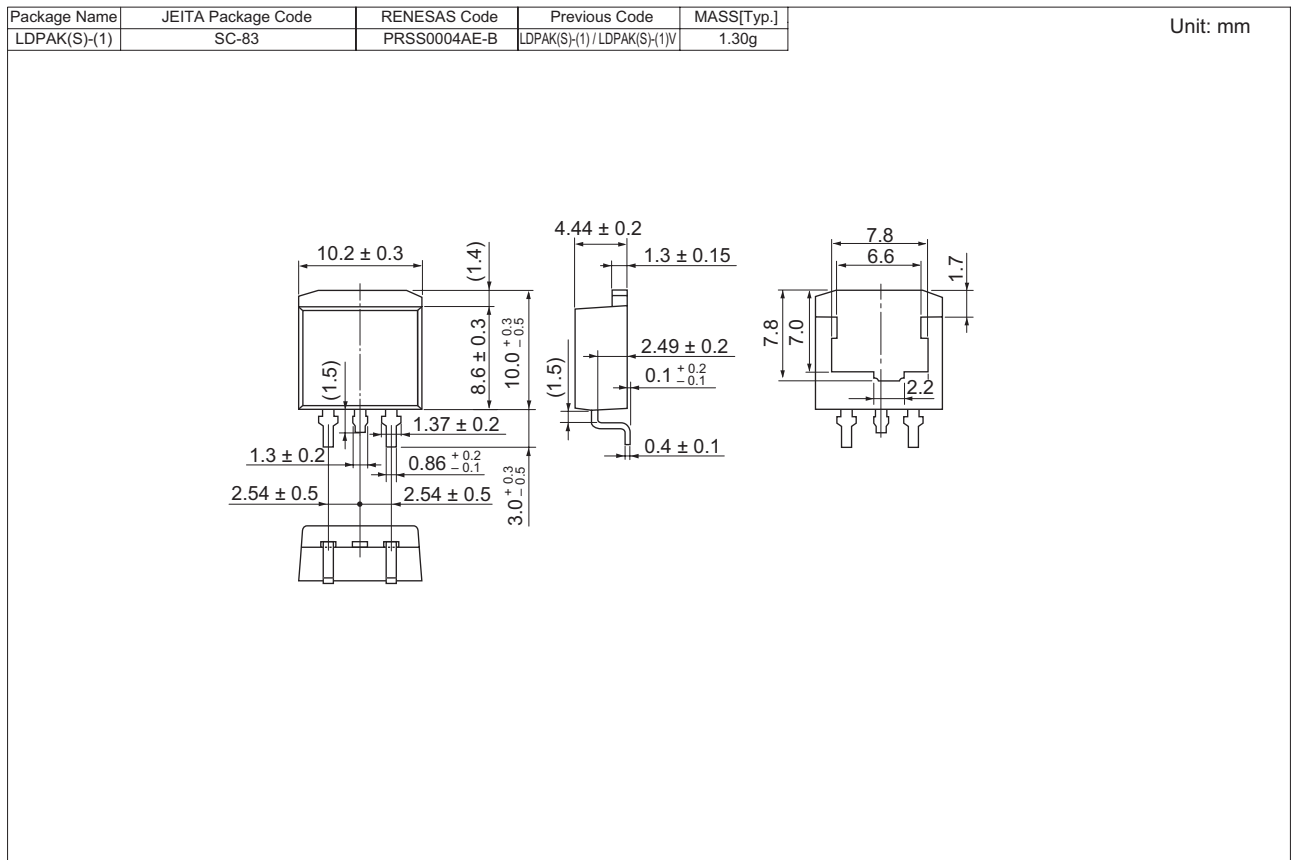
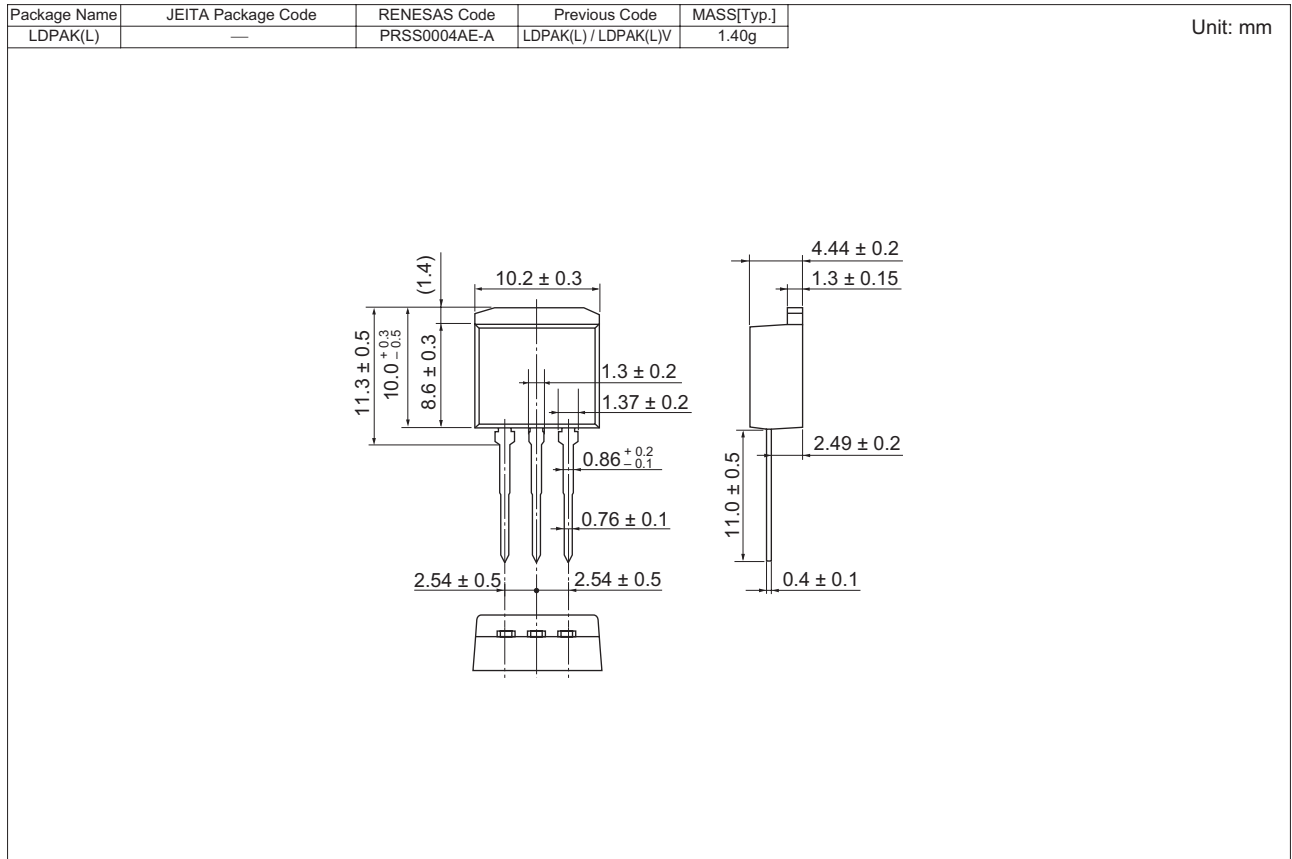
Switching Time Test Circuit



Switching Time Waveform



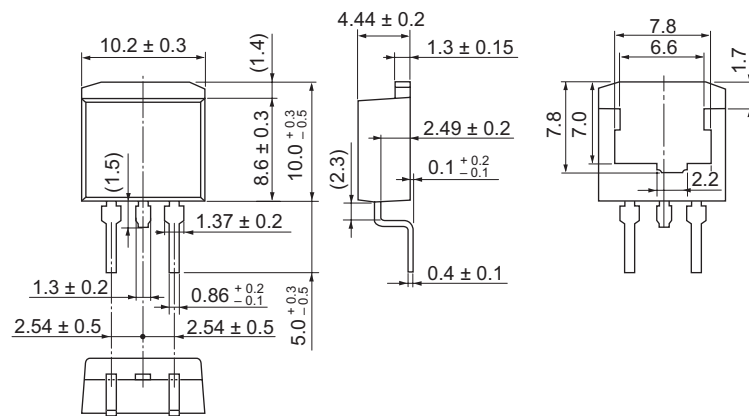
Package Dimensions



H5N2001LD, H5N2001LS, H5N2001LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(2)	—	PRSS0004AE-C	LDBPAK(S)-(2) / LDBPAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H5N2001LD-E	500 pcs	Box (Conductive Sack)
H5N2001LSTL-E	1000 pcs	Taping
H5N2001LMTL-E	1000 pcs	Taping

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