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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H5N2004DL, H5N2004DS

Silicon N Channel MOS FET
High Speed Power Switching

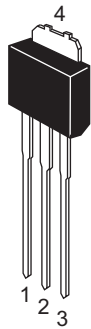
REJ03G1103-0200
(Previous: ADE-208-1372)
Rev.2.00
Sep 07, 2005

Features

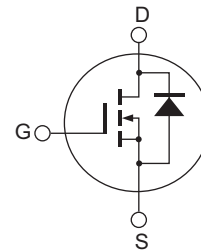
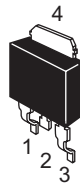
- Low on-resistance: $R_{DS(on)} = 0.38 \Omega$ typ.
- Low leakage current: $I_{DSS} = 1 \mu A$ max (at $V_{DS} = 200 V$)
- High speed switching: $t_f = 10 ns$ typ (at $V_{GS} = 10 V$, $V_{DD} = 100 V$, $I_D = 4 A$)
- Low gate charge: $Q_g = 14 nC$ typ (at $V_{DD} = 160 V$, $V_{GS} = 10 V$, $I_D = 8 A$)
- Avalanche ratings

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D (pulse)}$ ^{Note 1}	32	A
Body-drain diode reverse drain current	I_{DR}	8	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}$ ^{Note 1}	32	A
Avalanche current	I_{AP} ^{Note 3}	7	A
Channel dissipation	P_{ch} ^{Note 2}	30	W
Channel to case thermal impedance	θ_{ch-c}	4.17	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. $T_{ch} \leq 150^\circ C$

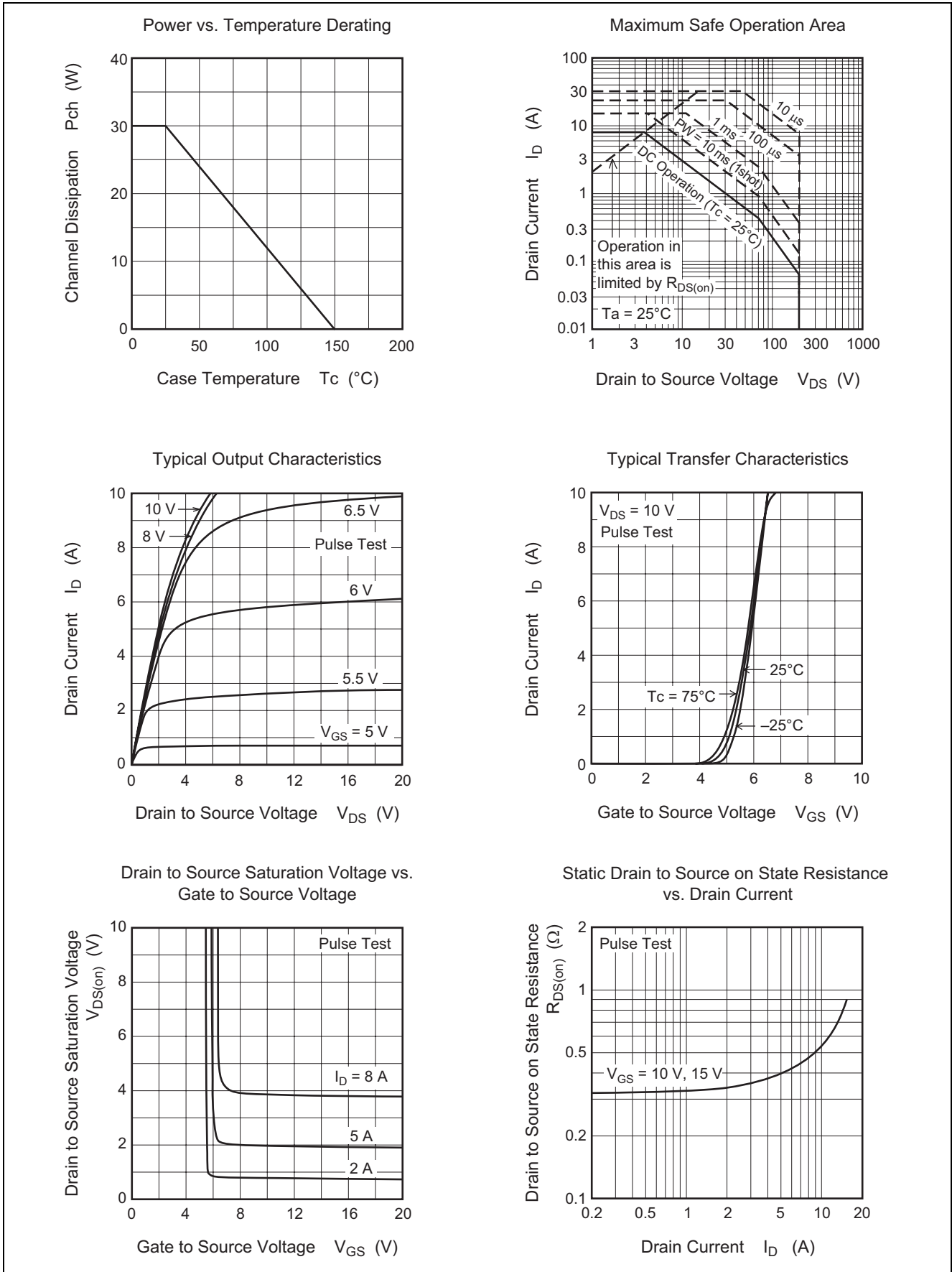
Electrical Characteristics

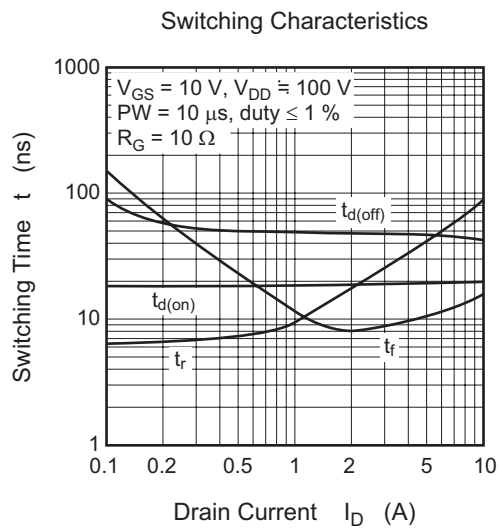
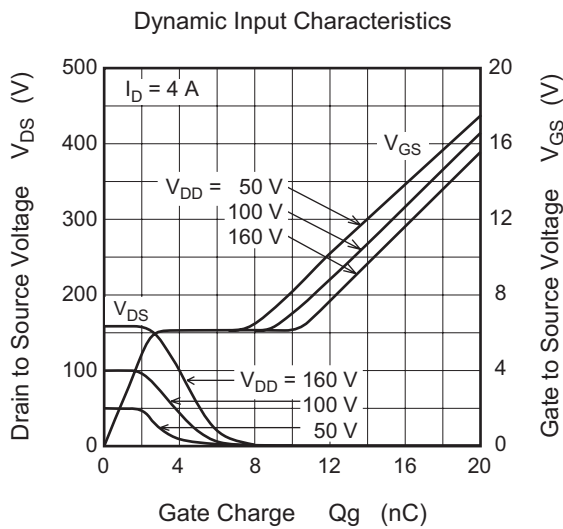
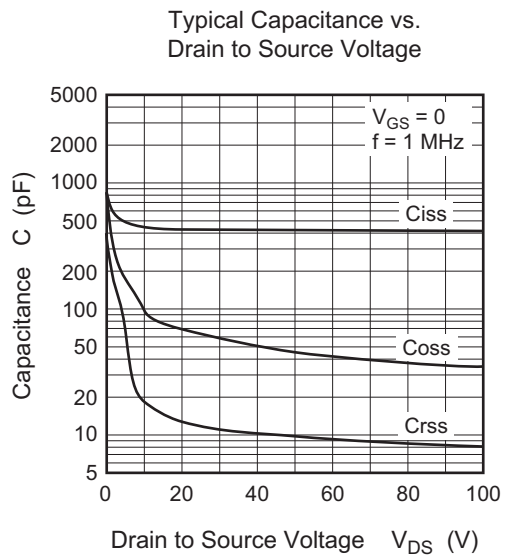
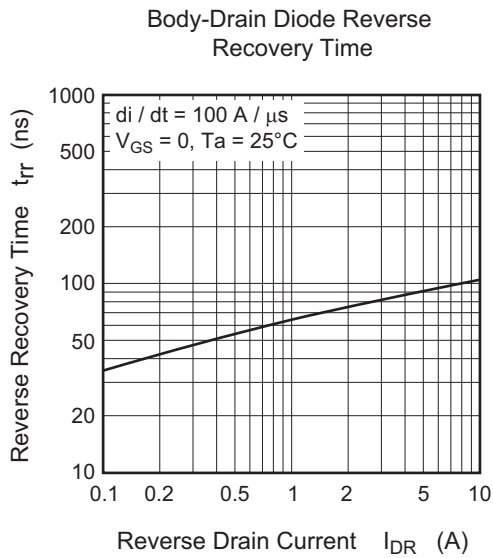
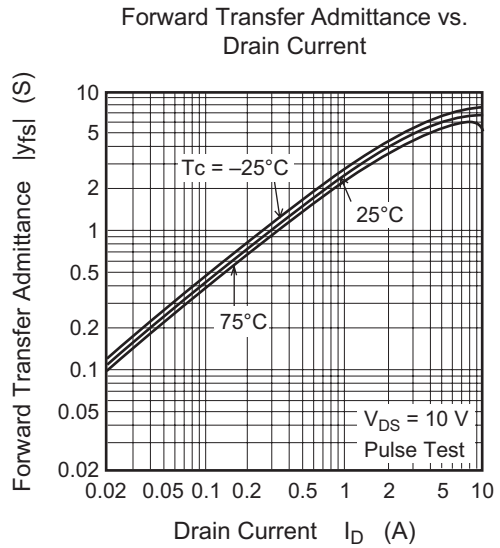
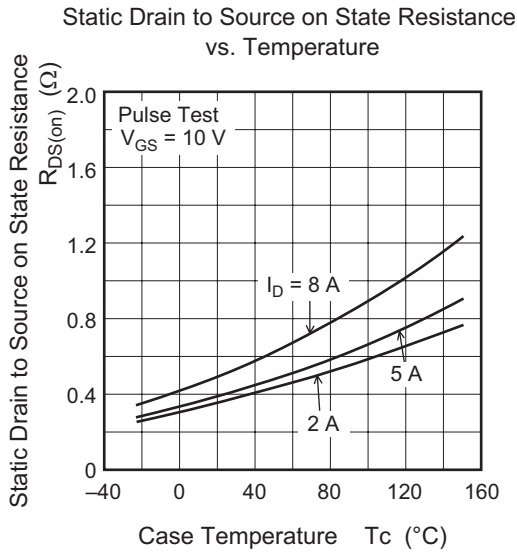
(Ta = 25°C)

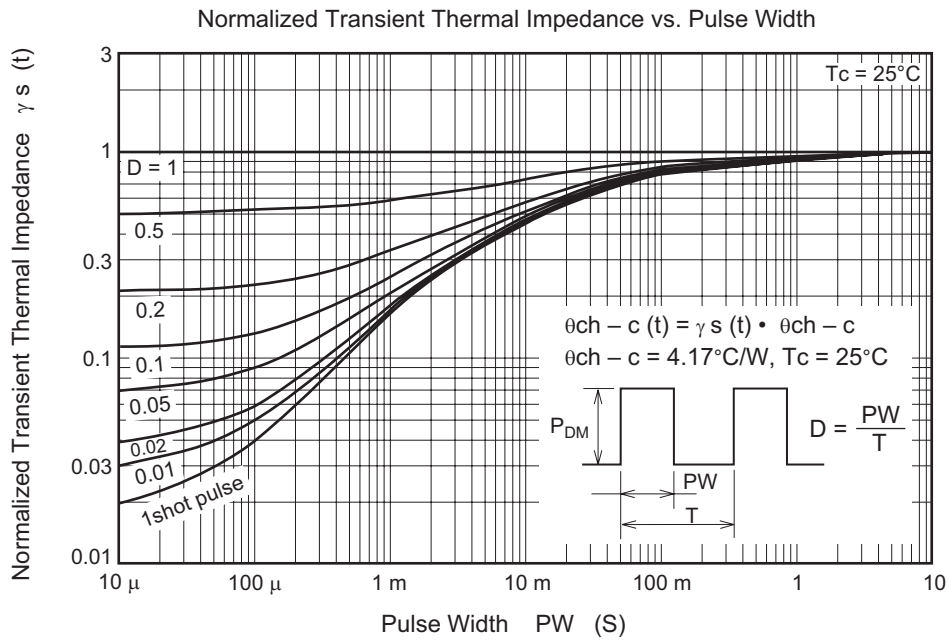
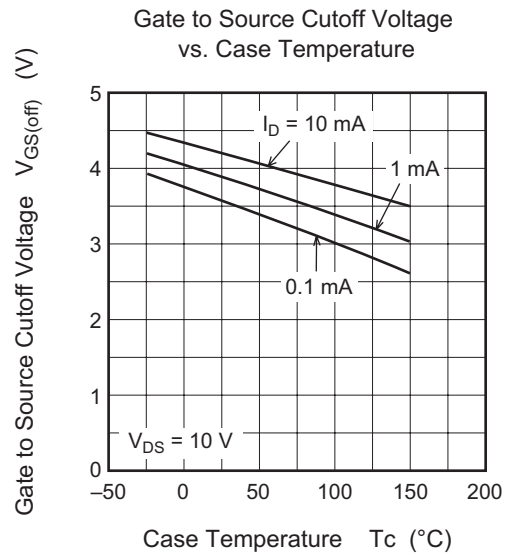
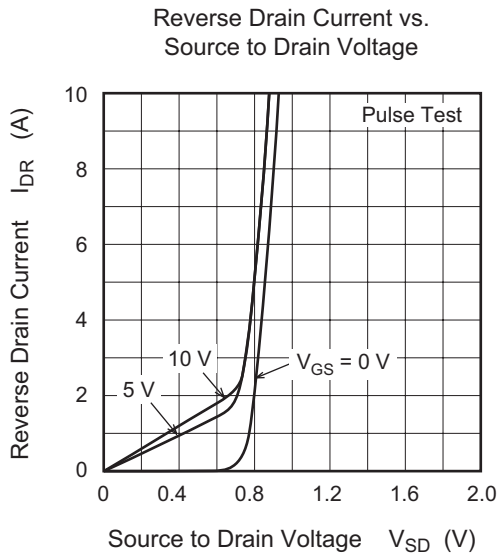
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR) DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS (off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS (on)}$	—	0.38	0.48	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	3.3	5.5	—	S	$I_D = 4 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	450	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	65	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	13	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d (on)}$	—	19	—	ns	$I_D = 4 \text{ A}$
Rise time	t_r	—	32	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d (off)}$	—	47	—	ns	$R_L = 25 \Omega$
Fall time	t_f	—	10	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	14	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	Q_{gs}	—	2.5	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	7.5	—	nC	$I_D = 4 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 8 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = 8 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	0.4	—	μC	$di_F/dt = 50 \text{ A}/\mu s$

Note: 4. Pulse test

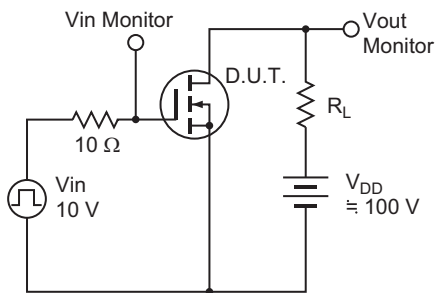
Main Characteristics



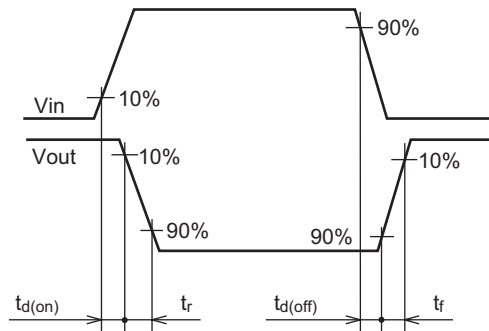




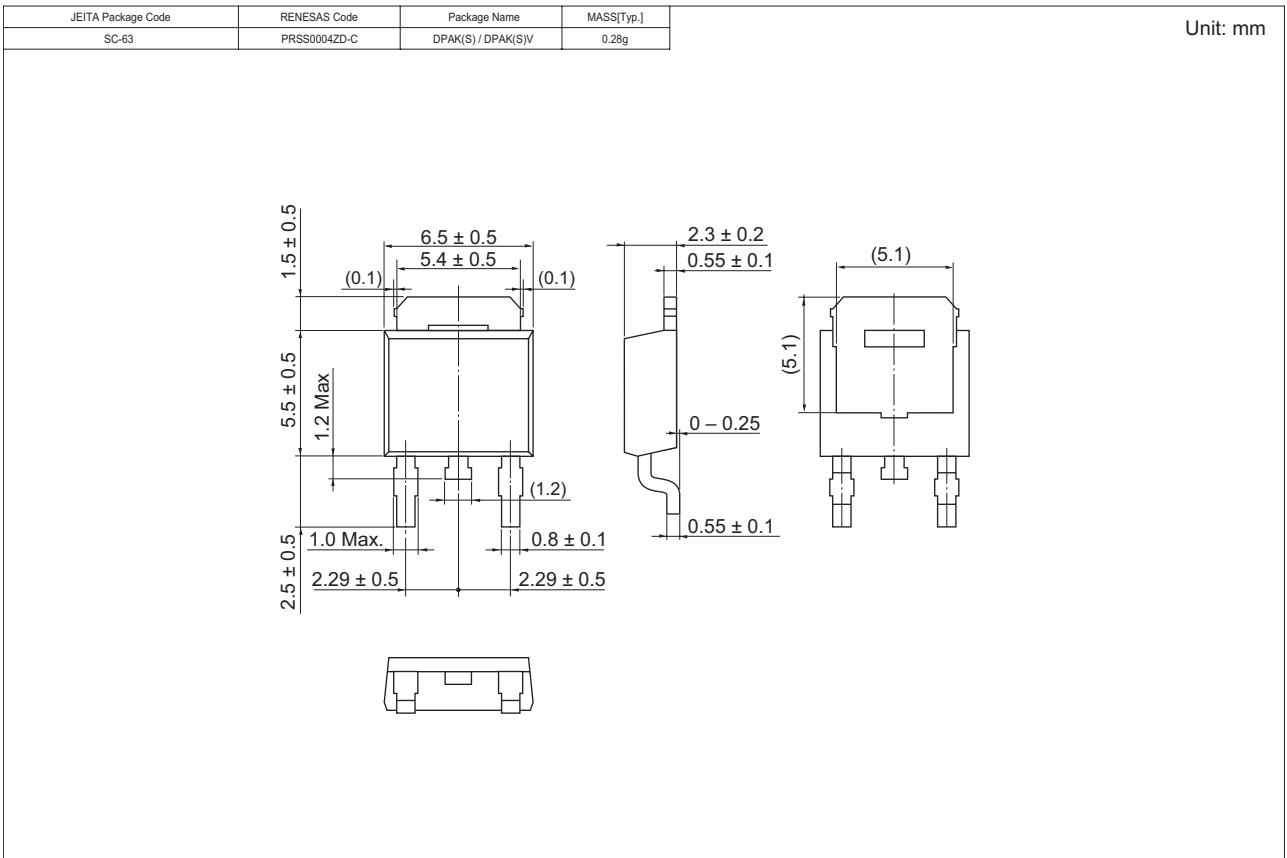
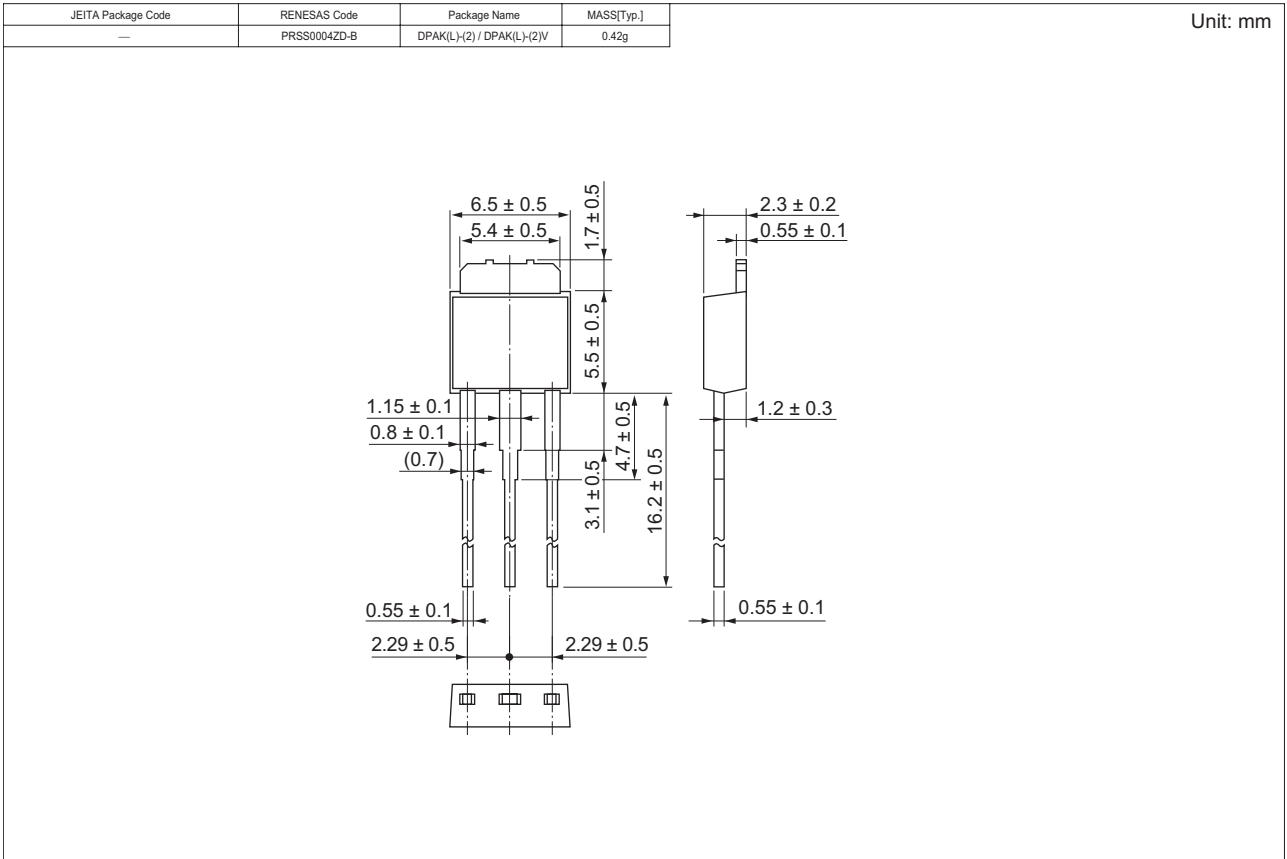
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
H5N2004DL-E	3200 pcs	Box (Sack)
H5N2004DSTL-E	3000 pcs	Taping

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