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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H7N0608LD, H7N0608LS, H7N0608LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G0144-0100Z

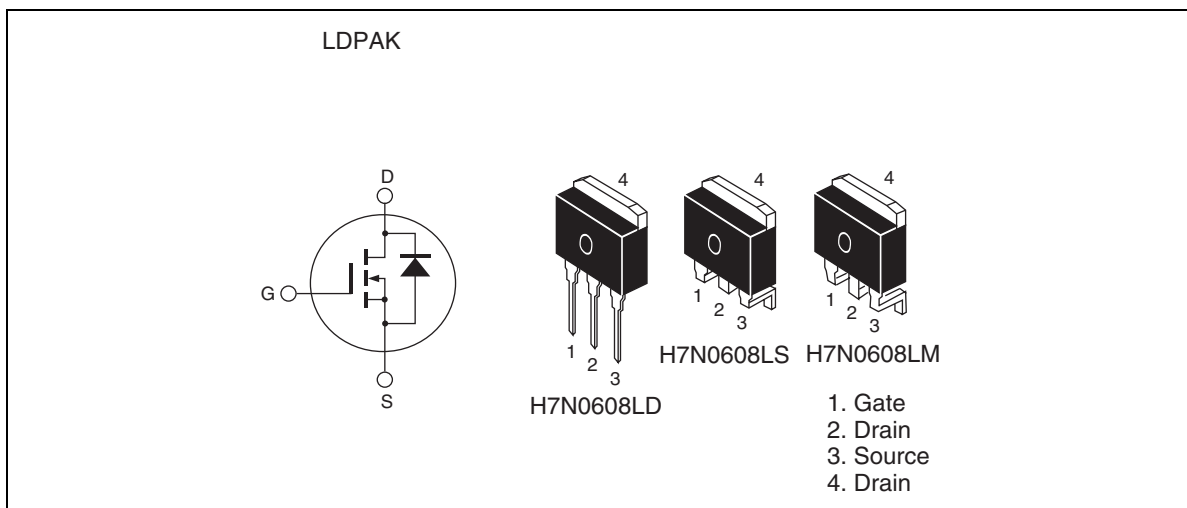
Rev.1.00

Oct.30.2003

Features

- Low on-resistance
 $R_{DS(on)} = 6.0 \text{ m}\Omega$ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	60	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	70	A
Drain peak current	I _D (pulse) ^{Note1}	280	A
Body-drain diode reverse drain current	I _{DR}	70	A
Avalanche current	I _{AP} ^{Note3}	40	A
Avalanche energy	E _{AR} ^{Note3}	137	mJ
Channel dissipation	P _{ch} ^{Note2}	80	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

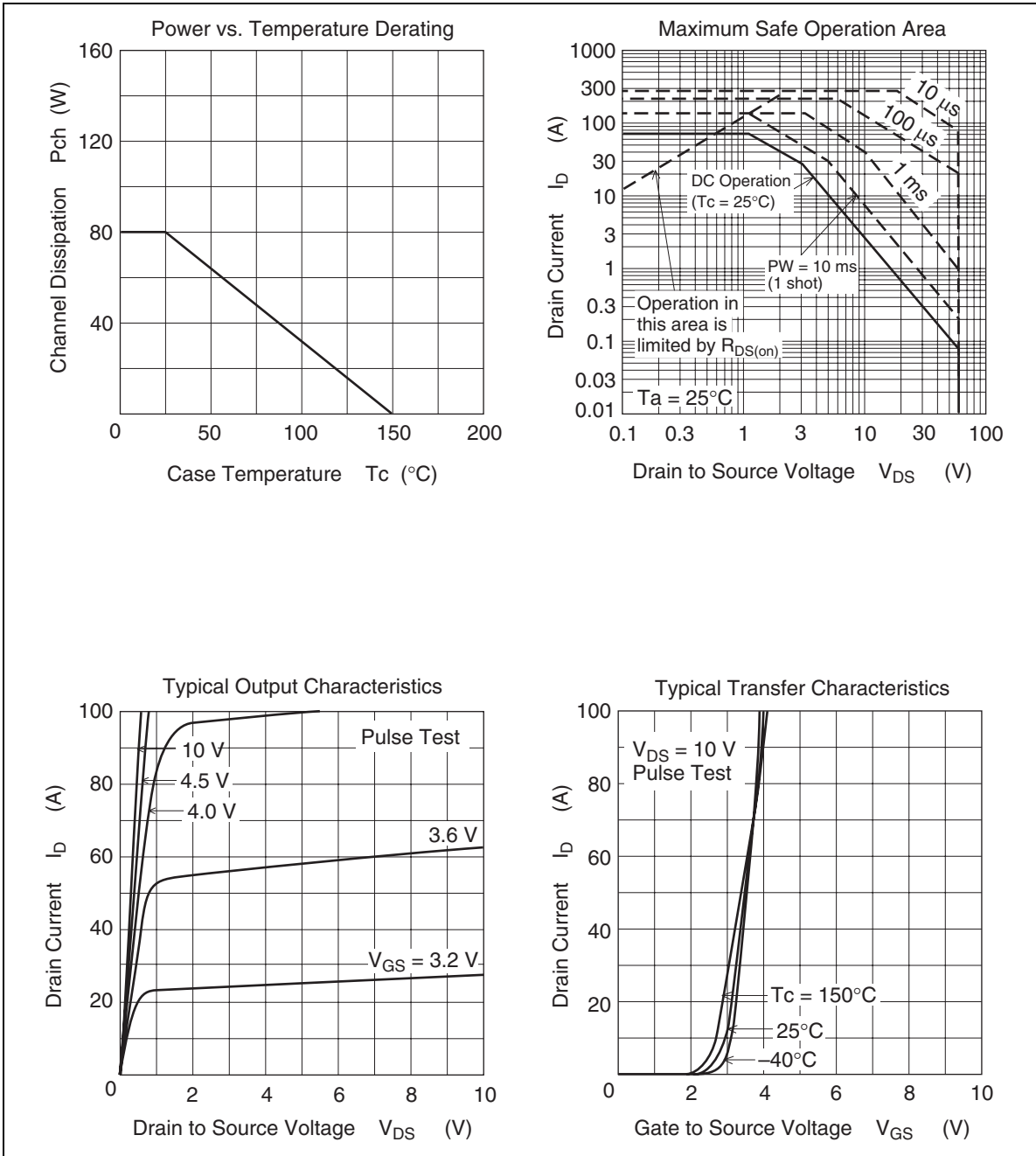
Electrical Characteristics

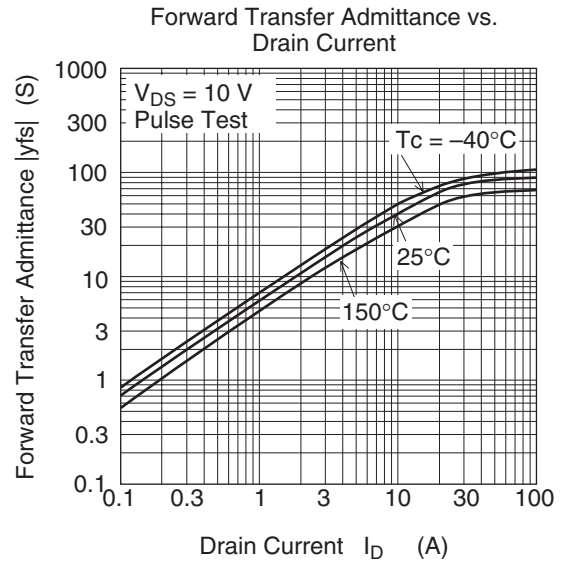
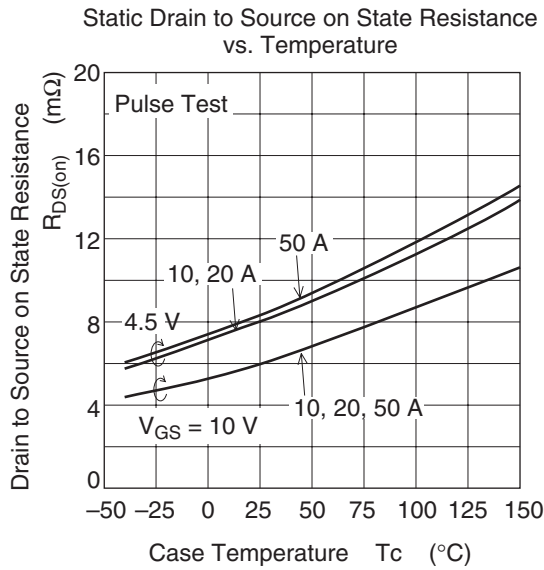
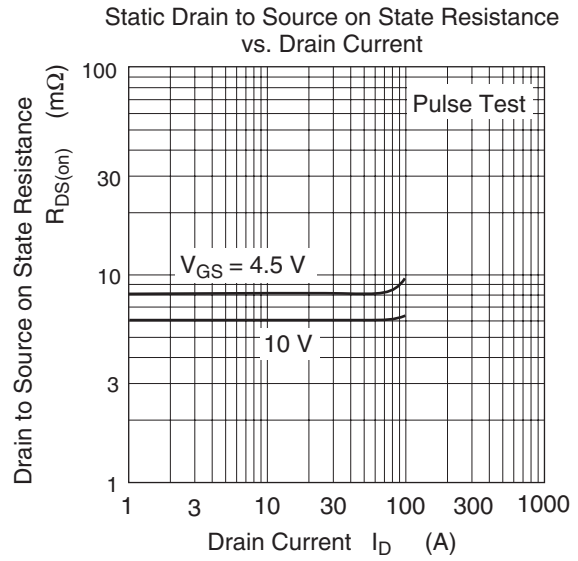
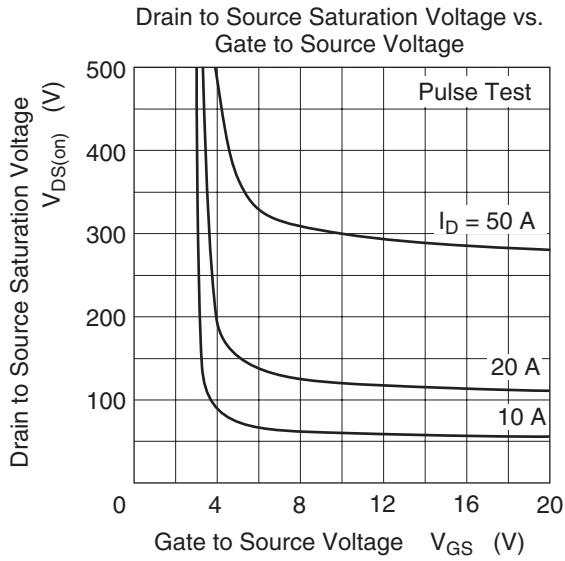
(Ta = 25°C)

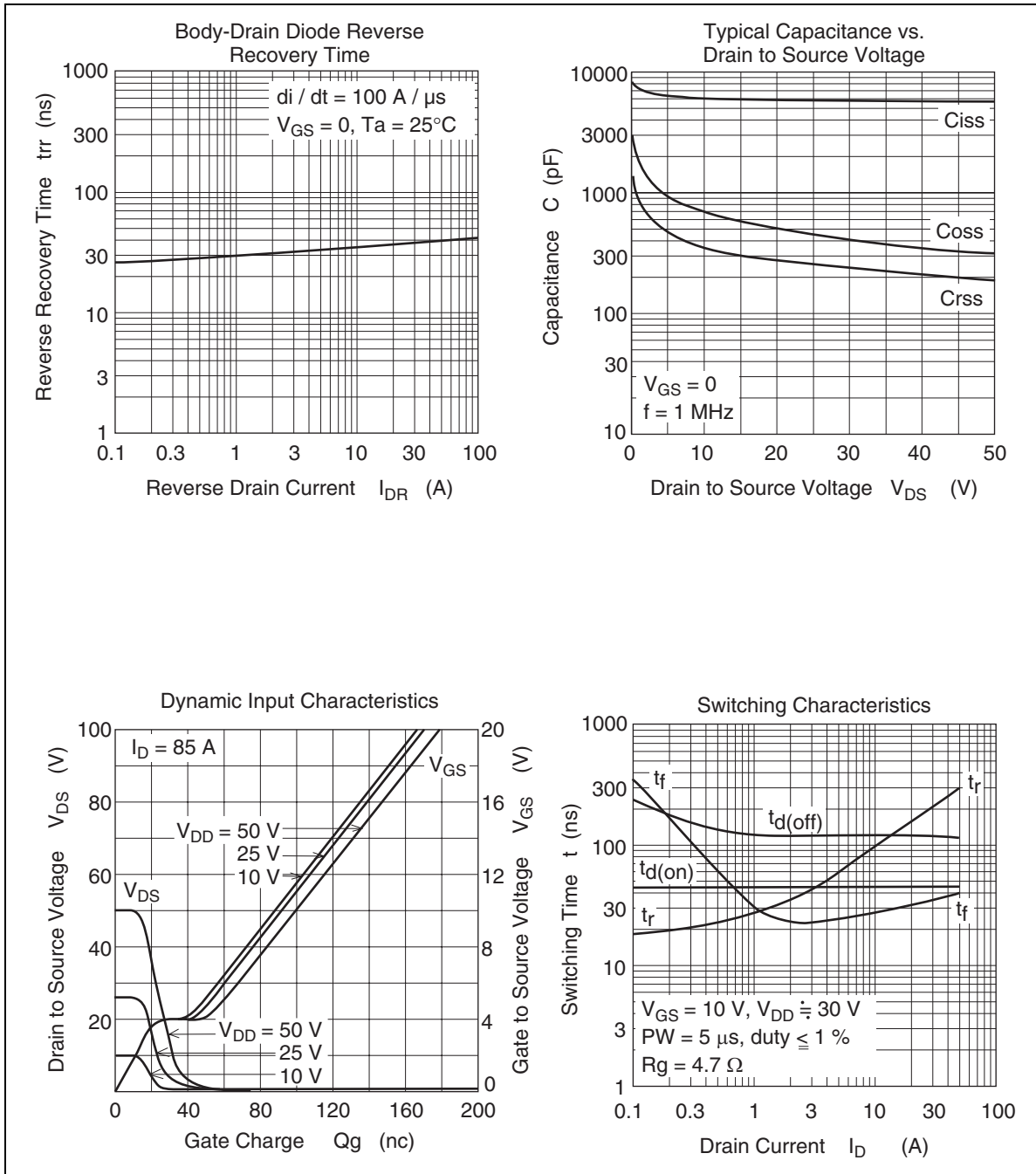
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown Voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}^{\text{Note1}}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	8.0	$\text{m}\Omega$	$I_D = 35 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note1}}$
		—	8.0	12	$\text{m}\Omega$	$I_D = 35 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note1}}$
Forward transfer admittance	$ y_{fs} $	45	75	—	S	$I_D = 35 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note1}}$
Input capacitance	C_{iss}	—	6200	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	680	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	350	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	100	—	nC	$V_{DD} = 25 \text{ V}$
Gate to source charge	Q_{gs}	—	20	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	20	—	nC	$I_D = 70 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	45	—	ns	$V_{GS} = 10 \text{ V}, I_D = 35 \text{ A}$
Rise time	t_r	—	220	—	ns	$R_L = 0.86 \text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	—	125	—	ns	$R_g = 4.7 \text{ }\Omega$
Fall time	t_f	—	35	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.94	—	V	$I_F = 70 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 70 \text{ A}, V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

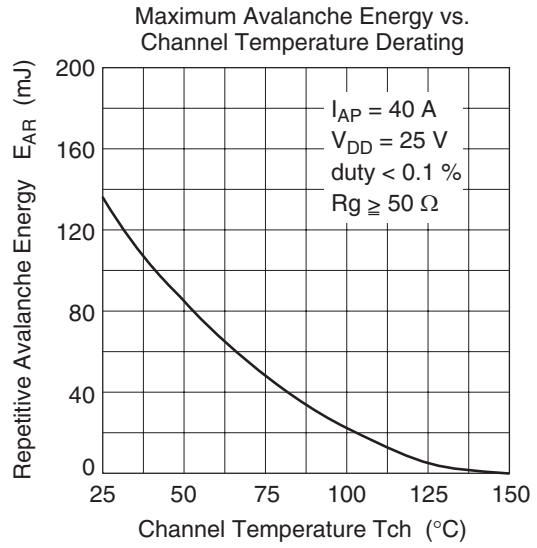
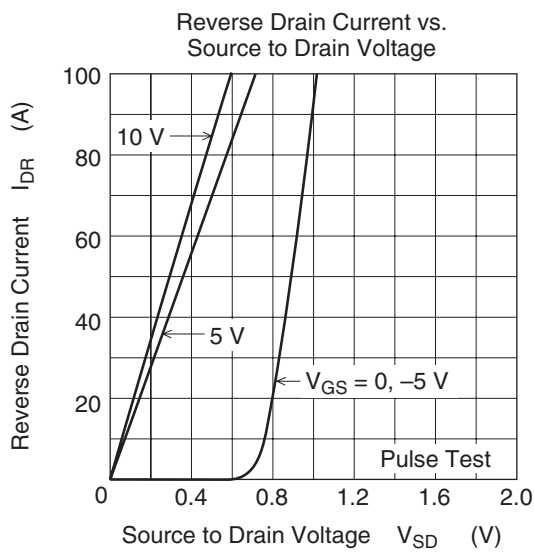
Notes: 1. Pulse test

Main Characteristics

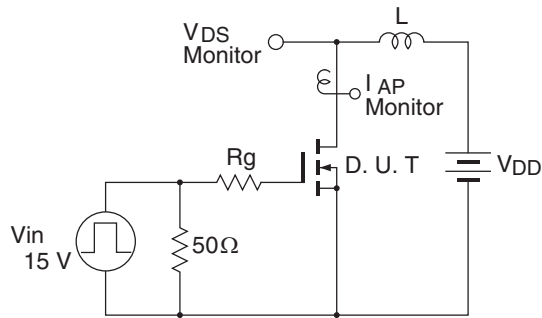






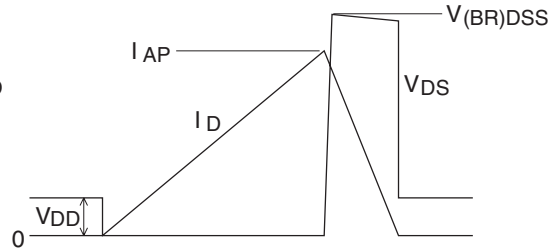


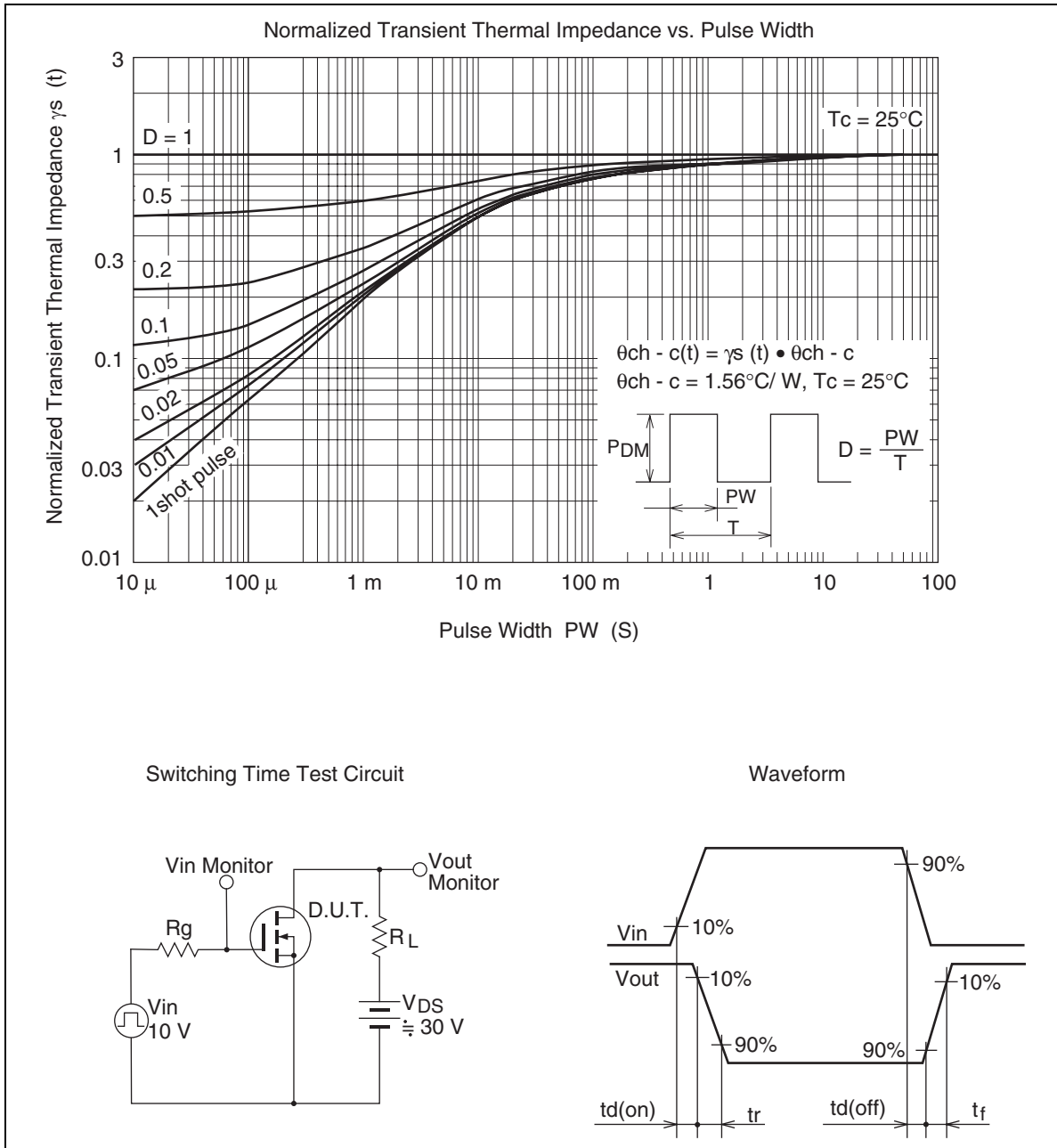
Avalanche Test Circuit



Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

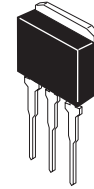
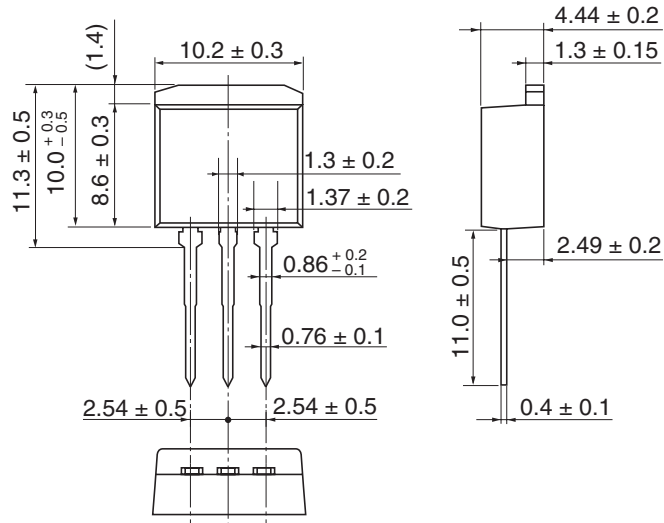




Package Dimensions

• H7N0608LD

As of January, 2003
Unit: mm

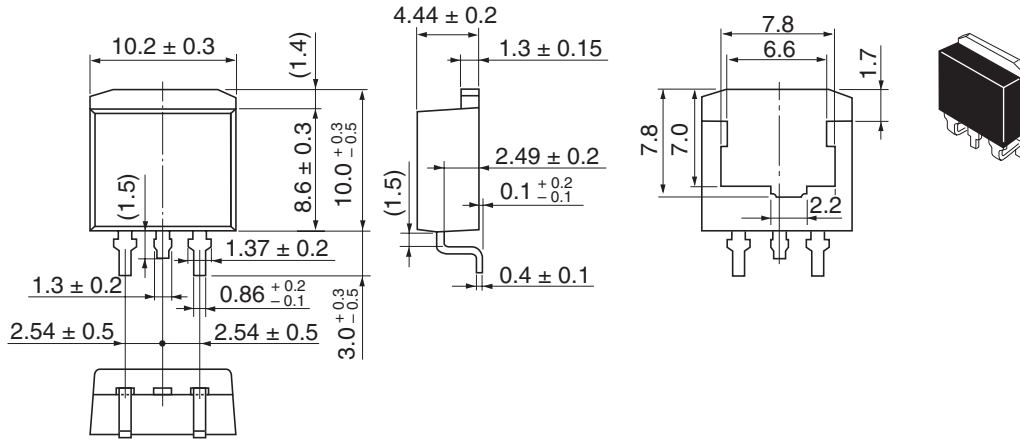


Package Code	LDBAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.40 g

H7N0608LD, H7N0608LS, H7N0608LM

• H7N0608LS

As of January, 2003
Unit: mm

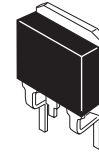
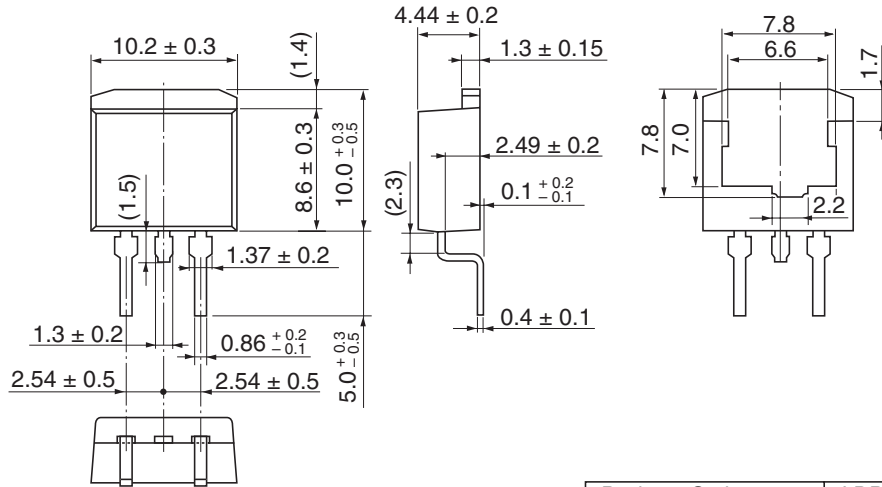


Package Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.30 g

H7N0608LD, H7N0608LS, H7N0608LM

• H7N0608LM

As of January, 2003
Unit: mm



Package Code	LDPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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