To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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H7N1002AB

Silicon N Channel MOS FET
High Speed Power Switching

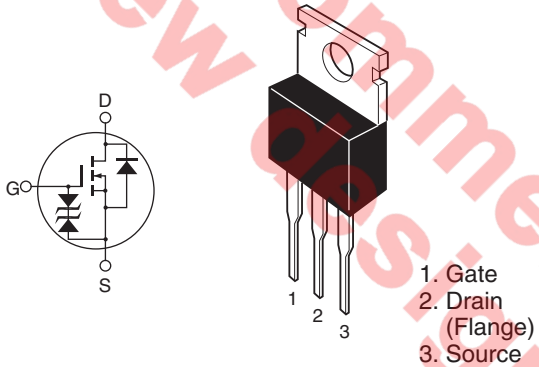
REJ03G0130-0200Z
Rev.2.00
Oct.30.2003

Features

- Low on-resistance
  $R_{DS(on)}$ = 8 mΩ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline

TO-220AB



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ Note1	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} Note3	50	A
Avalanche energy	E_{AR} Note3	166	mJ
Channel dissipation	Pch Note2	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

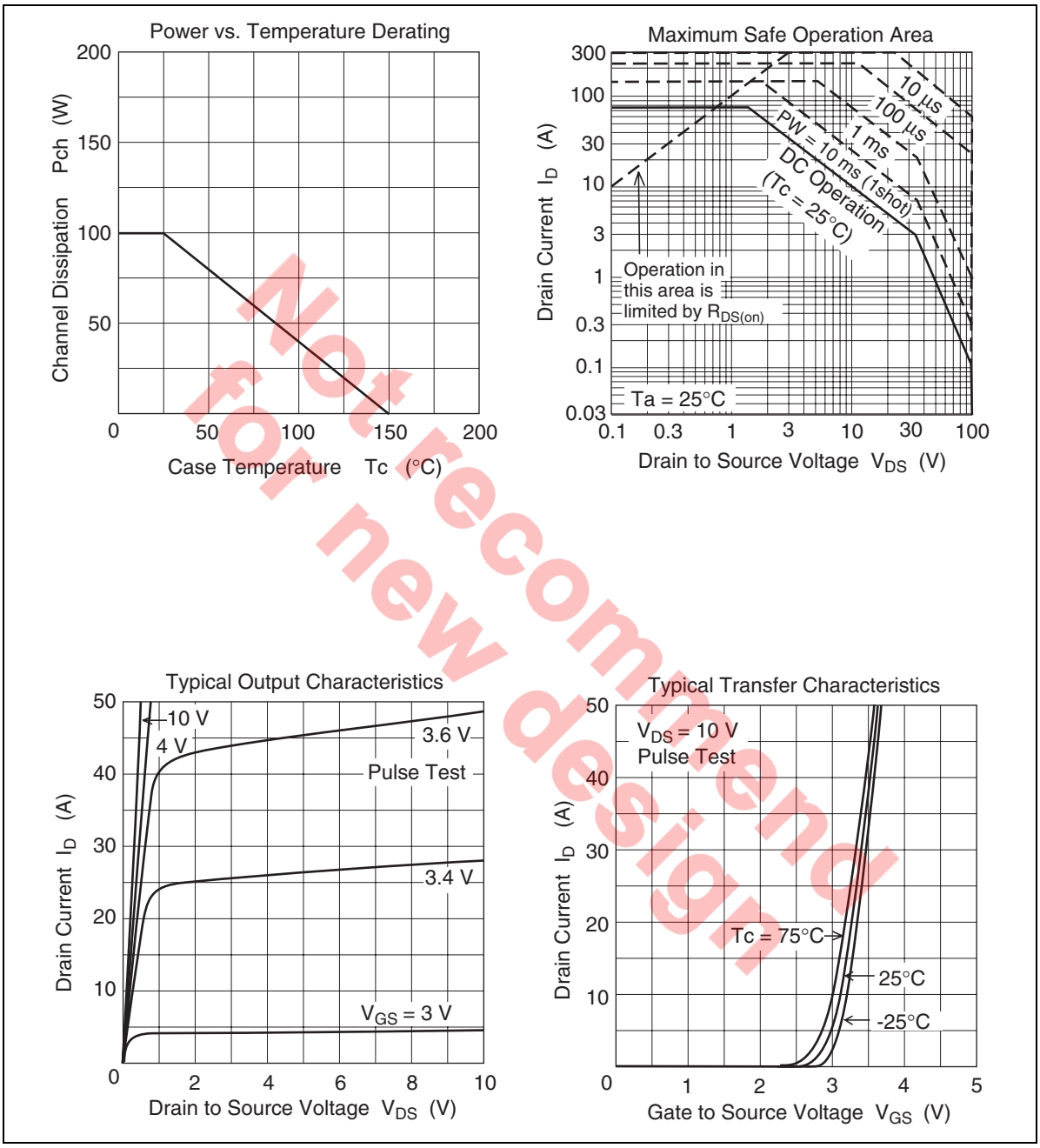
Electrical Characteristics

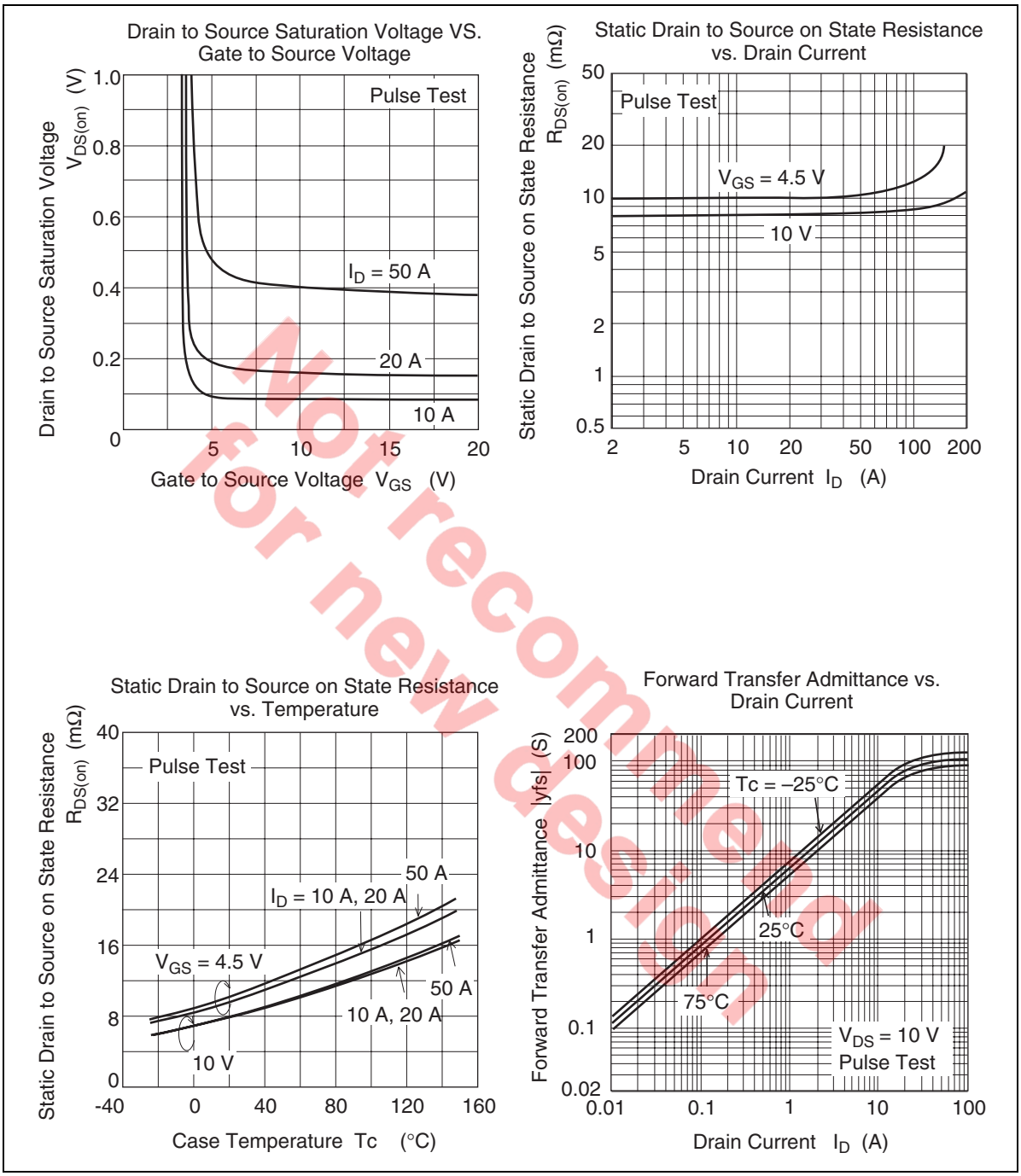
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown Voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	10	µA	V_{DS} = 100 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	I_D = 1 mA, V_{DS} = 10 V Note1
Static drain to source on state resistance	$R_{DS(on)}$	—	8	10	mΩ	I_D = 37.5 A, V_{GS} = 10 V Note1
		—	10	15	mΩ	I_D = 37.5 A, V_{GS} = 4.5 V Note1
Forward transfer admittance	$\|y_{fs}\|$	57	95	—	S	I_D = 37.5 A, V_{DS} = 10 V Note1
Input capacitance	Ciss	—	9700	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	740	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	330	—	pF	f = 1 MHz
Total gate charge	Qg	—	155	—	nc	V_{DD} = 50 V
Gate to source charge	Qgs	—	35	—	nc	V_{GS} = 10 V
Gate to drain charge	Qgd	—	33	—	nc	I_D = 75 A
Turn-on delay time	$t_{d(on)}$	—	43	—	ns	V_{GS} = 10 V, I_D = 37.5 A
Rise time	t_r	—	245	—	ns	R_L = 0.8 Ω
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	R_g = 4.7 Ω
Fall time	t_f	—	25	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.93	—	V	I_F = 75 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	70	—	ns	I_F = 75 A, V_{GS} = 0 diF/ dt = 100 A/µs

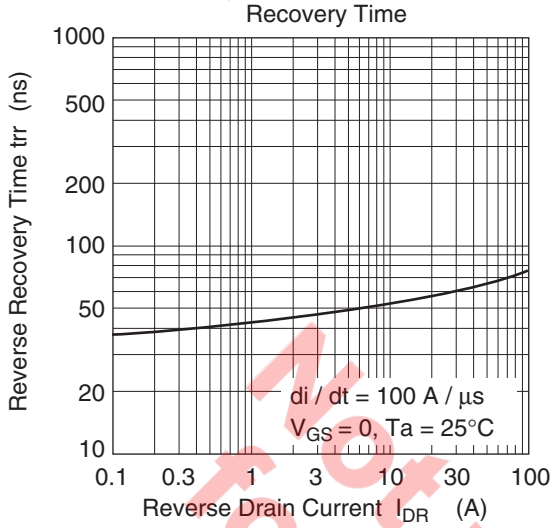
Notes: 1. Pulse test

Main Characteristics

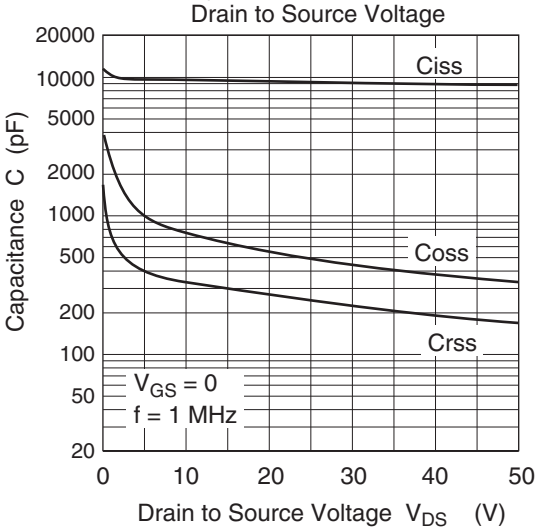




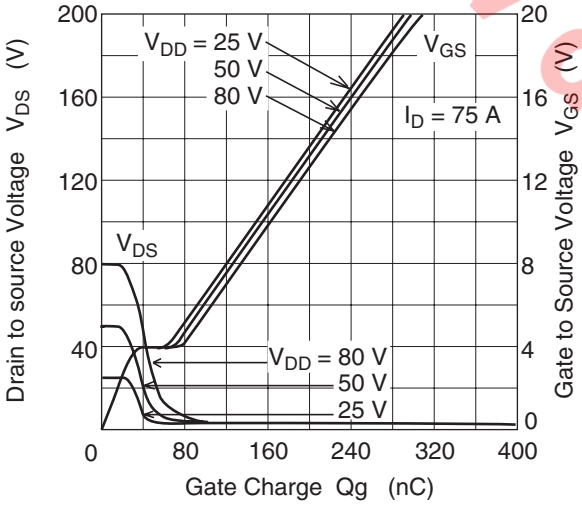
Body-Drain Diode Reverse Recovery Time



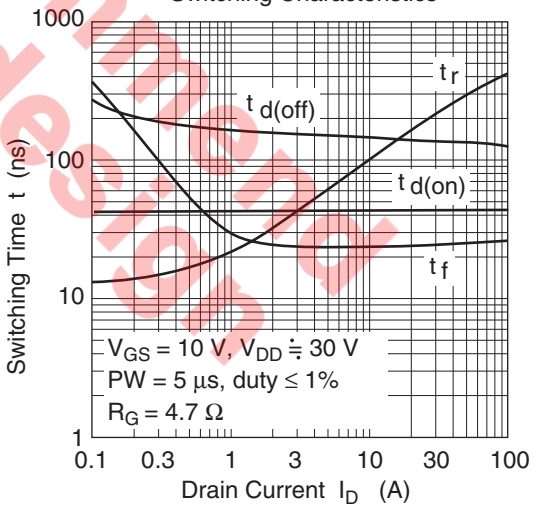
Typical Capacitance vs. Drain to Source Voltage



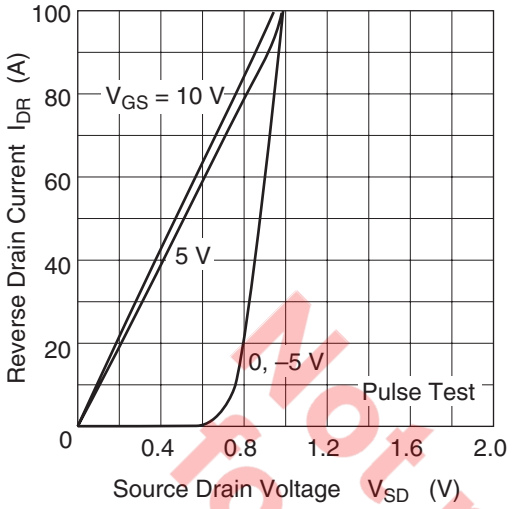
Dynamic Input Characteristics



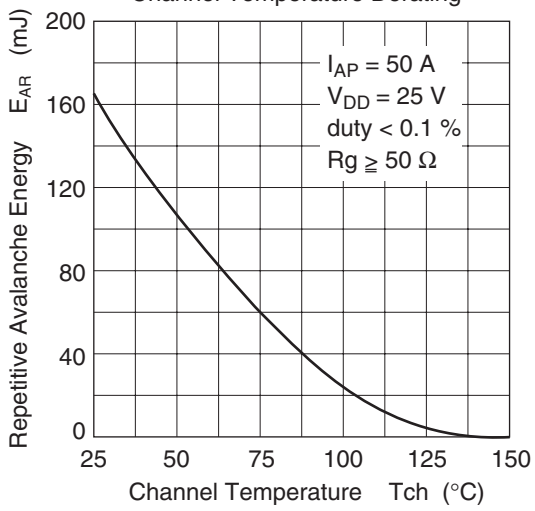
Switching Characteristics



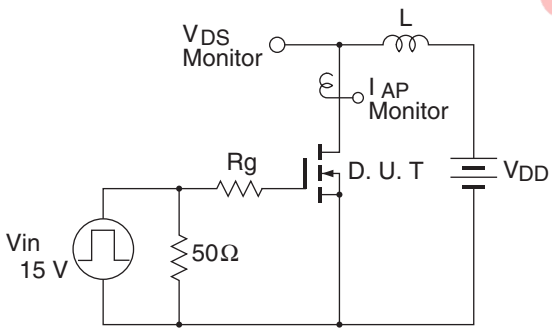
Reverses Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

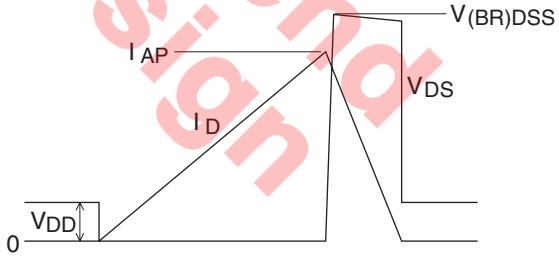


Avalanche Test Circuit

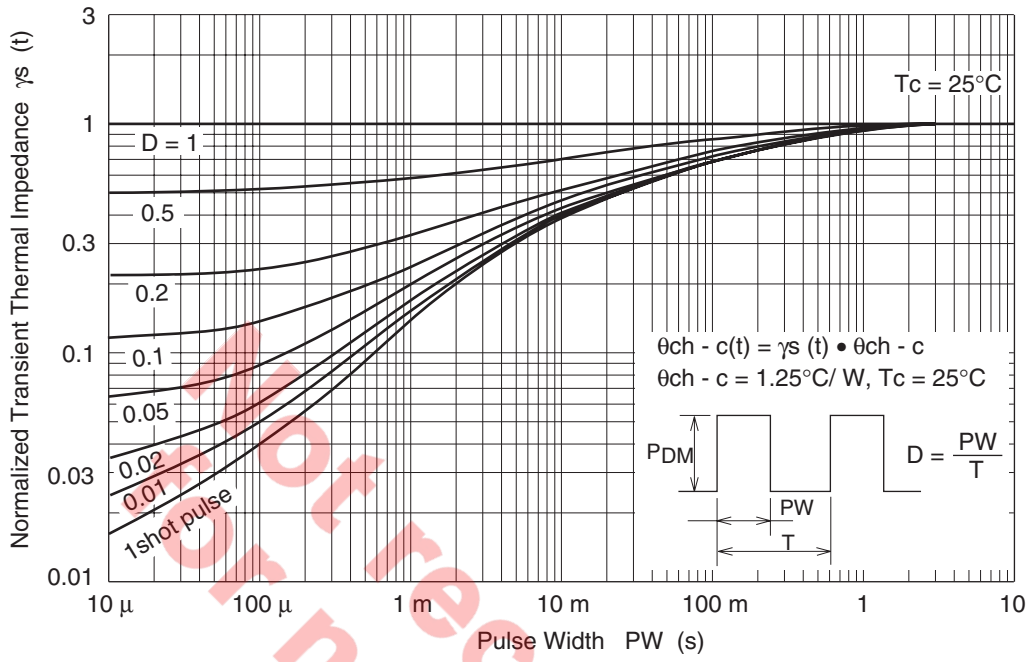


Avalanche Waveform

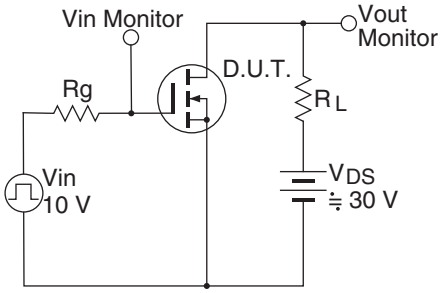
$$E_{AR} = \frac{1}{2} \bullet L \bullet I_{AP}^2 \bullet \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



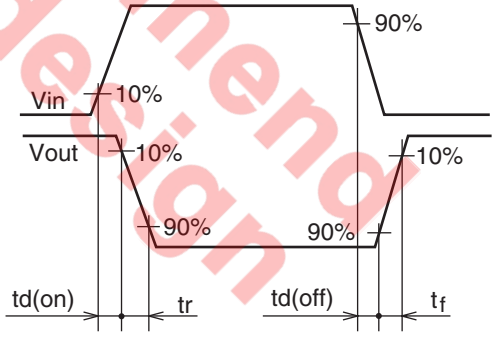
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

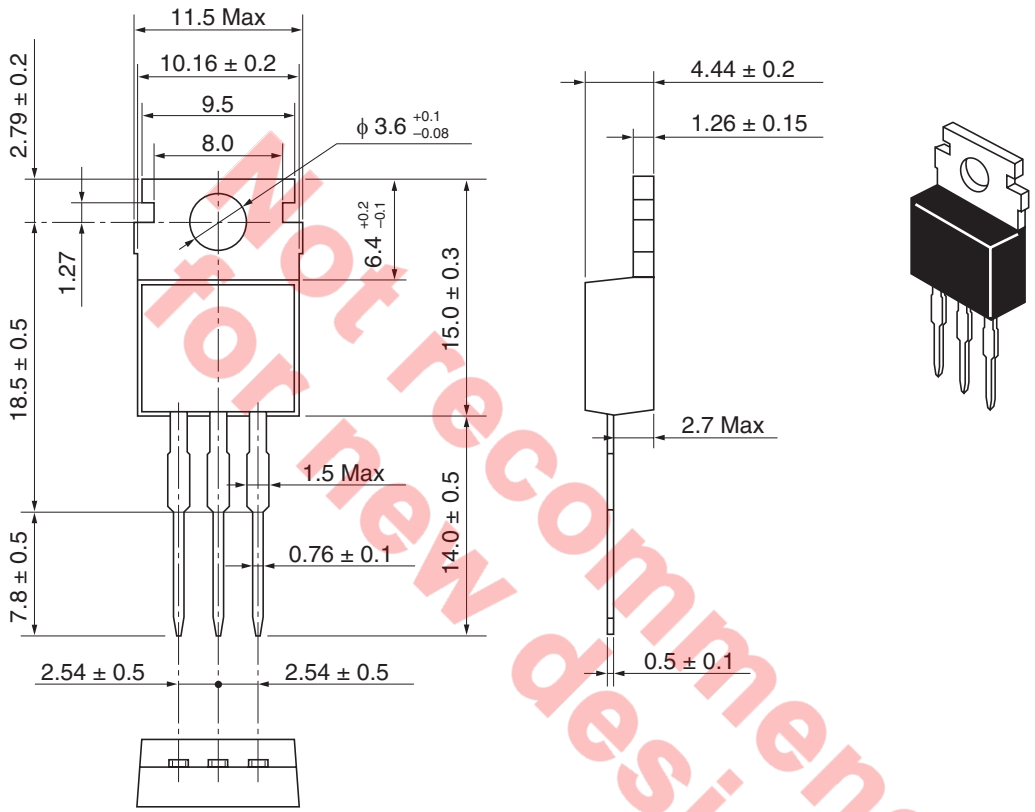


Switching Time Waveform



Package Dimensions

As of January, 2003
Unit: mm



Package Code	TO-220AB
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.8 g

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Colophon 1.0