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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H7N1005LD, H7N1005LS, H7N1005LM

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G0391-0200

Rev.2.00

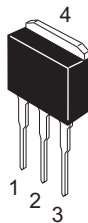
Oct 16, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 85 \text{ m}\Omega$ typ.
- Low drive current
- Capable of 4.5 V gate drive

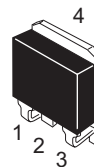
Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDKPAK (L))



H7N1005LD

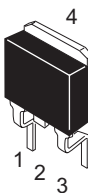
RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK (S)-(1))



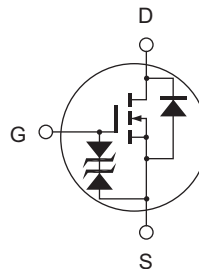
H7N1005LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDKPAK (S)-(2))



H7N1005LM



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	100	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	15	A
Drain peak current	I _{D (pulse)} ^{Note 1}	30	A
Body to drain diode reverse drain current	I _{DR}	30	A
Avalanche current	I _{AP} ^{Note 3}	8	A
Avalanche energy	E _{AR} ^{Note 3}	6.4	mJ
Channel dissipation	P _{ch} ^{Note 2}	30	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at Tc = 25°C
 3. Value at Tch = 25°C, Rg ≥ 50 Ω

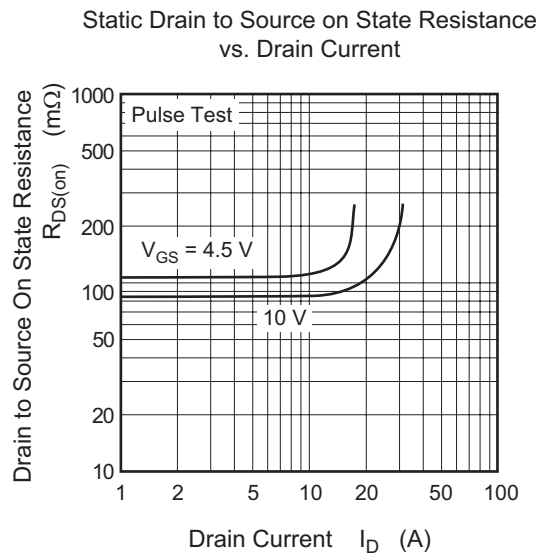
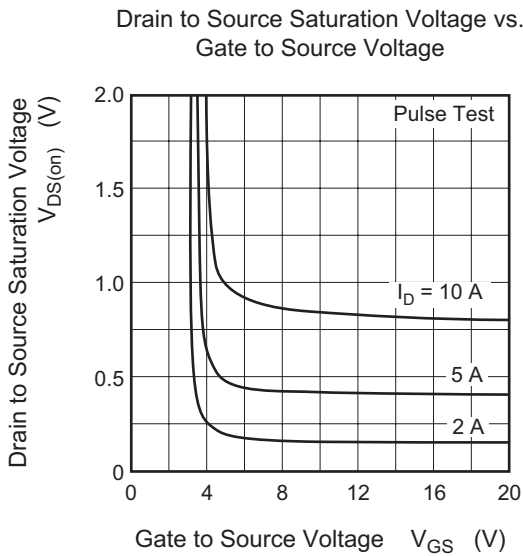
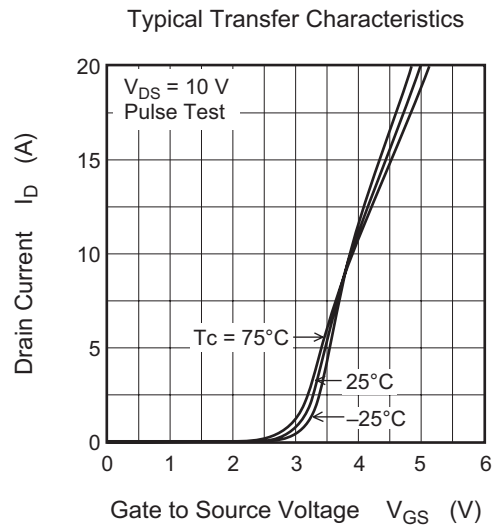
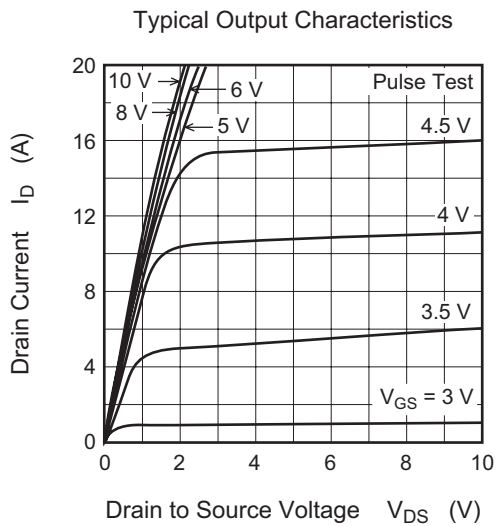
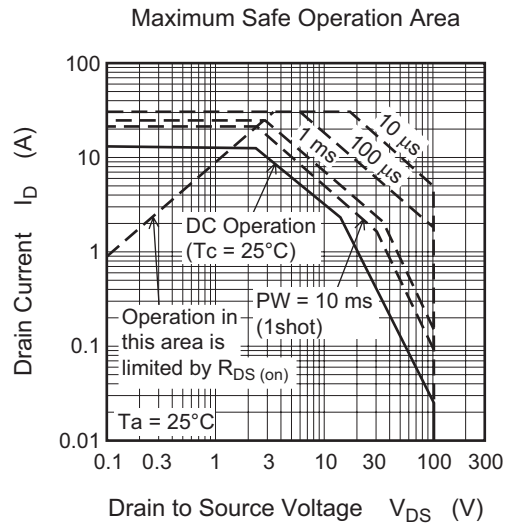
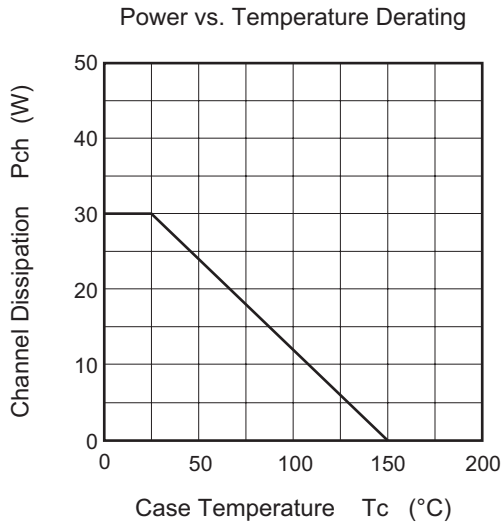
Electrical Characteristics

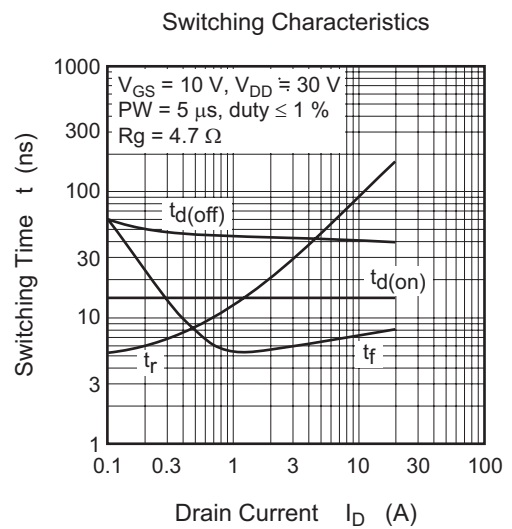
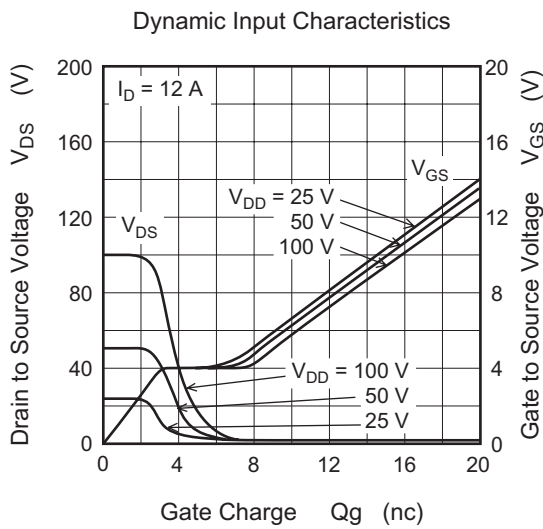
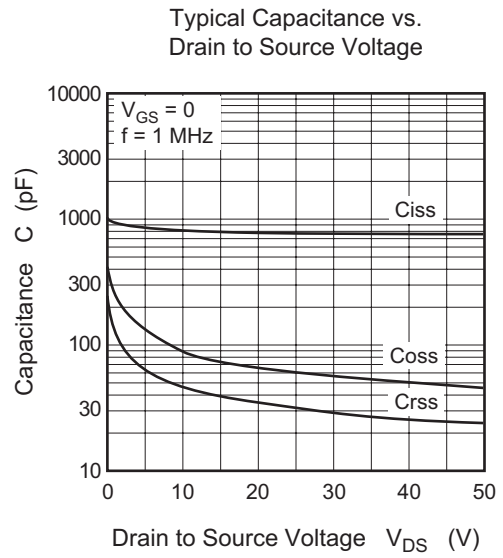
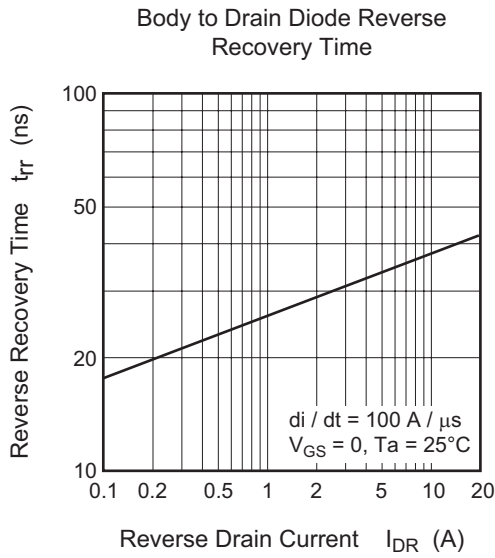
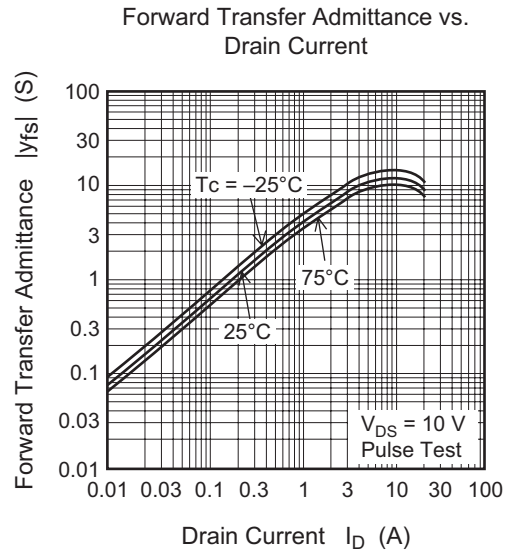
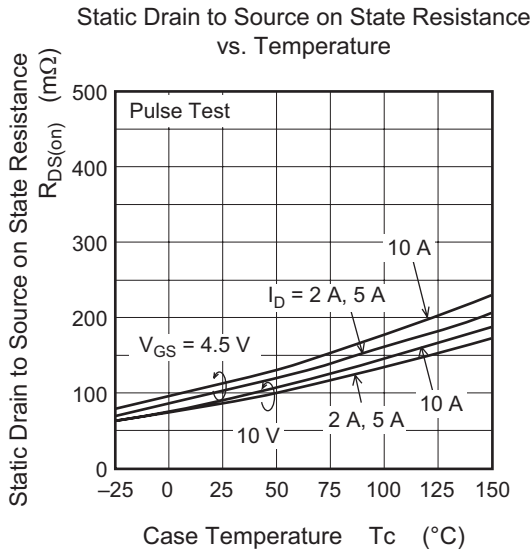
(Ta = 25°C)

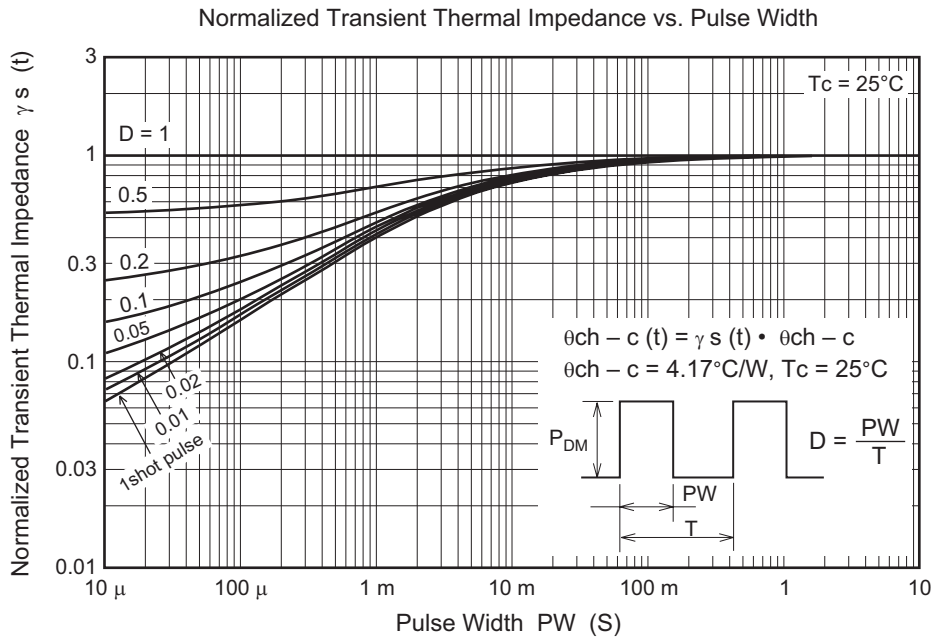
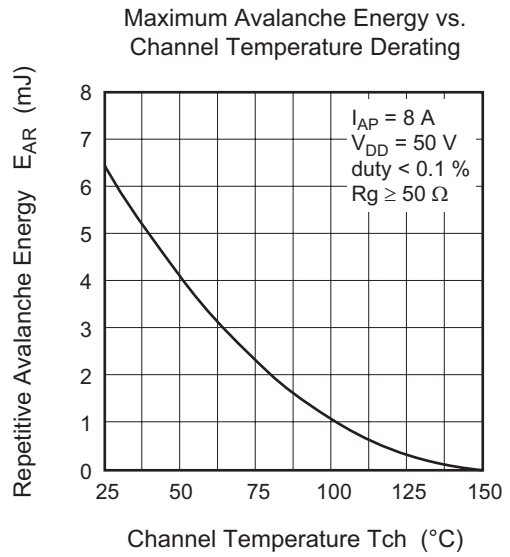
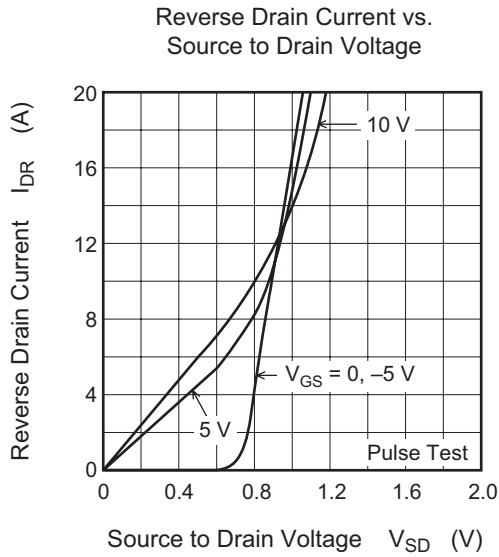
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	100	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR) GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 100 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	1.5	—	2.5	V	I _D = 1 mA, V _{DS} = 10 V ^{Note 4}
Static drain to source on state resistance	R _{DS (on)}	—	85	110	mΩ	I _D = 7.5 A, V _{GS} = 10 V ^{Note 4}
		—	105	155	mΩ	I _D = 7.5 A, V _{GS} = 4.5 V ^{Note 4}
Forward transfer admittance	y _{fs}	6.5	11	—	S	I _D = 7.5 A, V _{GS} = 10 V ^{Note 4}
Input capacitance	C _{iss}	—	830	—	pF	V _{DS} = 10 V
Output capacitance	C _{oss}	—	90	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	55	—	pF	f = 1 MHz
Total gate charge	Q _g	—	15	—	nC	V _{DD} = 50 V
Gate to source charge	Q _{gs}	—	3	—	nC	V _{GS} = 10 V
Gate to drain charge	Q _{gd}	—	4	—	nC	I _D = 15 A
Turn-on delay time	t _{d (on)}	—	15	—	ns	V _{GS} = 10 V, I _D = 7.5 A
Rise time	t _r	—	85	—	ns	R _L = 4 Ω
Turn-off delay time	t _{d (off)}	—	42	—	ns	R _g = 4.7 Ω
Fall time	t _f	—	6.8	—	ns	
Body to drain diode forward voltage	V _{DF}	—	0.93	—	V	I _F = 15 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	41	—	ns	I _F = 15 A, V _{GS} = 0 di _F /dt = 100 A/μs

Note: 4. Pulse test

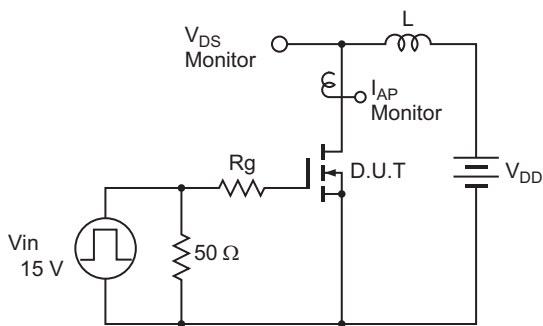
Main Characteristics





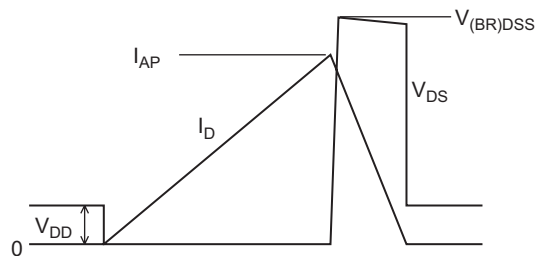


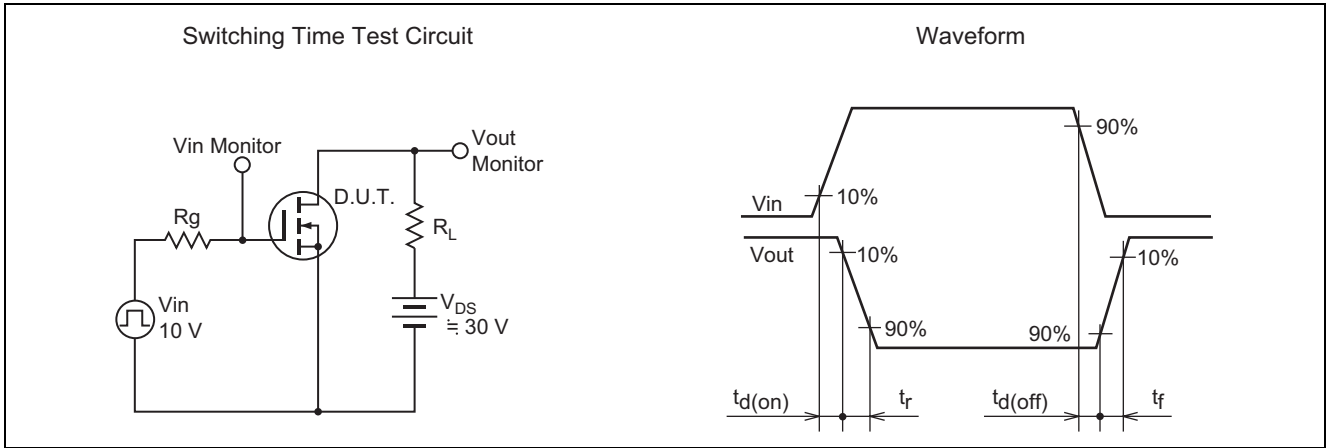
Avalanche Test Circuit



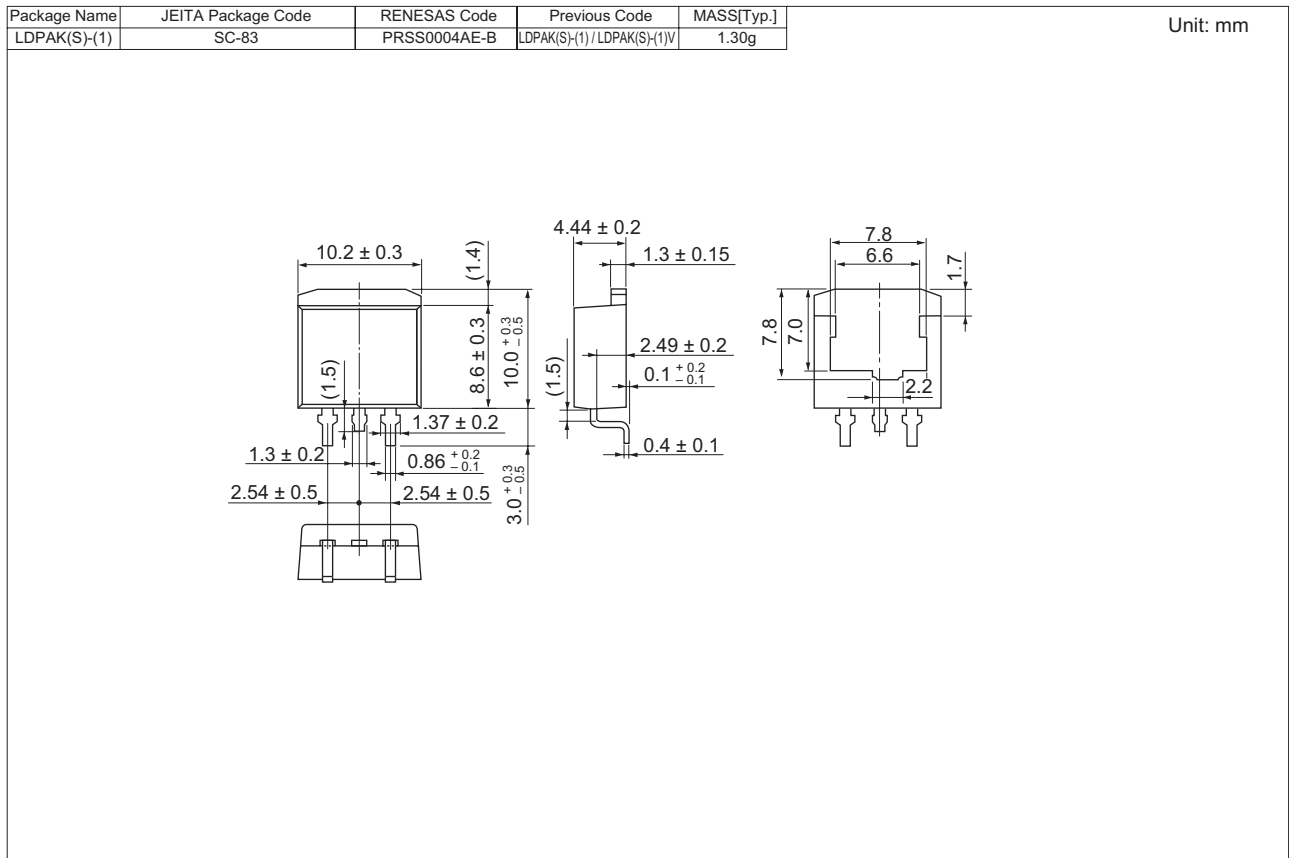
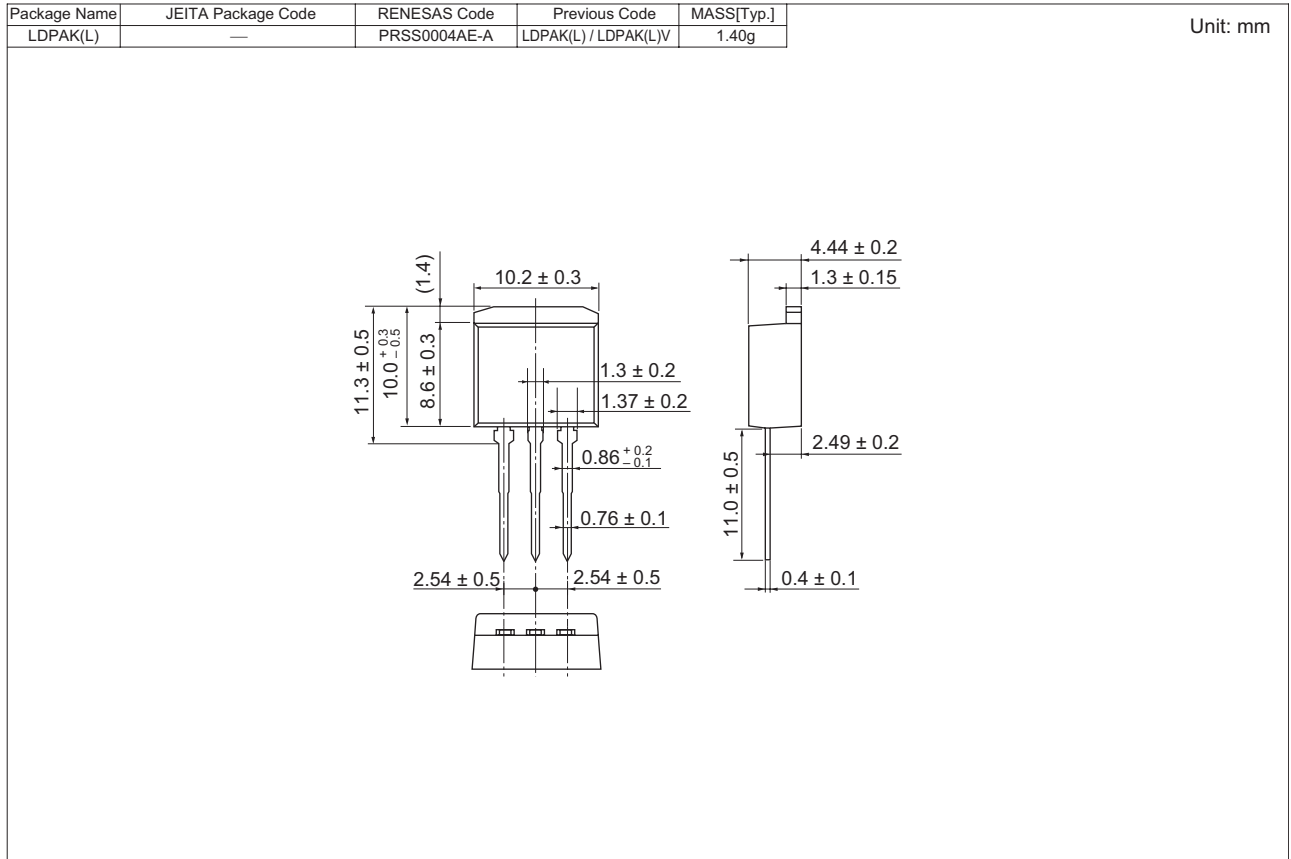
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$





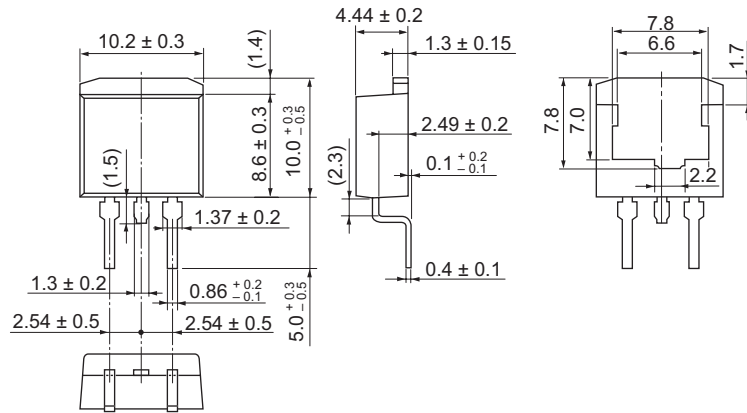
Package Dimensions



H7N1005LD, H7N1005LS, H7N1005LM

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(2)	—	PRSS0004AE-C	LDBPAK(S)-(2) / LDBPAK(S)-(2)V	1.35g

Unit: mm



Ordering Information

Part Name	Quantity	Shipping Container
H7N1005LD-E	500 pcs	Box (Conductive Sack)
H7N1005LSTL-E	1000 pcs	Taping
H7N1005LMTL-E	1000 pcs	Taping

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