16-bit CPU IP

H8S CPU subsystem (H8S C200)

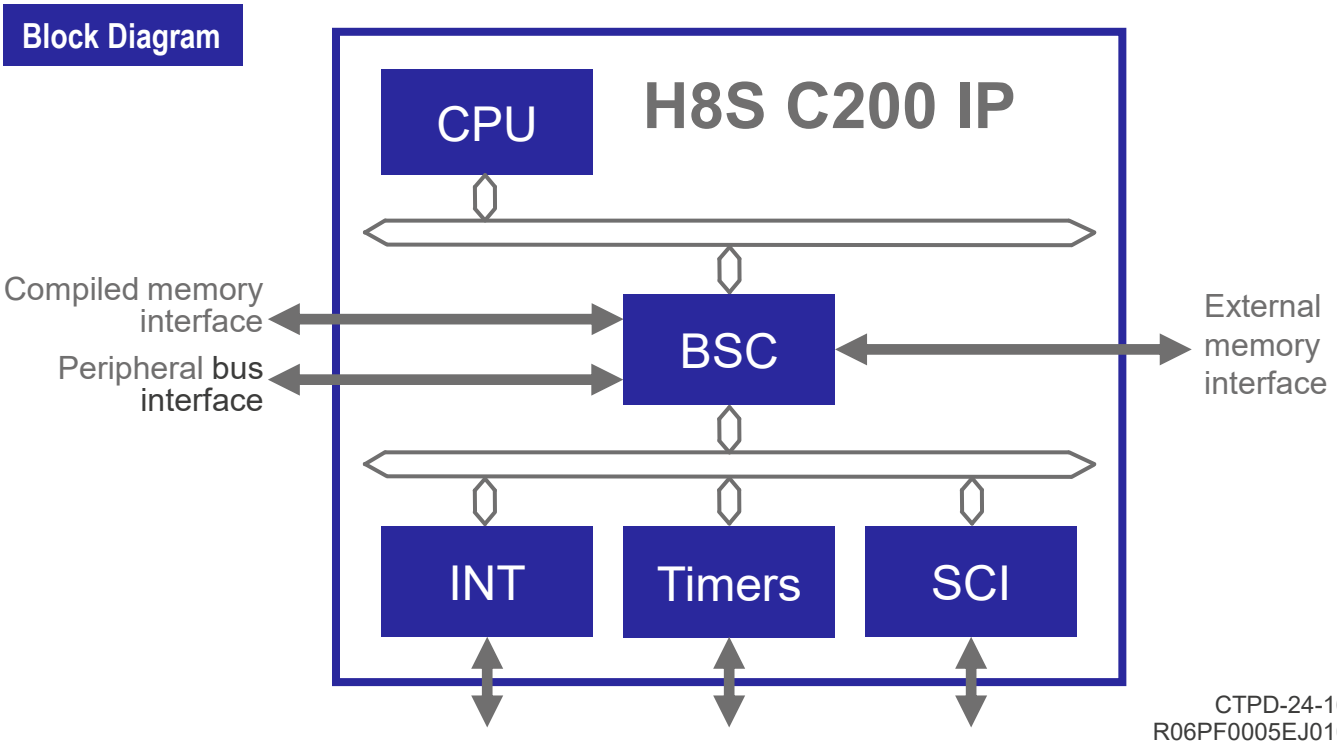
Overview

H8S is a high speed 16-bit CPU with an internal 32-bit architecture.
It is upward-compatible with H8/300 and H8/300H CPUs on an object level.
This subsystem IP, which is for IP license, supports basic and simple microcontroller functions, including bus controller (BSC), interrupt controller (INT), timers, serial communication interface (SCI) and on-chip debug functions.
Optional information packages for H8/327, H8/337, H8/3048, H8S/2655 and H8S/2355 approximation are also available.

Key Features

- An original subsystem for SoCs other than microcomputers
- 3 type interfaces available to connect user functions or IPs
  - compiled memory interface
  - external memory interface
  - peripheral bus interface
- 4 type timers
  - 16-bit free-running timer (FRT)
  - 8-bit timer
  - 14-bit PWM timer
  - Watchdog timer (WDT)
- Serial communication interface(SCI)
- Supporting on-chip debug functions (option)
- Applicable to various processes and FPGAs
- Handy size

Block Diagram



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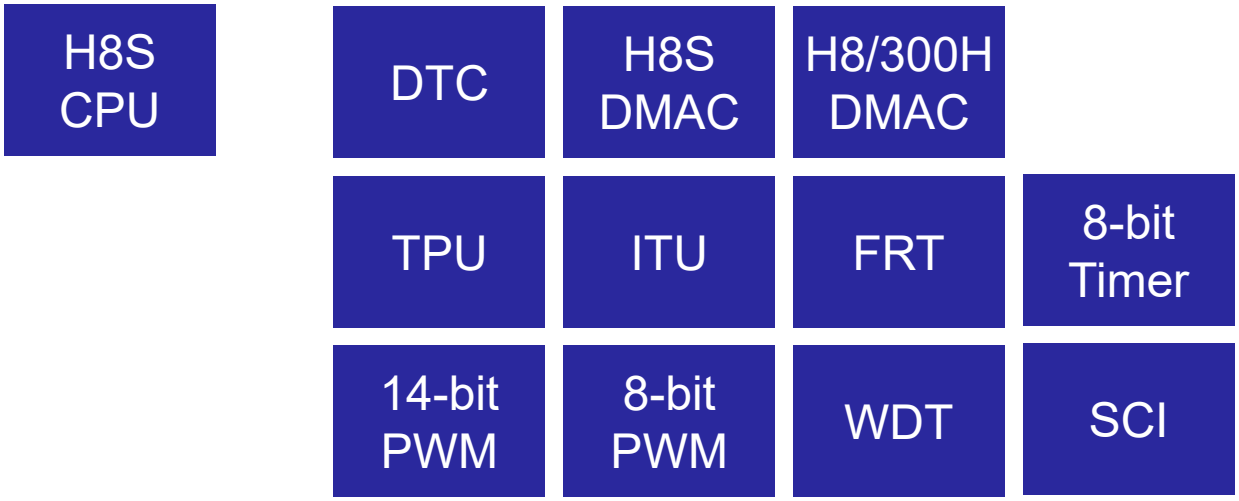
Sample Results and Evaluation Environments

As a sample result showing compatibility with H8S microcomputers, an application note program of H8S microcomputer is performed in an FPGA in which H8S CPU subsystem is implemented, by using the common development tools with H8S Microcontroller Products. As FPGA, Artix™A7 and MAX®10 are proven.
FPGA boards that MACNICA, Inc. Altima Company or Shinko Shoji LSI Design Center Co.,Ltd. delivers are proven and available for H8S CPU subsystem.

Other Microcomputer Functions (Option)

H8S IP is compatible with H8/300 and H8SX IPs on system, bus and interrupt interface. Many other microcomputer functions are available (option), which needs some modification in bus controller and interrupt controller, except optional information packages.



Deliverables

- Synthesizable Verilog RTL design
- Testbench
- Synthesis scripts

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