HA-2420

3.2µs Sample and Hold Amplifiers

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FN2856
Rev.7.00
October 24, 2013

The HA-2420 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and JFET input unity gain amplifier.

With an external hold capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note **AN517**.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA1-2420-2	-55 to +125	14 Ld CERDIP	F14.3

Features

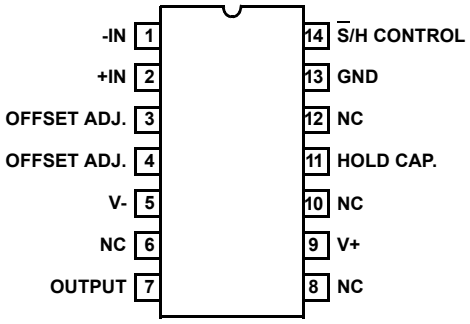
- Maximum Acquisition Time
  - 10V Step to 0.1% . . . . . 4µs (Max)
  - 10V Step to 0.01% . . . . . 6µs (Max)
- Low Droop Rate (C_H = 1000pF). . . . . 5µV/ms (Typ)
- Gain Bandwidth Product . . . . . 2.5MHz (Typ)
- Low Effective Aperture Delay Time . . . . . 30ns (Typ)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Pinout

HA-2420 (CERDIP)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 24V
Digital Input Voltage (Sample and Hold Pin) . . . . . +8V, -15V
Output Current . . . . . .Short Circuit Protected

Operating Conditions

Temperature Range
HA-2420-2 . . . . . -55°C to +125°C
Supply Voltage Range (Typical) . . . . . ±12V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package.	75	20

Maximum Junction Temperature (Ceramic Packages) . . . . . .+175°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .+300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input)

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	±10	-	-	V
Offset Voltage		25	-	2	4	mV
		Full	-	3	6	mV
Bias Current		25	-	40	200	nA
		Full	-	-	400	nA
Offset Current		25	-	10	50	nA
		Full	-	-	100	nA
Input Resistance		25	5	10	-	MΩ
Common Mode Range		Full	±10	-	-	V
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain	R_L = 2kΩ, V_O = $20V_{P-P}$	Full	25	50	-	kV/V
Common Mode Rejection	V_{CM} = ±10V	Full	80	90	-	dB
Hold Mode Feedthrough Attenuation (Note 2)	$f_{IN} \leq$ 100kHz	Full	-	-76	-	dB
Gain Bandwidth Product (Note 2)		25	-	2.5	-	MHz
OUTPUT CHARACTERISTICS						
Output Voltage Swing	R_L = 2kΩ	Full	±10	-	-	V
Output Current		25	-	-	-	mA
Full Power Bandwidth (Note 2)	V_O = $20V_{P-P}$	25	-	100	-	kHz
Output Resistance	DC	25	-	0.15	-	Ω
TRANSIENT RESPONSE						
Rise Time (Note 2)	V_O = $200mV_{P-P}$	25	-	75	100	ns
Overshoot (Note 2)	V_O = $200mV_{P-P}$	25	-	25	40	%
Slew Rate (Note 2)	V_O = $10V_{P-P}$	25	3.5	5	-	V/µs
DIGITAL INPUT CHARACTERISTICS						
Digital Input Current	V_{IN} = 0V	Full	-	-	-0.8	mA
	V_{IN} = 5V	Full	-	-	20	µA

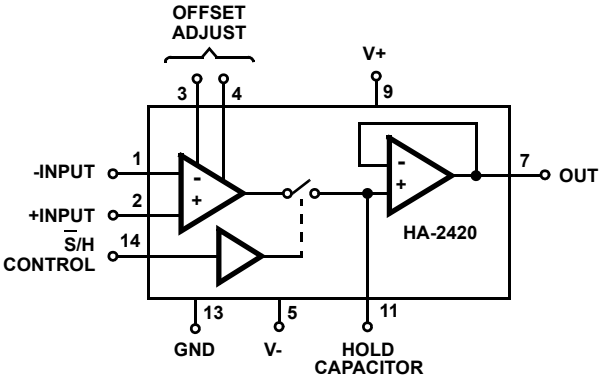
Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = 1000pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold), Unity Gain Configuration (Output tied to Negative Input) **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
Digital Input Voltage	Low	Full	-	-	0.8	V
	High	Full	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time (Note 2)	To 0.1% 10V Step	25	-	2.3	4	µs
Acquisition Time (Note 2)	To 0.01% 10V Step	25	-	3.2	6	µs
Hold Step Error	V_{IN} = 0V	25	-	10	20	mV
Hold Mode Settling Time	To ±1mV	25	-	860	-	ns
Aperture Time (Note 3)		25	-	30	-	ns
Effective Aperture Delay Time		25	-	30	-	ns
Aperture Uncertainty		25	-	5	-	ns
Drift Current (Note 2)	V_{IN} = 0V	25	-	5	-	pA
HA1-2420		Full	-	1.8	10	nA
POWER SUPPLY CHARACTERISTICS						
Supply Current (+)		25	-	3.5	5.5	mA
Supply Current (-)		25	-	2.5	3.5	mA
Power Supply Rejection		Full	80	90	-	dB

NOTES:

2. A_V = ±1, R_L = 2kΩ, C_L = 50pF.
3. Derived from computer simulation only; not tested.

Functional Diagram



Test Circuits and Waveforms

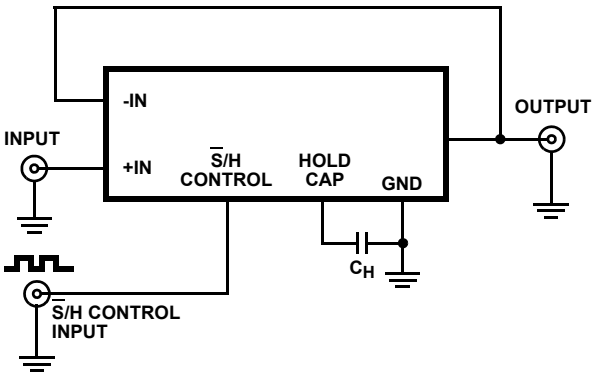
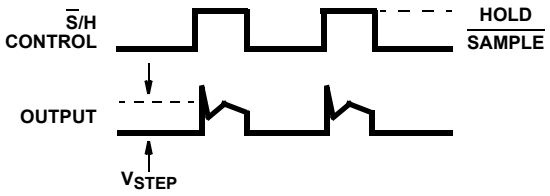
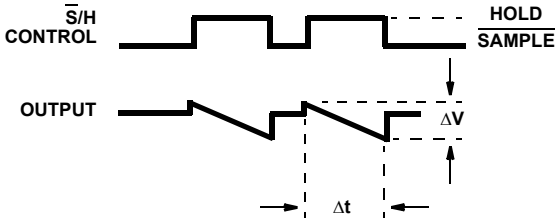


FIGURE 1. HOLD STEP ERROR AND DRIFT CURRENT



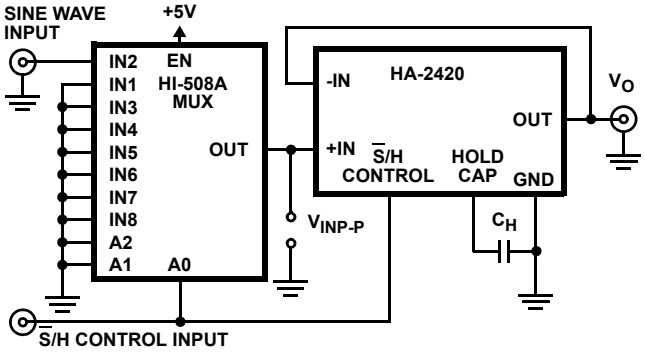
NOTE: Set rise/fall times of S/H Control to approximately 20ns.

FIGURE 2. HOLD STEP ERROR TEST



NOTE: Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$.

FIGURE 3. DRIFT CURRENT TEST



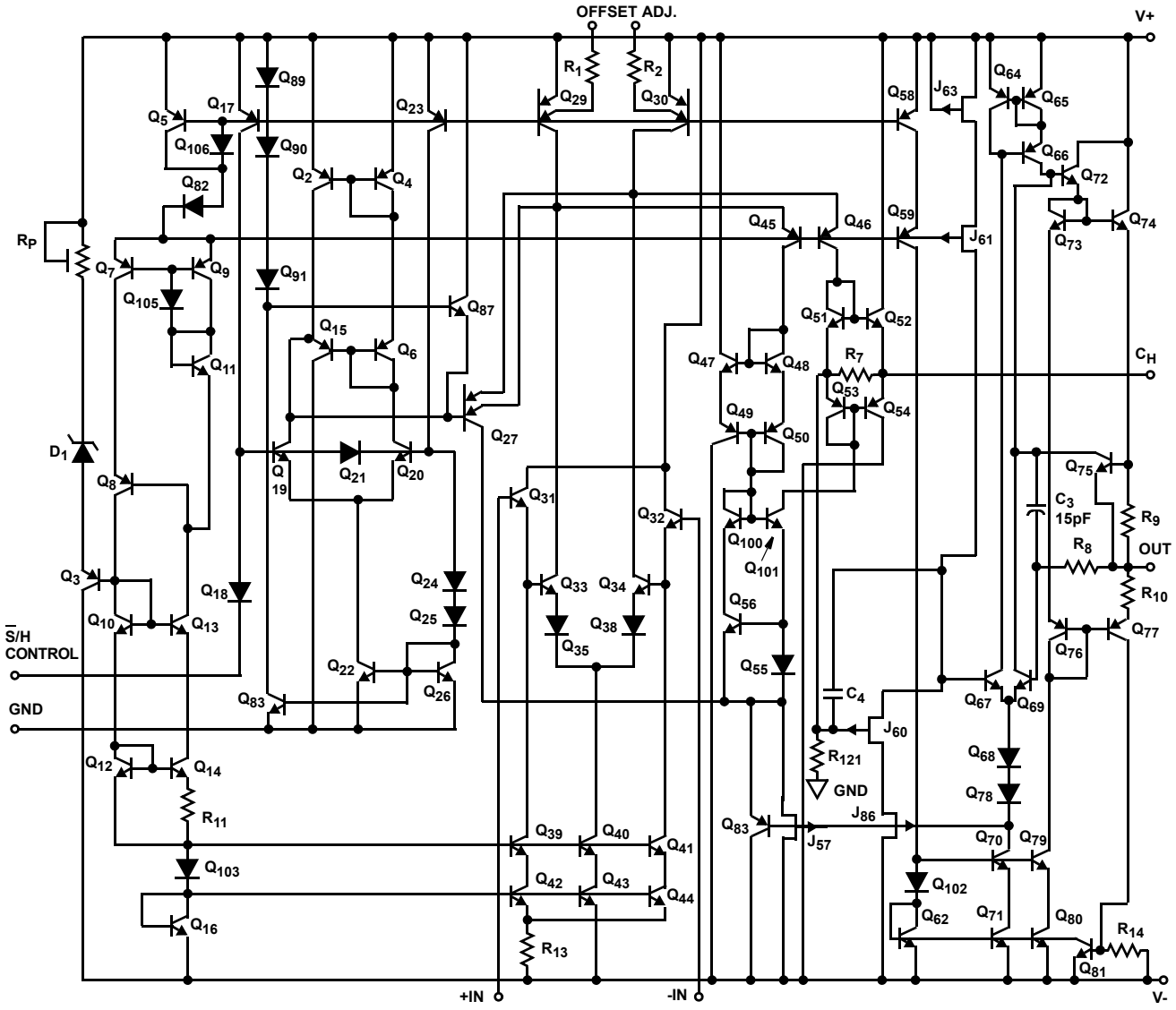
NOTE: Compute hold mode feedthrough attenuation from the formula:

$$\text{Feedthrough Attenuation} = 20\log\frac{V_{OUT}HOLD}{V_{IN}HOLD}$$

Where $V_{OUT}HOLD$ = Peak-to-Peak value of output sinewave during the hold mode.

FIGURE 4. HOLD MODE FEEDTHROUGH ATTENUATION

Schematic Diagram



Application Information

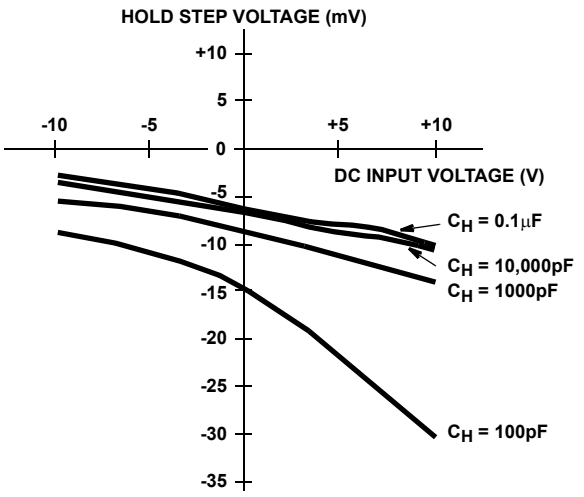


FIGURE 5. HOLD STEP vs INPUT VOLTAGE

Offset Adjustment

The offset voltage of the HA-2420, may be adjusted using a 100kΩ trim pot, as shown in Figure 8. The recommended adjustment procedure is:

Apply 0V to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.

Adjust the trim pot for 0V output in the hold mode.

Gain Adjustment

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10NOMINAL}) + (-10V)}{2}$$

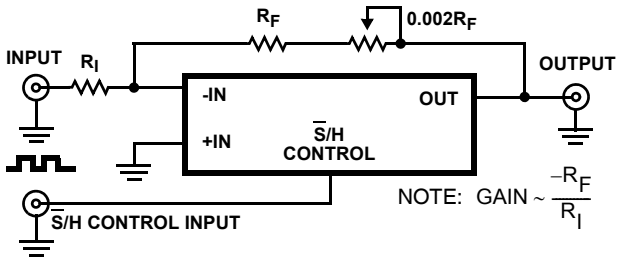


FIGURE 6. INVERTING CONFIGURATION

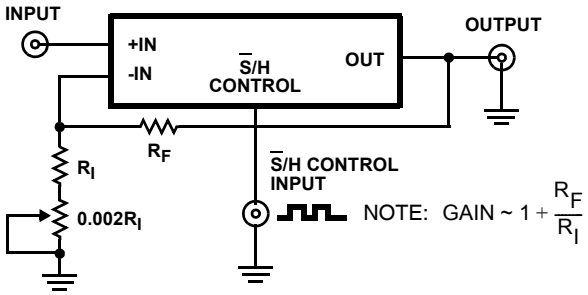


FIGURE 7. NON-INVERTING CONFIGURATION

Figure 8 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

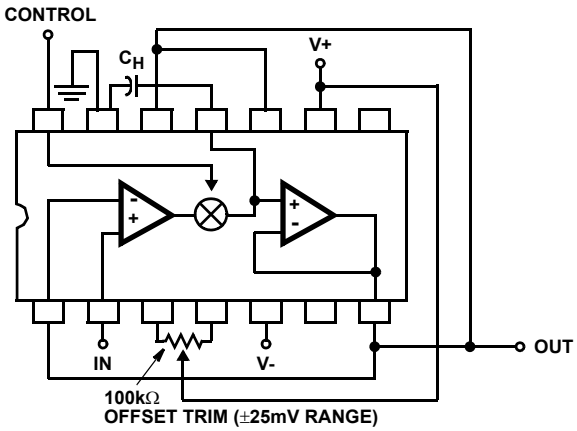


FIGURE 8. BASIC SAMPLE-AND-HOLD (TOP VIEW)

The method used to reduce leakage paths on the PC board and the device package is shown in Figure 9. This guard ring is recommended to minimize the drift during hold mode.

The hold capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below 85°C), Teflon, or Parlene types are recommended.

For more applications, consult Intersil Application Note **AN517**, or the factory applications group.

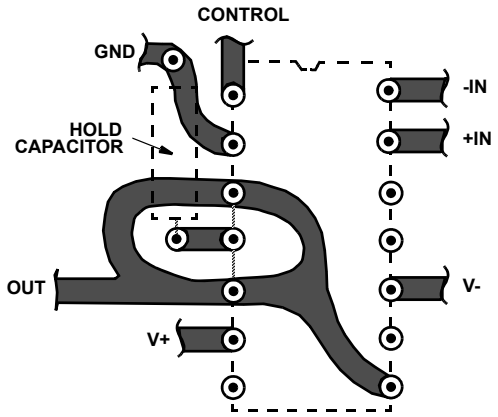


FIGURE 9. GUARD RING LAYOUT (BOTTOM VIEW)

Glossary of Terms

Acquisition Time

The time required following a “sample” command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

Aperture Time

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Effective Aperture Delay Time (EADT)

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

Drift Current

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta t}\ (V/s)$$

Typical Performance Curves

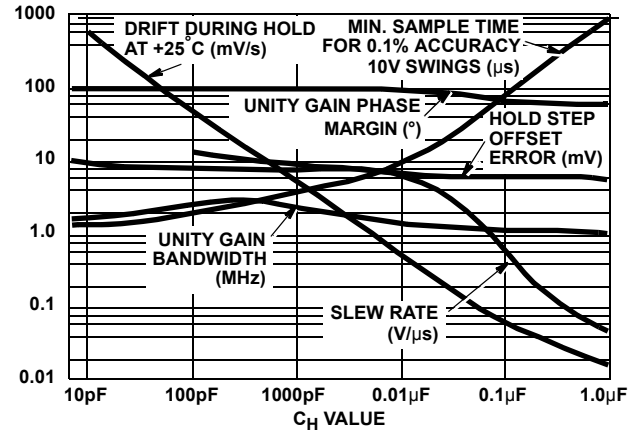


FIGURE 10. TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR

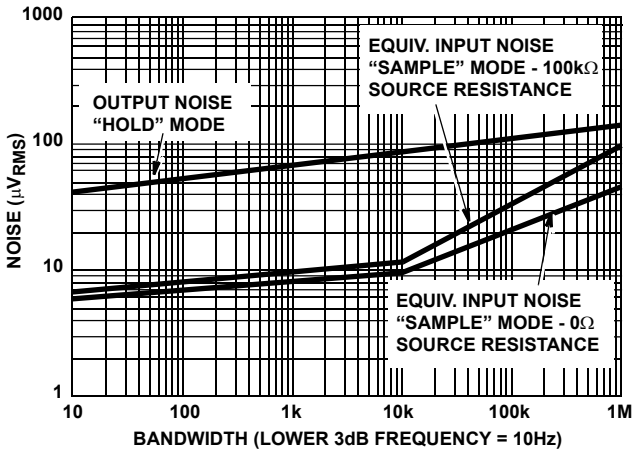


FIGURE 11. BROADBAND NOISE CHARACTERISTICS

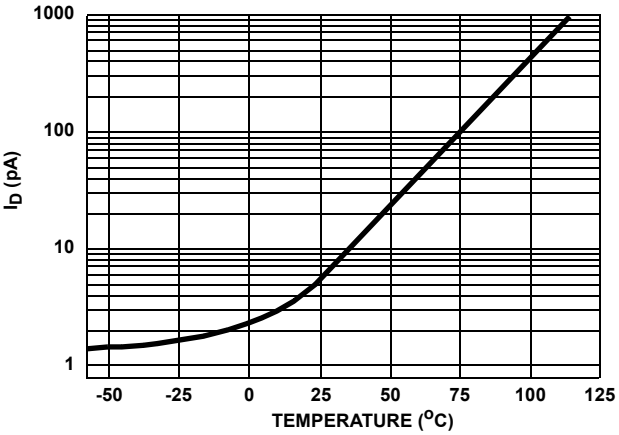


FIGURE 12. DRIFT CURRENT vs TEMPERATURE

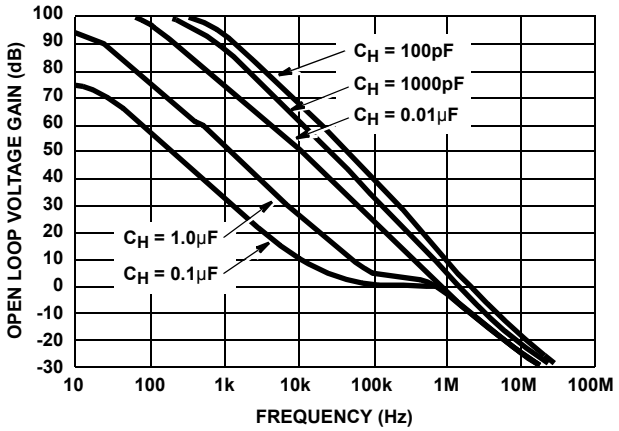


FIGURE 13. OPEN LOOP FREQUENCY RESPONSE

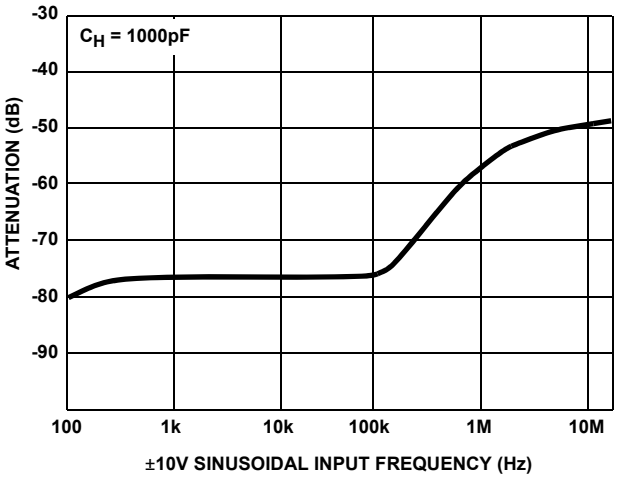


FIGURE 14. HOLD MODE FEED THROUGH ATTENUATION

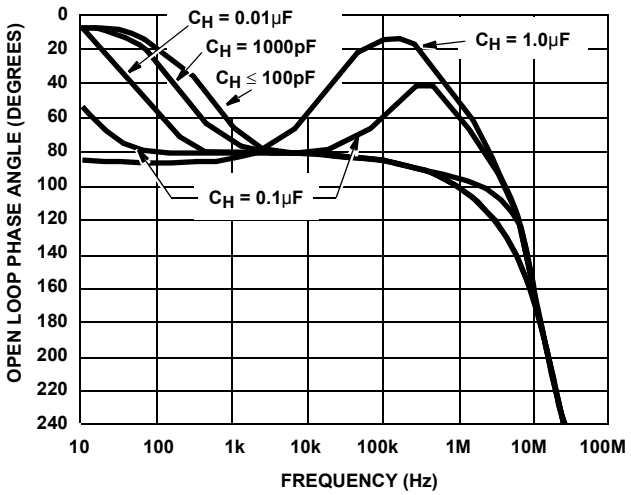


FIGURE 15. OPEN LOOP PHASE RESPONSE

Typical Performance Curves (Continued)

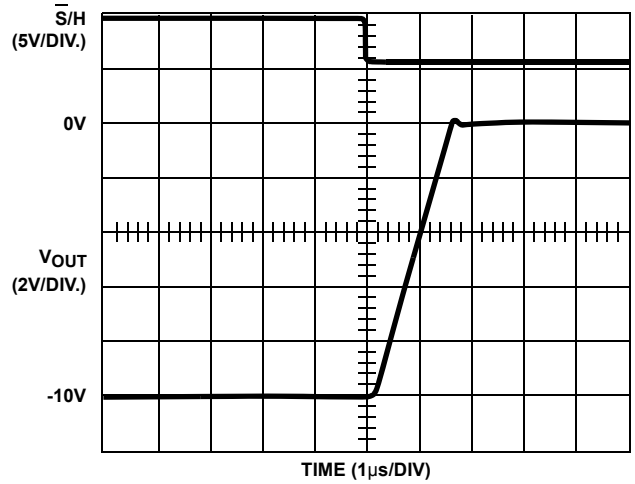


FIGURE 16. ACQUISITION TIME (C_H = 1000pF)

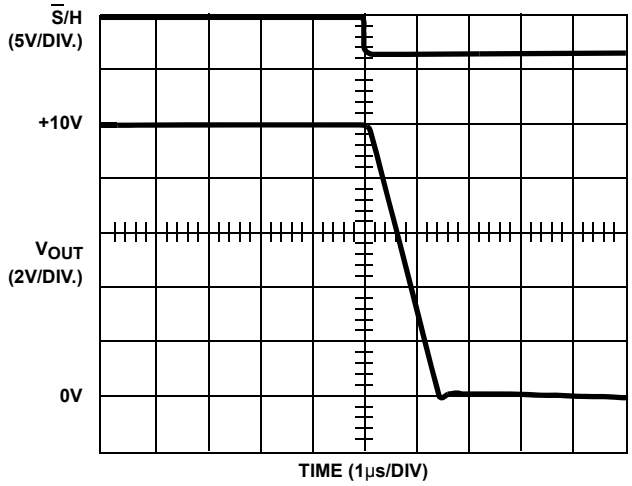


FIGURE 17. ACQUISITION TIME (C_H = 1000pF)

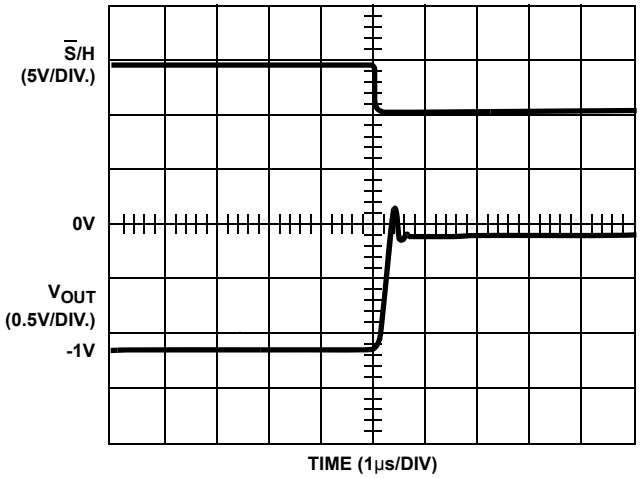


FIGURE 18. ACQUISITION TIME (C_H = 1000pF)

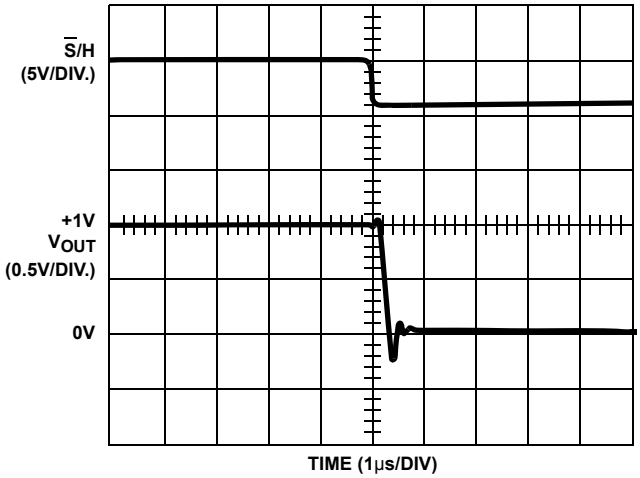


FIGURE 19. ACQUISITION TIME (C_H = 1000pF)

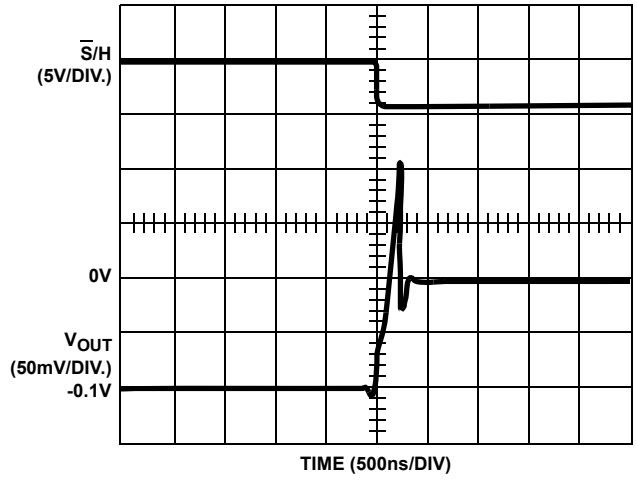


FIGURE 20. ACQUISITION TIME (C_H = 1000pF)

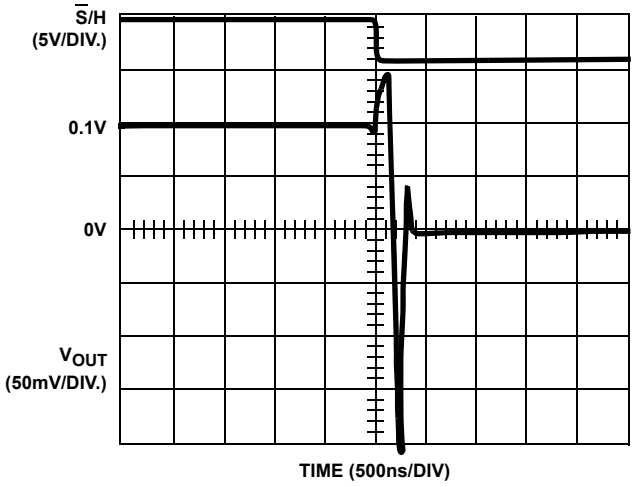


FIGURE 21. ACQUISITION TIME (C_H = 1000pF)

Die Characteristics

DIE DIMENSIONS:
102 mils x 61 mils x 19 mils
2590µm x 1550µm x 483µm

METALLIZATION:
Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL:
V-

BACKSIDE FINISH:
Gold, Nickel, Silicon, etc.

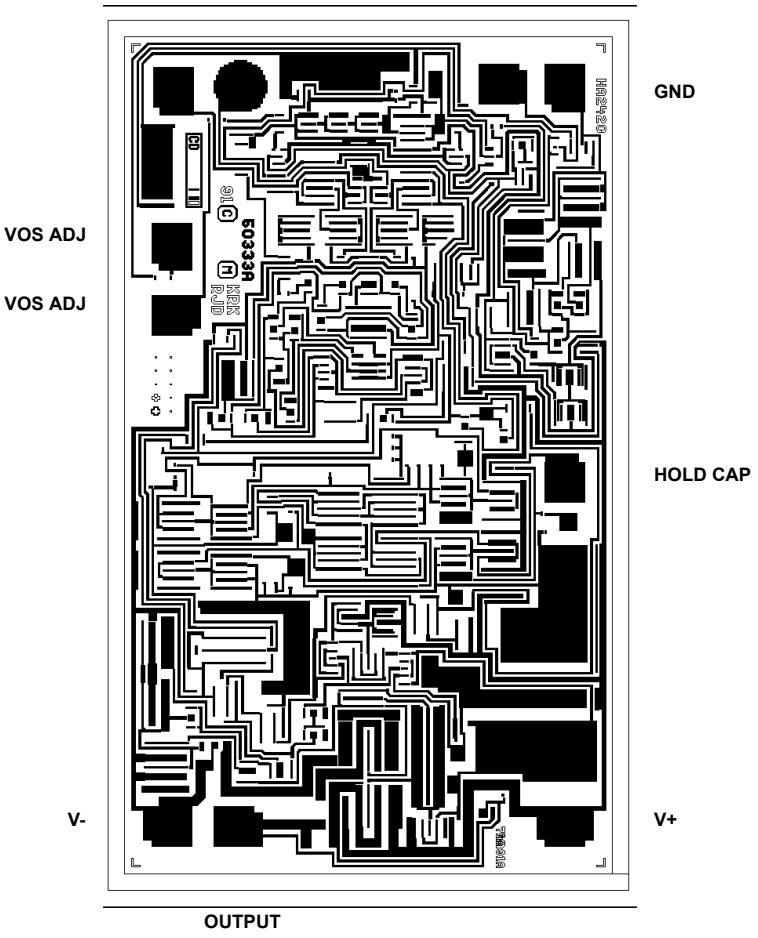
PASSIVATION:
Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

TRANSISTOR COUNT:
78

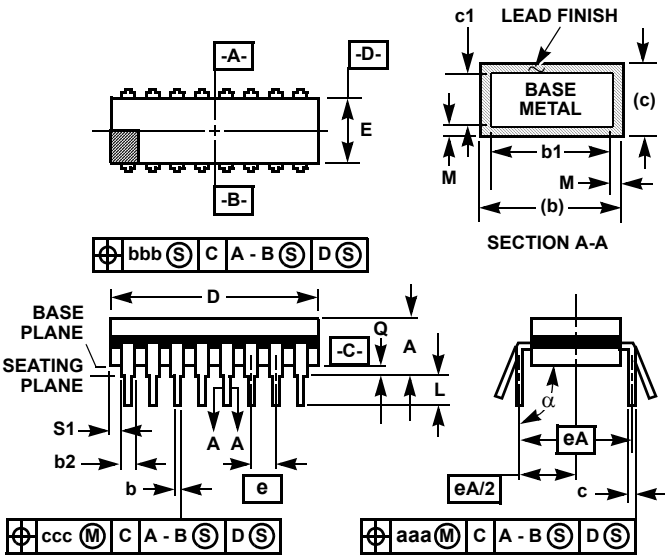
PROCESS:
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2420



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94