

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended  
for new design

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To all our customers

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Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

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# HAT1041T

Silicon P Channel Power MOS FET  
High Speed Power Switching

**RENESAS**

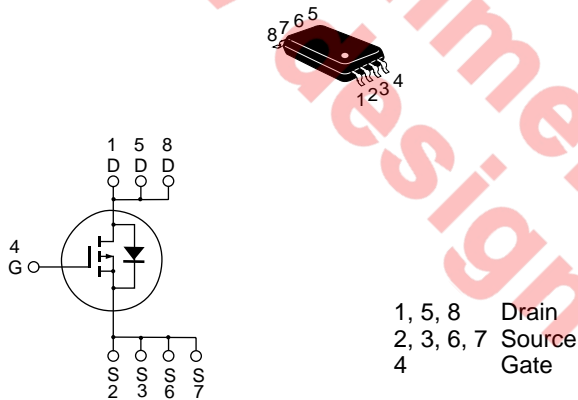
ADE-208-1238F (Z)  
7th. Edition  
Jan. 2001

## Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

## Outline

TSSOP-8



## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-20	V
Gate to source voltage	$V_{GSS}$	±12	V
Drain current	$I_D$	-6.0	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-48	A
Body-drain diode reverse drain current	$I_{DR}$	-6.0	A
Channel dissipation	Pch <sup>Note2</sup>	1.3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$

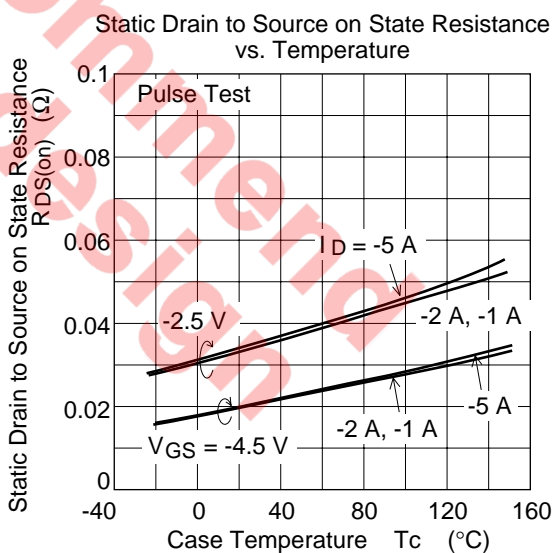
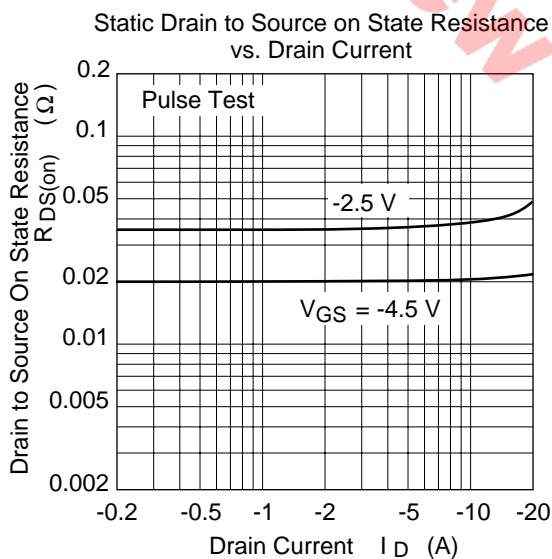
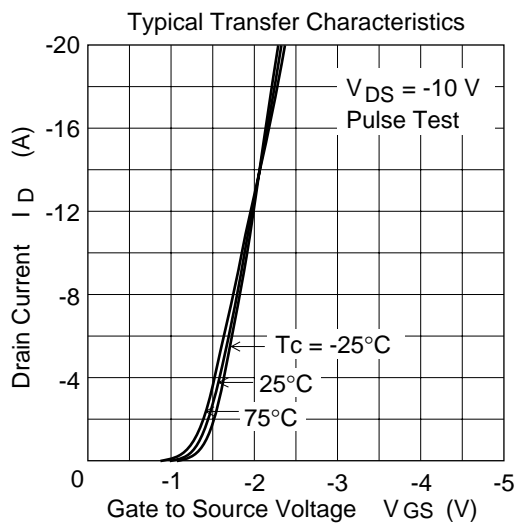
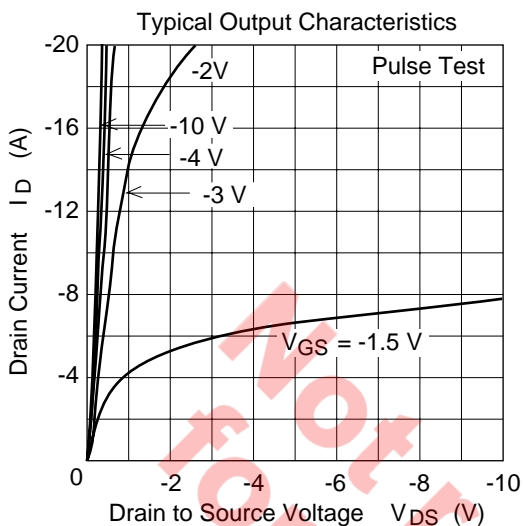
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

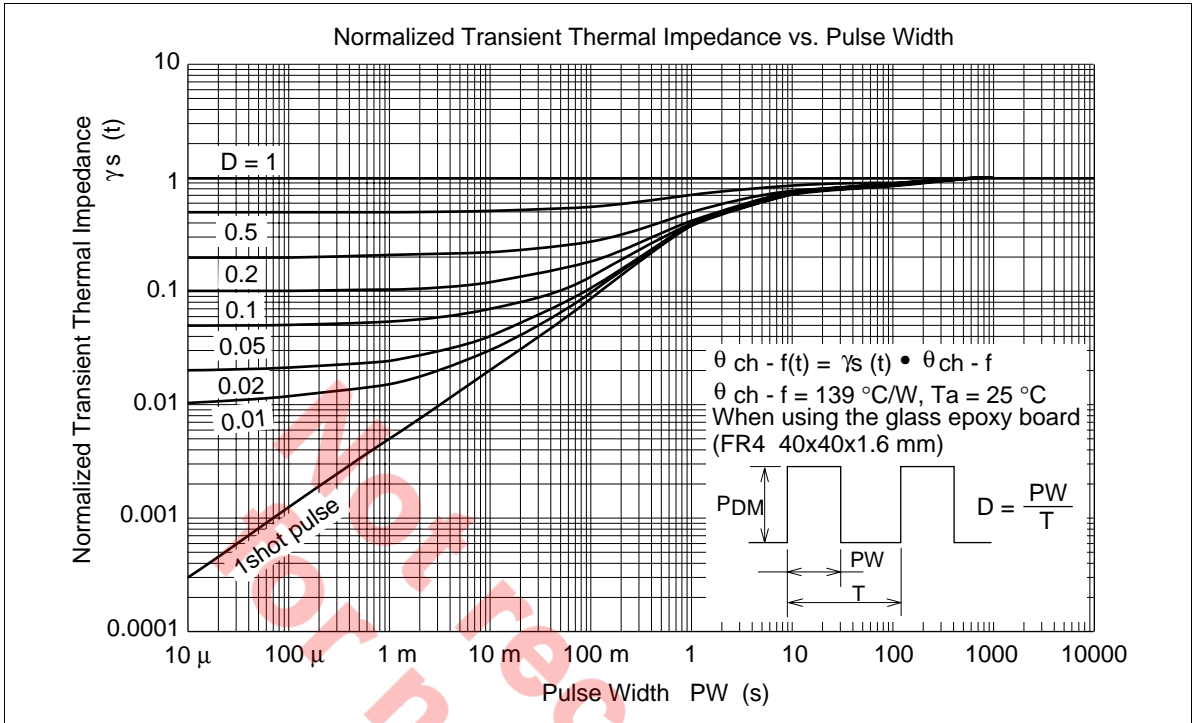
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10mA, V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±0.1	μA	$V_{GS} = \pm 12V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	μA	$V_{DS} = -20V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10V, I_D = -1mA$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.020	0.026	Ω	$I_D = -3A, V_{GS} = -4.5V$ <sup>Note3</sup>
	$R_{DS(on)}$	—	0.035	0.045	Ω	$I_D = -3A, V_{GS} = -2.5V$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	6.5	11	—	S	$I_D = -3A, V_{DS} = -10V$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	1850	—	pF	$V_{DS} = -10V$
Output capacitance	$C_{oss}$	—	590	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	380	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	30	—	ns	$V_{GS} = -4V, I_D = -3A$
Rise time	$t_r$	—	145	—	ns	$V_{DD} \cong -10V$
Turn-off delay time	$t_{d(off)}$	—	210	—	ns	
Fall time	$t_f$	—	170	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	-0.85	-1.10	V	$I_F = -6.0A, V_{GS} = 0$ <sup>Note3</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	70	—	ns	$I_F = -6.0A, V_{GS} = 0$ $diF/dt = 20A/\mu s$

Note: 3. Pulse test

Main Characteristics



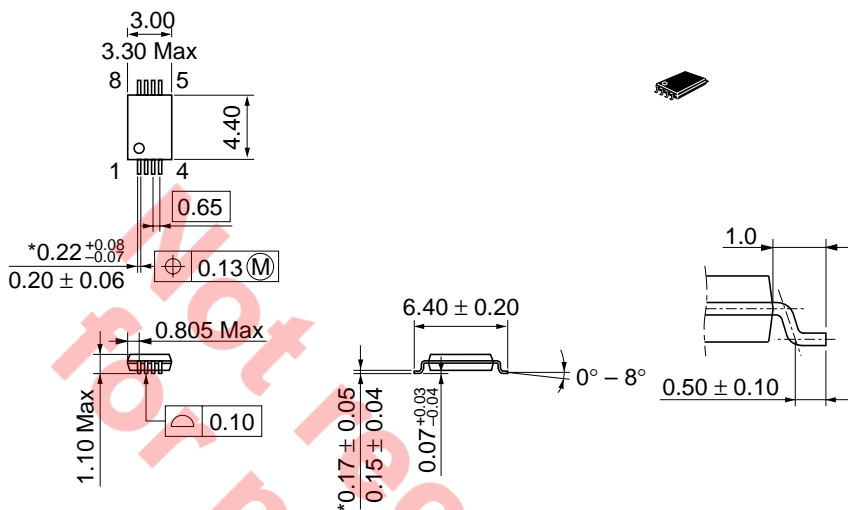


new design  
 recommend



Package Dimensions

As of January, 2001  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-8D
JEDEC	—
EIAJ	—
Mass (reference value)	—

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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL       NorthAmerica       : <http://semiconductor.hitachi.com/>  
          Europe                : <http://www.hitachi-eu.com/hel/ecg>  
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic Components Group  
Dornacher Straße 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 585160

Hitachi Asia Ltd.  
Hitachi Tower  
16 Collyer Quay #20-00,  
Singapore 049318  
Tel : <65>-538-6533/538-8577  
Fax : <65>-538-6933/538-3877  
URL : <http://www.hitachi.com.sg>

Hitachi Asia Ltd.  
(Taipei Branch Office)  
4/F, No. 167, Tun Hwa North Road,  
Hung-Kuo Building,  
Taipei (105), Taiwan  
Tel : <886>-(2)-2718-3666  
Fax : <886>-(2)-2718-8180  
Telex : 23222 HAS-TP  
URL : <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon,  
Hong Kong  
Tel : <852>-(2)-735-9218  
Fax : <852>-(2)-730-0281  
URL : <http://www.hitachi.com.hk>

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