

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Renesas Technology Home Page: <http://www.renesas.com>

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

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HAT2057RA

Silicon N Channel Power MOS FET
High Speed Power Switching

RENESAS

ADE-208-1636 (Z)

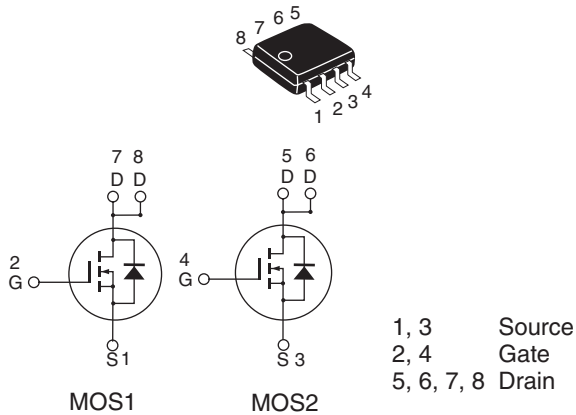
1st. Edition
Feb. 2003

Features

- Low on-resistance
- Capable of 1.5 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	+6,-3	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	32	A
Body-drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	P_{ch} ^{Note2}	2	W
Channel dissipation	P_{ch} ^{Note3}	3	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$

2. 1 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$

3. 2 Drive operation: When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10\text{s}$

Electrical Characteristics

(Ta = 25°C)

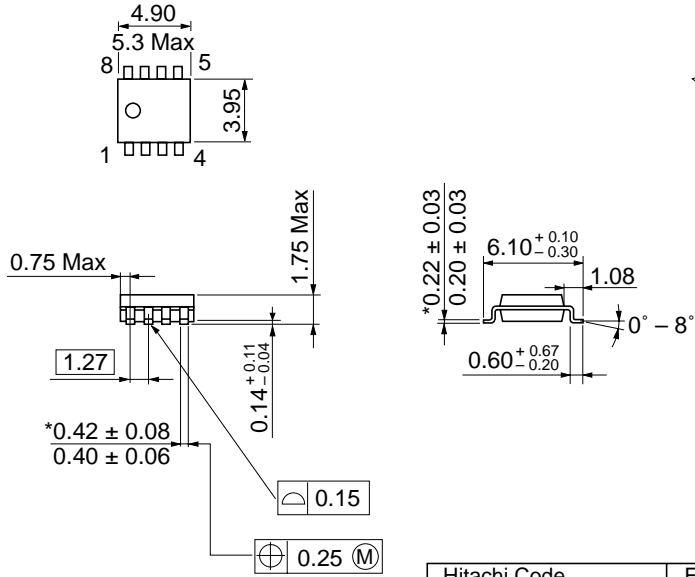
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.2	μA	$V_{GS} = +6 \text{ V}, -3\text{V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 10 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.15	—	0.90	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	26	33	$\text{m}\Omega$	$I_D = 2 \text{ A}, V_{GS} = 4 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	40	60	$\text{m}\Omega$	$I_D = 2 \text{ A}, V_{GS} = 1.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	8	13	—	S	$I_D = 2 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1100	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	155	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	125	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 4 \text{ V}, I_D = 2 \text{ A}$
Rise time	t_r	—	25	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	65	—	ns	$R_g = 4.7 \Omega$
Fall time	t_f	—	13	—	ns	$R_L = 5 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.80	1.04	V	$I_F = 4, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 4\text{A}, V_{GS} = 0$ $diF/dt = 20 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions

As of July, 2002

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

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