HAT3029R

Silicon N/P Channel Power MOS FET
Power Switching

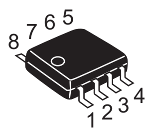
REJ03G1597-0601
Rev.6.01
Nov.24.2016

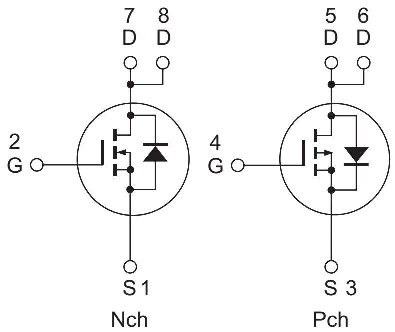
Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)





1, 3 Source
2, 4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	30	–30	V
Gate to source voltage	V_{GSS}	±20	-20/+10	V
Drain current	I_D	6	–6	A
Drain peak current	$I_{D(pulse)}$ [Note1]	48	–48	A
Body-drain diode reverse drain current	I_{DR}	6	–6	A
Channel dissipation	Pch [Note2]	1.3		W
Channel dissipation	Pch [Note3]	2.0		W
Channel temperature	Tch	150		°C
Storage temperature	Tstg	–55 to +150		°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s
3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics

(Ta = 25°C)

• N Channel

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	27	34	mΩ	I_D = 3 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	40	58	mΩ	I_D = 3 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	6	10	—	S	I_D = 3 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	410	—	pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	110	—	pF	
Reverse transfer capacitance	Crss	—	41	—	pF	
Total gate charge	Qg	—	3.1	—	nC	V_{DD} = 10 V V_{GS} = 4.5 V I_D = 6 A
Gate to source charge	Qgs	—	1.1	—	nC	
Gate to drain charge	Qgd	—	1.1	—	nC	
Turn-on delay time	$t_{d(on)}$	—	5.4	—	ns	V_{GS} = 10 V, I_D = 3 A V_{DD} ≅ 10 V R_L = 3.33 Ω Rg = 4.7 Ω
Rise time	t_r	—	10	—	ns	
Turn-off delay time	$t_{d(off)}$	—	36	—	ns	
Fall time	t_f	—	3.0	—	ns	
Body–drain diode forward voltage	V_{DF}	—	0.84	1.10	V	IF = 6 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	20	—	ns	IF = 6 A, V_{GS} = 0 di_F/dt = 100 A/ μs

Notes: 4. Pulse test

• P Channel

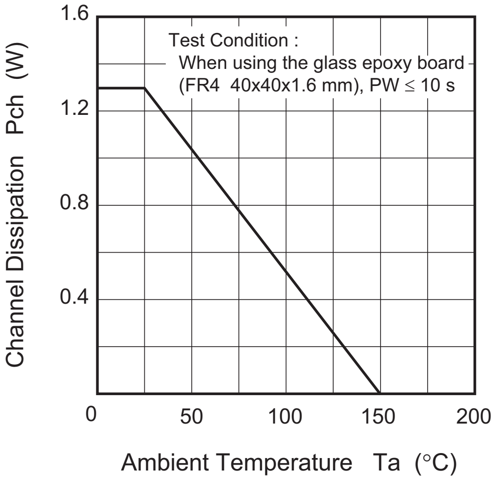
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = -20,+10 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–1	μA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–1.0	—	–2.5	V	V_{DS} = –10 V, I_D = –1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	25	32	mΩ	I_D = –3 A, V_{GS} = –10 V Note4
	$R_{DS(on)}$	—	36	53	mΩ	I_D = –3 A, V_{GS} = – 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	6	10	—	S	I_D = –3 A, V_{DS} = –10 V Note4
Input capacitance	Ciss	—	1330	—	pF	V_{DS} = –10 V V_{GS} = 0 f = 1MHz
Output capacitance	Coss	—	215	—	pF	
Reverse transfer capacitance	Crss	—	155	—	pF	
Total gate charge	Qg	—	11.5	—	nC	V_{DD} = –10 V V_{GS} = –4.5 V I_D = -6 A
Gate to source charge	Qgs	—	3.2	—	nC	
Gate to drain charge	Qgd	—	4.4	—	nC	
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	V_{GS} = –10 V, I_D = –3 A V_{DD} ≅ –10 V R_L = 3.33 Ω R_g = 4.7 Ω
Rise time	t_r	—	19	—	ns	
Turn-off delay time	$t_{d(off)}$	—	47	—	ns	
Fall time	t_f	—	8	—	ns	
Body–drain diode forward voltage	V_{DF}	—	–0.84	–1.10	V	IF = –6 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	20	—	ns	IF = –6 A, V_{GS} = 0 di_F/dt =100A/μs

Notes: 4. Pulse test

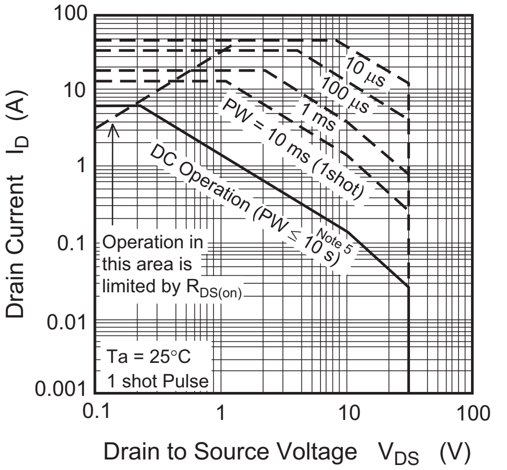
Main Characteristics

• N Channel

Power vs. Temperature Derating

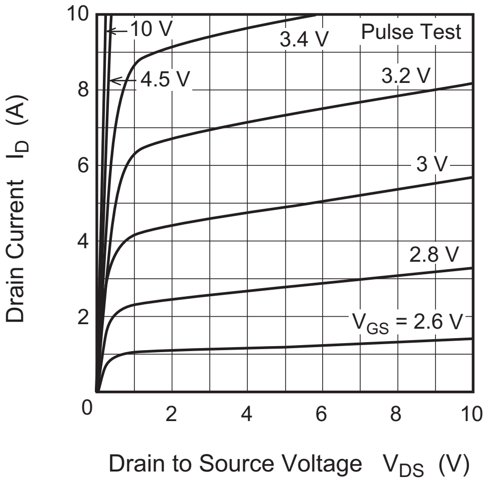


Maximum Safe Operation Area

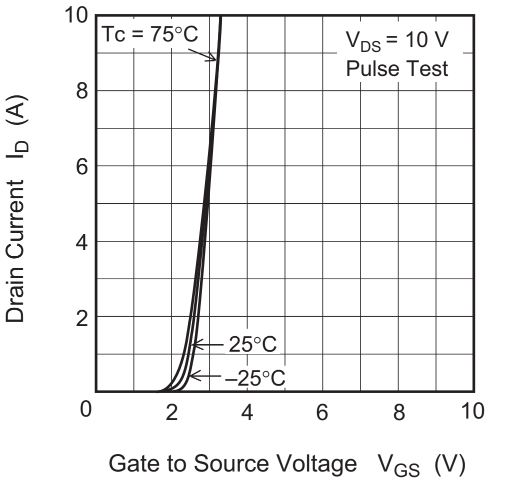


Note 5 : When using the glass epoxy board (FR4 40x40x1.6 mm)

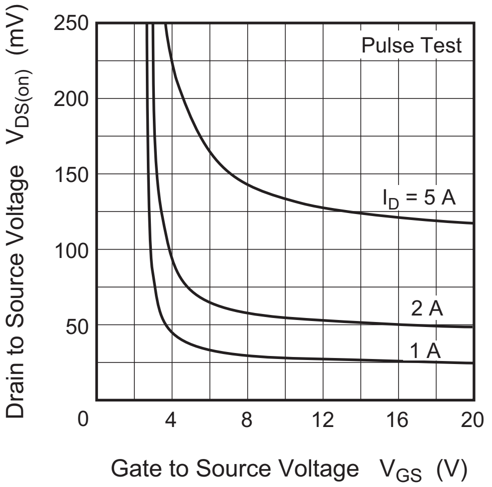
Typical Output Characteristics



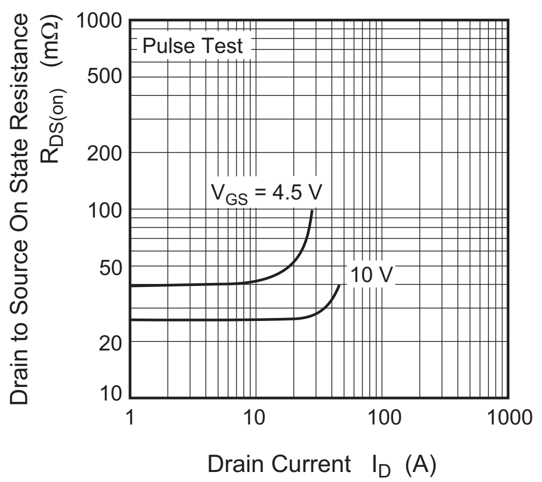
Typical Transfer Characteristics



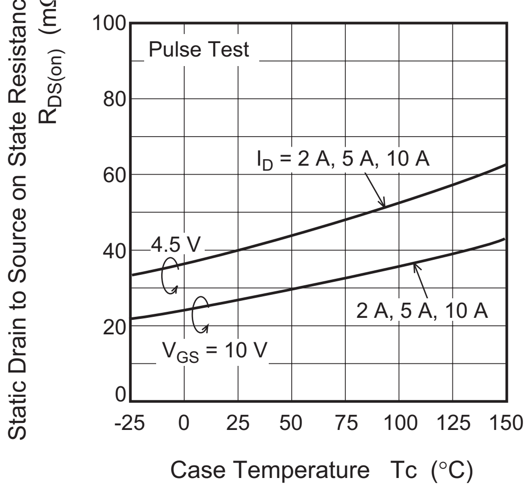
Drain to Source Saturation Voltage vs. Gate to Source Voltage



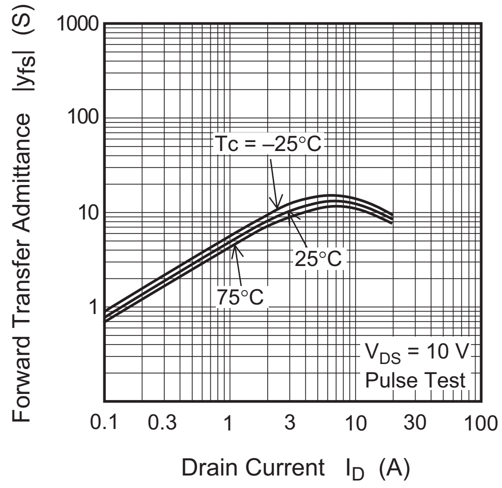
Static Drain to Source on State Resistance vs. Drain Current



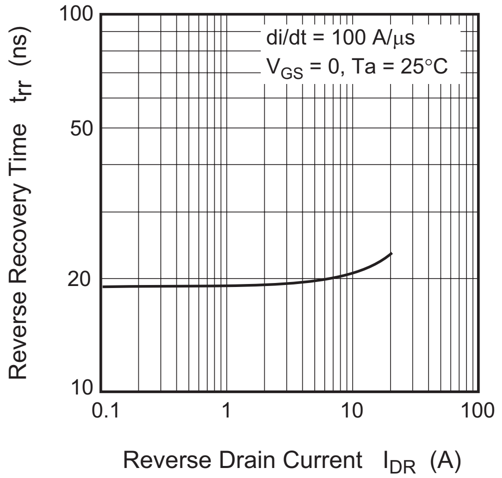
Static Drain to Source on State Resistance vs. Temperature



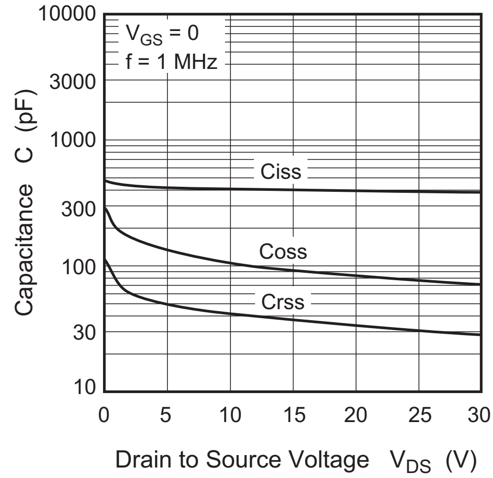
Forward Transfer Admittance vs. Drain Current



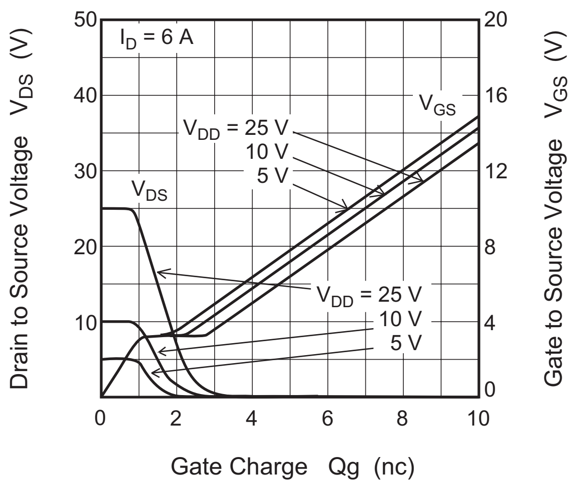
Body–Drain Diode Reverse Recovery Time



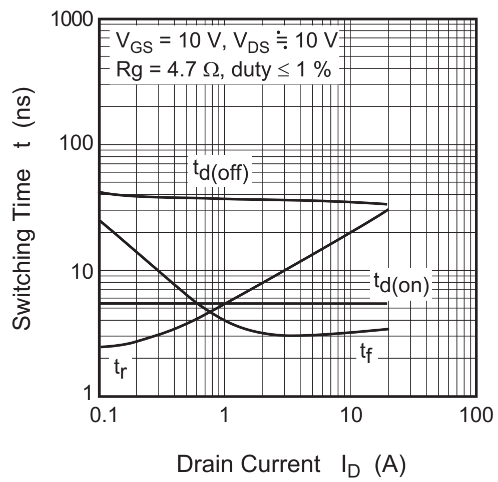
Typical Capacitance vs. Drain to Source Voltage



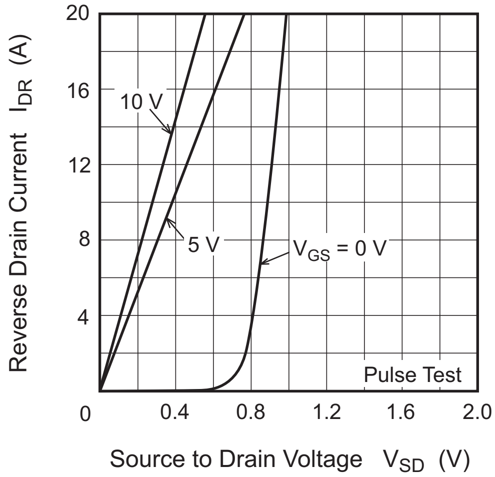
Dynamic Input Characteristics



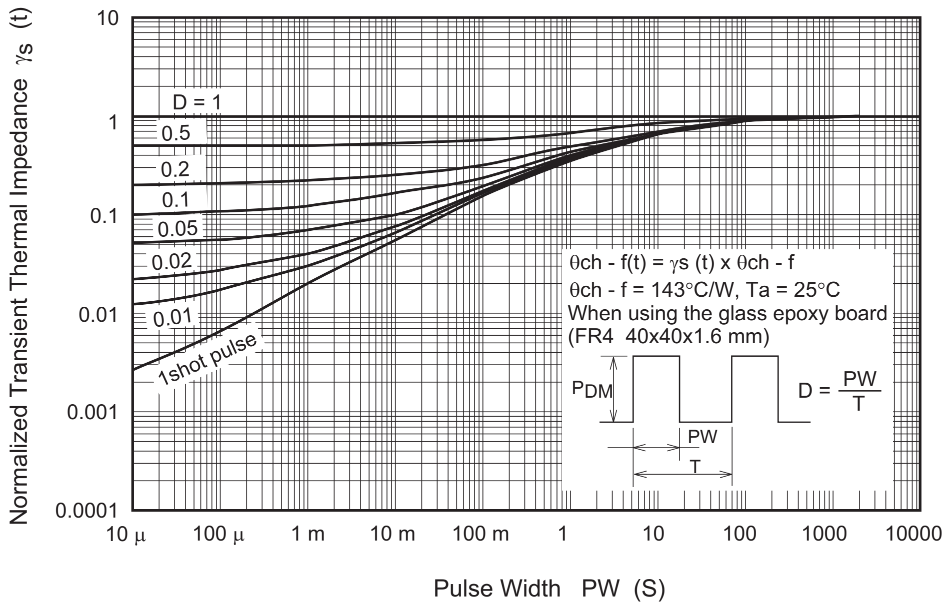
Switching Characteristics



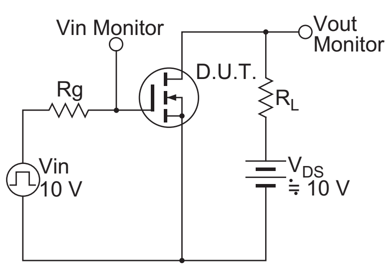
Reverse Drain Current vs.
Source to Drain Voltage



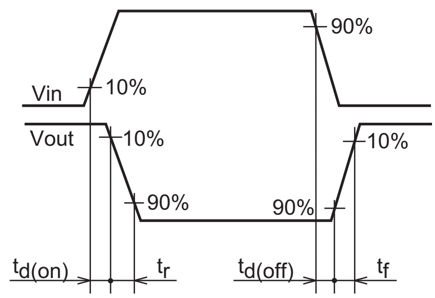
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

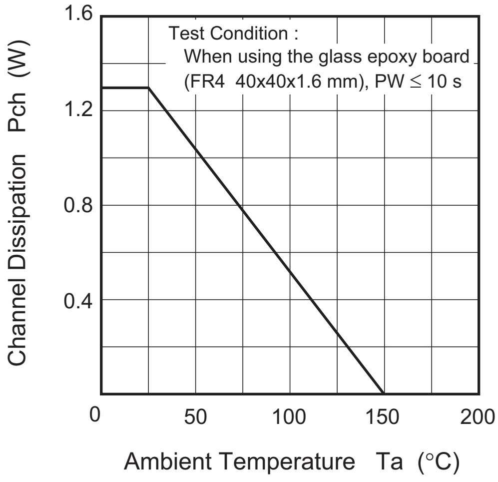


Switching Time Waveform

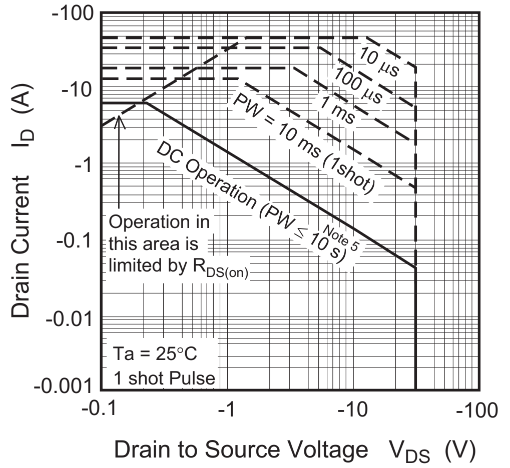


• **P Channel**

Power vs. Temperature Derating

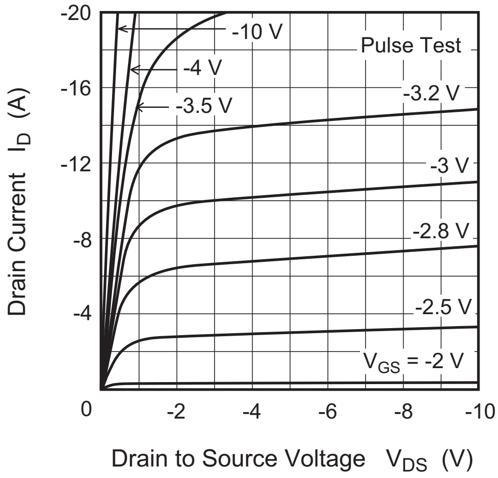


Maximum Safe Operation Area

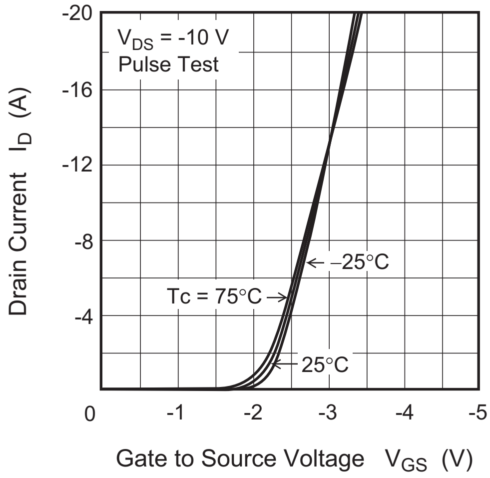


Note 5 : When using the glass epoxy board (FR4 40x40x1.6 mm)

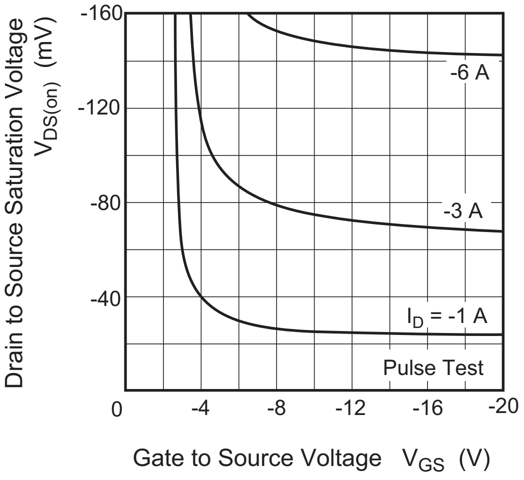
Typical Output Characteristics



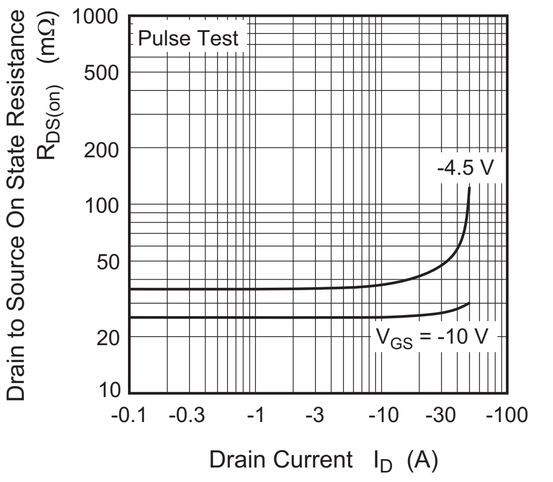
Typical Transfer Characteristics



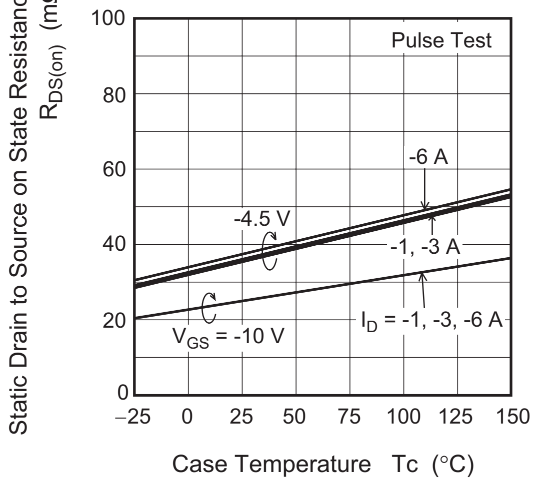
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



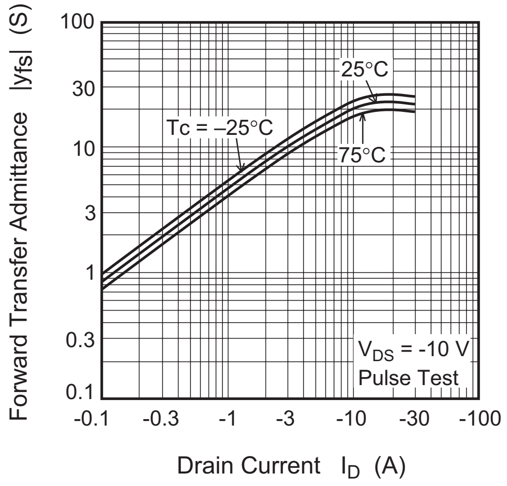
Static Drain to Source on State Resistance
vs. Drain Current



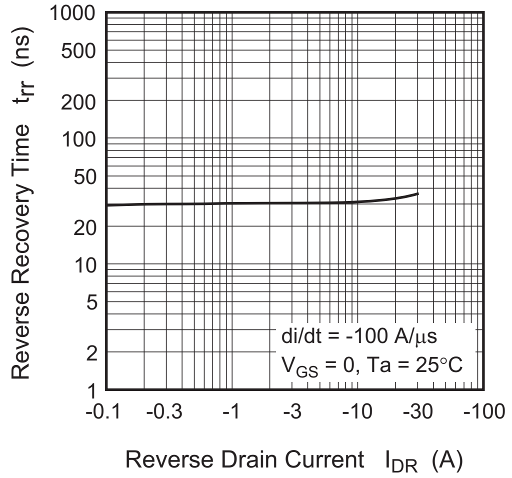
Static Drain to Source on State Resistance
vs. Temperature



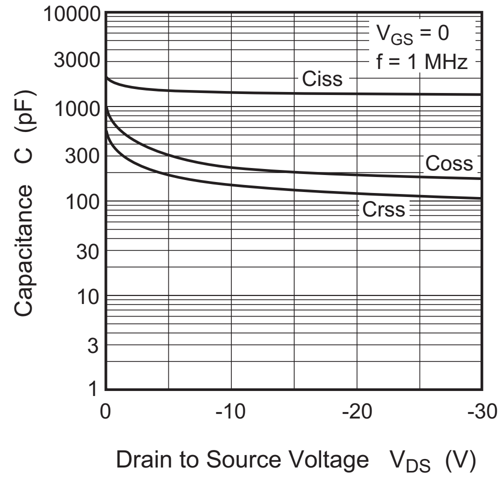
Forward Transfer Admittance vs.
Drain Current



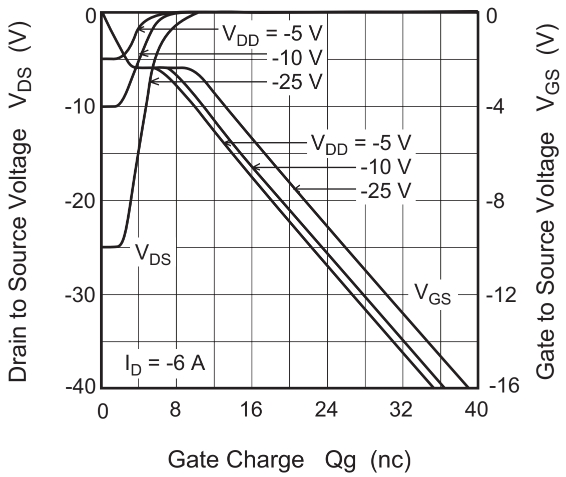
Body–Drain Diode Reverse
Recovery Time



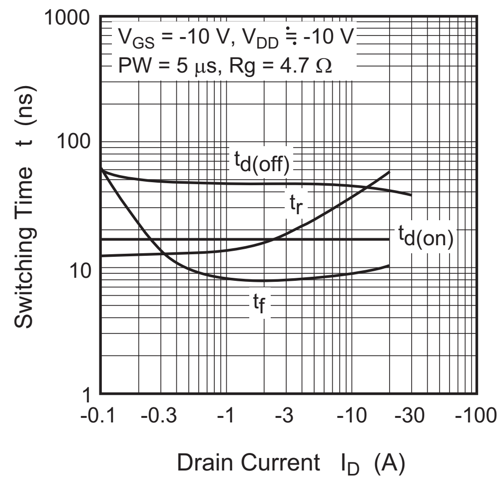
Typical Capacitance vs.
Drain to Source Voltage

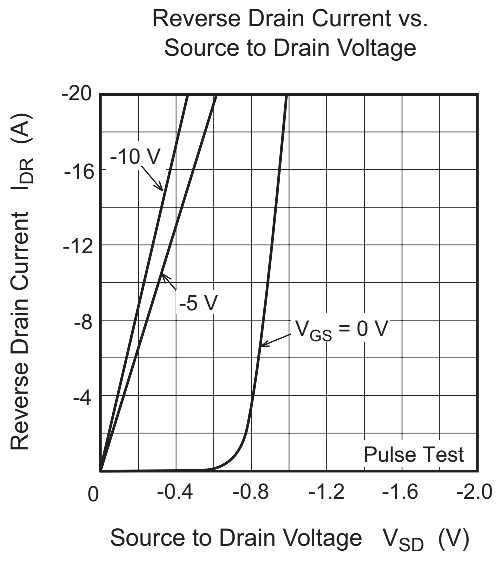


Dynamic Input Characteristics

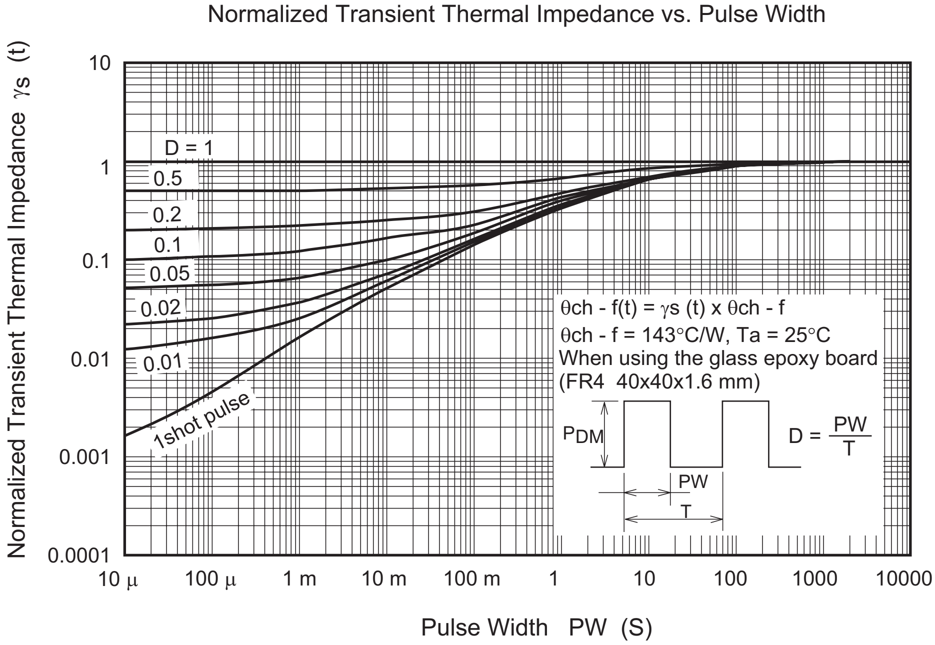


Switching Characteristics

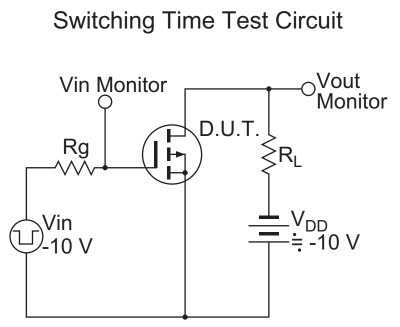




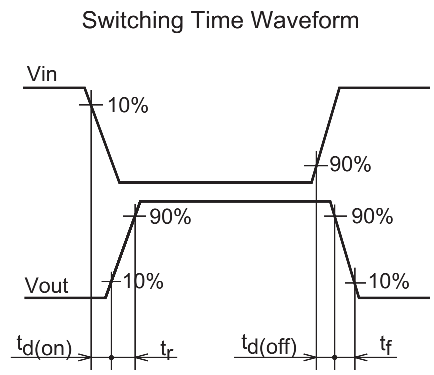
Reverse Drain Current vs.
Source to Drain Voltage
Reverse Drain Current I_DR (A)
Source to Drain Voltage V_SD (V)
-20
-16
-12
-8
-4
0
-0.4
-0.8
-1.2
-1.6
-2.0
-10 V
-5 V
V_GS = 0 V
Pulse Test



Normalized Transient Thermal Impedance vs. Pulse Width
Normalized Transient Thermal Impedance γs (t)
Pulse Width PW (S)
10
1
0.1
0.01
0.001
0.0001
10 μ
100 μ
1 m
10 m
100 m
1
10
100
1000
10000
D = 1
0.5
0.2
0.1
0.05
0.02
0.01
1shot pulse
θch - f(t) = γs (t) x θch - f
θch - f = 143°C/W, Ta = 25°C
When using the glass epoxy board
(FR4 40x40x1.6 mm)
P_DM
D = PW / T
PW
T



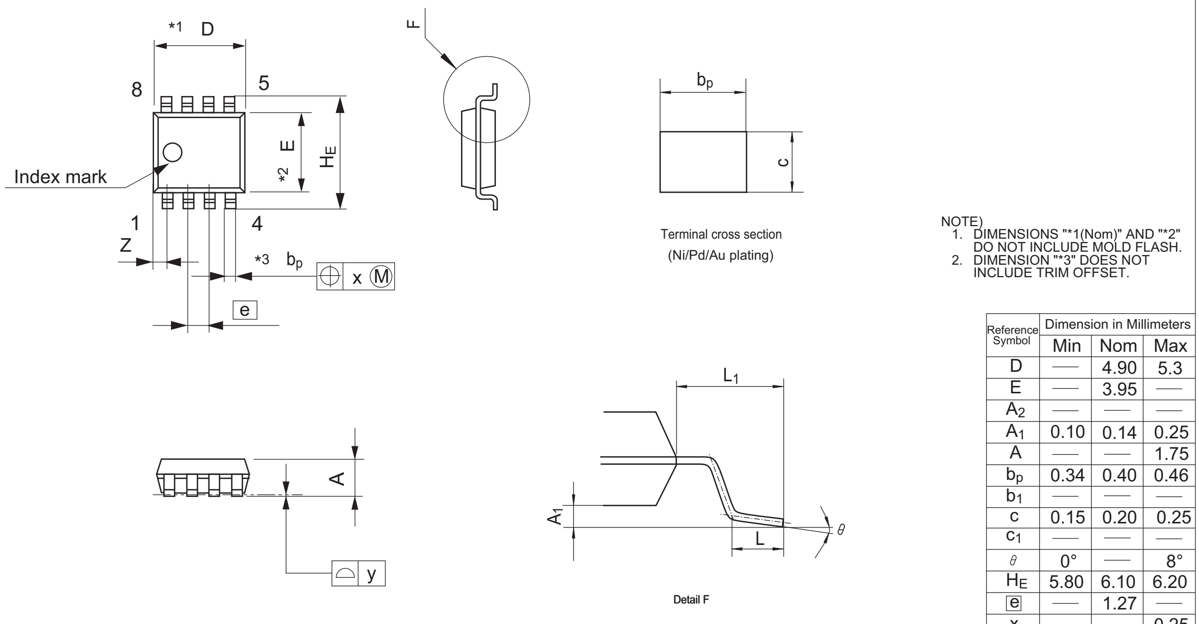
Switching Time Test Circuit
Vin Monitor
Vout
Monitor
D.U.T.
Rg
R_L
Vin
-10 V
V_DD
= -10 V



Switching Time Waveform
Vin
10%
90%
Vout
90%
90%
10%
10%
td(on)
tr
td(off)
tf

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
HAT3029R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

General Precautions in the Handling of Power MOSFET and IGBT Products

The following usage notes are applicable to general purpose Power MOSFET and IGBT products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Derating

Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it are within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data.

2. Quality grade

— The quality grade of this product is “Standard”.
— If you plan to use this product to “High quality” application, please inform to Renesas.
— Fail safe system is necessary to prevent malfunction even if this product is broken.

Notice

注意事项

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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Colophon 5.0