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# **HD74LS156**

# Dual 2-line-to-4-line Decoders / Demultiplexers (with open collector outputs)

REJ03D0441-0300 Rev.3.00 Jul.13.2005

This circuit features dual 1-line-to-4-line demultiprexer with individual strobes and common binary-address input. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating.

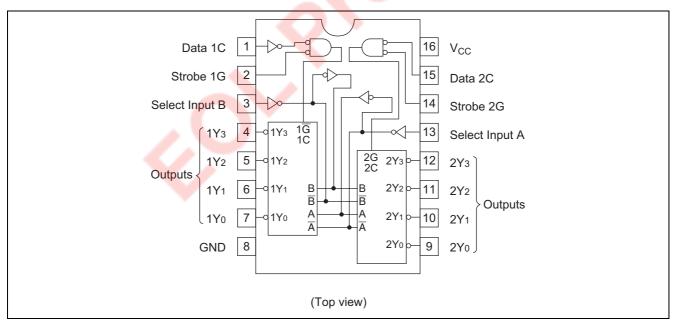
#### **Features**

Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS156P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_
HD74LS156RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	FP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

## Pin Arrangement



## **Function Table**

#### • 2-to-4-line Decoder / 1-to-4-line Demultiplexer

	Inp	uts		Outputs			
Se	lect	Strobe	Data	1Y <sub>0</sub>	1Y <sub>1</sub>	41/	1Y <sub>3</sub>
В	Α	1G	1C	110	''1	1Y <sub>2</sub>	113
Х	Х	Н	Х	Н	Н	Н	Н
L	L	L	Н	L	Н	Н	Н
L	Н	L	Н	Н	L	Н	Н
Н	L	L	Н	Н	Н	L	Н
Н	Н	L	Н	Н	Н	Н	L
Х	Х	Х	L	Н	Н	Н	Н

	Inp	outs		Outputs				
Se	elect	Strobe	Data	2Y <sub>0</sub>	07		2V	
В	Α	2G	2C	210	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>	
Х	Х	Н	Х	Н	Н	Н	Н	
L	L	L	L	L	Н	Н	Н	
L	Н	L	L	Н	L	H	Н	
Н	L	L	L	Н	Н	L	Н	
Н	Н	L	L	Н	Н	Н	L	
Х	Х	Х	Н	H	Н	Н	Н	

## • 3-to-8-line Decoder / 1-to-8-line Demultiplexer

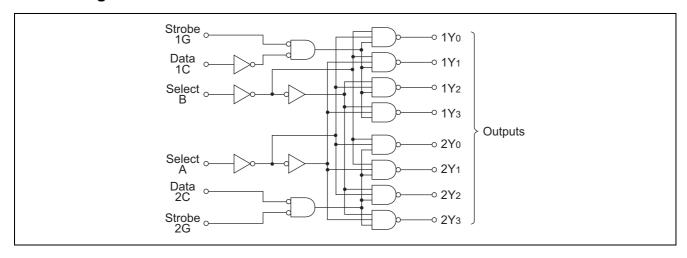
Inputs				Outputs							
Select Strobe or Data		(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)		
C*1	В	Α	G* <sup>2</sup>	2Y <sub>0</sub>	2Y <sub>1</sub>	2Y <sub>2</sub>	2Y <sub>3</sub>	1Y <sub>0</sub>	1Y <sub>1</sub>	1Y <sub>2</sub>	1Y <sub>3</sub>
Х	Х	X	Н	Н	Н	Н	Н	Τ	Н	Η	Н
L	L	L	L	اـ	Н	Н	Н	Τ	Н	Η	Н
L	L	Н	L	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	L	Н	Н	Н	Н	Н
L	Н	Н	L	Н	Н	Н	L	Н	Н	Н	Н
Н	L	L	L	Н	Н	Н	Н	L	Н	Н	Н
Н	L	Н		Н	Н	Н	Н	Н	L	Н	Н
Н	Н	L (	L	Н	Н	Н	Н	Н	Н	L	Н
Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	L

Notes: 1. C; input 1C and 2C connected together

2. G; inputs 1G and 2G connected together

3. H; high level, L; low level, X; irrelevant

## **Block Diagram**



## **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	Tstg	−65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## **Recommended Operating Conditions**

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
High level output voltage	$V_{OH}$	_		5.5	V
Low level output current	I <sub>OL</sub>	_		8	mA
Operating temperature	Topr	-20	25	75	°C

## **Electrical Characteristics**

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$ 

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	$V_{IH}$	2.0	_	_	V	
Input voltage	V <sub>IL</sub>	_	_	0.8	V	
Output current	I <sub>OH</sub>	1	1	100	μΑ	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$ $V_{OH} = 5.5 \text{V}$
Output voltage	V <sub>OL</sub>	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$
Output voltage		_	_	0.5	V	$I_{OL} = 8 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$
	I <sub>IH</sub>	_	_	20	μΑ	$V_{CC} = 5.25 \text{ V}, V_{I} = 2.7 \text{ V}$
Input current	I <sub>IL</sub>	_	_	-0.4	mA	$V_{CC} = 5.25 \text{ V}, V_{I} = 0.4 \text{ V}$
	I <sub>I</sub>	_	_	0.1	mA	$V_{CC} = 5.25 \text{ V}, V_{I} = 7 \text{ V}$
Supply current**	I <sub>CC</sub>	_	6.1	10	mA	V <sub>CC</sub> = 5.25 V
Input clamp voltage	$V_{IK}$			-1.5	V	$V_{CC} = 4.75 \text{ V}, I_{IN} = -18 \text{ mA}$

Notes:  $^*V_{CC} = 5 \text{ V}$ ,  $Ta = 25^{\circ}C$ 

<sup>\*\*</sup>  $I_{CC}$  is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

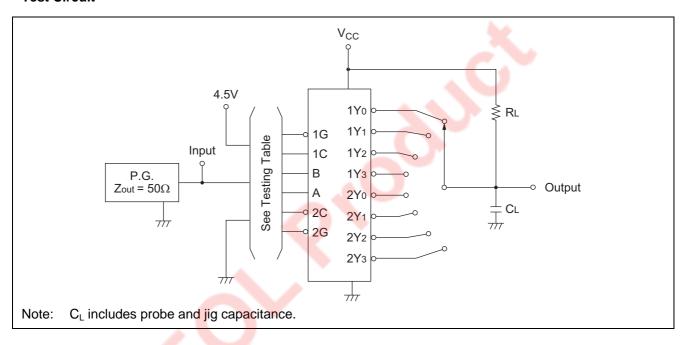
## **Switching Characteristics**

$$(V_{CC} = 5 \text{ V}, \text{ Ta} = 25^{\circ}\text{C})$$

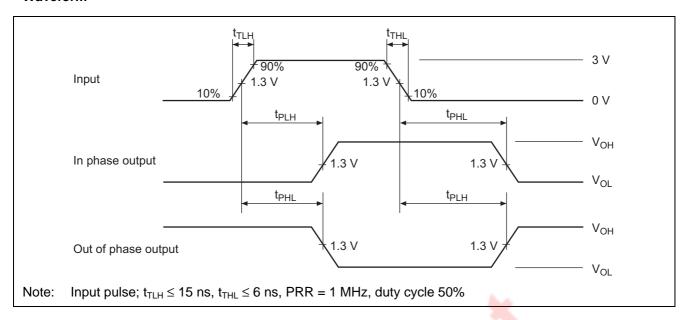
Item	Symbol	Inputs	Output	Level of logic	min.	typ.	max.	Unit	Condition
Propagation	t <sub>PLH</sub>	A, B, 2C, 1G or 2G	Y	2		25	40		
	t <sub>PHL</sub>	A, B, 2C, 1G or 2G	Y	2		34	51	ns	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$
delay time	t <sub>PLH</sub>	A or B	Υ	3		31	46		
	t <sub>PHL</sub>	A or B	Υ	3		34	51		
	t <sub>PLH</sub>	1C	Υ	3		32	48		
	t <sub>PHL</sub>	1C	Υ	3		32	48		

## **Testing Method**

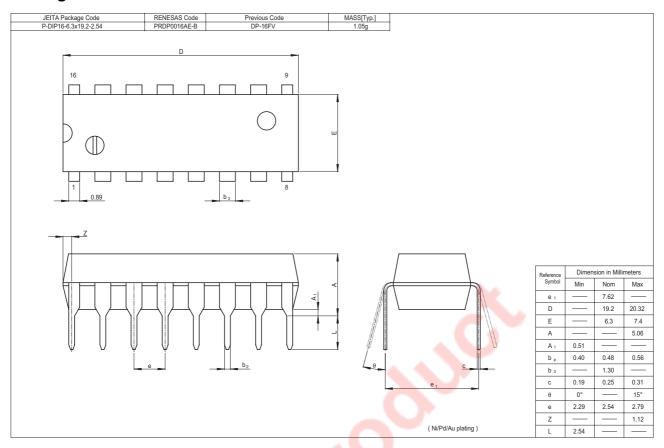
## **Test Circuit**

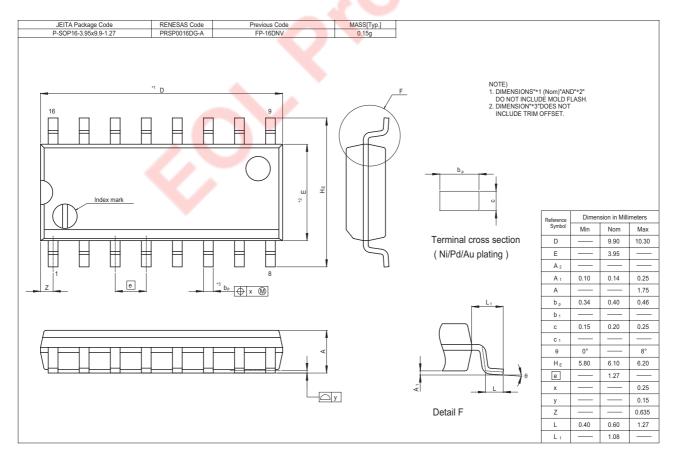


#### Waveform



## **Package Dimensions**





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