To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS669

Synchronous Up / Down 4-bit Binary Counter

REJ03D0493–0200
Rev.2.00
Feb.18.2005

This synchronous preset table 4-bit binary counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input trigger the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. the load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up / down input. when the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages.

Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable P, enable T, load, up / down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

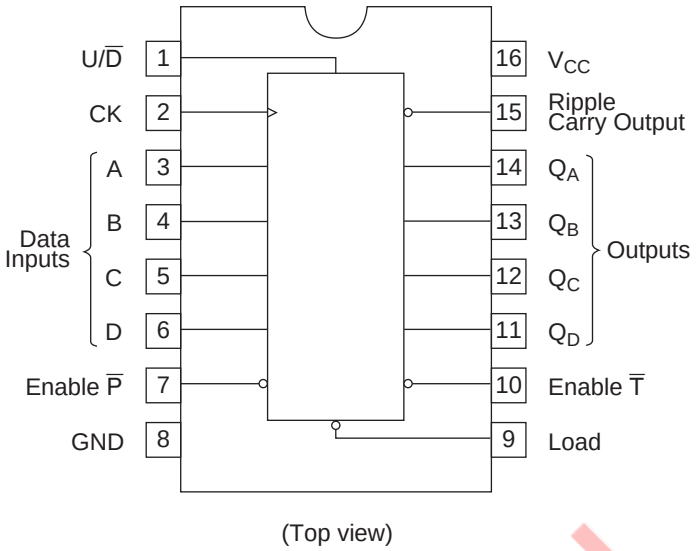
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS669FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

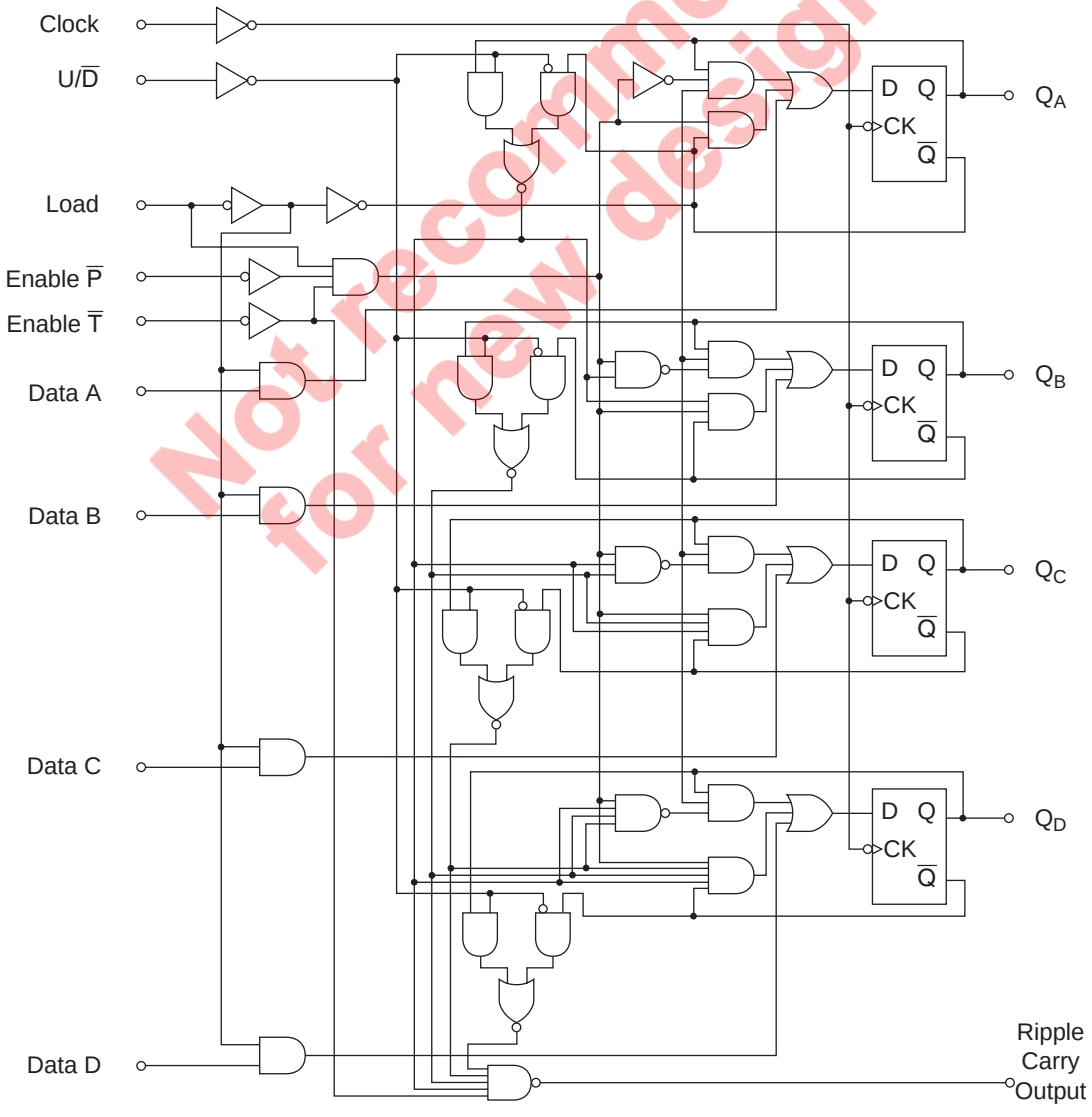
Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Count frequency		f_{count}	0	—	25	MHz
Clock pulse width		$t_{w\,(CK)}$	25	—	—	ns
Setup time	Input Data A, B, C, D	t_{su}	25	—	—	ns
	Enable $\overline{P}$, $\overline{T}$		35	—	—	
	Load		30	—	—	
	Up/Down		35	—	—	
Hold time		t_h	0	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5	V	I_{OL} = 8 mA
Input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clock, $\overline{T}$		—	—	20		
	Load		—	—	40		
	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clock, $\overline{T}$		—	—	–0.4		
	Load		—	—	–0.8		
	A, B, C, D, $\overline{P}$, U/$\overline{D}$	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clock, $\overline{T}$		—	—	0.1		
	Load		—	—	0.2		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**		I_{CC}	—	20	34	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

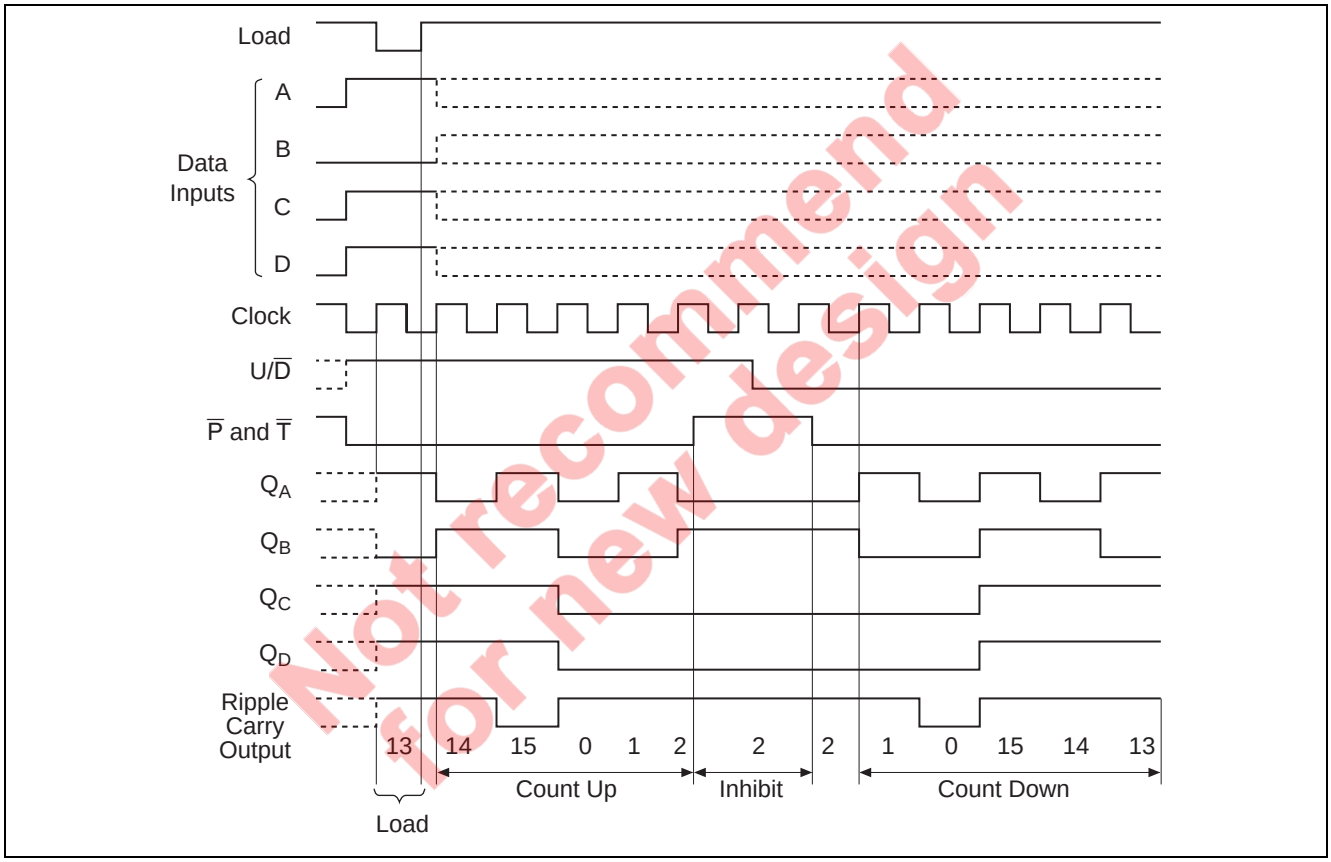
** I_{CC} is measured after applying a momentary 4.5 V, then ground, to clock input with all other inputs grounded the outputs open.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

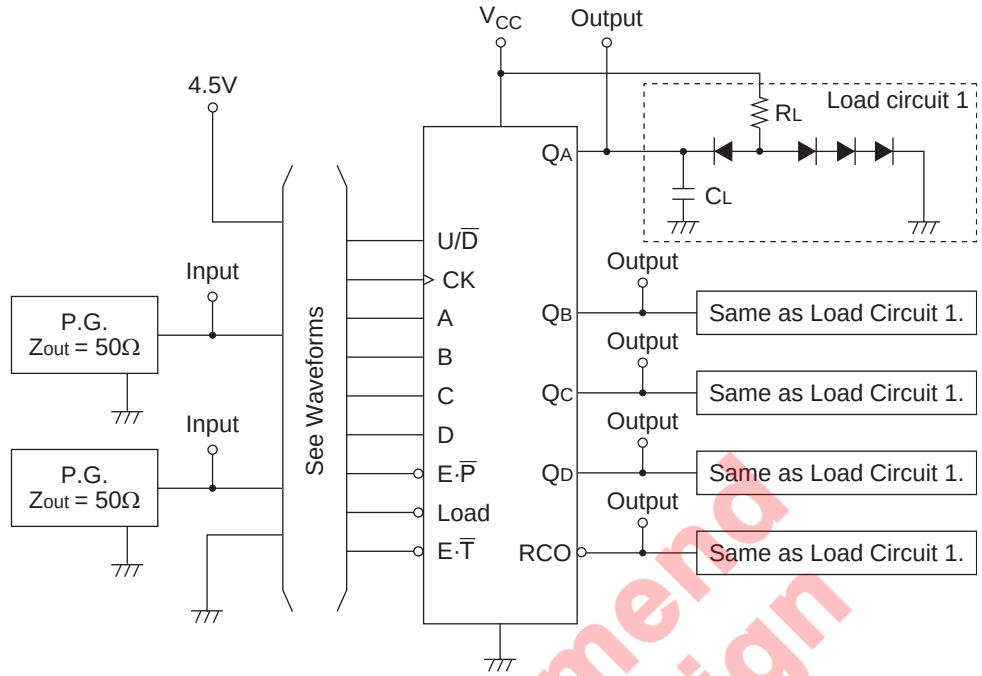
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	32	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clock	Ripple Carry	—	26	40	ns	
	t_{PHL}			—	40	60		
	t_{PLH}	Clock	Q_A to Q_D	—	18	27	ns	
	t_{PHL}			—	18	27		
	t_{PLH}	Enable $\overline{T}$	Ripple Carry	—	11	17	ns	
	t_{PHL}			—	29	45		
	t_{PLH}	Up/Down	Ripple Carry	—	22	35	ns	
	t_{PHL}			—	26	40		

Count Sequence



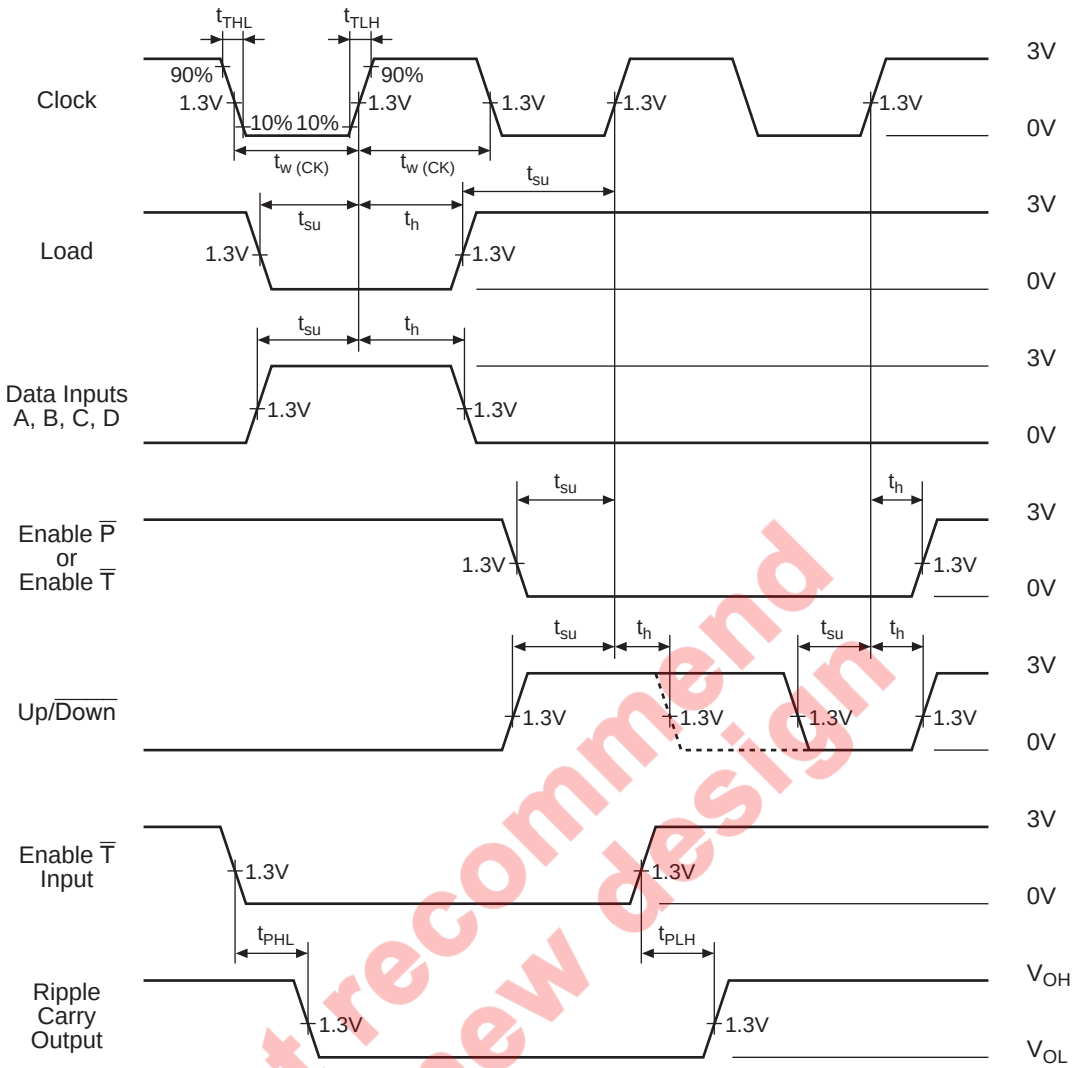
Testing Method

Test Circuit



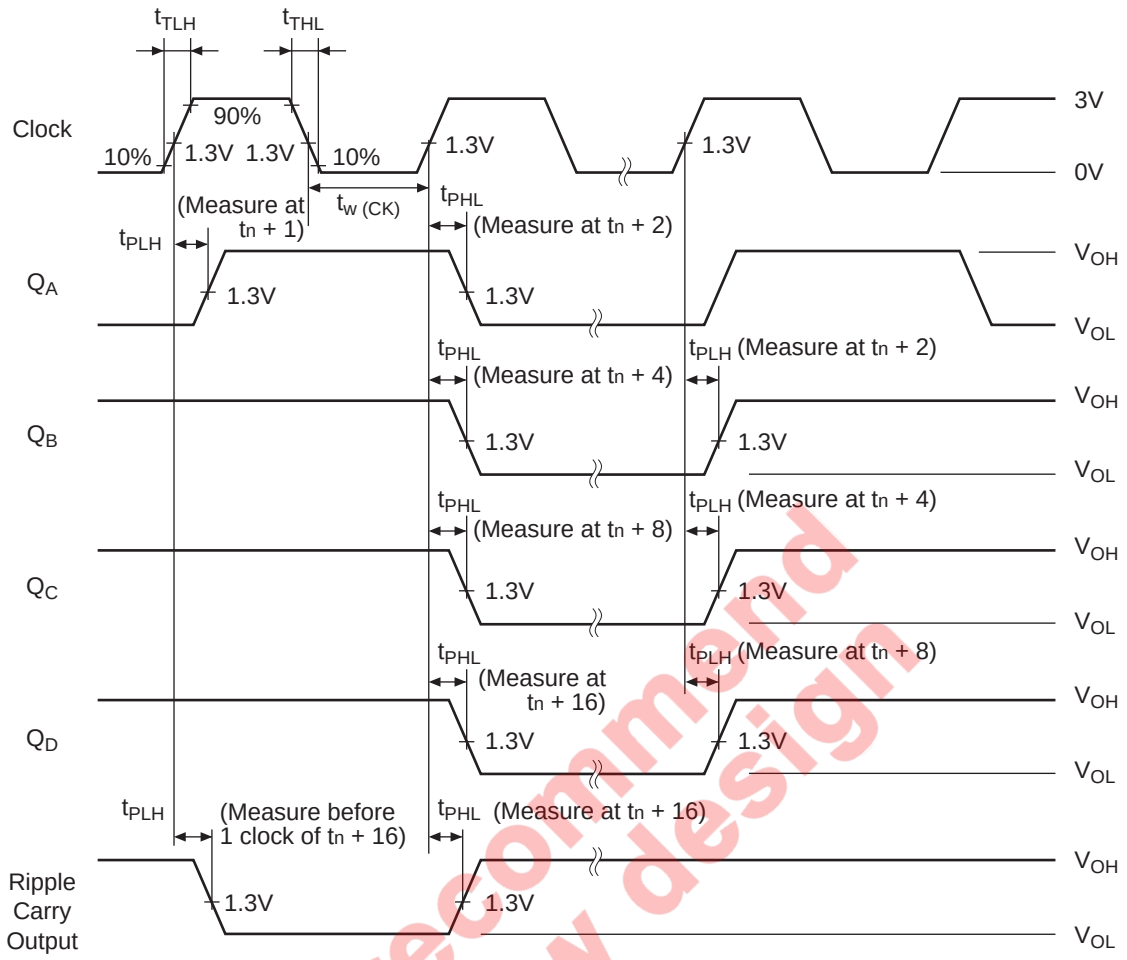
Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveforms 1



Notes:
1. t_{PLH} and t_{PHL} from enable $\overline{T}$ input to ripple carry output assume that the counter is at the maximum count (Q_A through Q_D high).
2. Propagation delay time from up / douwn to ripple carry must be measured with the counter at either aminimum or a maximum count. As the logic level of the up / down input is changed, the riiple carry output will follow. If the count is minimum (0) are ripple carry output transition will be in phase. If the count is macimum (15) the ripple carry output will be out of phase.
3. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

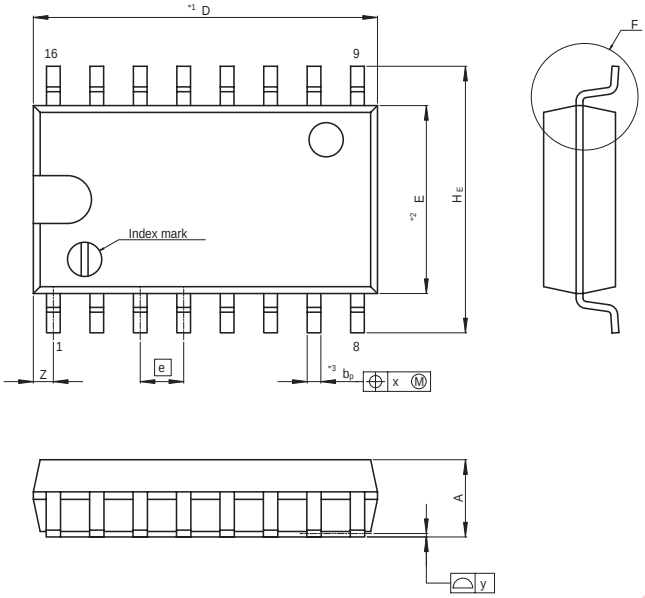
Waveforms 2



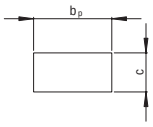
Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%.
2. For f_{max} $t_{TLH} = t_{THL} \leq 2.5$ ns.
3. t_n is the bit-time when all outputs are low.

Package Dimensions

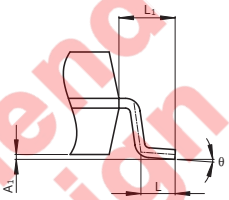
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

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http://www.renesas.com

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