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RENESAS HD74LVC125A

Quad. Bus Buffer Gates with 3-state Outputs

REJ03D0348–0400Z (Previous ADE-205-108C (Z)) Rev.4.00 Jul. 23, 2004

Description

The HD74LVC125A has four bus buffer gates in a 14 pin package. The device require the three state control input C to be taken high to put the output into the high impedance condition, whereas the device requires the control input to be low to put the output into high impedance. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0 \text{ V to } 5.5 \text{ V}$
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current $\pm 24 \text{ mA}$ (@V_{CC} = 3.0 V to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC125AFPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74LVC125ATELL	TSSOP-14 pin	TTP-14DV	Т	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs		
С	A	Outputs Y
Н	X	Z
L	L	L
L	Н	Н
LL. LBade Law		

H: High level

L: Low level

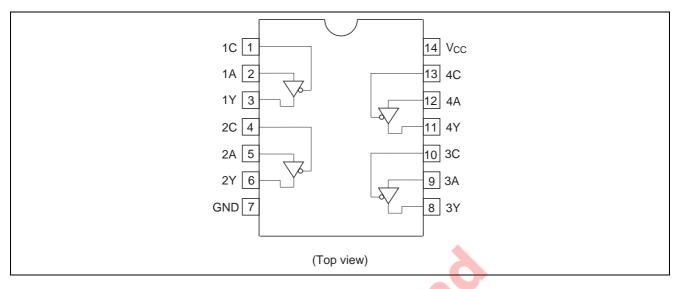
X: Immaterial

Z: High impedance



HD74LVC125A

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	A	Unit	Conditions
Supply voltage	Vcc	–0.5 to 6.0		V	
Input diode current	I _{IK}	-50		mA	$V_1 = -0.5 V$
Input voltage	VI	–0.5 to 6.0		V	
Output diode current	I _{OK}	-50		mA	$V_{\rm O} = -0.5 \ V$
		50			$V_{\rm O} = V_{\rm CC} + 0.5 \ V$
Output voltage	Vo	–0.5 to V _{CC} +0.5		V	Output "H" or "L"
		-0.5 to 6.0			Output "Z" or V _{CC} :OFF
Output current	Io 🧹	±50		mA	
V _{CC} , GND current / pin	I _{CC} or I _{GND}	±100		mA	
Storage temperature	Tstg	-65 to +150		°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	Vcc	1.5 to 5.5	V	Data hold
		2.0 to 5.5		At operation
Input / output voltage	VI	0 to 5.5	V	C, A
	Vo	0 to V _{CC}	V	Output "H" or "L"
		0 to 5.5		Output "Z" or V _{CC} :OFF
Operating temperature	Та	-40 to 85	۵°	
Output current	I _{ОН}	-12	mA	$V_{CC} = 2.7 V$
		-24 ^{*2}		V_{CC} = 3.0 V to 5.5 V
	I _{OL}	12	mA	$V_{CC} = 2.7 V$
		24 ^{*2}		V_{CC} = 3.0 V to 5.5 V
Input rise / fall time *1	t _r , t _f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

2. Duty cycle $\leq 50\%$

Electrical Characteristics

		Ta = −40 to 85°C				
Item	Symbol	V _{cc} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.7 to 3.6	2.0	A	V	
		4.5 to 5.5	V _{CC} ×0.7	-		
	V _{IL}	2.7 to 3.6	-	0.8	V	
		4.5 to 5.5		V _{CC} ×0.3		
Output voltage	V _{OH}	2.7 to 5.5	V _{cc} -0.2		V	I _{OH} = -100 μA
		2.7	2.2	-		$I_{OH} = -12 \text{ mA}$
		3.0	2.4	\sim		
		3.0	2.2	_		$I_{OH} = -24 \text{ mA}$
		4.5	3.8	_		
	V _{OL}	2.7 to 5.5	—	0.2	V	I _{OL} = 100 μA
		2.7	_	0.4		I _{OL} = 12 mA
		3.0	_	0.55		I _{OL} = 24 mA
	~ 6	4.5	_	0.55		
Input current	I _{IN}	0 to 5.5	_	±5.0	μA	$V_{IN} = 5.5 V_{CC} GND$
Off state output current	I _{IOZ}	2.7 to 5.5	—	±5.0	μΑ	$V_{IN} = V_{CC}, GND,$
						$V_{OUT} = 5.5 V \text{ or GND}$
Output leak current	I _{OFF}	0	_	20	μΑ	$V_{IN} / V_{OUT} = 5.5 V$
Quiescent supply current	I _{CC}	2.7 to 3.6	_	±10	μΑ	V_{IN} / V_{OUT} = 3.6 to 5.5 V
		2.7 to 5.5	_	10		$V_{IN} = V_{CC}$ or GND
	ΔI_{CC}	3.0 to 3.6	_	500	μA	V_{IN} = one input at (V _{CC} -0.6) V,
						other inputs at V_{CC} or GND

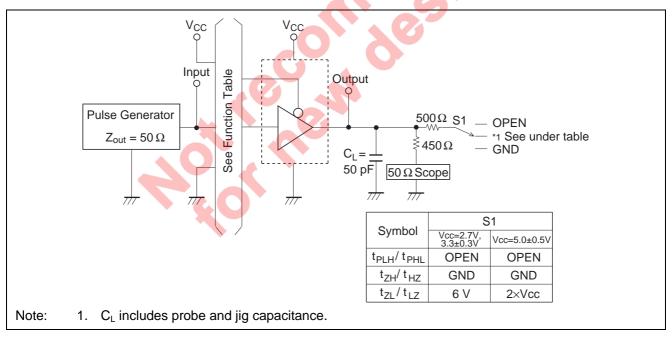
Switching Characteristics

			Ta = -40 to 85°C				From	То
Item	Symbol	V _{cc} (V)	Min	Тур	Мах	Unit	(Input)	(Output)
Propagation delay time	t _{PLH}	2.7	_		6.5	ns	А	Y
	t _{PHL}	3.3±0.3	1.5		6.0			
		5.0±0.5	_		5.0			
Output enable time	t _{ZH}	2.7	_		8.0	ns	С	Y
	t _{ZL}	3.3±0.3	1.5		7.0			
		5.0±0.5	_		6.0			
Output disable time	t _{HZ}	2.7	_		6.5	ns	С	Y
	t _{LZ}	3.3±0.3	1.5		5.5			
		5.0±0.5	_		4.5			
Between output pins skew	^{*1} t _{OSLH}	2.7	_		_	ns		
	t _{OSHL}	3.3±0.3	_		1.0			
		5.0±0.5	_		1.0			
Input capacitance	CIN	2.7	_	3.0	—	pF		
Output capacitance	Co	2.7	_	15.0		pF		

Note: 1. This parameter is characterized but not tested.

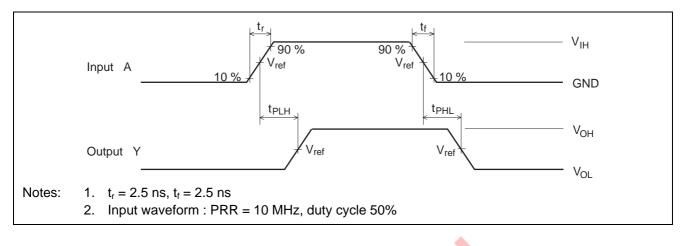
 $tos_{LH} = |t_{PLHm} - t_{PLHn}|, tos_{HL} = |t_{PHLm} - t_{PHLn}|$

Test Circuit

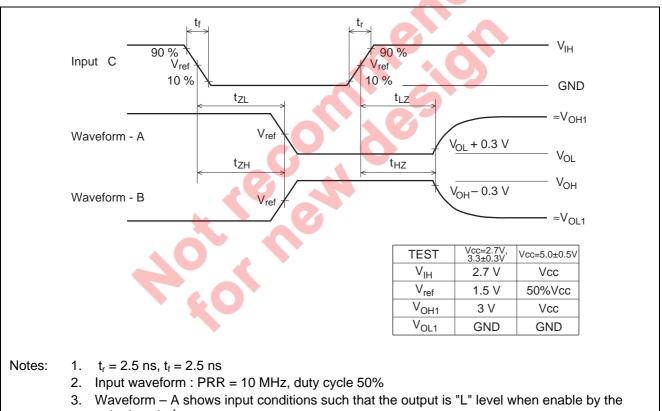


HD74LVC125A

Waveforms - 1

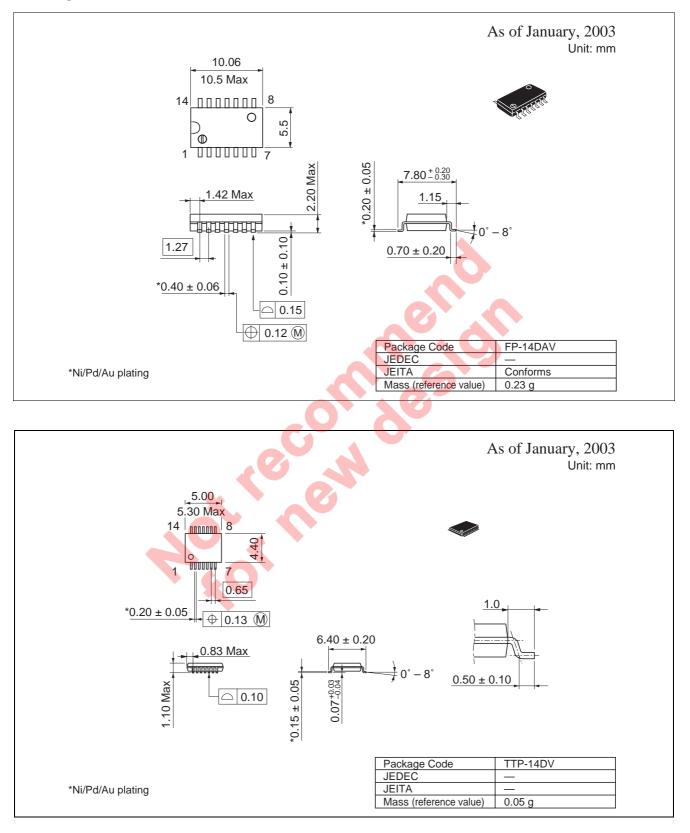


Waveforms - 2



- output control.
- 4. Waveform B shows input conditions such that the output is "H" level when enable by the output control.

Package Dimensions





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