To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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# HD74LVCZ244A

## Octal Buffers / Line Drivers with 3–state Outputs

REJ03D0371–0300
(Previous ADE-205-230A (Z))
Rev.3.00
Aug. 18, 2004

### Description

The HD74LVCZ244A has eight line drivers with three state outputs in a 20 pin package. This device is a noninverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls four buffers.

When $V_{CC}$ is between 0 and 1.5 V, the device is in the high impedance state during power up or power down.

Low voltage and high-speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC}$ = 2.7 to 5.5 V
- All inputs $V_{IH}$ (Max) = 5.5 V (@$V_{CC}$ = 0 to 5.5 V)
- All outputs $V_O$ (Max) = 5.5 V (@$V_{CC}$ = 0 V or output off state)
- Typical $V_{OL}$ ground bounce < 0.8 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- Typical $V_{OH}$ undershoot > 2.0 V (@$V_{CC}$ = 3.3 V, Ta = 25°C)
- High impedance state during power up and power down
- Power off disables outputs, permitting live insertion
- High output current ±24 mA (@$V_{CC}$ = 3.0 to 5.5 V)
- Ordering Information

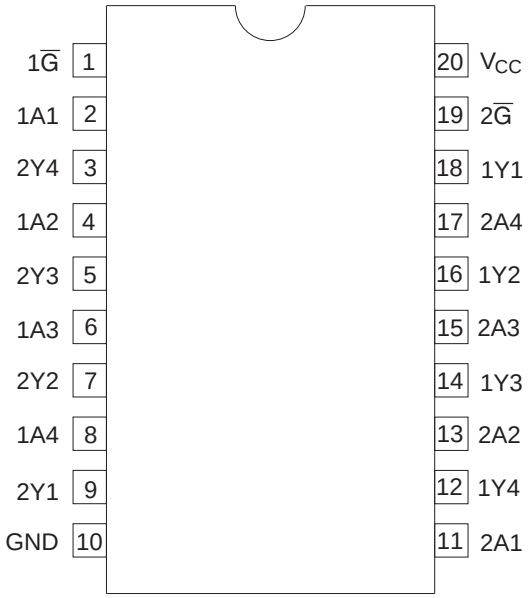
| Part Name | Package Type | Package Code | Package Abbreviation | Taping Abbreviation (Quantity) |
|---|---|---|---|---|
| HD74LVCZ244AFPEL | SOP–20 pin (JEITA) | FP–20DAV | FP | EL (2,000 pcs/reel) |
| HD74LVCZ244ATELL | TSSOP–20 pin | TTP–20DAV | T | ELL (2,000 pcs/reel) |

### Function Table

| Inputs | | |
|---|---|---|
| $\overline{G}$ | A | Output Y |
| H | X | Z |
| L | H | H |
| L | L | L |

H: High level
L: Low level
X: Immaterial
Z: High impedance

## Pin Arrangement




(Top view)

## Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | –0.5 to 7.0 | V | |
| Input voltage | $V_I$ | –0.5 to 7.0 | V | |
| Output voltage | $V_O$ | –0.5 to 7.0 | V | Output “Z” or $V_{CC}$ : OFF |
| | | –0.5 to $V_{CC}$+0.5 | | Output “H” or “L” |
| Input diode current | $I_{IK}$ | –50 | mA | $V_I$ < 0 |
| Output diode current | $I_{OK}$ | –50 | mA | $V_O$ < 0 |
| Output current | $I_O$ | ±50 | mA | |
| $V_{CC}$, GND current | $I_{CC}$ or $I_{GND}$ | ±100 | mA | |
| Storage temperature | Tstg | –65 to 150 | °C | |

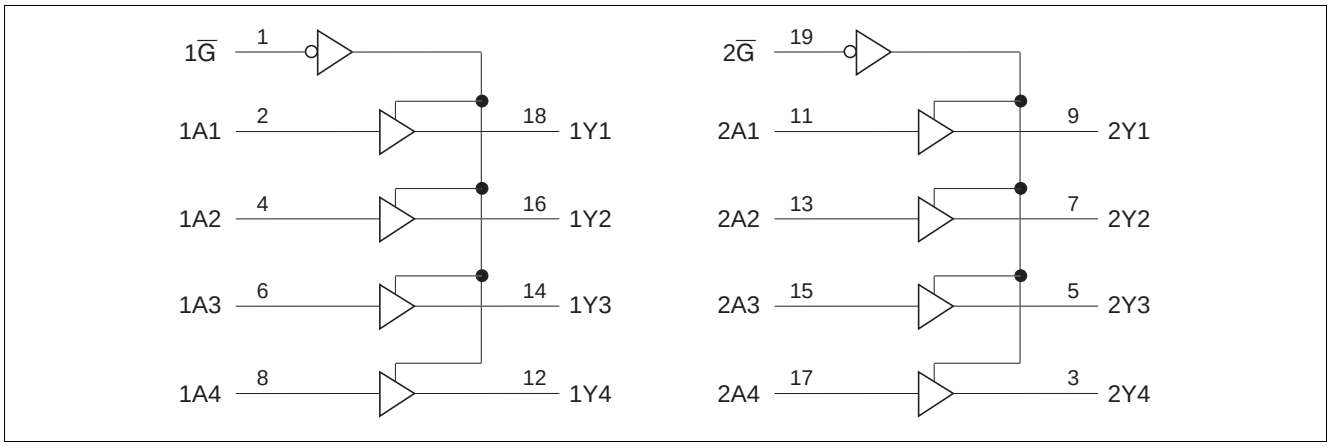
Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

| Item | Symbol | Ratings | Unit | Conditions |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.7 to 5.5 | V | At operation |
| Input voltage | $V_I$ | 0 to 5.5 | V | |
| Output voltage | $V_O$ | 0 to 5.5 | V | Output “Z” or $V_{CC}$ : OFF |
| | | 0 to $V_{CC}$ | | Output “H” or “L” |
| Output current | $I_{OH}$ | –12 | mA | $V_{CC}$ = 2.7 V |
| | | –24 *1 | | $V_{CC}$ = 3.0 to 5.5 V |
| | $I_{OL}$ | 12 | mA | $V_{CC}$ = 2.7 V |
| | | 24 *1 | | $V_{CC}$ = 3.0 to 5.5 V |
| Input rise / fall time | $t_r$, $t_f$ | 0 to 6 | ns / V | |
| Operating temperature | Ta | –40 to +85 | °C | |

Note: 1. Duty cycle ≤ 50%

## Logic Diagram



## Electrical Characteristics

(Ta = –40 to 85°C)

| Item | Symbol | $V_{CC}$ (V) | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input voltage | $V_{IH}$ | 2.7 to 3.6 | 2.0 | — | — | V | |
| | | 4.5 to 5.5 | $V_{CC}$×0.7 | — | — | | |
| | $V_{IL}$ | 2.7 to 3.6 | — | — | 0.8 | V | |
| | | 4.5 to 5.5 | — | — | $V_{CC}$×0.3 | | |
| Output voltage | $V_{OH}$ | 2.7 to 5.5 | $V_{CC}$–0.2 | — | — | V | $I_{OH}$ = –100 µA |
| | | 2.7 | 2.2 | — | — | | $I_{OH}$ = –12 mA |
| | | 3.0 | 2.4 | — | — | | |
| | | 3.0 | 2.2 | — | — | | $I_{OH}$ = –24 mA |
| | | 4.5 | 3.8 | — | — | | |
| | $V_{OL}$ | 2.7 to 5.5 | — | — | 0.2 | V | $I_{OL}$ = 100 µA |
| | | 2.7 | — | — | 0.4 | | $I_{OL}$ = 12 mA |
| | | 3.0 | — | — | 0.55 | | $I_{OL}$ = 24 mA |
| | | 4.5 | — | — | 0.55 | | |
| Input current | $I_{IN}$ | 0 to 5.5 | — | — | ±5 | µA | $V_{IN}$ = 0 to 5.5 V |
| Off state output current | $I_{OZ}$ | 2.7 to 5.5 | — | — | ±5 | µA | $V_{OUT}$ = 0 to 5.5 V |
| | $I_{OZPU}$ | 0 to 1.5 | — | — | ±5 | | $V_{OUT}$ = 0.5 to 5.5 V, |
| | $I_{OZPD}$ | 1.5 to 0 | — | — | ±5 | | Output enable = don't care |
| Output leak current | $I_{OFF}$ | 0 | — | — | ±5 | µA | $V_{IN}$ or $V_O$ = 5.5 V |
| Quiescent supply current | $I_{CC}$ | 2.7 to 3.6 | — | — | 225 | µA | $V_{IN}$ = 3.6 to 5.5 V [*1], $I_O$ = 0 |
| | | 2.7 to 5.5 | — | — | 350 | | $V_{IN}$ = $V_{CC}$ or GND |
| | $\Delta I_{CC}$ | 2.7 to 3.6 | — | — | 500 | µA | $V_{IN}$ = one input at ($V_{CC}$–0.6) V, other inputs at $V_{CC}$ or GND |
| Input capacitance | $C_{IN}$ | 3.3 | — | 3.4 | — | pF | $V_{IN}$ = $V_{CC}$ or GND |
| Output capacitance | $C_O$ | 3.3 | — | 7.5 | — | pF | $V_{OUT}$ = $V_{CC}$ or GND |

Note: 1. This applies in the disabled state only.

## Switching Characteristics

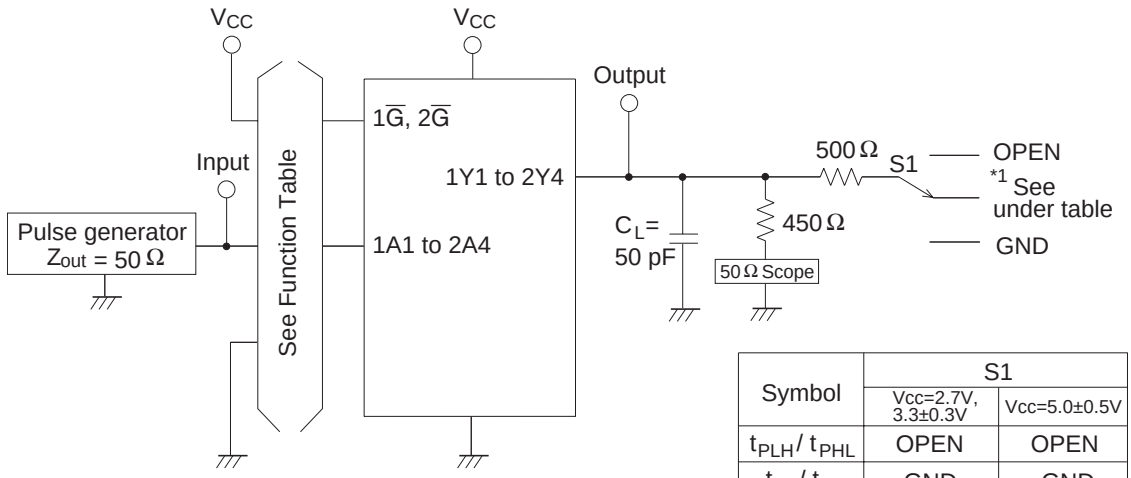
(Ta = –40 to 85°C)

| Item | Symbol | $V_{CC}$ (V) | Min | Typ | Max | Unit | FROM (Input) | TO (Output) |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time | $t_{PLH}$ | 2.7 | — | — | 6.9 | ns | A | Y |
| | $t_{PHL}$ | 3.3±0.3 | 1.5 | — | 5.9 | | | |
| | | 5.0±0.5 | — | — | 4.5 | | | |
| Output enable time | $t_{ZH}$ | 2.7 | — | — | 8.6 | ns | $\overline{G}$ | Y |
| | $t_{ZL}$ | 3.3±0.3 | 1.5 | — | 7.6 | | | |
| | | 5.0±0.5 | — | — | 6.1 | | | |
| Output disable time | $t_{HZ}$ | 2.7 | — | — | 6.8 | ns | $\overline{G}$ | Y |
| | $t_{LZ}$ | 3.3±0.3 | 1.5 | — | 6.5 | | | |
| | | 5.0±0.5 | — | — | 5.5 | | | |
| Between output pin skew [*1] | $t_{OSLH}$ | 2.7 | — | — | — | ns | | |
| | $t_{OSHL}$ | 3.3±0.3 | — | — | 1.0 | | | |
| | | 5.0±0.5 | — | — | 1.0 | | | |

Note: 1. This parameter is characterized but not tested.

$t_{OSLH} = |t_{PLHm} – t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} – t_{PHLn}|$

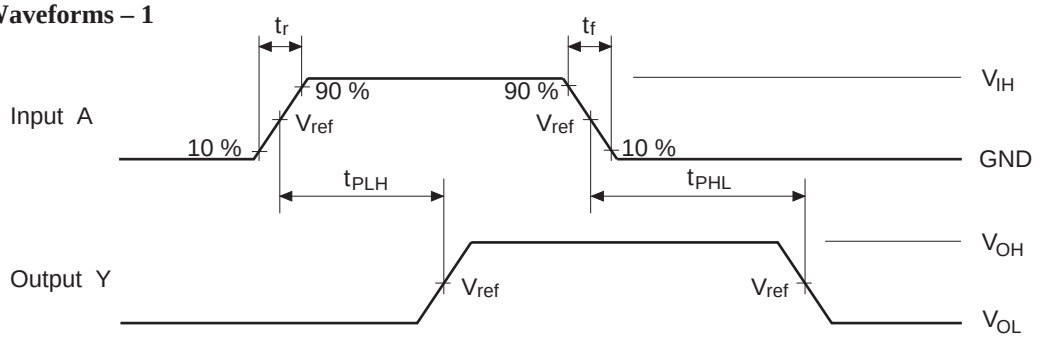
## Test Circuit



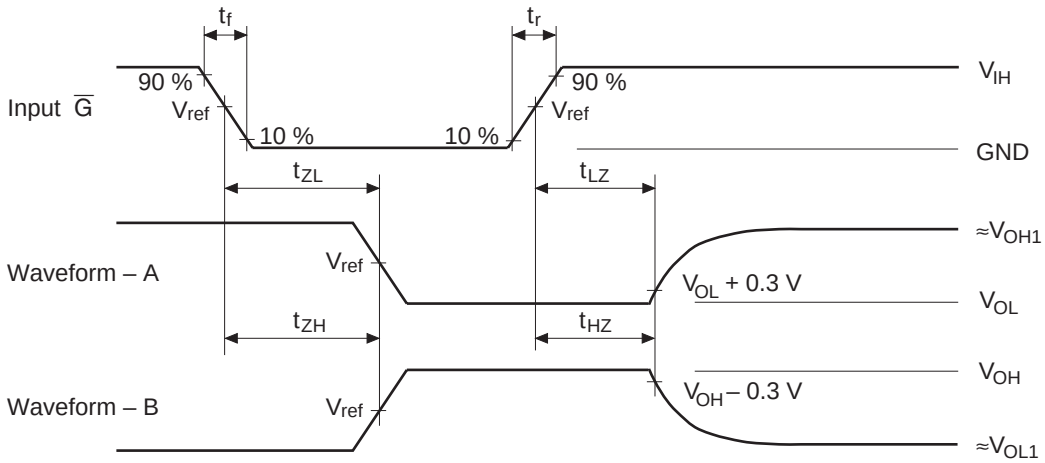

| Symbol | S1 | |
|---|---|---|
| | Vcc=2.7V, 3.3±0.3V | Vcc=5.0±0.5V |
| $t_{PLH}$ / $t_{PHL}$ | OPEN | OPEN |
| $t_{ZH}$ / $t_{HZ}$ | GND | GND |
| $t_{ZL}$ / $t_{LZ}$ | 6 V | 2×$V_{CC}$ |

Note: 1. $C_L$ includes probe and jig capacitance.

• **Waveforms – 1**



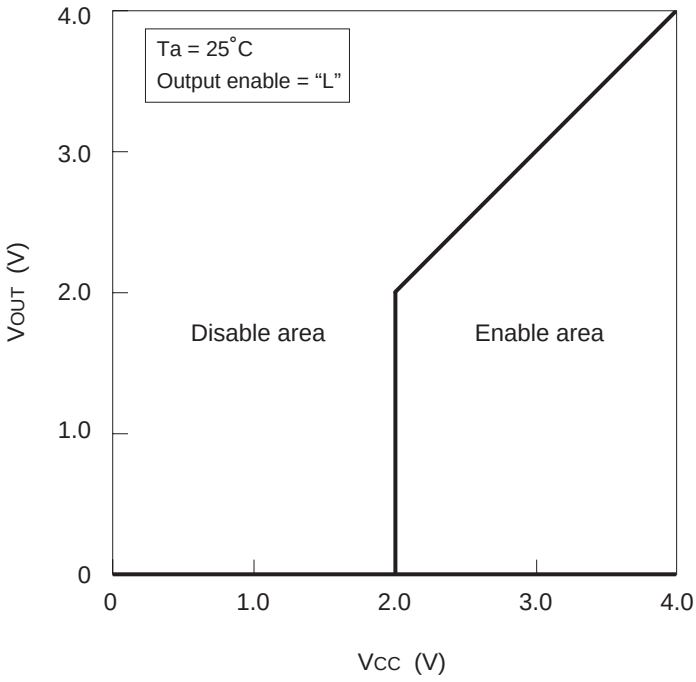

• **Waveforms – 2**




| TEST | Vcc=2.7V, 3.3±0.3V | Vcc=5.0±0.5V |
|---|---|---|
| $V_{IH}$ | 2.7 V | $V_{CC}$ |
| $V_{ref}$ | 1.5 V | 50%$V_{CC}$ |
| $V_{OH1}$ | 3 V | $V_{CC}$ |
| $V_{OL1}$ | GND | GND |

Notes: 1. Input waveform : PRR = 10 MHz, duty cycle 50%, $t_r$ = 2.5 ns, $t_f$ = 2.5 ns
2. Waveform – A shows input conditions such that the output is “L” level when enabled by the output control.
3. Waveform – B shows input conditions such that the output is “H” level when enabled by the output control.

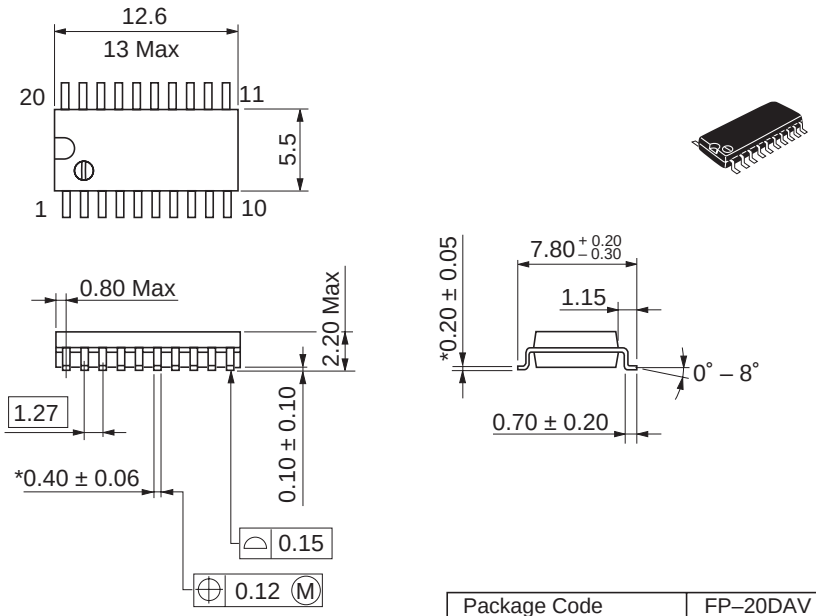
## Power up / down Characteristics



## Package Dimensions

As of January, 2002

Unit: mm

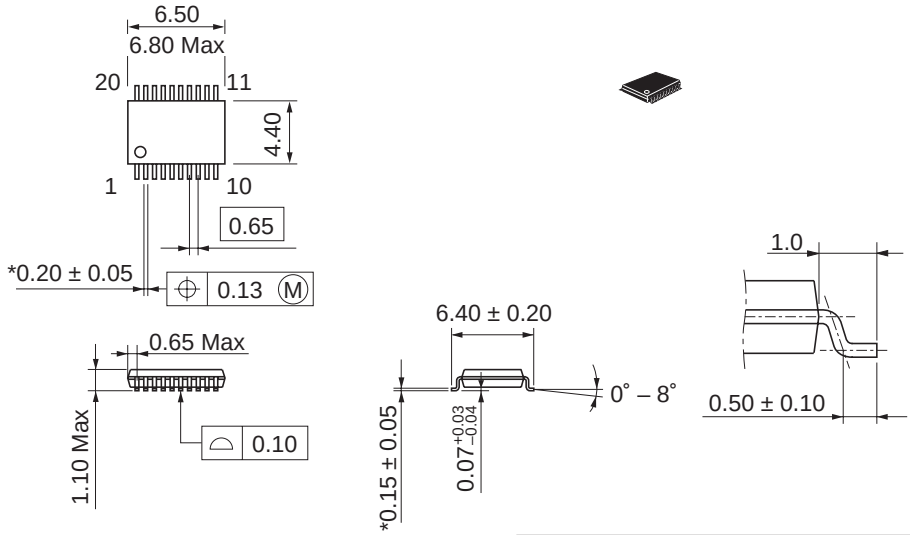



*Pd plating

| | |
|---|---|
| Package Code | FP–20DAV |
| JEDEC | — |
| JEITA | Conforms |
| Mass (reference value) | 0.31 g |

As of January, 2002

Unit: mm




*Pd plating

| | |
|---|---|
| Package Code | TTP–20DAV |
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 0.07 g |

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