

## HIP2100

100V/2A Peak, Low Cost, High Frequency Half Bridge Driver

FN4022  
Rev.16.00  
Aug 8, 2019

The [HIP2100](#) is a high frequency, 100V Half Bridge N-Channel power MOSFET driver IC. The low-side and high-side gate drivers are independently controlled and matched to 8ns. This gives the user maximum flexibility in dead-time selection and driver protocol. Undervoltage protection on both the low-side and high-side supplies force the outputs low. An on-chip diode eliminates the discrete diode required with other driver ICs. A new level-shifter topology yields the low-power benefits of pulsed operation with the safety of DC operation. Unlike some competitors, the high-side output returns to its correct state after a momentary undervoltage of the high-side supply.

### Applications

- Telecom Half Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters

### Related Literature

For a full list of related documents, visit our website:

- [HIP2100](#) device page

### Features

- Drives N-Channel MOSFET Half Bridge
- SOIC, EPSONIC, and QFN Package Options
- SOIC and EPSONIC Packages Compliant with 100V Conductor Spacing Guidelines of IPC-2221
- Pb-Free (RoHS Compliant)
- Bootstrap Supply Max Voltage to 114VDC
- On-Chip 1 $\Omega$  Bootstrap Diode
- Fast Propagation Times for Multi-MHz Circuits
- Drives 1000pF Load with Rise and Fall Times Typ 10ns
- CMOS Input Thresholds for Improved Noise Immunity
- Independent Inputs for Non-Half Bridge Topologies
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground, or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Range
- Supply Undervoltage Protection
- 3 $\Omega$  Driver Output Resistance
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220
  - QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, which Improves PCB Efficiency and has a Thinner Profile

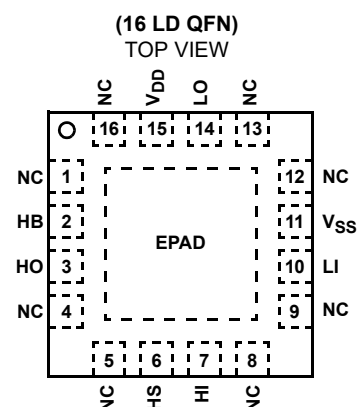
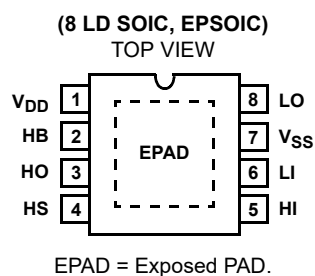
## Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
HIP2100IBZ	2100 IBZ	-40 to +125	-	8 Ld SOIC	M8.15
HIP2100IBZT	2100 IBZ	-40 to +125	2.5k	8 Ld SOIC	M8.15
HIP2100EIBZ	2100 EIBZ	-40 to +125	-	8 Ld EPSOIC	M8.15C
HIP2100EIBZT	2100 EIBZ	-40 to +125	2.5k	8 Ld EPSOIC	M8.15C
HIP2100IRZ	HIP 2100IRZ	-40 to +125	-	16 Ld 5x5 QFN	L16.5x5
HIP2100IRZT	HIP 2100IRZ	-40 to +125	6k	16 Ld 5x5 QFN	L16.5x5
HIP2100EVAL2	Evaluation Board				

### NOTES:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [HIP2100](#) device page. For more information about MSL, see [TB363](#).

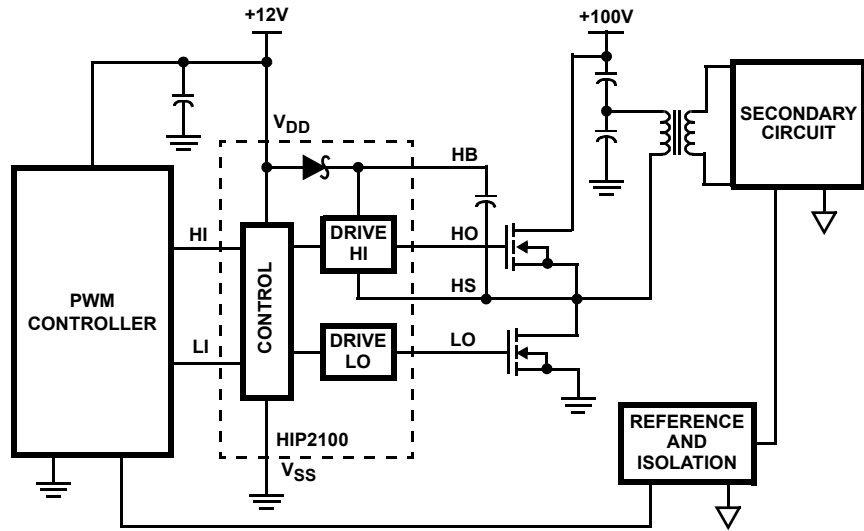
## Pinouts



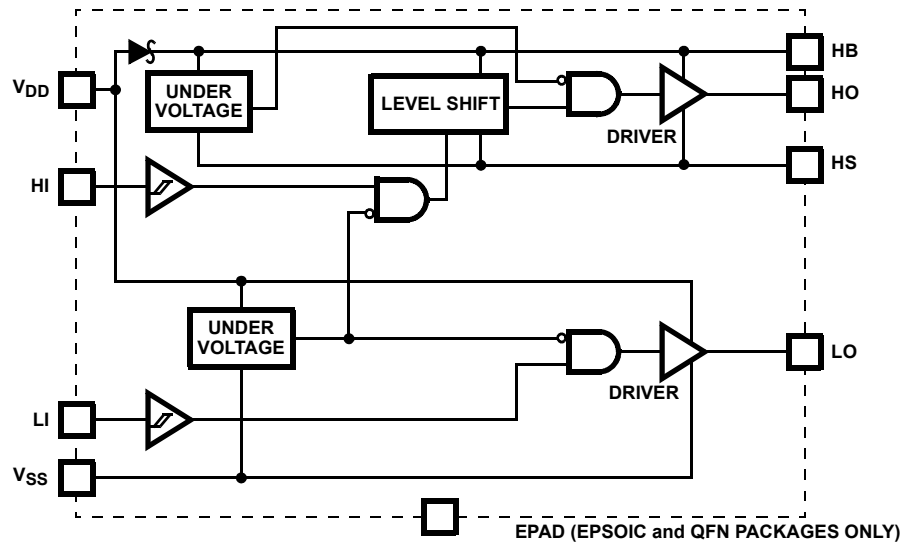
## Pin Descriptions

SYMBOL	DESCRIPTION
V <sub>DD</sub>	Positive Supply to lower gate drivers. De-couple this pin to V <sub>SS</sub> . Bootstrap diode connected to HB.
HB	High-Side Bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip.
HO	High-Side Output. Connect to gate of High-Side power MOSFET.
HS	High-Side Source connection. Connect to source of High-Side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	High-Side input.
LI	Low-Side input.
V <sub>SS</sub>	Chip negative supply, generally will be ground.
LO	Low-Side Output. Connect to gate of Low-Side power MOSFET.
EPAD	Exposed Pad. Connect to ground or float. The EPAD is electrically isolated from all other pins.

**Application Block Diagram**



**Functional Block Diagram**



\*EPAD = Exposed Pad. The EPAD is electrically isolated from all other pins. For best thermal performance connect the EPAD to the PCB power ground plane.

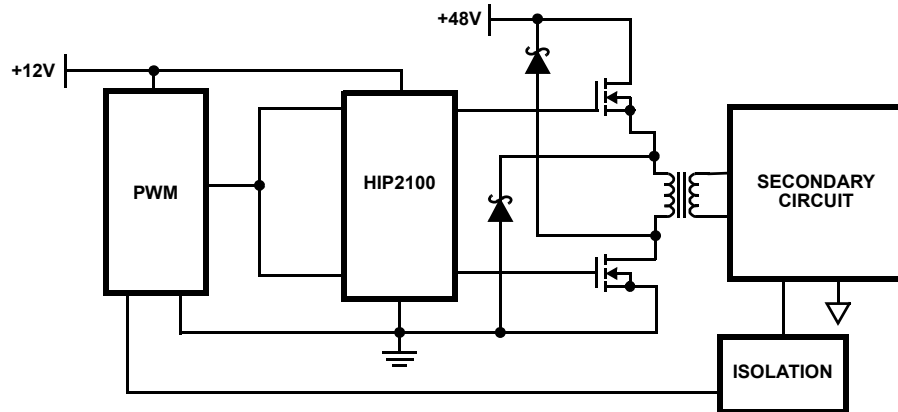


FIGURE 1. TWO-SWITCH FORWARD CONVERTER

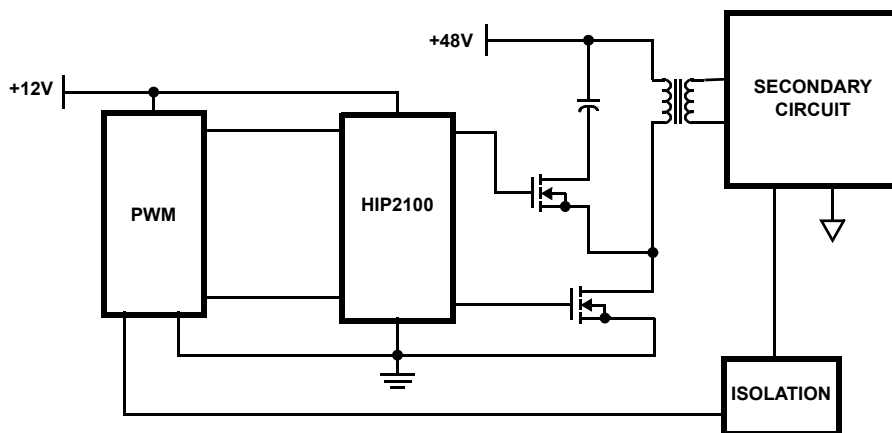


FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE CLAMP

**Absolute Maximum Ratings**

Supply Voltage, $V_{DD}$ , $V_{HB}$ - $V_{HS}$ (Notes 4, 5)	-0.3V to 18V
LI and HI Voltages (Note 5)	-0.3V to $V_{DD}$ +0.3V
Voltage on LO (Note 4)	-0.3V to $V_{DD}$ +0.3V
Voltage on HO (Note 4)	$V_{HS}$ -0.3V to $V_{HB}$ +0.3V
Voltage on HS (Continuous) (Note 4)	-1V to 110V
Voltage on HB (Note 4)	+118V
Average Current in $V_{DD}$ to HB diode	100mA
ESD Classification	Class 1 (1kV)

**Maximum Recommended Operating Conditions**

Supply Voltage, $V_{DD}$	+9V to 14.0VDC
Voltage on HS	-1V to 100V
Voltage on HS (Repetitive Transient)	-5V to 105V
Voltage on HB	$V_{HS}$ +8V to $V_{HS}$ +14.0V and $V_{DD}$ -1V to $V_{DD}$ +100V
HS Slew Rate	<50V/ns

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- The HIP2100 is capable of derated operation at supply voltages exceeding 14V. [Figure 16 on page 9](#) shows the high-side voltage derating curve for this mode of operation.
- All voltages referenced to  $V_{SS}$  unless otherwise specified.
- $\theta_{JA}$  is measured with the component mounted on a high-effective thermal conductivity test board in free air. See [TB379](#) for details.
- $\theta_{JA}$  is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features.  $\theta_{JC}$ , the "case temp" is measured at the center of the exposed metal pad on the package underside. See [TB379](#) for details.

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
SOIC (Note 6)	95	50
EPSONIC (Note 7)	40	3.0
QFN (Note 7)	37	6.5
Max Power Dissipation at +25°C in Free Air (SOIC, Note 6)	1.3W	
Max Power Dissipation at +25°C in Free Air (EPSONIC, Note 7)	3.1W	
Max Power Dissipation at +25°C in Free Air (QFN, Note 7)	3.3W	
Storage Temperature Range	-65°C to +150°C	
Junction Temperature Range	-55°C to +150°C	
Pb-Free Reflow Profile	see <a href="#">TB493</a>	

**Electrical Specifications**  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, unless otherwise specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C TO } +125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN (Note 8)	MAX (Note 8)	
<b>SUPPLY CURRENTS</b>								
$V_{DD}$ Quiescent Current	$I_{DD}$	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
$V_{DD}$ Operating Current	$I_{DDO}$	f = 500kHz	-	1.5	2.5	-	3	mA
Total HB Quiescent Current	$I_{HB}$	LI = HI = 0V	-	0.1	0.15	-	0.2	mA
Total HB Operating Current	$I_{HBO}$	f = 500kHz	-	1.5	2.5	-	3	mA
HB to $V_{SS}$ Current, Quiescent	$I_{HBS}$	$V_{HS} = V_{HB} = 114V$	-	0.05	1	-	10	$\mu\text{A}$
HB to $V_{SS}$ Current, Operating	$I_{HBSO}$	f = 500kHz	-	0.7	-	-	-	mA
<b>INPUT PINS</b>								
Low Level Input Voltage Threshold	$V_{IL}$		4	5.4	-	3	-	V
High Level Input Voltage Threshold	$V_{IH}$		-	5.8	7	-	8	V
Input Voltage Hysteresis	$V_{IHYS}$		-	0.4	-	-	-	V
Input Pulldown Resistance	$R_I$		-	200	-	100	500	k $\Omega$
<b>UNDERVOLTAGE PROTECTION</b>								
$V_{DD}$ Rising Threshold	$V_{DDR}$		7	7.3	7.8	6.5	8	V
$V_{DD}$ Threshold Hysteresis	$V_{DDH}$		-	0.5	-	-	-	V
HB Rising Threshold	$V_{HBR}$		6.5	6.9	7.5	6	8	V
HB Threshold Hysteresis	$V_{HBH}$		-	0.4	-	-	-	V

**Electrical Specifications**  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, unless otherwise specified. (Continued)

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C TO } +125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN (Note 8)	MAX (Note 8)	
<b>BOOT STRAP DIODE</b>								
Low-Current Forward Voltage	$V_{DL}$	$I_{VDD-HB} = 100\mu\text{A}$	-	0.45	0.55	-	0.7	V
High-Current Forward Voltage	$V_{DH}$	$I_{VDD-HB} = 100\text{mA}$	-	0.7	0.8	-	1	V
Dynamic Resistance	$R_D$	$I_{VDD-HB} = 100\text{mA}$	-	0.8	1	-	1.5	$\Omega$
<b>LO GATE DRIVER</b>								
Low Level Output Voltage	$V_{OLL}$	$I_{LO} = 100\text{mA}$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	$V_{OHL}$	$I_{LO} = -100\text{mA}$ , $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	$I_{OHL}$	$V_{LO} = 0V$	-	2	-	-	-	A
Peak Pulldown Current	$I_{OLL}$	$V_{LO} = 12V$	-	2	-	-	-	A
<b>HO GATE DRIVER</b>								
Low Level Output Voltage	$V_{OLH}$	$I_{HO} = 100\text{mA}$	-	0.25	0.3	-	0.4	V
High Level Output Voltage	$V_{OHH}$	$I_{HO} = -100\text{mA}$ , $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.3	-	0.4	V
Peak Pullup Current	$I_{OHH}$	$V_{HO} = 0V$	-	2	-	-	-	A
Peak Pulldown Current	$I_{OLH}$	$V_{HO} = 12V$	-	2	-	-	-	A

**Switching Specifications**  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO, unless otherwise specified.

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = +25^\circ\text{C}$			$T_J = -40^\circ\text{C TO } +125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN (Note 8)	MAX (Note 8)	
Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	$t_{LPHL}$		-	20	35	-	45	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	$t_{HPHL}$		-	20	35	-	45	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	$t_{LPLH}$		-	20	35	-	45	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	$t_{HPLH}$		-	20	35	-	45	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	$t_{MON}$		-	2	8	-	10	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	$t_{MOFF}$		-	2	8	-	10	ns
Either Output Rise/Fall Time	$t_{RC}$ , $t_{FC}$	$C_L = 1000\text{pF}$	-	10	-	-	-	ns
Either Output Rise/Fall Time (3V to 9V)	$t_R$ , $t_F$	$C_L = 0.1\mu\text{F}$	-	0.5	0.6	-	0.8	$\mu\text{s}$
Either Output Rise Time Driving DMOS	$t_{RD}$	$C_L = \text{IRFR120}$	-	20	-	-	-	ns
Either Output Fall Time Driving DMOS	$t_{FD}$	$C_L = \text{IRFR120}$	-	10	-	-	-	ns
Minimum Input Pulse Width that Changes the Output	$t_{PW}$		-	-	-	-	50	ns
Bootstrap Diode Turn-On or Turn-Off Time	$t_{BS}$		-	10	-	-	-	ns

## NOTE:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

**Timing Diagrams**

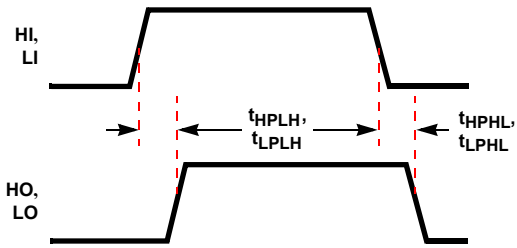


FIGURE 3.

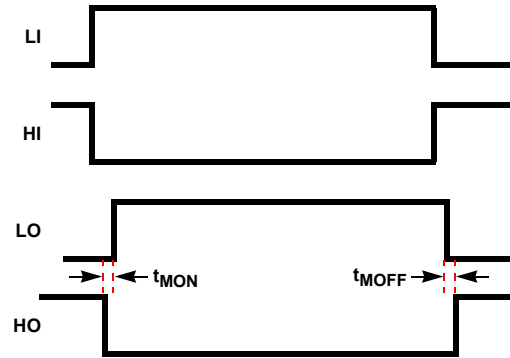


FIGURE 4.

**Typical Performance Curves**

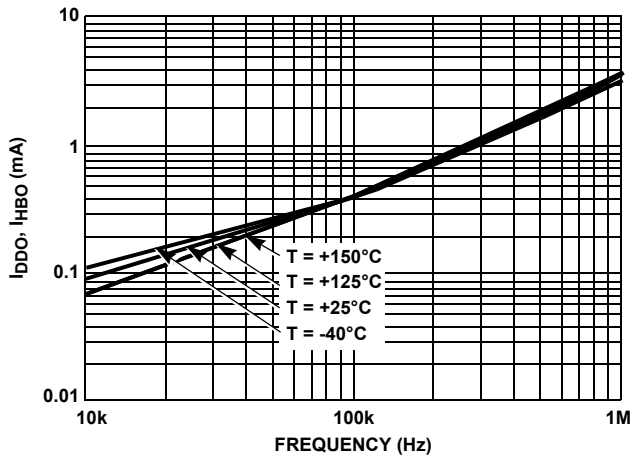


FIGURE 5. OPERATING CURRENT vs FREQUENCY

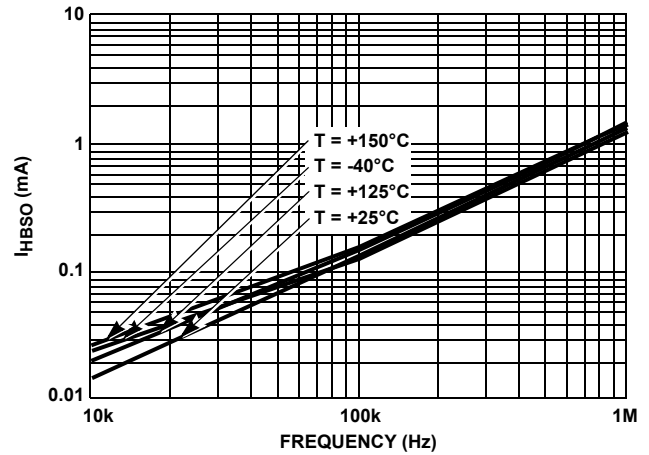


FIGURE 6. HB TO V<sub>SS</sub> OPERATING CURRENT vs FREQUENCY

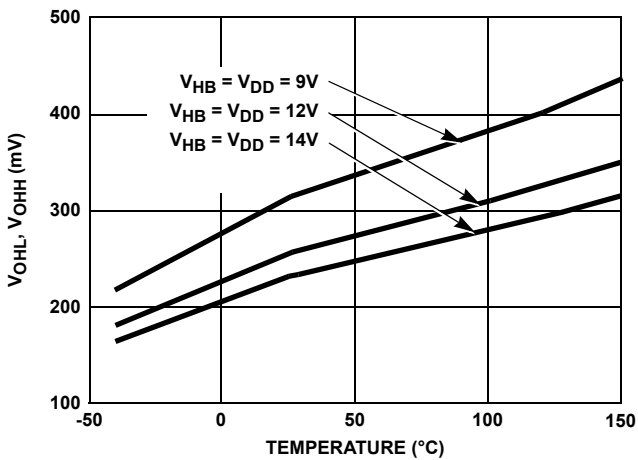


FIGURE 7. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

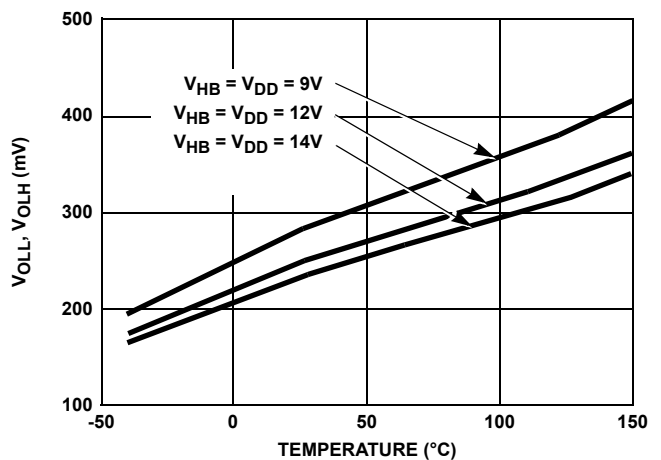
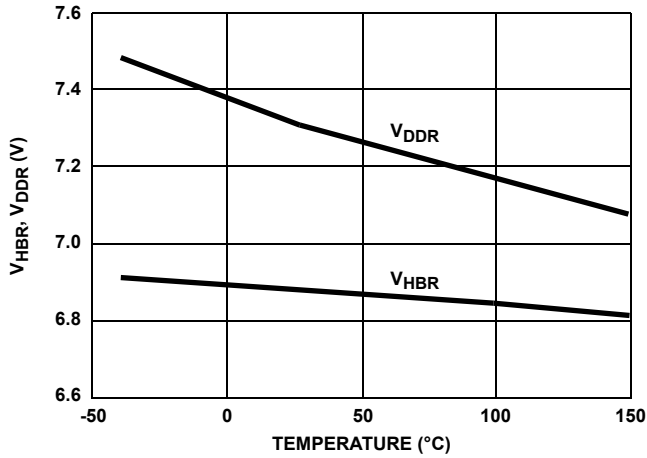
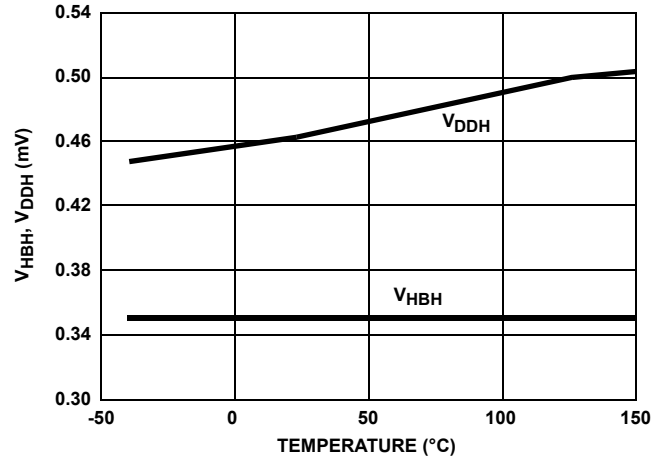


FIGURE 8. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

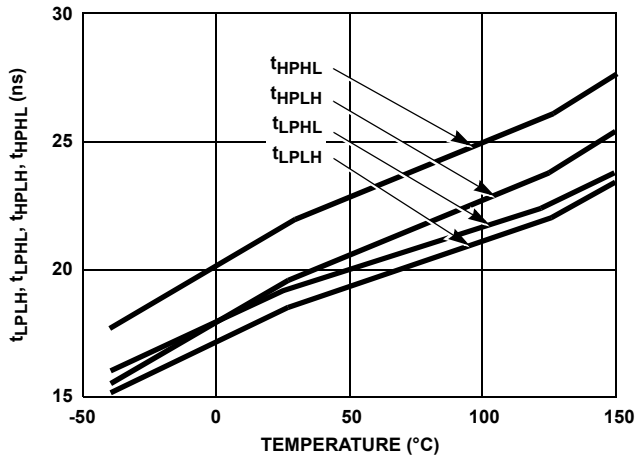
**Typical Performance Curves** (Continued)



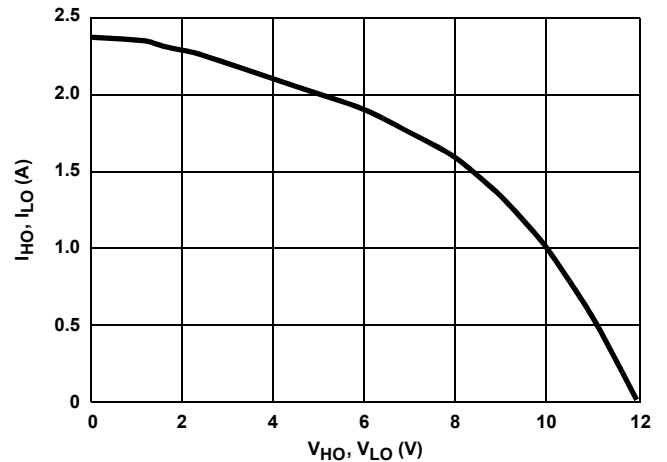
**FIGURE 9. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE**



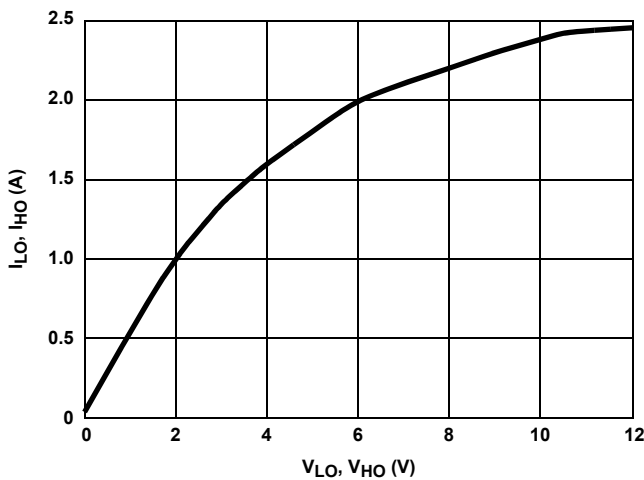
**FIGURE 10. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE**



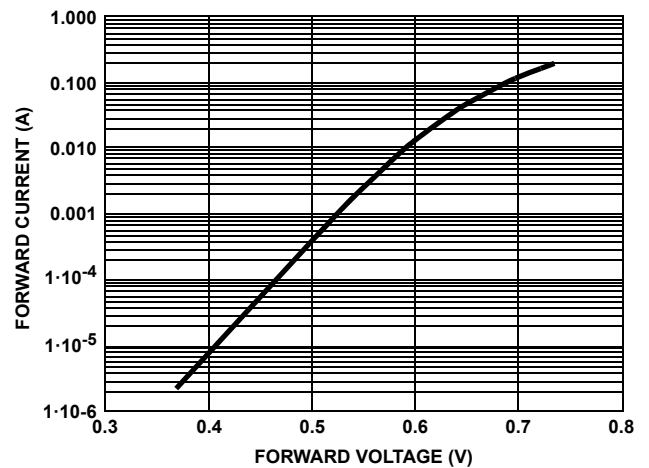
**FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE**



**FIGURE 12. PEAK PULLUP CURRENT vs OUTPUT VOLTAGE**



**FIGURE 13. PEAK PULLDOWN CURRENT vs OUTPUT VOLTAGE**



**FIGURE 14. BOOTSTRAP DIODE I-V CHARACTERISTICS**



**Typical Performance Curves** (Continued)

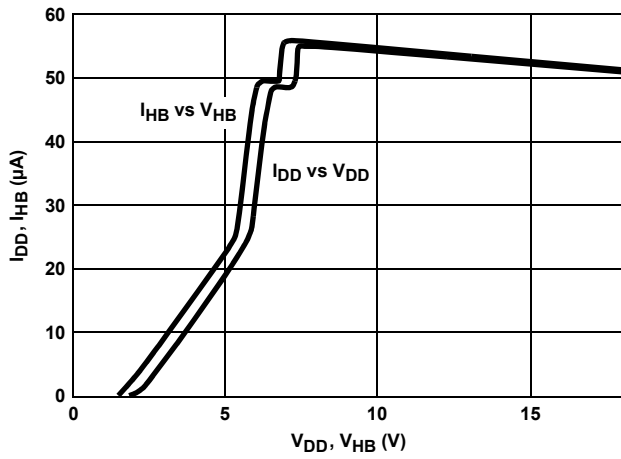


FIGURE 15. QUIESCENT CURRENT vs VOLTAGE

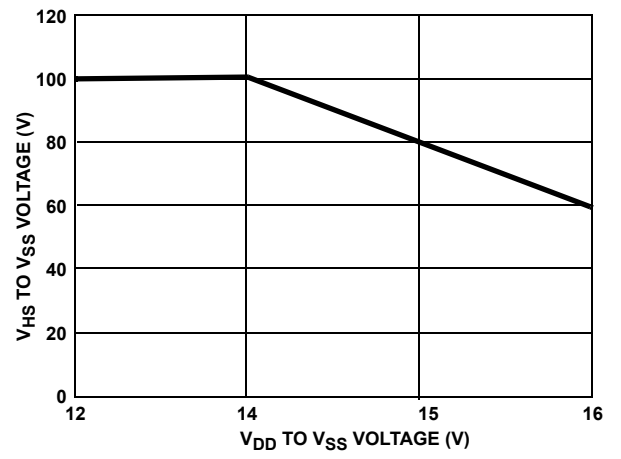


FIGURE 16. V<sub>HS</sub> VOLTAGE vs V<sub>DD</sub> VOLTAGE

## Revision History

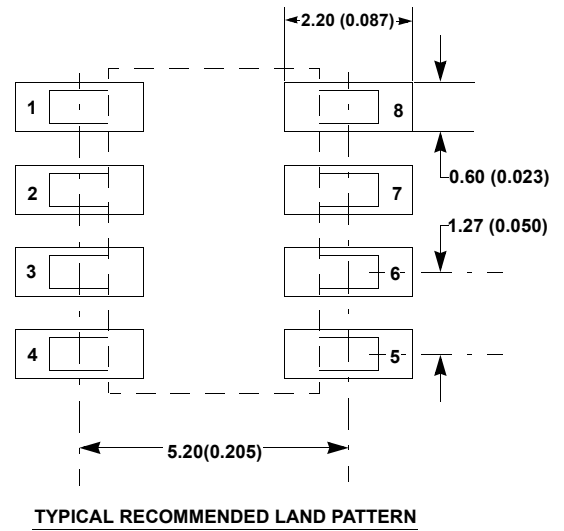
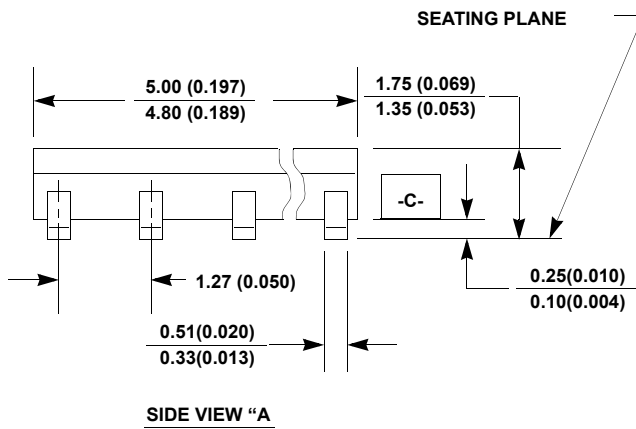
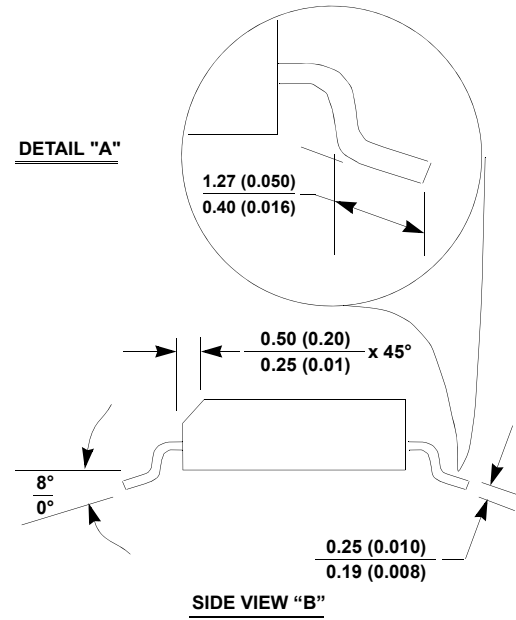
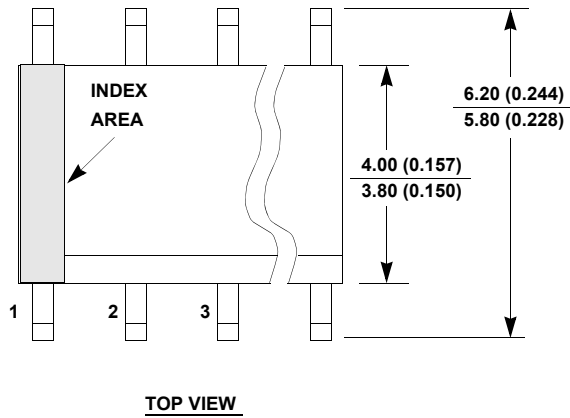
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Aug 8, 2019	FN4022.16	<p>Added Related Literature</p> <p>Updated Links throughout.</p> <p>Updated Ordering Information table by removing retired parts, adding tape and reel information, and adding Note 3.</p> <p>Removed all information for DFN package.</p> <p>Removed About Intersil section.</p> <p>Updated disclaimer</p> <p>Updated POD M8.15C to the latest revision changes are as follows:</p> <ul style="list-style-type: none"> <li>-Updated Millimeter MIN and MAX values for A from: 1.43 MIN and 1.68 MAX to: 1.422 MIN and 1.700 MAX</li> <li>-Updated Inch MAX for A from: 0.066 to: 0.067</li> <li>-A1 Inches changed MIN from: 0.001 to 0.0, and A1 Millimeters MIN from 0.03 to 0.0</li> <li>-L Millimeter Min changed from: 0.41 to 0.406</li> </ul>
Aug 31, 2015	FN4022.15	<p>Updated Ordering Information Table on page 2.</p> <p>Added Revision History and About Intersil sections.</p> <p>Updated POD M8.15 from rev 1 to rev 4. Changes since rev 1:</p> <p>Updated to new format by removing table, moving dimensions onto drawing and adding land pattern Typical Recommended Land Pattern, changed the following:</p> <ul style="list-style-type: none"> <li>2.41(0.095) to 2.20(0.087)</li> <li>0.76 (0.030) to 0.60(0.023)</li> <li>0.200 to 5.20(0.205)</li> </ul> <p>Changed Note 1 "1982" to "1994"</p>

**Package Outline Drawings**

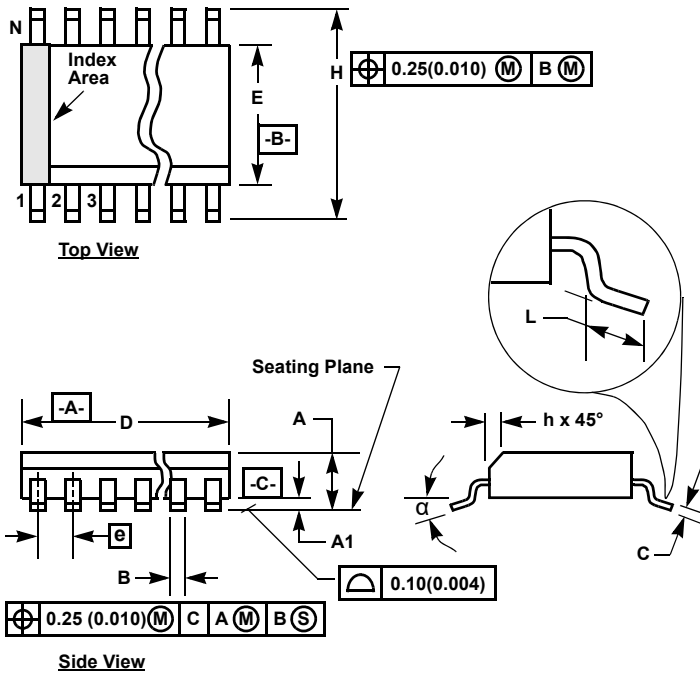
For the most recent package outline drawing, see [M8.15](#).

**M8.15**  
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**  
 Rev 4, 1/12



**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.



M8.15C  
8 Lead Narrow Body Small Outline Exposed Pad  
Plastic Package (EPSOIC)

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.056	0.067	1.422	1.700	-
A1	0.0	0.005	0.0	0.13	-
B	0.0138	0.0192	0.35	0.49	9
C	0.0075	0.0098	0.19	0.25	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.811	3.99	4
e	0.050 BSC		1.27 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.406	0.89	6
N	8		8		7
$\alpha$	0°	8°	0°	8°	-
P	-	0.126	-	3.200	11
P1	-	0.099	-	2.514	11

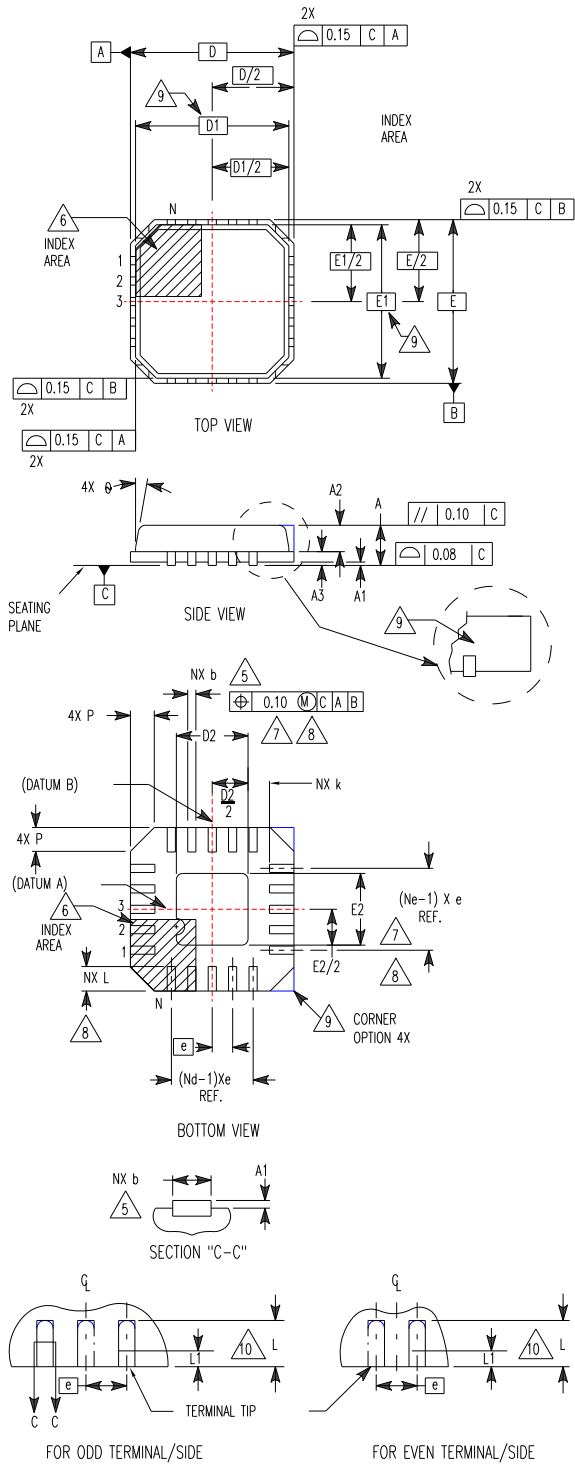
Rev. 2 5/19

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion, and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: Millimeter. Converted inch dimensions are not necessarily exact.
11. Dimensions "P" and "P1" are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.

For the most recent package outline drawing, see [L16.5x5](#).

L16.5x5  
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (QFN)  
(COMPLIANT TO JEDEC MO-220VHBB ISSUE C)



SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.28	0.33	0.40	5, 8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.55	2.70	2.85	7, 8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.55	2.70	2.85	7, 8
e	0.80 BSC			-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N	16			2
Nd	4			3
Ne	4	4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
  3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
    - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
    - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
  6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
  11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.