HS-1135RH

Radiation Hardened, High Speed, Low Power Current Feedback Amplifier with Programmable Output Limiting

The HS-1135RH is a radiation hardened, high speed, low power current feedback amplifier built with the Renesas proprietary complementary bipolar UHF-1 (DI bonded wafer) process. They are QML approved and processed in full compliance with MIL-PRF-38535. This amplifier features user programmable output limiting, via the V_H and V_L pins.

The HS-1135RH is the ideal choice for high speed, low power applications requiring output limiting (such as flash A/D drivers), especially those requiring fast overdrive recovery times. The limiting function allows the designer to set the maximum and minimum output levels to protect downstream stages from damage or input saturation. The sub-nanosecond overdrive recovery time ensures a quick return to linear operation following an overdrive condition.

Component and composite video systems also benefit from this op amp's performance, as indicated by the gain flatness, and differential gain and phase specifications.

Features

- Electrically Screened to SMD #5962-96767
- QML Qualified per MIL-PRF-38535 Requirements
- User Programmable Output Voltage Limiting
- Fast Overdrive Recovery: <1ns (Typ)
- Low Supply Current: 6.9mA (Typ)
- Wide -3dB Bandwidth: 360MHz (Typ)
- High Slew Rate: 1200V/µs (Typ)
- High Input Impedance: 2MΩ (Typ)
- Excellent Gain Flatness (to 50MHz): ±0.07dB (Typ)
- TID Rad Hard Assurance (RHA) testing
  - HDR (50-300rad(Si)/s): 300krad(Si)
- Latch Up: None (DI Technology)

Applications

- Flash A/D Driver
- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Imaging Systems

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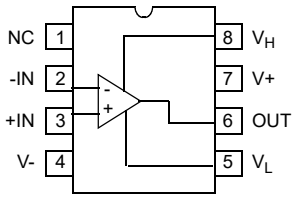
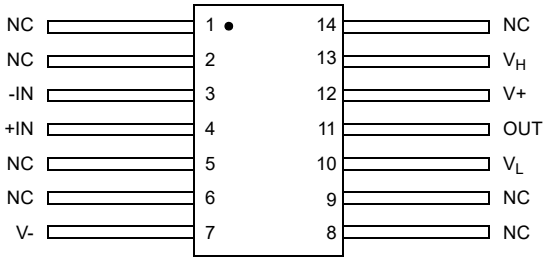
1. Pin Information

1.1 Pin Assignments



GDIP1-T8 (CERDIP)
OR CDIP2-TI (SBDIP)
TOP VIEW



CDFP3-F14 (FLATPACK)
TOP VIEW

1.2 Pin Descriptions

Pin Number 8 Ld CERDIP	Pin Number 14 Ld Flatpack	Pin Name	Description
1	1, 2, 5, 6, 8, 9, 14	NC	No Connect
2	3	-IN	Inverting input
3	4	+IN	Non-inverting input
4	7	V-	Negative power supply
5	10	V_L	Sets the lower output clamping level.
6	11	OUT	Amplifier output
7	12	V+	Positive power supply
8	13	V_H	Sets the upper output clamping level.

2. Clamp Operation

2.1 General

The HS-1135RH features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

2.2 Clamp Circuitry

Figure 1 shows a simplified schematic of the HS-1135RH input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of (V_{-IN} - V_{OUT})/R_F. This current is mirrored onto the high impedance node (Z) by Q_{X3}-Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current (-I_{BIAS}) required to keep the output at the final voltage.

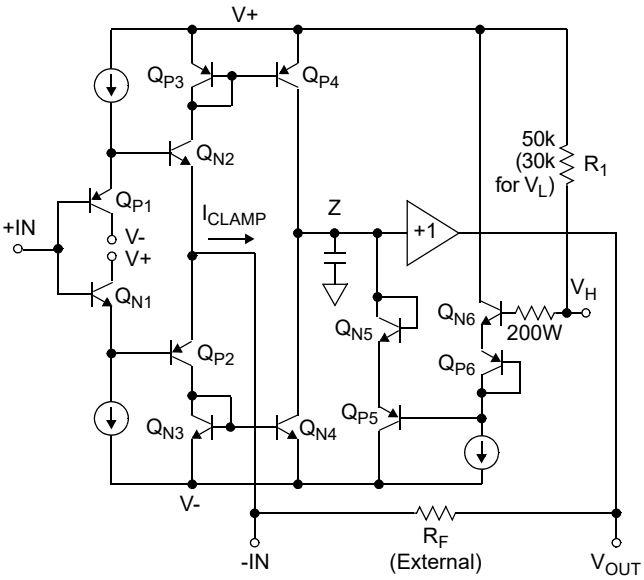


Figure 1. Simplified V_H Clamp Circuitry

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5. QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H. R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as (V_{-IN} - V_{OUT})/R_F . As an example, a unity gain circuit with V_{IN} = 2V, V_H = 1V, and R_F = 510Ω would have I_{CLAMP} = (2-1)/510Ω = 1.96mA. Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

2.3 Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors always ran at the same current level, there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (V_{-IN} -$V_{OUTCLAMPED}$) and R_F, so clamp accuracy degrades as the overdrive increases, or as R_F decreases. As an example, the specified accuracy of ±60mV for a 2X overdrive with R_F = 510Ω degrades to ±220mV for R_F = 240Ω at the same overdrive, or to ±250mV for a 3X overdrive with R_F = 510Ω.

Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity.

2.4 Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HS-1135RH could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150 - 200mV AC signal will still be present at the output.

2.5 Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of Unclamped Performance and Clamped Performance highlight the HS-1135RH's sub nanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 4.0ns for the unclamped pulse, and 4.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. *Note*: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HS-1135RH propagation delay is 500ps.

3. Use of Die in Hybrid Applications

This amplifier is designed with compensation to negate the package parasitics that typically lead to instabilities. As a result, the use of die in hybrid applications results in overcompensated performance due to lower parasitic capacitances. Reducing R_F below the recommended values for packaged units will solve the problem. For A_V = +2 the recommended starting point is 300Ω, while unity gain applications should try 400Ω.

4. PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board.

IMPORTANT: The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

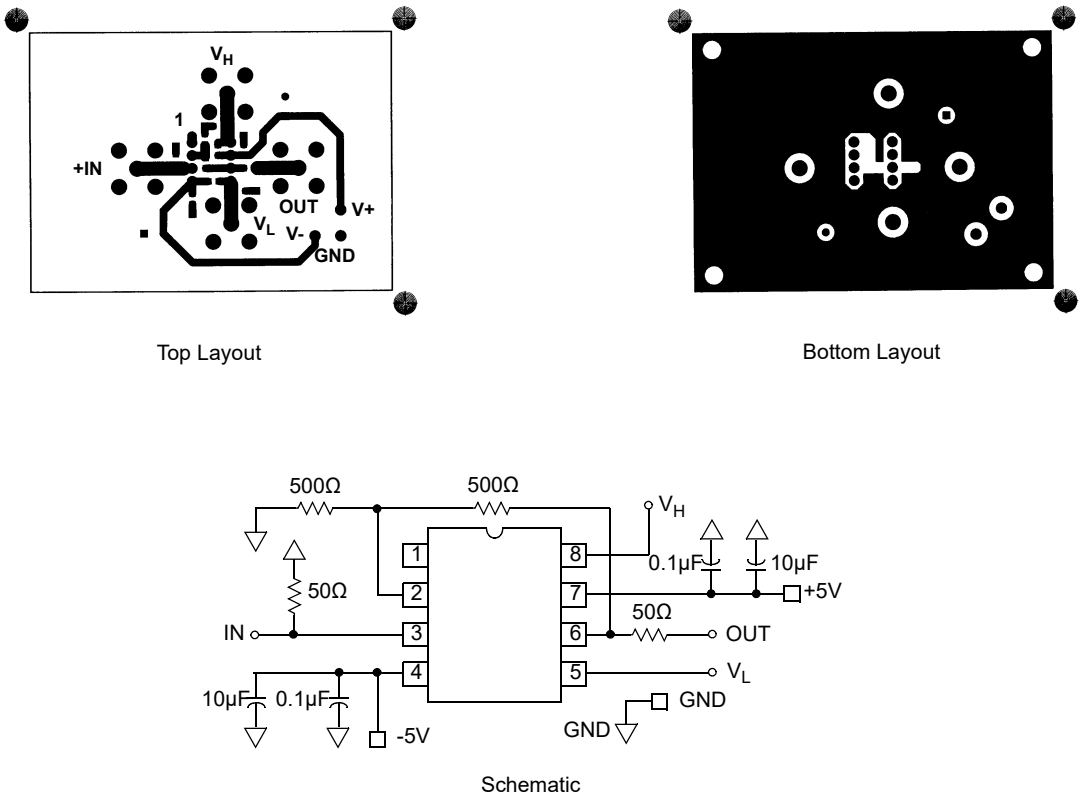
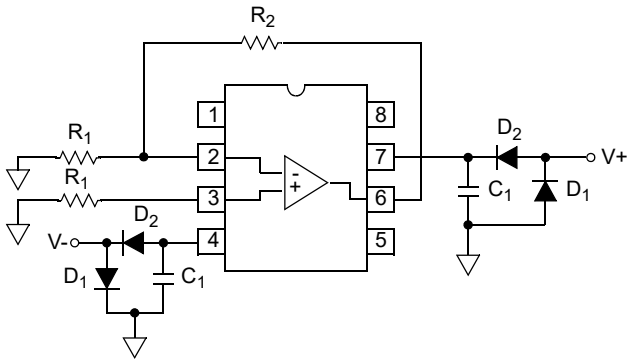


Figure 2. Evaluation Board Schematic and Layout

5. Burn-In Circuit

HS-1135RH CERDIP

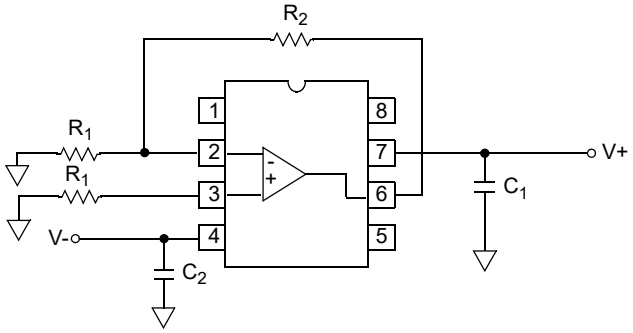


Notes:

- R_1 = 1kΩ, ±5% (Per Socket)
- R_2 = 10kΩ, ±5% (Per Socket)
- C_1 = 0.01µF (Per Socket) or 0.1µF (Per Row) Minimum
- D_1 = 1N4002 or Equivalent (Per Board)
- D_2 = 1N4002 or Equivalent (Per Socket)
- V+ = +5.5V ±0.5V
- V- = -5.5V ±0.5V

6. Irradiation Circuit

HS-1135RH CERDIP



Notes:

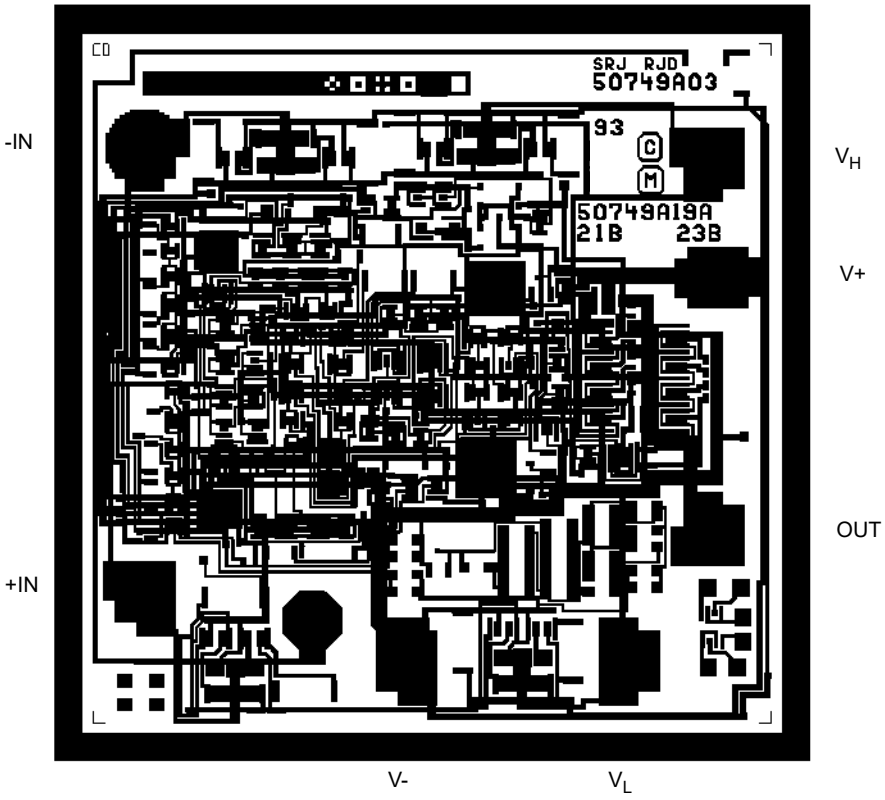
- R_1 = 1kΩ, ±5%
- R_2 = 10kΩ, ±5%
- C_1 = C_2 = 0.01µF
- V+ = +5.0V ±0.5V
- V- = -5.0V ±0.5V

7. Die and Assembly Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimension	59 mils x 58.2 mils x 19 mils ±1 mil 1500µm x 1480µm x 483µm ±25.4µm
Interface Materials	
Glassivation	Type: Nitride Thickness: 4kÅ ±0.5kÅ
Top Metallization	Type: Metal 1: AlCu(2%)/TiW Thickness: Metal 1: 8kÅ ±0.4kÅ Type: Metal 2: AlCu(2%) Thickness: Metal 2: 16kÅ ±0.8kÅ
Substrate	UHF-1, Bonded Wafer, DI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$<2\times10^5 A/cm^2$
Transistor Count	89

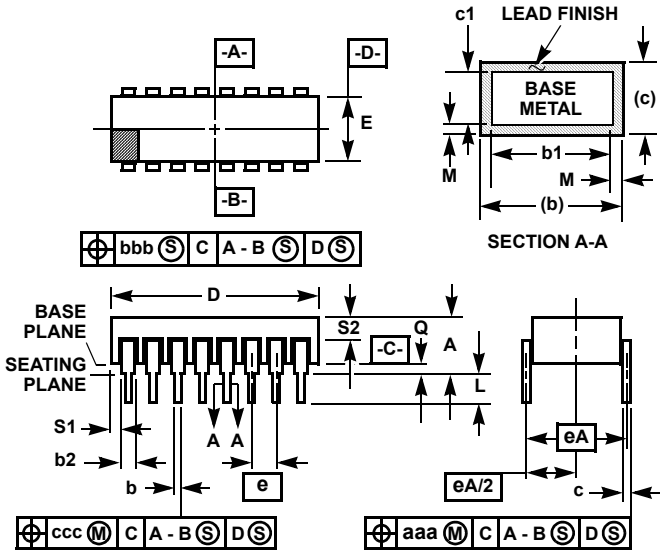
7.1 Metallization Mask Layout



8. Package Outline Drawings

For the most recent package outline drawing, see D8.3.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90º	105º	90º	105º	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

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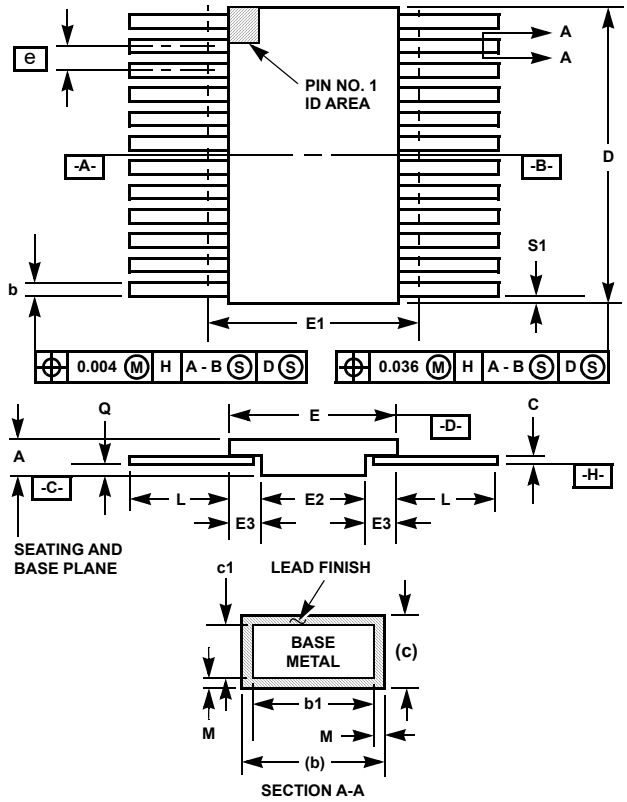
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

For the most recent package outline drawing, see K14.A.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

9. Ordering Information

SMD Ordering Number[1]	Internal Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
5962F9676701VPC	HS7B-1135RH-Q	HDR to 300krad(Si)	8 Ld SBDIP	D8.3	Tray	-55 to +125°C
5962F9676701VXC	HS9-1135RH-Q		8 Ld Flatpack	K14.A		
HS7B-1135RH/PROTO[3]	HS7B-1135RH/PROTO	N/A	8 Ld SBDIP	D8.3		
HS9-1135RH/PROTO	HS9-1135RH/PROTO		8 Ld Flatpack	K14.A		

1. SMD Ordering Note - Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

10. Revision History

Revision	Date	Description
4.00	May 1, 2024	Placed in the latest template. Updated Feature bullet. Added Pin Description table. Updated Ordering Information table. Updated PC Board Layout section. Added Revision history section.

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