HS-26C31RH, HS-26C31EH

Radiation Hardened Quad Differential Line Driver

FN3401
Rev 8.01
Aug 5, 2022

The HS-26C31RH, HS-26C31EH are quad differential line drivers designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26C31RH, HS-26C31EH accept CMOS levels and converts them to RS-422 compatible outputs. These circuits uses special outputs that enable the drivers to power-down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Detailed Electrical Specifications for these devices are contained in SMD 5962-96663. A link is provided on our homepage for downloading.

Applications

- Line transmitter for MIL-STD-1553 serial data bus
- Line Transmitter for RS422

Features

- Electrically screened to SMD #5962-96663
- QML qualified per MIL-PRF-38535 requirements
- 1.2 Micron radiation hardened CMOS
- EIA RS-422 compatible outputs (except for IOS)
- CMOS inputs
- High impedance outputs when disabled or powered down
- Low power dissipation. . . . . 2.75mW standby (max)
- Operating supply range . . . . 4.5V to 5.5V
- Low output impedance . . . . 10Ω or less
- Radiation acceptance testing - HS-26C31RH
  - HDR (50-300rad (Si)/s). . . . . 300krad(Si)
- Radiation acceptance testing - HS-26C31EH
  - HDR (50-300rad(Si)/s) . . . . 300krad(Si)
  - LDR (0.01rad(Si)/s) . . . . .50krad(Si)
- SEL immune to LET . . . . .100MeV*cm^2/mg
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

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Ordering Information

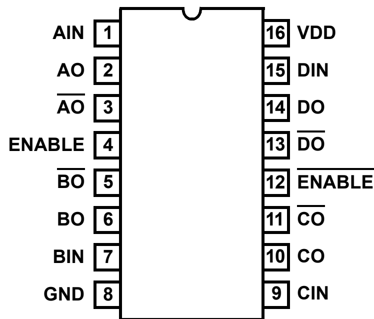
SMD Part Number (Note 1)	Part Number (Note 2)	Radiation Hardness (Total Ionizing Dose)	Package (RoHS Compliant)	Package Drawing	Carrier Type	Temp. Range
5962F9666301QEC	HS1-26C31RH-8	HDR to 300krad(Si)	16 LD SBDIP	D16.3	Tube	-55 to +125°C
5962F9666301QXC	HS9-26C31RH-8		16 LD FLATPACK	K16.A	Tray	
5962F9666301VEC	HS1-26C31RH-Q		16 LD SBDIP	D16.3	Tube	
5962F9666301VXC	HS9-26C31RH-Q		16 LD FLATPACK	K16.A	Tray	
5962F9666301V9A	HS0-26C31RH-Q (Note 3)		Die	N/A	N/A	
5962F9666301VYC	HS9G-26C31RH-Q (Notes 4, 5)		16 LD FLATPACK	K16.A	Tray	
N/A	HS1-26C31RH/PROTO (Note 5)	N/A	16 LD SBDIP	D16.3	Tube	
	HS0-26C31RH/SAMPLE (Notes 3, 5)		Die	N/A	N/A	
	HS9-26C31RH/PROTO (Note 5)		16 LD FLATPACK	K16.A	Tray	
	HS9G-26C31RH/PROTO (Notes 4, 5)		16 LD FLATPACK	K16.A	Tray	
5962F9666303VEC	HS1-26C31EH-Q	HDR to 300krad(Si) LDR to 50krad(Si)	16 LD SBDIP	D16.3	Tube	
5962F9666303VXC	HS9-26C31EH-Q		16 LD FLATPACK	K16.A	Tray	
5962F9666303V9A	HS0-26C31EH-Q (Note 3)		Die	N/A	N/A	

NOTES:

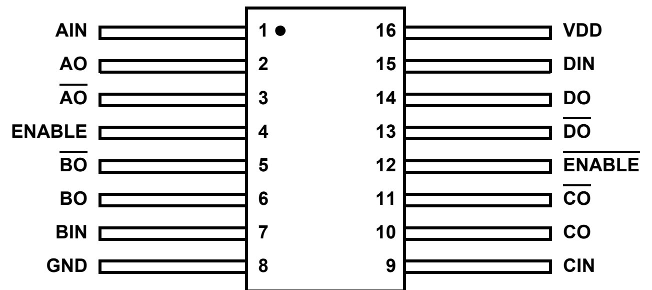
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = +25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The lid of these packages are connected to the ground pin of the device.
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

Pin Configurations

HS1-26C31RH, HS1-26C31EH
(16 LD SBDIP) CDIP2-T16
TOP VIEW



HS9-26C31RH, HS9-26C31EH
(16 LD FLATPACK) CDFP4-F16
TOP VIEW



Logic Diagram

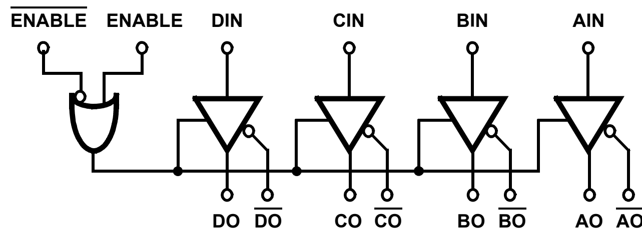


TABLE 1. TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	$\overline{\text{ENABLE}}$	IN	OUT	$\overline{\text{OUT}}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF (0V)	X	X	X	HI-Z	HI-Z

X = Don’t Care
0 = Low
1 = High

Die Characteristics

DIE DIMENSIONS:

96.5 mils x 195 mils x 19 mils ±1mil
(2451μm x 4953μm x 483μm ±25μm)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8kÅ ±1kÅ

Metallization:

M1: Mo/TiW (Bottom)
Thickness: 5800Å ±1kÅ
M2: Al/Si/Cu (Top)
Thickness: 10kÅ ±1kÅ

Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

Internally tied to V_{DD}

ADDITIONAL INFORMATION:

Worst Case Current Density:

$<2.0x10^5 A/cm^2$

Bond Pad Size:

110μmx100μm

Metallization Mask Layout

HS-26C31RH, HS-26C31EH

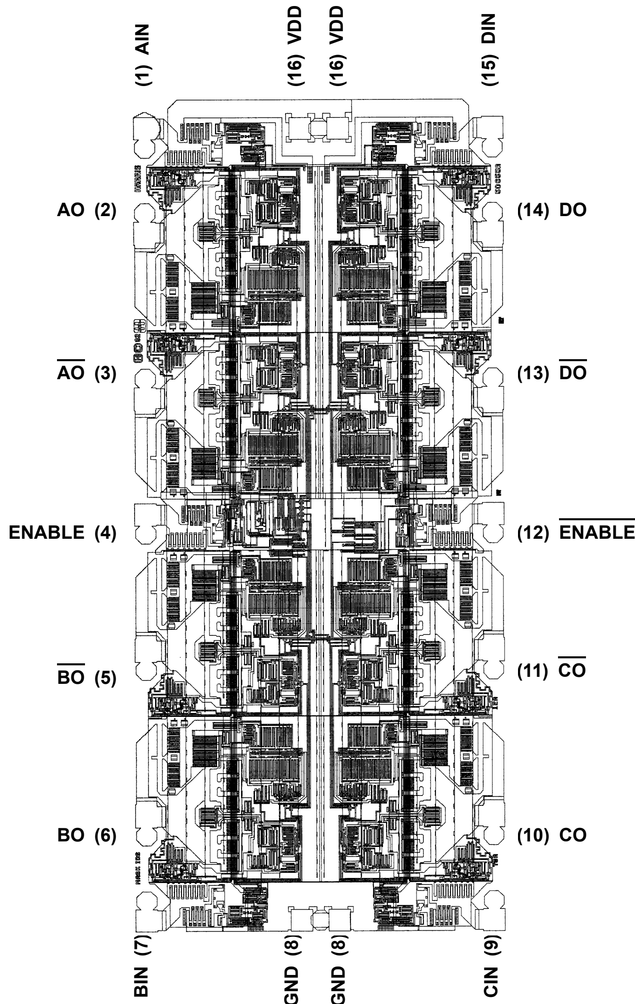


TABLE 2. HS-26C31RH, HS-26C31EH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1 X COORDINATES	RELATIVE TO PIN 1 Y COORDINATES
1	AIN	0	0
2	A0	0	-570.7
3	$\overline{A0}$	0	-1483.5
4	ENABLE	0	-2124.8
5	$\overline{B0}$	0	-2873.5
6	B0	0	-3786.3
7	BIN	0	-4357
8	GND	852.4	-4357
8	GND	1062.4	-4357
9	CIN	1912.8	-4357
10	$\overline{C0}$	1912.8	-3786.3
11	C0	1912.8	-2873.5
12	$\overline{ENABLE}$	1912.8	-2124.8
13	$\overline{D0}$	1912.8	-1483.5
14	D0	1912.8	-570.7
15	DIN	1912.8	0
16	VIN	1062.4	0
16	VIN	852.4	0

NOTE: Dimensions in microns.

Revision History

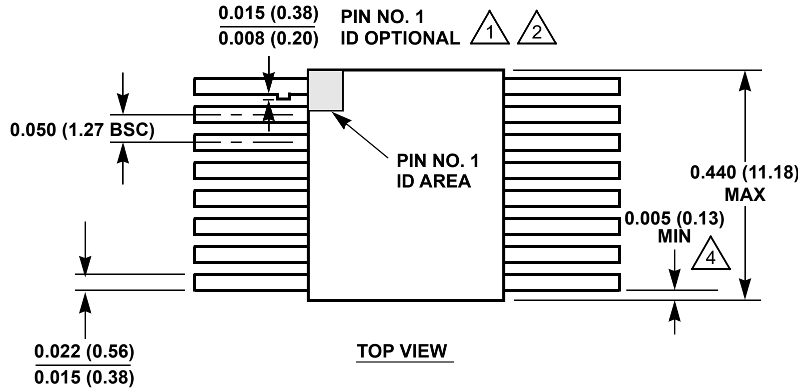
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

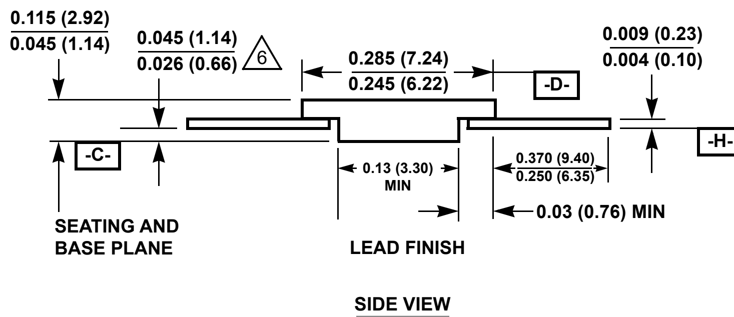
DATE	REVISION	CHANGE
Aug 5, 2022	8.01	Updated Table 1.
Oct 21, 2021	8.00	In the Features section on page 1 added Radiation acceptance testing bullets for RH and EH parts. Updated Ordering Information table by adding carrier type and radiation testing information columns, verified part numbers in table are correct, and added Notes 1, 3, and 5. Added Truth Table. Updated the Die Characteristics information as follows: -Die thickness changed from:21mils, to:19mils. -Updated Metallization M1 thickness by adding ±1kÅ. -Updated Substrate Potential (Powered Up) information. Added Table 2 to the Metallization Mask Layout section. Added Revision History. Added POD drawings.

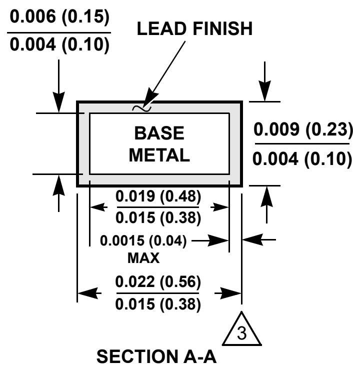
Package Outline Drawings

For the most recent package outline drawing, see K16.4.

K16.A
16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10



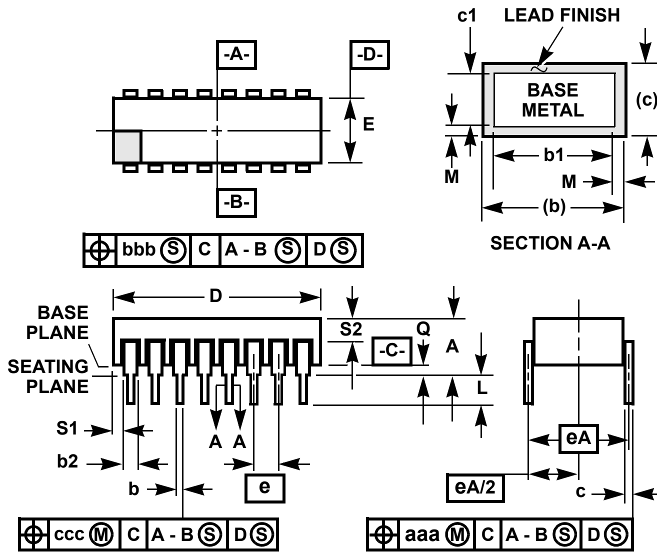




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see D16.3.



D16.3
MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 Lead Ceramic Dual-In-Line Metal Seal Package (SBDIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

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