HS-26CLV32RH, HS-26CLV32EH

Radiation Hardened 3.3V Quad Differential Line Receivers

FN4907
Rev 7.00
Oct 21, 2021

The HS-26CLV32RH, HS-26CLV32EH are radiation hardened 3.3V quad differential line receivers designed for digital data transmission over balanced lines, in low voltage, RS-422 protocol applications. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CLV32RH, HS-26CLV32EH have an input sensitivity of 200mV (typical) over a common-mode input voltage range of -4V to +7V. The receivers are also equipped with input fail-safe circuitry, which causes the outputs to go to a logic “1” when the inputs are open. The device has unique inputs that remain high impedance when the receiver is disabled or powered-down, maintaining signal integrity in multi-receiver applications.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95689. A link is provided on our homepage for downloading.

Applications

- Line receiver for MIL-STD-1553 serial data bus
- Line receiver for RS422

Features

- Electrically screened to SMD # 5962-95689
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
- Low stand-by current . . . . . 13mA (max)
- Operating supply range . . . . . 3.0V to 3.6V
- Enable input levels. . . . . V_{IH} > 0.7 x V_{DD}; V_{IL} < 0.3 x V_{DD}
- CMOS output levels . . . . . V_{OH} > 2.55V; V_{OL} < 0.4V
- Input fail-safe circuitry
- High impedance inputs when disabled or powered-down
- Radiation acceptance testing - HS-26CLV32RH
  - HDR (50-300rad (Si)/s). . . . . 300krad(Si)
- Radiation acceptance testing - HS-26CLV32EH
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . .50krad(Si)
- SEL immune to LET . . . . . .100MeV*cm^2/mg
- Full -55°C to +125°C military temperature range
- Pb-free (RoHS compliant)

Ordering Information

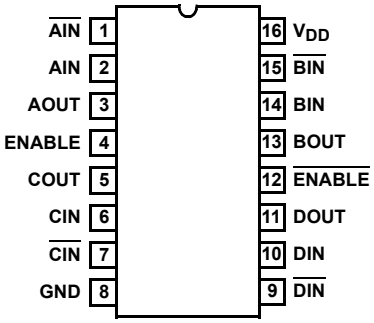
ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
5962F9568902QEC	HS1-26CLV32RH-8	HDR to 300krad(Si)	16 Ld SBDIP	D16.3	Tube	-55 to +125°C
5962F9568902QXC	HS9-26CLV32RH-8		16 Ld Flatpack	K16.A	Tray	
5962F9568902VEC	HS1-26CLV32RH-Q		16 Ld SBDIP	D16.3	Tube	
5962F9568902VXC	HS9-26CLV32RH-Q		16 Ld Flatpack	K16.A	Tray	
5962F9568902V9A	HS0-26CLV32RH-Q (Note 3)		Die	N/A	N/A	
5962F9568902VYC	HS9G-26CLV32RH-Q (Note 4)		16 Ld Flatpack	K16.A	Tray	
N/A	HS0-26CLV32RH/SAMPLE (Notes 3, 5)	N/A	Die	N/A	N/A	
	HS1-26CLV32RH/PROTO (Note 5)		16 Ld SBDIP	D16.3	Tube	
	HS9-26CLV32RH/PROTO (Note 5)		16 Ld Flatpack	K16.A	Tray	
	HS9G-26CLV32RH/PROTO (Notes 4, 5)		16 Ld Flatpack	K16.A	Tray	
5962F9568904VEC	HS1-26CLV32EH-Q	HDR to 300krad(Si) LDR to 50krad(Si)	16 Ld SBDIP	D16.3	Tube	
5962F9568904VXC	HS9-26CLV32EH-Q		16 Ld Flatpack	K16.A	Tray	
5962F9568904V9A	HS0-26CLV32EH-Q (Note 3)		Die	N/A	N/A	
5962F9568904VYC	HS9G-26CLV32EH-Q (Note 4)		16 Ld Flatpack	K16.A	Tray	

NOTES:

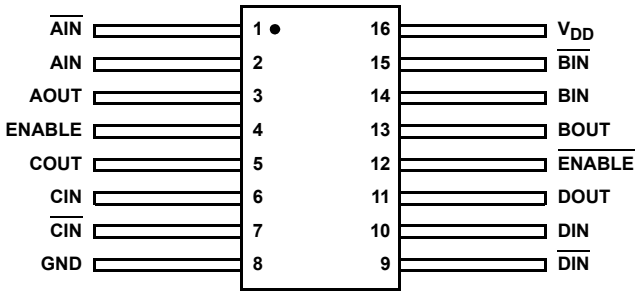
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
4. The lid of these packages are connected to the ground pin of the device.
5. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

Pin Configurations

HS1-26CLV32RH, HS1-26CLV32EH
(16 LD SBDIP)
MIL-STD-1835: CDIP2-T16
TOP VIEW



HS9-26CLV32RH, HS9-26CLV32EH
(16 LD FLATPACK)
MIL-STD-1835: CDFP4-F16
TOP VIEW



NOTES:

6. For details on input output structures refer to application note AN9520.
7. For details on package dimensions refer MIL-STD-1835.

Logic Diagram

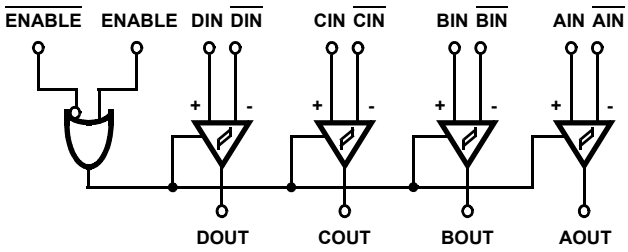


TABLE 1. TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1
OFF	X	X	X	HI-Z

X = Don't Care
0 = Low
1 = High

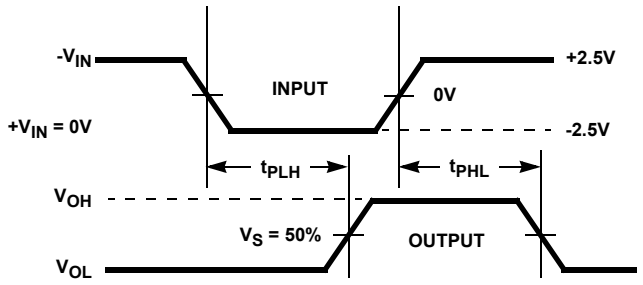


FIGURE 1. PROPAGATION DELAY TIMING DIAGRAM

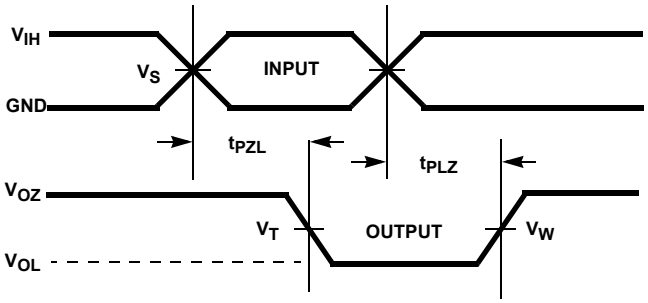


FIGURE 2. THREE-STATE LOW TIMING DIAGRAM

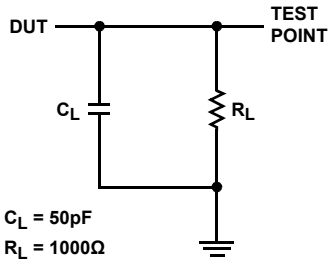


FIGURE 3. PROPAGATION DELAY LOAD CIRCUIT

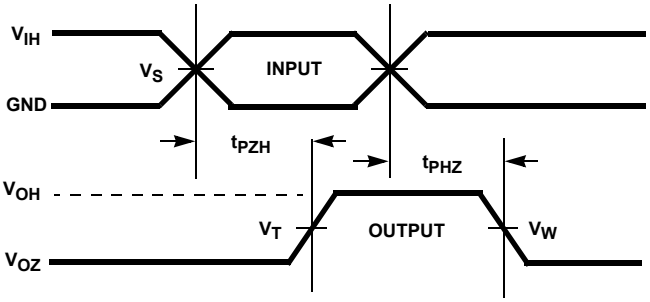


FIGURE 4. THREE-STATE HIGH TIMING DIAGRAMS

TABLE 2. THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26CLV32RH HS-26CLV32EH	UNITS
V_{DD}	3.00	V
V_{IH}	3.00	V
V_S	50	%
V_T	50	%
V_W	V_{OL} + 0.5	V
GND	0	V

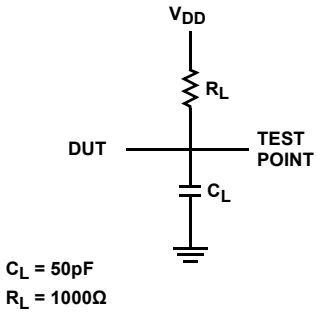


FIGURE 5. THREE-STATE LOW LOAD CIRCUIT

TABLE 3. THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26CLV32RH HS-26CLV32EH	UNITS
V_{DD}	3.0	V
V_{IH}	3.0	V
V_S	50	%
V_T	50	%
V_W	V_{OH} - 0.5	V
GND	0	V

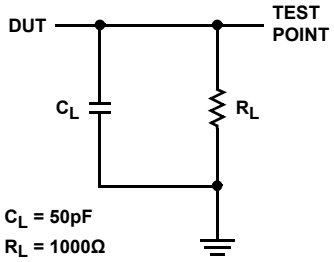


FIGURE 6. THREE-STATE HIGH LOAD CIRCUIT

Die Characteristics

DIE DIMENSIONS:

78 mils x 123 mils x 19mils ±1mil
(1981µm x 3124µm x 483µm ±25µm)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8kÅ ±1kÅ

Metallization:

M1: Mo/TiW (Bottom)
Thickness: 5800Å ±1kÅ
M2: Al/Si/Cu (Top)
Thickness: 10kÅ ±1kÅ

Substrate:

AVLSI1RA

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

Internally tied to V_{DD}

Worst Case Current Density:

< $2.0e5A/cm^2$

Bond Pad Size:

110µm x 100µm

Transistor Count:

315

Metallization Mask Layout

HS-26CLV32RH, HS-26CLV32EH

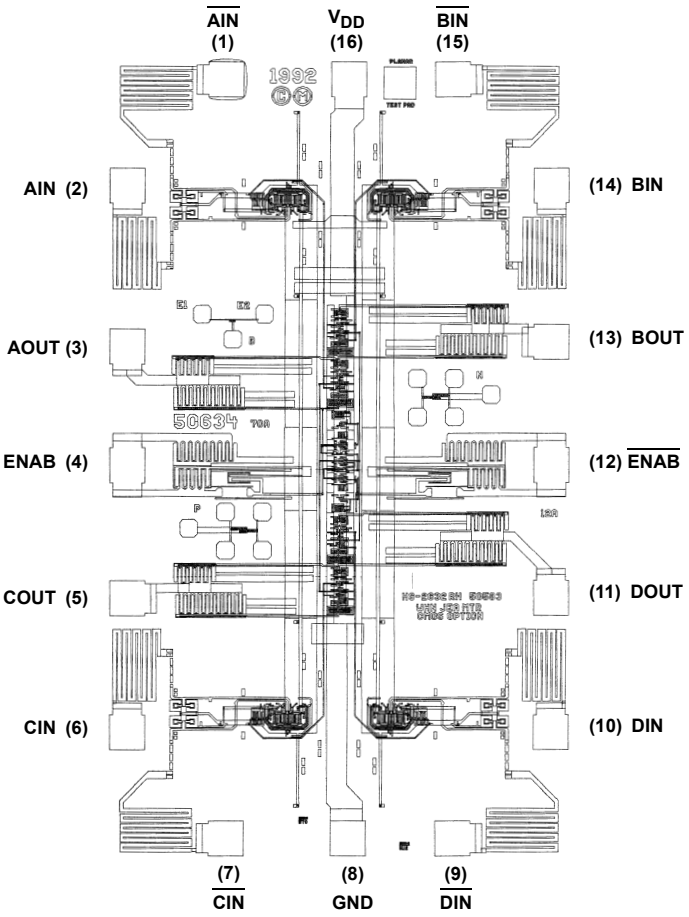


TABLE 4. HS-26CLV32RH, HS-26CLV32EH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	AIN	0	0
2	AIN	-337.1	-362
3	AOUT	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	COUT	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	CIN	0	-2595.7
8	GND	418.4	-2596.7
9	DIN	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	DOUT	1113.5	-1774.4
12	ENABLE	1113.5	-1319.3
13	BOUT	1113.5	-898.4
14	BIN	1113.5	-362
15	BIN	776.4	0
16	V_{DD}	420.2	1

NOTE: Dimensions in microns

Revision History

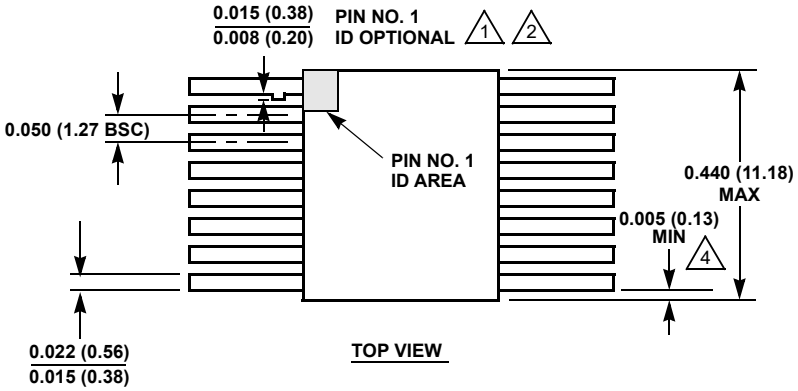
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

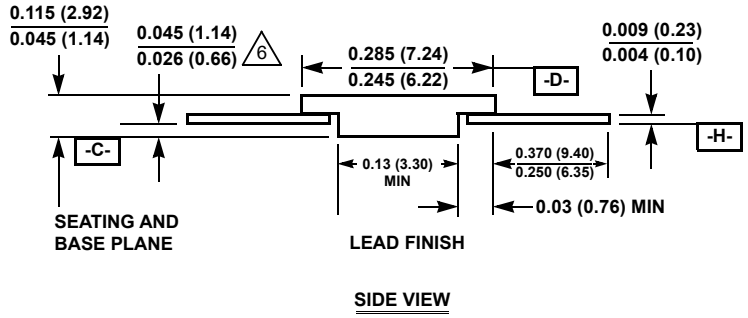
DATE	REVISION	CHANGE
Oct 21, 2021	7.00	Removed Related Literature section. In Features section on page 1 added Radiation acceptance testing bullets for RH and EH parts. In Ordering Information table on page 2 verified the part numbers in the table are correct, added carrier type and radiation testing information columns, and re-ordered the notes in the table and added notes 3 and 5. Added Truth Table, Timing Diagrams, and Load Circuit Diagrams. Updated the Die Characteristics information as follows: -Changed the die thickness from: 21mils, to: 19mils -Updated Worst Case Current Density. -Added Transistor count. Removed About Intersil section.
Feb 6, 2017	6.00	Added Related Literature section. Updated Ordering Information table on page 2. Added Note 2 on page 2. Added Revision History and About Intersil sections. Added POD drawings.

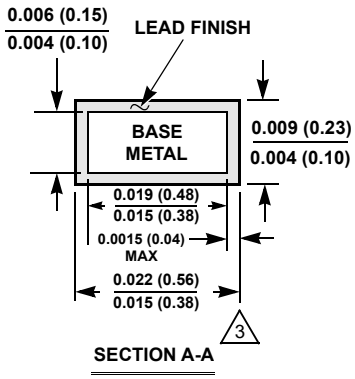
Package Outline Drawings

For the most recent package outline drawing, see K16.4.

K16.A
16 Lead Ceramic Metal Seal Flatpack Package
Rev 2, 1/10



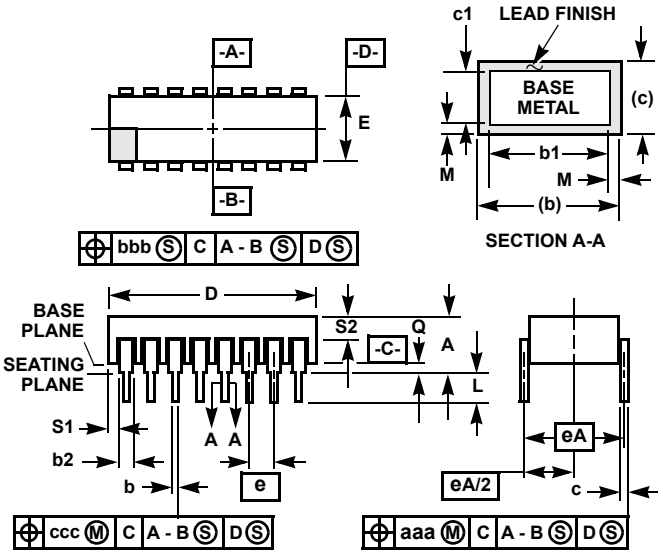




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see D16.3.



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3
MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 Lead Ceramic Dual-In-Line Metal Seal Package ***(SBDIP)***

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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