

## HS-26CT32RH, HS-26CT32EH

Radiation Hardened Quad Differential Line Receivers

FN2930  
Rev 7.00  
Oct 21, 2021

The [HS-26CT32RH](#), [HS-26CT32EH](#) are differential line receivers designed for digital data transmission over balanced lines and meets the requirements of EIA Standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

The HS-26CT32RH, HS-26CT32EH have an input sensitivity of typically of 200mV over the common mode input voltage range of  $\pm 7V$ . The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. TTL compatible Enable and Disable functions are common to all four receivers.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95631. A link is provided on our homepage for downloading.

### Applications

- Line receiver for MIL-STD-1553 serial data bus
- Line receiver for RS422

### Features

- Electrically screened to SMD # [5962-95631](#)
- QML qualified per MIL-PRF-38535 requirements
- 1.2 micron radiation hardened CMOS
- EIA RS-422 compatible inputs
- TTL compatible enable inputs
- Operation with TTL based on  $V_{IH} = V_{DD}/2$
- Input fail-safe circuitry
- Low power dissipation 138mW standby (max)
- High impedance inputs when disabled or powered-down
- Operating supply range . . . . . 4.5V to 5.5V
- Radiation acceptance testing - HS-26CT32RH
  - HDR (50-300rad (Si)/s) . . . . . 300krad(Si)
- Radiation acceptance testing - HS-26CT32EH
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . 50krad(Si)
- SEL immune to LET . . . . . 100MeV\*cm<sup>2</sup>/mg
- Full -55 °C to +125 °C military temperature range
- Pb-free (RoHS compliant)

## Ordering Information

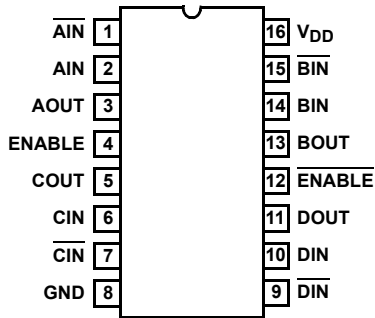
ORDERING SMD NUMBER (Note 1)	PART NUMBER (Note 2)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS COMPLIANT)	PKG. DWG. #	CARRIER TYPE	TEMP. RANGE
5962F9563101QEC	HS1-26CT32RH-8	HDR to 300krad(Si)	16 LD SBDIP	D16.3	Tube	-55 to +125° C
5962F9563101QXC	HS9-26CT32RH-8		16 LD Flatpack	K16.A	Tray	
5962F9563101VEC	HS1-26CT32RH-Q		16 LD SBDIP	D16.3	Tube	
5962F9563101VXC	HS9-26CT32RH-Q		16 LD Flatpack	K16.A	Tray	
5962F9563101V9A	HS0-26CT32RH-Q (Note 3)		Die	N/A	N/A	
5962F9563101VYC	HS9G-26CT32RH-Q (Note 4)		16 LD Flatpack	K16.A	Tray	
N/A	HS1-26CT32RH/PROTO (Note 5)	N/A	16 LD SBDIP	D16.3	Tube	
	HS9-26CT32RH/PROTO (Note 5)		16 LD Flatpack	K16.A	Tray	
	HS0-26CT32RH/SAMPLE (Notes 3, 5)		Die	N/A	N/A	
	HS9G-26CT32RH/PROTO (Notes 4, 5)		16 LD Flatpack	K16.A	Tray	
5962F9563102VEC	HS1-26CT32EH-Q	HDR to 300krad(Si), LDR to 50krad(Si)	16 LD SBDIP	K16.A	Tube	
5962F9563102VXC	HS9-26CT32EH-Q		16 LD Flatpack	K16.A	Tray	
5962F9563102V9A	HS0-26CT32EH-Q (Note 3)		Die	N/A	N/A	

### NOTES:

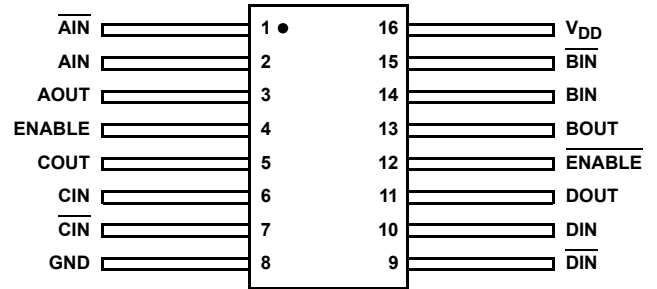
- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- Die product tested at  $T_A = +25^\circ\text{C}$ . The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in SMD.
- The lid of these packages are connected to the ground pin of the device.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because they are not DLA qualified devices.

## Pin Configurations

HS1-26CT32RH, HS1-26CT32EH  
(16 LD SBDIP)  
MIL-STD-1835: CDIP2-T16  
TOP VIEW



HS9-26CT32RH, HS9-26CT32EH  
(16 LD FLATPACK)  
MIL-STD-1835: CDFP4-F16  
TOP VIEW



NOTES:

- 6. For details on input output structures refer to application note [AN9520](#).
- 7. For details on package dimensions refer MIL-STD-1835.

## Logic Diagram

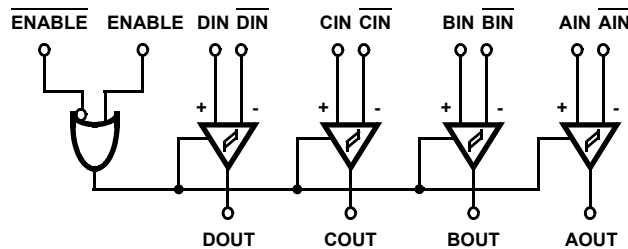


TABLE 1. TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	ENAB	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	$VID \geq VTH$ (Max)	1
ON	1	X	$VID \leq VTH$ (Min)	0
ON	X	0	$VID \geq VTH$ (Max)	1
ON	X	0	$VID \leq VTH$ (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1
OFF	X	X	X	HI-Z

X = Don't Care  
0 = Low  
1 = High

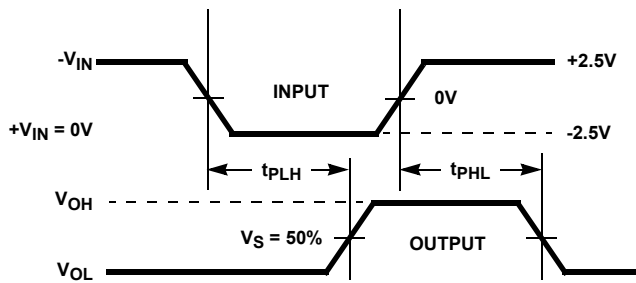


FIGURE 1. PROPAGATION DELAY TIMING DIAGRAM

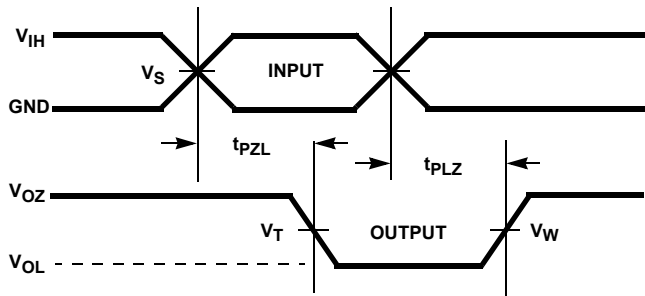


FIGURE 2. THREE-STATE LOW TIMING DIAGRAM

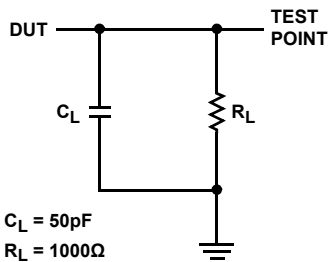


FIGURE 3. PROPAGATION DELAY LOAD CIRCUIT

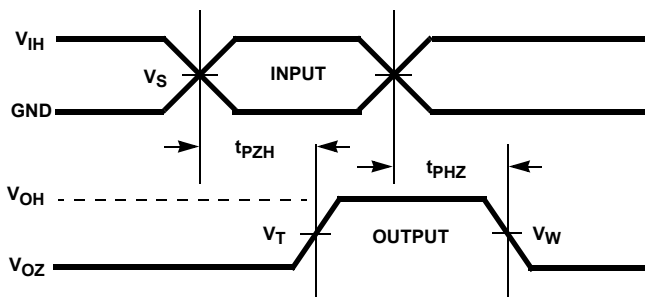
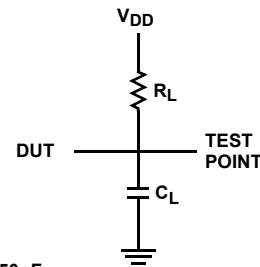


FIGURE 4. THREE-STATE HIGH TIMING DIAGRAMS

TABLE 2. THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26CT32RH HS-26CT32EH	UNITS
V <sub>DD</sub>	4.50	V
V <sub>IH</sub>	4.50	V
V <sub>S</sub>	50	%
V <sub>T</sub>	50	%
V <sub>W</sub>	V <sub>OL</sub> + 0.5	V
GND	0	V

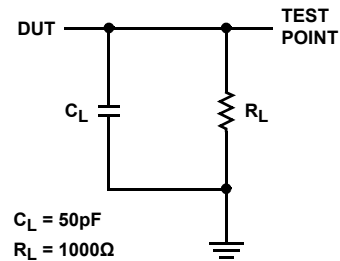


C<sub>L</sub> = 50pF  
R<sub>L</sub> = 1000Ω

FIGURE 5. THREE-STATE LOW LOAD CIRCUIT

TABLE 3. THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26CT32RH HS-26CT32EH	UNITS
V <sub>DD</sub>	4.50	V
V <sub>IH</sub>	4.50	V
V <sub>S</sub>	50	%
V <sub>T</sub>	50	%
V <sub>W</sub>	V <sub>OH</sub> - 0.5	V
GND	0	V



C<sub>L</sub> = 50pF  
R<sub>L</sub> = 1000Ω

FIGURE 6. THREE-STATE HIGH LOAD CIRCUIT

# Die Characteristics

## DIE DIMENSIONS:

78 mils x 123 mils x 19mils ±1mil  
 (1981µm x 3124µm x 483µm ±25µm)

## INTERFACE MATERIALS:

### Glassivation:

Type: PSG (Phosphorus Silicon Glass)  
 Thickness: 8kÅ ±1kÅ

### Metallization:

M1: Mo/TiW (Bottom)  
 Thickness: 5800Å ±1kÅ  
 M2: Al/Si/Cu (Top)  
 Thickness: 10kÅ ±1kÅ

### Substrate:

AVLSI1RA

### Backside Finish:

Silicon

## ASSEMBLY RELATED INFORMATION:

### Substrate Potential (Powered Up):

Internally tied to V<sub>DD</sub>

### Worst Case Current Density:

< 2.0e5 A/cm<sup>2</sup>

### Bond Pad Size:

110µm x 100µm

### Transistor Count:

315

# Metallization Mask Layout

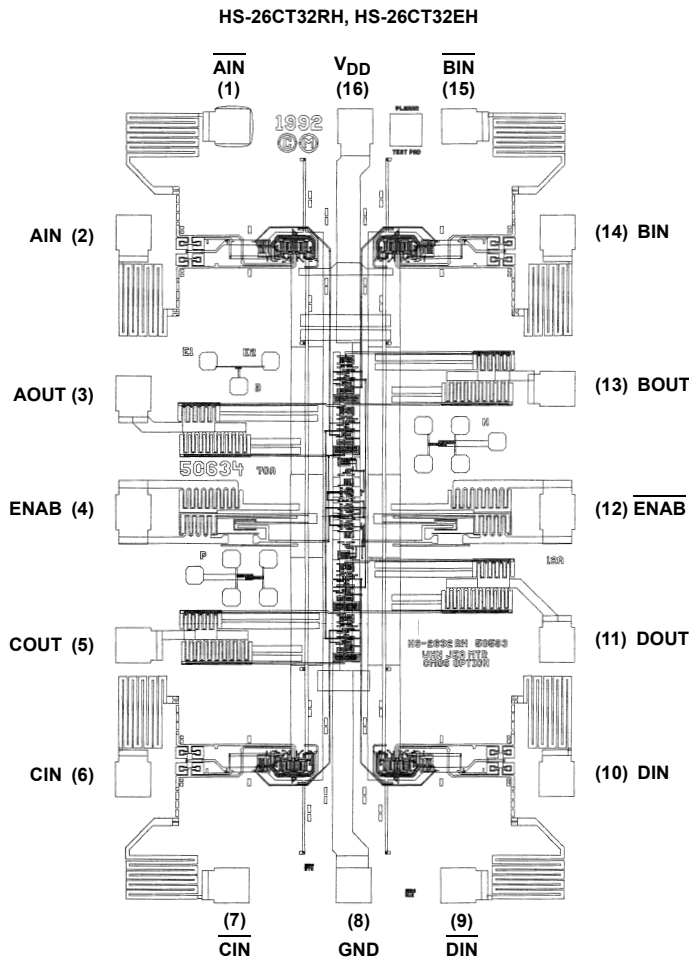


TABLE 4. HS-26CT32RH, HS-26CT32EH PAD COORDINATES

PIN NUMBER	PAD NAME	RELATIVE TO PIN 1	
		X COORDINATES	Y COORDINATES
1	AIN	0	0
2	AIN	-337.1	-362
3	AOUT	-337.1	-912.5
4	ENABLE	-337.1	-1319.3
5	COUT	-337.1	-1774.4
6	CIN	-337.1	-2233.7
7	CIN	0	-2595.7
8	GND	418.4	-2596.7
9	DIN	776.4	-2595.7
10	DIN	1113.5	-2233.7
11	DOUT	1113.5	-1774.4
12	ENABLE	1113.5	-1319.3
13	BOUT	1113.5	-898.4
14	BIN	1113.5	-362
15	BIN	776.4	0
16	V <sub>DD</sub>	420.2	1

NOTE: Dimensions in microns

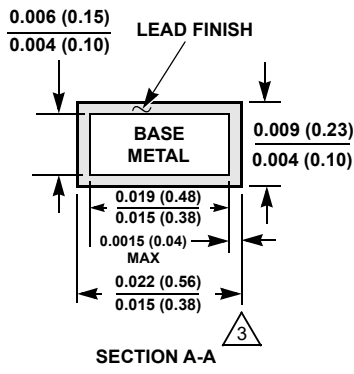
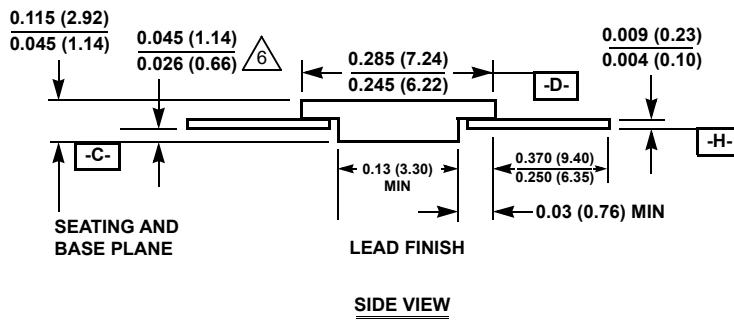
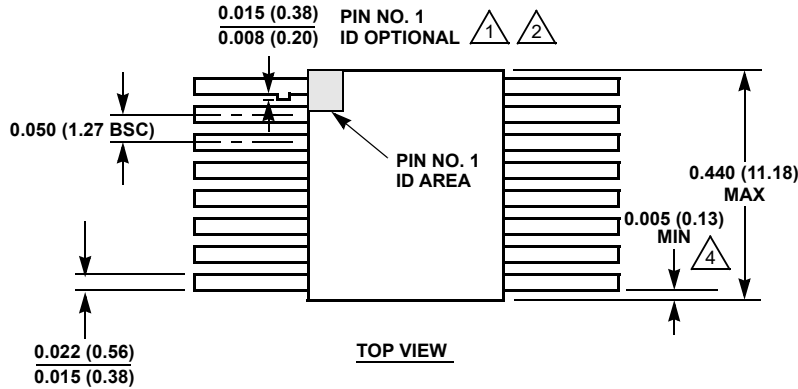
**Revision History** The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Oct 21, 2021	7.00	<p>In the Features section on page 1 added Radiation acceptance testing bullets for RH and EH parts.</p> <p>Updated Ordering Information table on page 2 by adding carrier type and radiation testing information columns, verified part numbers in table are correct, and added Notes 1, 3, and 4.</p> <p>Added Notes 6 and 7.</p> <p>Added Figures 1-6 and Tables 2 and 3.</p> <p>Added Truth Table.</p> <p>Updated the Die Characteristics information as follows:</p> <ul style="list-style-type: none"> <li>-Updated die dimensions</li> <li>-Updated Glassivation Thickness</li> <li>-Updated Metallization thickness by adding <math>\pm 1\text{k}\text{\AA}</math>.</li> <li>-Updated Substrate potential</li> <li>-Updated Worst Case Current Density</li> <li>-Updated Transistor count</li> </ul> <p>Added Table 4 to the Metallization Mask Layout section.</p> <p>Added Revision History</p> <p>Added POD drawings.</p>

# Package Outline Drawings

For the most recent package outline drawing, see [K16.4](#).

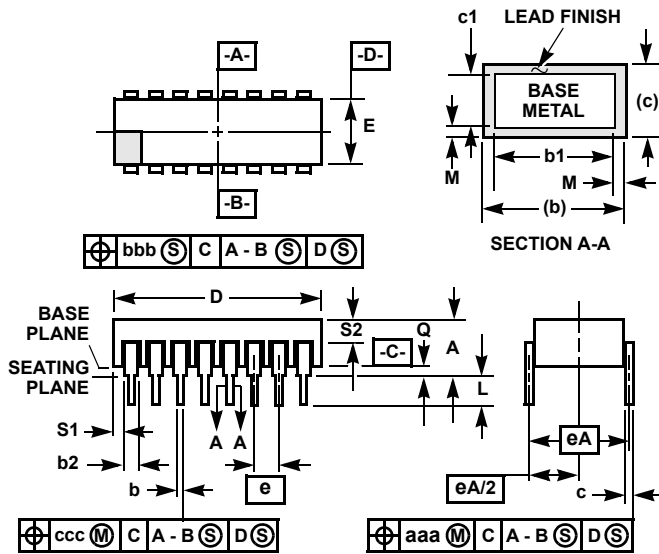
K16.A  
 16 Lead Ceramic Metal Seal Flatpack Package  
 Rev 2, 1/10



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

For the most recent package outline drawing, see [D16.3](#).



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

**D16.3**

MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)

16 Lead Ceramic Dual-In-Line Metal Seal Package (SBDIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
$\alpha$	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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(Rev.1.0 Mar 2020)

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