ISL28177

40V General Purpose Precision Operational Amplifier

FN7859
Rev 2.00
April 5, 2012

The ISL28177 is an OP07 replacement featuring low input offset voltage, low input bias current, and competitive noise and AC performance. The ESD ratings are best among competitive parts at 5kV HBM, 300V MM, and 2.2kV CDM. The amplifier operates over the 6V (±3V) to 40V (±20V) range.

Applications include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial sensors.

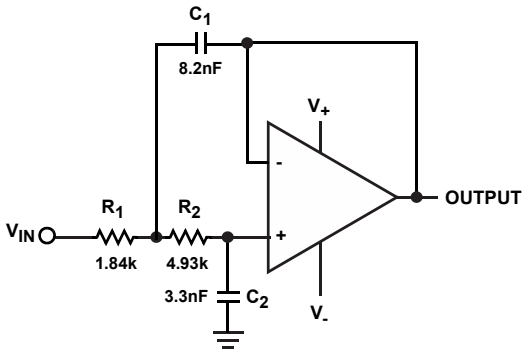
The ISL28177 is available in the SOT23-5 and SOIC-8 packages and operates over the extended temperature range to -40°C to +125°C.

Features

- Wide Supply Range . . . . . 6V (±3V) to 40V (±20V)
- Low Input Offset Voltage . . . . . 150µV, Max
- Input Bias Current . . . . . .1nA, Max
- Low Noise . . . . . .9.5nV/√Hz @ 1kHz
- Gain Bandwidth 600kHz
- Exceptional ESD Performance . . . . . .5kV HBM, 300V MM, 2.2kV CDM
- Operating Temperature Range . . . . . .-40°C to +125°C
- Packages
  - ISL28177 (Single) SOT23-5, SOIC-8

Applications

- Precision Active Filters
- Medical and Analytical Instrumentation
- Precision Power Supply Controls
- Industrial Sensors



SALLEN-KEY LOW PASS FILTER (10kHz)

FIGURE 1. TYPICAL APPLICATION

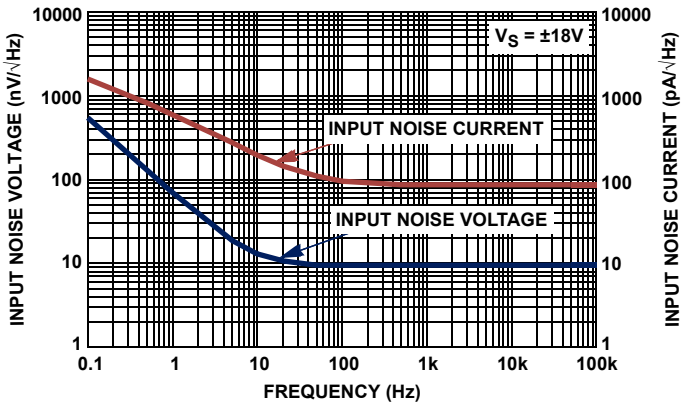


FIGURE 2. INPUT NOISE PERFORMANCE

Ordering Information

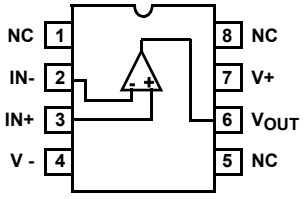
PART NUMBER (Note 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL28177FBZ	28177 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28177FBZ-T13 (Note 1)	28177 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28177FBZ-T7 (Note 1)	28177 FBZ	-40 to +125	8 Ld SOIC	M8.15E
ISL28177FBZ-T7A (Note 1)	28177 FBZ	-40 to +125	8 Ld SOIC	M8.15E
Coming Soon ISL28177FHZ	TBD	-40 to +125	SOT23-5	P5.064A

NOTES:

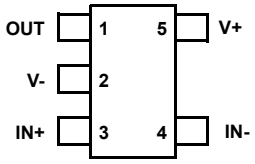
1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28177. For more information on MSL please see techbrief TB363.

Pin Configurations

ISL28177
(8 LD SOIC)
TOP VIEW

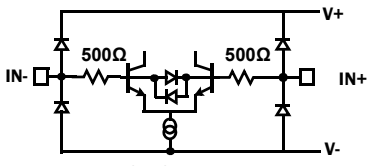


ISL28177
(5 LD SOT-23)
TOP VIEW

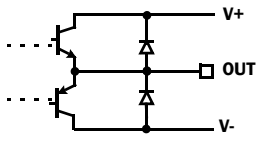


Pin Descriptions

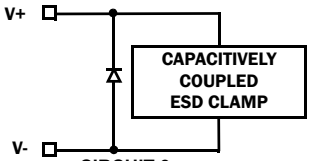
ISL28177 (8 LD SOIC)	ISL28177 (5 LD SOT-23)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	3	IN+	Circuit 1	Amplifier non-inverting input
4	2	V-	Circuit 3	Negative power supply
2	4	IN-	Circuit 1	Amplifier inverting input
7	5	V+	Circuit 3	Positive power supply
6	1	V_{OUT}	Circuit 2	Amplifier output
1, 5, 8	-	NC	-	No internal connection



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Absolute Maximum Ratings

Maximum Supply Voltage 44V
Maximum Differential Input Voltage . . . . . 44V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Voltage . . . . . 44V or V_- - 0.5V to V_+ + 0.5V
Min/Max Input Current 20mA
Output Short-Circuit Duration (1 output at a time) . . . . . Indefinite
ESD Ratings
Human Body Model (Tested per JESD22-A114F) 5kV
Machine Model (Tested per JESD22-A115-A) 300V
Charged Device Model (Tested per CDM-22CIOID) 2.2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 Package (Notes 4, 5)	TBD	TBD
8 Ld SOIC Package (Notes 4, 5)	125	73

Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature Range . . . . . -40°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Operating Voltage Range . . . . . 6V (±3V) to 40V (±20V)

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_S = ±5V to ±15V, R_L = Open, V_{CM} = 0V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{OS}	Input Offset Voltage				150	µV
		-40°C to +85°C			250	µV
		-40°C to +125°C			**350**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient	-40°C to +125°C		**0.5**	**1.4**	µV/°C
ΔV_{OS}/Time	Long Term V_{OS} Stability			0.4		µV/mo
I_B	Input Bias Current			0.2	1	nA
		-40°C to +125°C			**1**	nA
I_{OS}	Input Offset Current			0.2	1	nA
		-40°C to +125°C			**1**	nA
e_N	Input Noise Voltage	f = 0.1Hz to 10Hz		0.38		μV_{P-P}
	Input Noise Voltage Density	f = 10Hz		13		nV/√Hz
	Input Noise Voltage Density	f = 100Hz		9.6		nV/√Hz
	Input Noise Voltage Density	f = 1kHz		9.5		nV/√Hz
i_N	Input Noise Current Density	f = 1kHz		87		fA/√Hz
V_{CMIR}	Common Mode Input Voltage Range	Guaranteed by CMRR test	V_- +2		V_+ -2	V
CMRR	Common Mode Rejection Ratio	V_{CM} = V_- +2V to V_+ - 2V	120	140		dB
			120			dB
PSRR	Power Supply Rejection Ratio	V_S = ±3V to ±20V	115	130		dB
			115			dB
V_{OL}	Output Voltage Low, V_{OUT} to V_-	R_L = 2kΩ		1.2	1.25	V
		R_L = 2kΩ, -40°C to +125°C			**1.3**	V
V_{OH}	Output Voltage High, V_+ to V_{OUT}	R_L = 2kΩ		1.2	1.25	V
		R_L = 2kΩ, -40°C to +125°C			**1.3**	V
SR	Slew Rate	R_L = 2kΩ, C_L = 100pF		0.2		V/µs
GBWP	Gain Bandwidth Product	R_L = 100kΩ, C_L = 60pF		600		kHz
AVOL	Large Signal Gain	V_{OUT} = ±3V to ±13V, R_L = 10kΩ	120	140		dB
			120			dB

Electrical Specifications V_S = ±5V to ±15V, R_L = Open, V_{CM} = 0V, T_A = +25°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
I_S	Supply Current			1.18	1.4	mA
					1.7	mA
V_S	Supply Voltage		±3V		±20V	V
I_{SC}	Short Circuit Current			30		mA

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, unless otherwise specified.

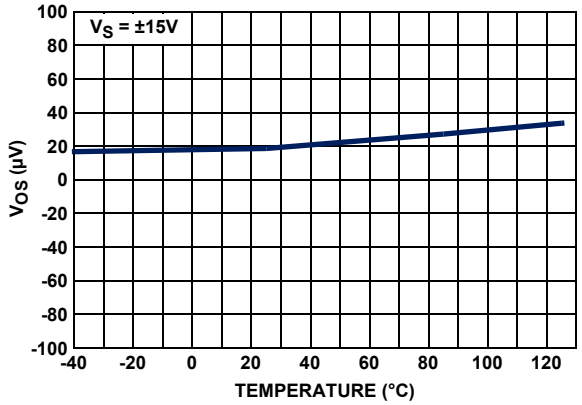


FIGURE 3. INPUT OFFSET VOLTAGE (V_{OS}) vs TEMPERATURE

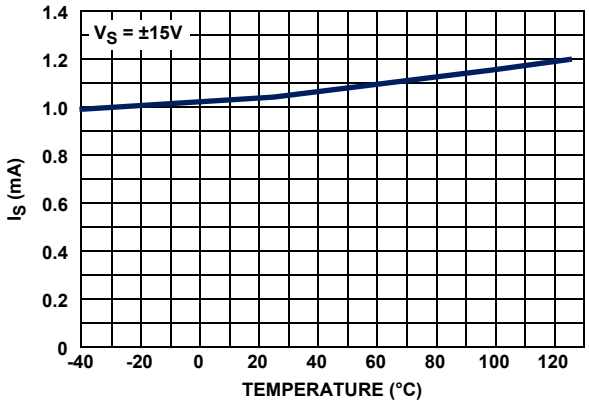


FIGURE 4. POWER SUPPLY CURRENT (I_S) vs TEMPERATURE

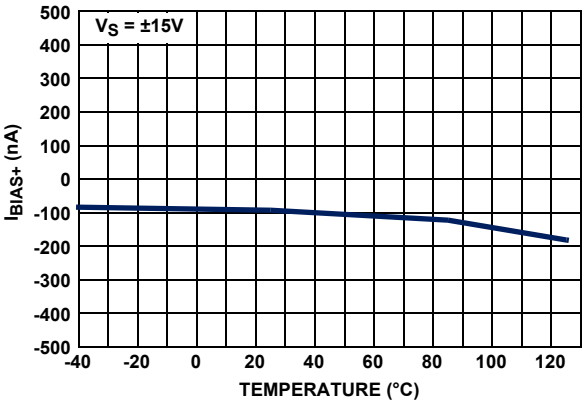


FIGURE 5. POSITIVE INPUT BIAS CURRENT (I_{IB+}) vs TEMPERATURE

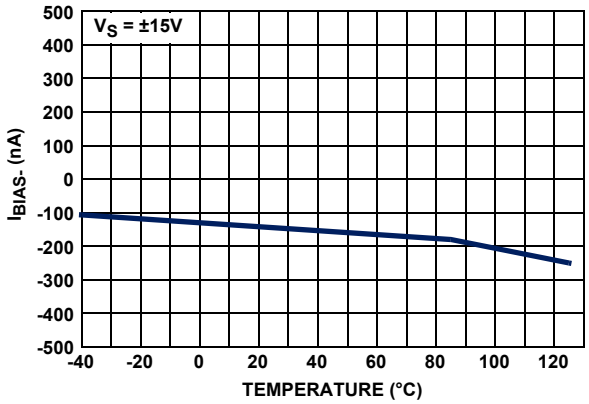


FIGURE 6. NEGATIVE INPUT BIAS CURRENT (I_{IB-}) vs TEMPERATURE

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

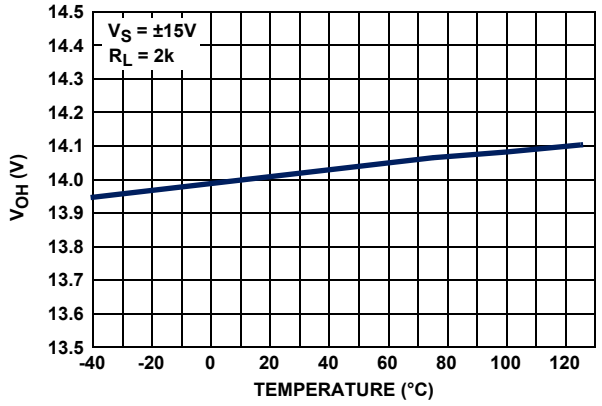


FIGURE 7. POSITIVE OUTPUT VOLTAGE (V_{OH}) vs TEMPERATURE

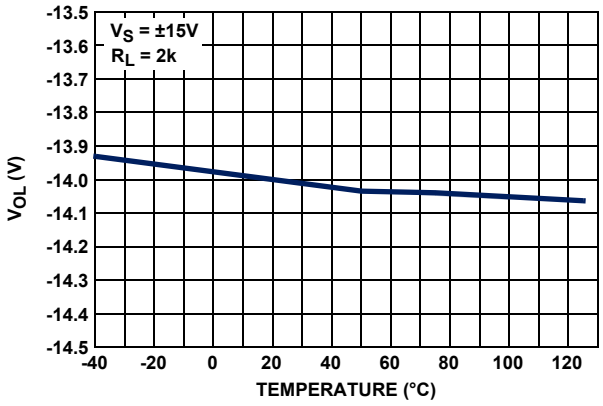


FIGURE 8. POSITIVE OUTPUT VOLTAGE (V_{OL}) vs TEMPERATURE

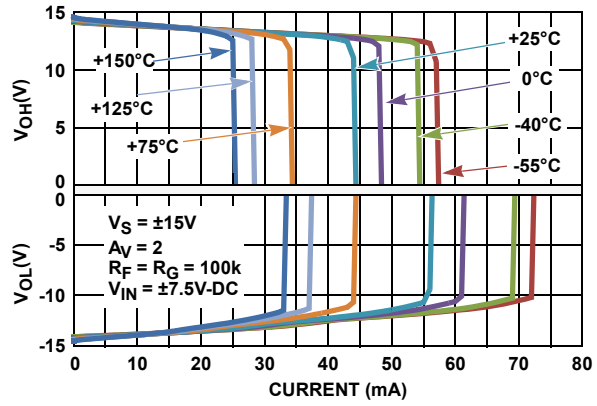


FIGURE 9. POSITIVE OUTPUT VOLTAGE (V_{OUT}) vs OUTPUT CURRENT (I_{OUT}) vs TEMPERATURE

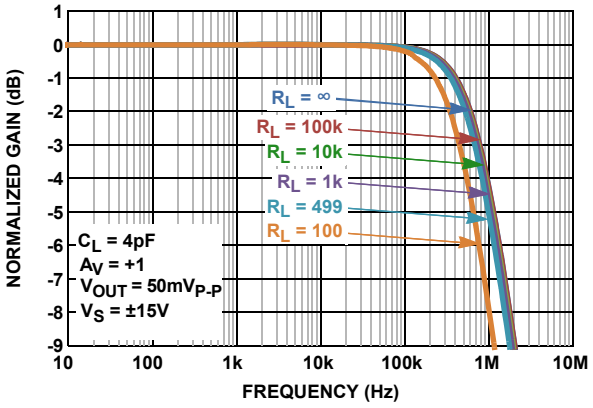


FIGURE 10. UNITY GAIN FREQUENCY RESPONSE vs R_L

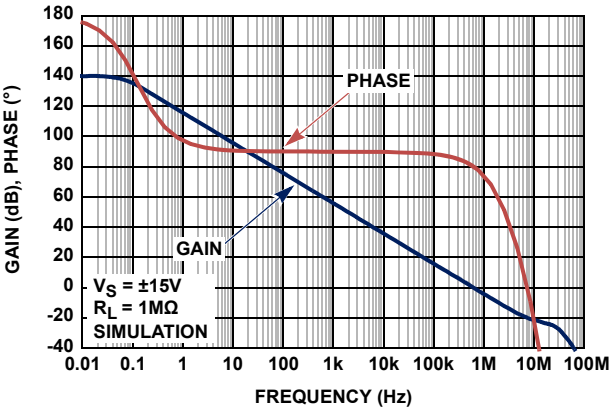


FIGURE 11. OPEN LOOP GAIN-PHASE vs FREQUENCY

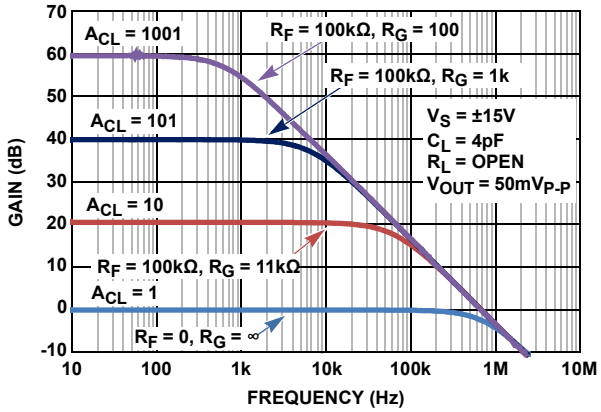


FIGURE 12. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

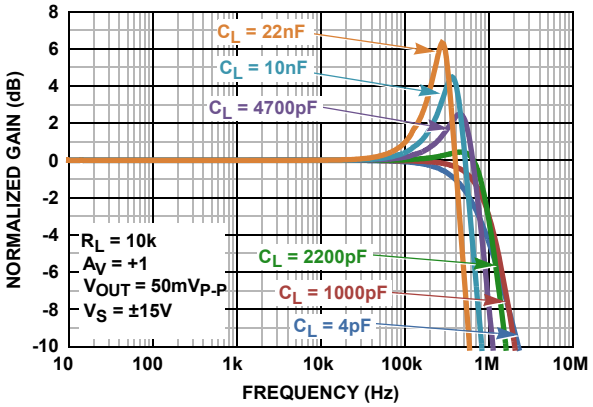


FIGURE 13. UNITY GAIN FREQUENCY RESPONSE vs C_L

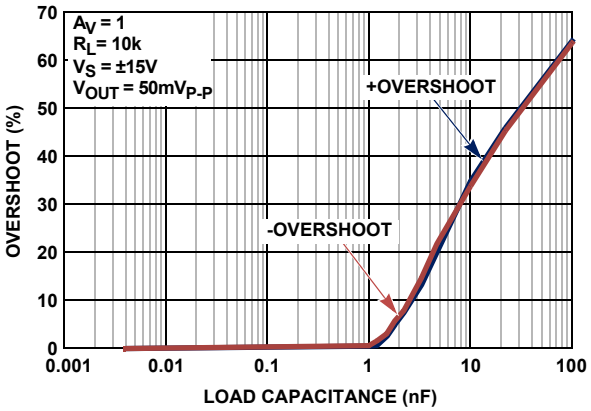


FIGURE 14. OVERSHOOT vs LOAD CAPACITANCE

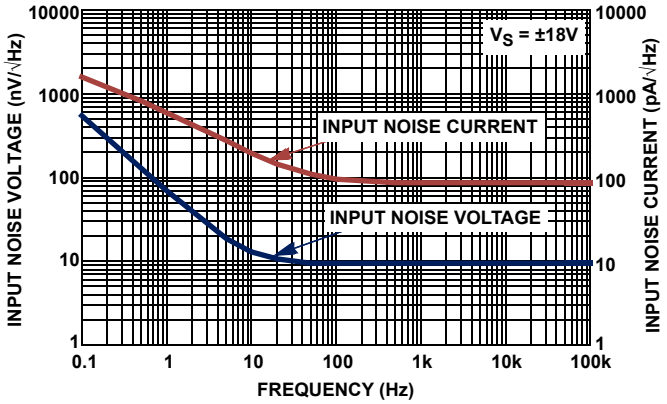


FIGURE 15. INPUT NOISE VOLTAGE AND CURRENT SPECTRAL DENSITY

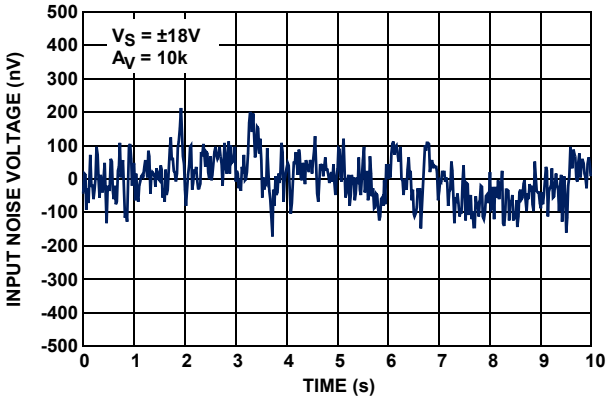


FIGURE 16. INPUT NOISE VOLTAGE 0.1Hz TO 10Hz

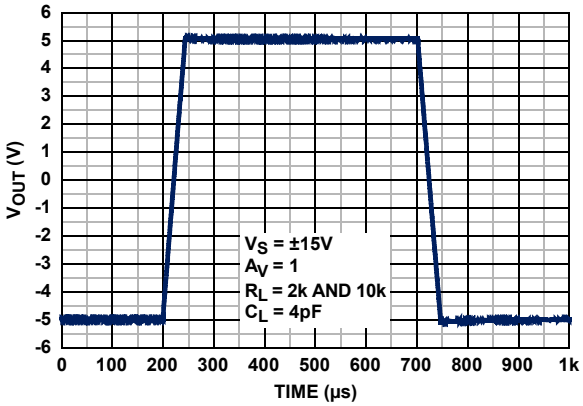


FIGURE 17. LARGE SIGNAL TRANSIENT RESPONSE

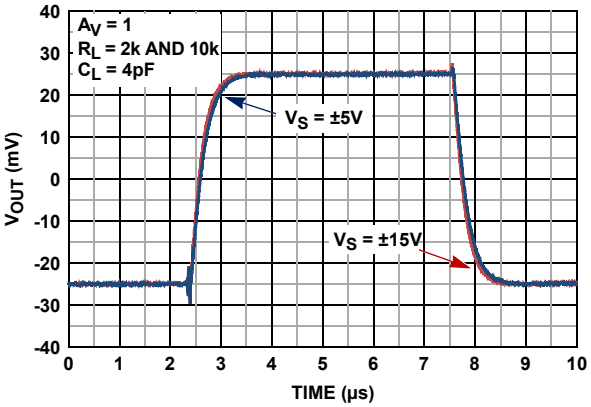


FIGURE 18. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves $V_S = \pm15V$, $V_{CM} = 0V$, R_L = Open, unless otherwise specified. **(Continued)**

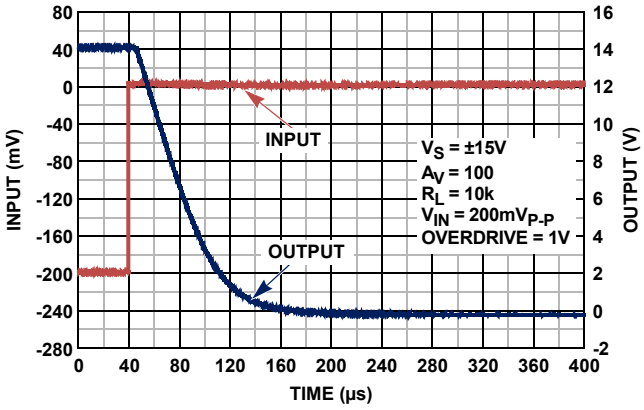


FIGURE 19. POSITIVE OUTPUT OVERLOAD RESPONSE TIME

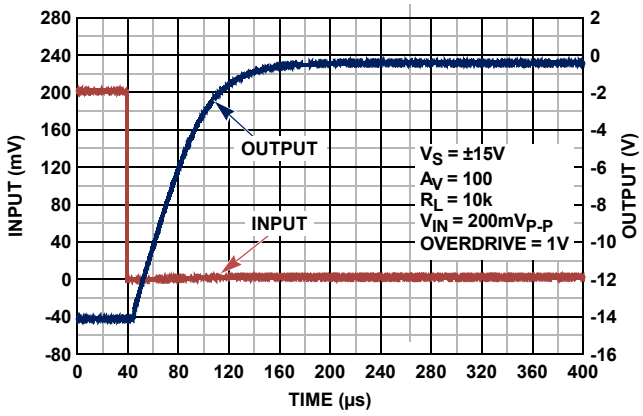


FIGURE 20. NEGATIVE OUTPUT OVERLOAD RESPONSE TIME

Applications Information

Functional Description

The ISL28177 is a low noise op amp fabricated in a 40V complementary bipolar DI process designed for general purpose low power applications. It utilizes a super-beta NPN input stage with input bias current cancellation for low input bias current and low input noise voltage. A complimentary bipolar output stage enables high capacitive load drive without external compensation.

Operating Voltage Range

The ISL28177 is designed to operate over the 6V (±3V) to 40V (±20V) range. The common mode input voltage range extends to 2V from each rail, and the output voltage swings to 1.3V of each rail.

Input Performance

The super-beta NPN input pair reduces input bias current while maintaining good frequency response, low input bias current and low noise. Input bias cancellation circuits provide additional bias current reduction to <1nA, and excellent temperature stabilization and low TCV_{OS}.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 500Ω current limiting resistors and an anti-parallel diode pair across the inputs (Figure 21).

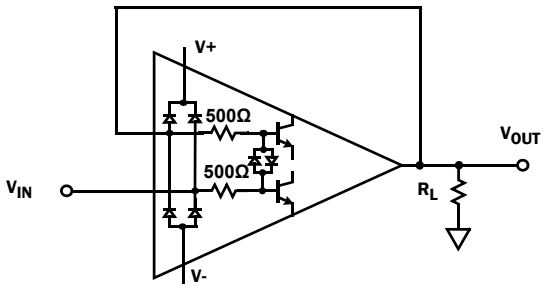


FIGURE 21. INPUT ESD DIODE CURRENT LIMITING

The series resistors limit the high feed-through currents that can occur in pulse applications when the input dv/dt exceeds the 0.2V/µs slew rate of the amplifier. Without the series resistors, the input can forward-bias the anti-parallel diodes causing current to flow to the output, resulting in severe distortion and possible diode failure. Figure 17 provides an example of distortion free large signal response using a $10V_{P-P}$ input pulse with an input rise time of <1ns. The series resistors enable the input differential voltage to be equal to the maximum power supply voltage (40V) without damage.

In applications where one or both amplifier input terminals are at risk of exposure to high voltages beyond the power supply rails, current limiting resistors may be needed at the input terminal to limit the current through the power supply ESD diodes to 20mA max.

Output Current Limiting

The output current is internally limited to approximately ±30mA at +25°C and can withstand a short circuit to either rail as long as the power dissipation limits are not exceeded. Continuous operation under these conditions may degrade long term reliability.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL28177 is immune to output phase reversal.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperature under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of 1 amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of 1 amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

ISL28177 SPICE Model

Figure 22 shows the SPICE model schematic and Figure 23 shows the net list for the SPICE model. The model is a simplified version of the actual device and simulates important AC and DC parameters. AC parameters incorporated into the model are: 1/f and flatband noise voltage, Slew Rate, CMRR, Gain and Phase. The DC parameters are, VOS, I_{OS}, total supply current and output voltage swing. The model uses typical parameters given in the "Electrical Specifications" table beginning on page 3. The AVOL is adjusted for 140dB with the dominant pole at 0.075Hz. The CMRR is set 145dB, f_{cm} = 500kHz. The input stage models the actual device to present an accurate AC representation. The model is configured for ambient temperature of +25°C.

Figures 24 through 37 show the characterization vs simulation results for the Noise Voltage, Closed Loop Gain vs Frequency, Small Signal 0.1V Step, Large Signal 5V Step Response, Open Loop Gain Phase, CMRR, Unity Gain Frequency Response vs C_L and Output Voltage Swing for ±15V supplies.

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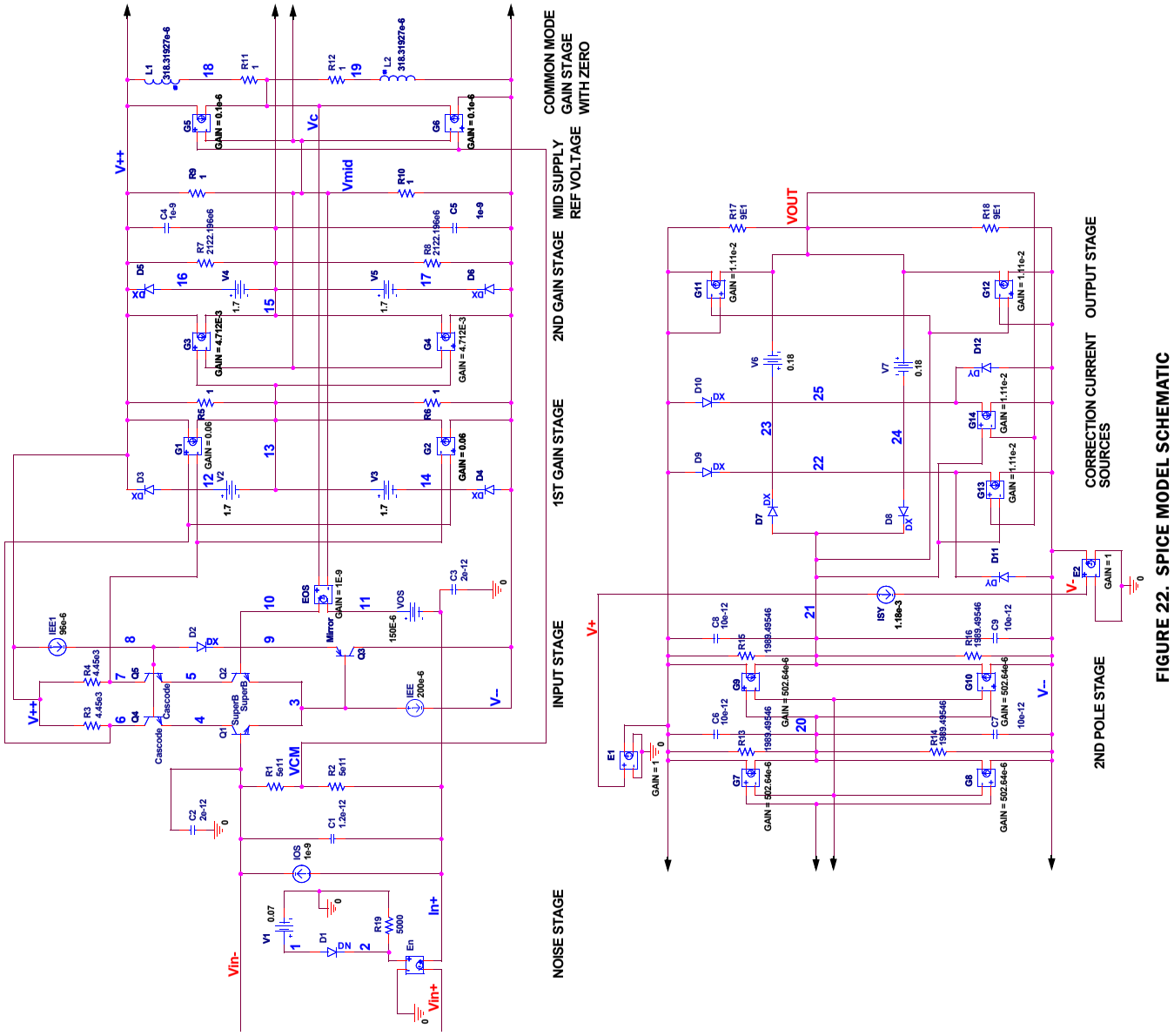

FIGURE 22. SPICE MODEL SCHEMATIC

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*ISL28177 Macromodel
**Revision History:
*Revision A, LaFontaine December 14, 2011
*Model for Noise, quiescent supply currents,
*CMRR 145dB, fcm=500kHz, AVOL 140dB
*f=0.075Hz SR = 0.2V/us, GBWP 600kHz,
*2nd pole 8Mhz, output voltage clamp
*and short ckt current limit.
*
*Copyright 2011 by Intersil Corporation
*Refer to data sheet "LICENSE
*STATEMENT", Use of this model indicates
*your acceptance with the terms and
*provisions in the License Statement.
*
*Intended use:
*This Pspice Macromodel is intended to give
*typical DC and AC performance
*characteristics under a wide range of
*external circuit configurations using
*compatible simulation platforms - such as
*iSim PE.
*
*Device performance features supported by
*this model
*Typical, room temp., nominal power supply
*voltages used to produce the following
*characteristics:
*Open and closed loop I/O impedances
*Open loop gain and phase
*Closed loop bandwidth and frequency
*response
*Loading effects on closed loop frequency
*response
*Input noise terms including 1/f effects
*Slew rate
*Input and Output Headroom limits to I/O
*voltage swing
*Supply current at nominal specified supply
*voltages
**
*Device performance features NOT
*supported by this model:
*Harmonic distortion effects
*Disable operation (if any)
*Thermal effects and/or over temperature
*parameter variation
*Limited performance variation vs. supply
*voltage is modeled
*Part to part performance variation due to
*normal process parameter spread
*Any performance difference arising from
*different packaging
* source
:
*                  +input
*                       |    -input
*                       |      | +Vsupply
*                       |      |    |    -Vsupply
*                       |      |    |    |    output
*                       |      |    |    |      |
.subckt ISL28177 Vin+ Vin- V+ V- VOUT
* source ISL28177_SPICEMODEL
*
*Voltage Noise
E_En        IN+ VIN+ 2 0 1
D_D1         1 2 DN
V_V1         1 0 0.07
R_R19         2 0  5000
*
*Input Stage
I_IOS        IN+ VIN- DC 1e-9
C_C1         IN+ VIN-  1.2e-12
C_C2         0 VIN-  2e-12
C_C3         0 IN+ 2e-12
R_R1         VCM VIN-  5e11
R_R2         IN+ VCM  5e11
R_R3         6 V++  4.45e3
R_R4         7 V++  4.45e3
Q_Q1         4 VIN- 3 SuperB
Q_Q2         5 10 3 SuperB
Q_Q3         V-- 3 9 Mirror
Q_Q4         6 8 4 Cascode
Q_Q5         7 8 5 Cascode
I_IEE        3 V-- DC 200e-6
I_IEE1        V++ 8 DC 96e-6
D_D2         8 9 DX
E_EOS         10 11 VC VMID 1E-9
V_VOS         11 IN+ 30E-6
*
*1st Gain Stage
G_G1         V++ 13 6 7 0.06
G_G2         V-- 13 6 7 0.06
R_R5         13 V++  1
R_R6         V-- 13  1
V_V2         12 13 1.7
V_V3         13 14 1.7
D_D3         12 V++ DX
D_D4         V-- 14 DX
*
*2nd Gain Stage
G_G3         V++ 15 13 VMID 4.712E-3
G_G4         V-- 15 13 VMID 4.712E-3
R_R7         15 V++  2122.196e6
R_R8         V-- 15  2122.196e6
V_V4         16 15 1.7
V_V5         15 17 1.7
D_D5         16 V++ DX
D_D6         V-- 17 DX
C_C4         15 V++  1e-9
C_C5         V-- 15  1e-9
*
*Mid supply Ref
R_R9         VMID V++  1
R_R10         V-- VMID  1
E_E1         V++ 0 V+ 0 1
E_E2         V-- 0 V- 0 1
I_ISY        V+ V- DC 1.18e-3
*
*Common Mode Gain Stage with Zero
G_G5         V++ VC VCM VMID 0.1e-6
G_G6         V-- VC VCM VMID 0.1e-6
R_R11         VC 18  1
R_R12         19 VC  1
L_L1        18 V++  318.31927e-6
L_L2        19 V--  318.31927e-6
*
*2nd Pole Stage
G_G7         V++ 20 15 VMID 502.64e-6
G_G8         V-- 20 15 VMID 502.64e-6
G_G9         V++ 21 20 VMID 502.64e-6
G_G10         V-- 21 20 VMID 502.64e-6
R_R13         20 V++  1989.49546
R_R14         V-- 20  1989.49546
R_R15         21 V++  1989.49546
R_R16         V-- 21  1989.49546
C_C6        20 V++  10e-12
C_C7         V-- 20  10e-12
C_C8         21 V++  10e-12
C_C9         V-- 21  10e-12
*
*Output Stage with Correction Current
Sources
G_G11         VOUT V++ V++ 21 1.11e-2
G_G12         V-- VOUT 21 V-- 1.11e-2
G_G13         22 V-- VOUT 21 1.11e-2
G_G14         25 V-- 21 VOUT 1.11e-2
D_D7        21 23 DX
D_D8        24 21 DX
D_D9        V++ 22 DX
D_D10         V++ 25 DX
D_D11         V-- 22 DY
D_D12         V-- 25 DY
V_V6        23 VOUT 0.18
V_V7        VOUT 24 0.18
R_R17         VOUT V++  9E1
R_R18         V-- VOUT  9E1
*
.model SuperB npn
+ is=184E-15 bf=30e3 va=15 ik=70E-3 rb=50
+ re=0.065 rc=35 cje=1.5E-12 cjc=2E-12
+ kf=0 af=0
.model Cascode npn
+ is=502E-18 bf=150 va=300 ik=17E-3
+rb=140 re=0.011 rc=900 cje=0.2E-12
+cjc=0.16E-12f kf=0 af=0
.model Mirror pnp
+ is=4E-15 bf=150 va=50 ik=138E-3 rb=185
+ re=0.101 rc=180 cje=1.34E-12
+ cjc=0.44E-12

+ kf=0 af=0
.model DN D(KF=6.69e-9 AF=1)
.MODEL DX D(IS=1E-12 Rs=0.1)
.MODEL DY D(IS=1E-15 BV=50 Rs=1)
.ends subckt ISL28177
```

FIGURE 23. SPICE NET LIST

Characterization vs Simulation Results

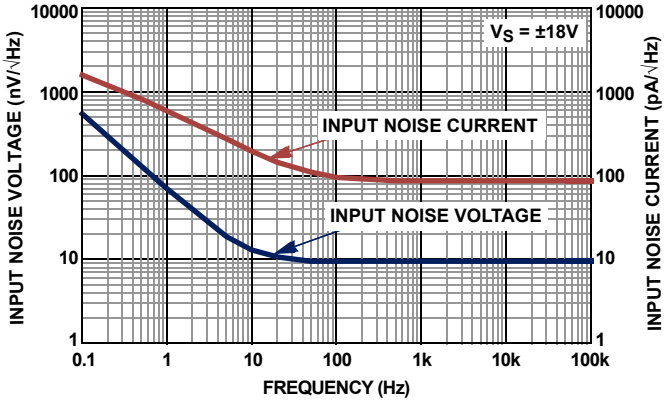


FIGURE 24. CHARACTERIZED INPUT NOISE VOLTAGE

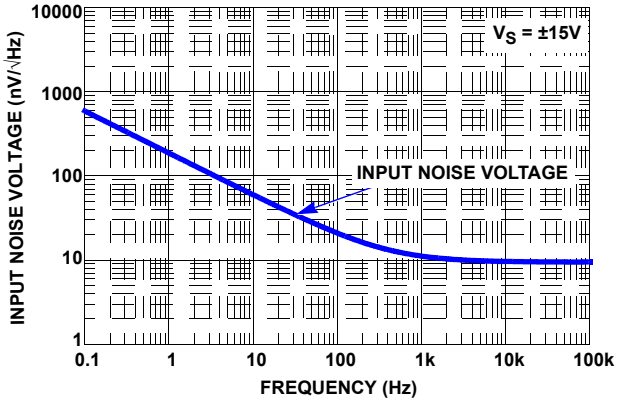


FIGURE 25. SIMULATED INPUT NOISE VOLTAGE

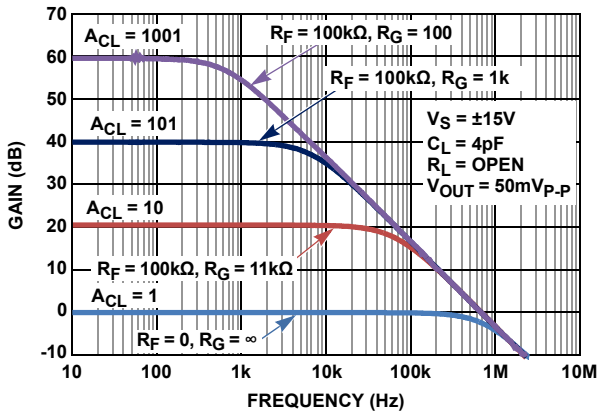


FIGURE 26. CHARACTERIZED CLOSED LOOP GAIN vs FREQUENCY

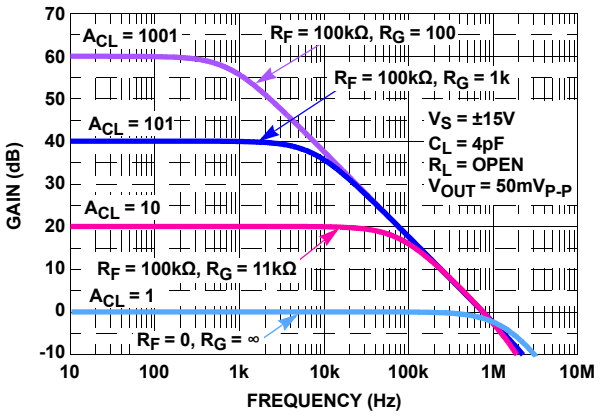


FIGURE 27. SIMULATED CLOSED LOOP GAIN vs FREQUENCY

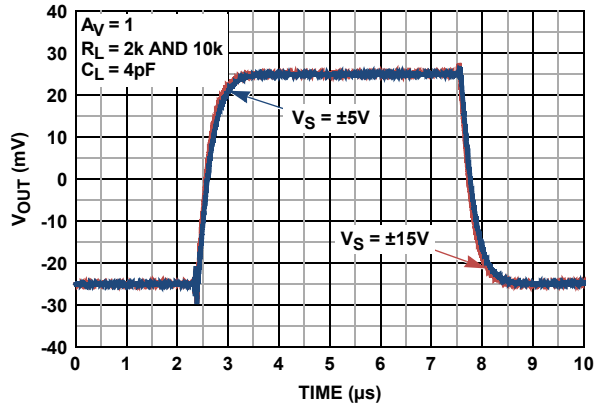


FIGURE 28. CHARACTERIZED SMALL SIGNAL TRANSIENT RESPONSE vs R_L, V_S = ±0.9V, ±2.5V

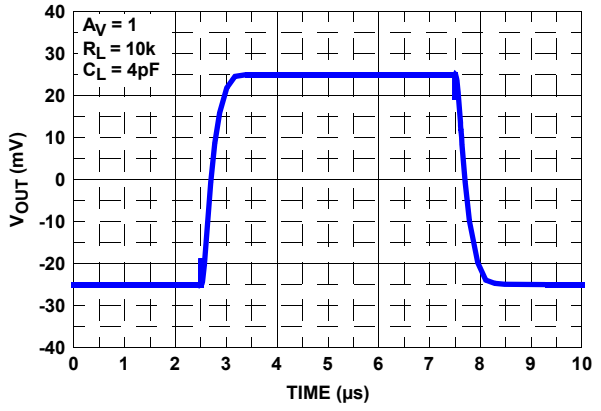


FIGURE 29. SIMULATED SMALL SIGNAL TRANSIENT RESPONSE V_S = ±15V

Characterization vs Simulation Results (Continued)

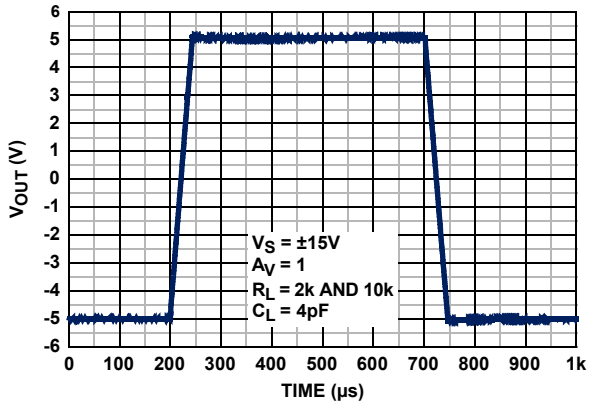


FIGURE 30. CHARACTERIZED LARGE SIGNAL TRANSIENT RESPONSE vs R_L, V_S = ±15V

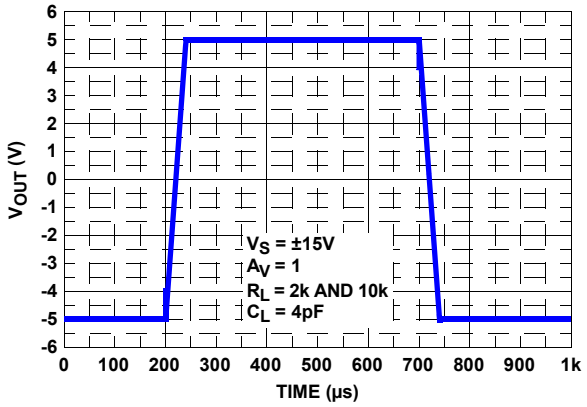


FIGURE 31. SIMULATED LARGE SIGNAL TRANSIENT RESPONSE, V_S = ±14V

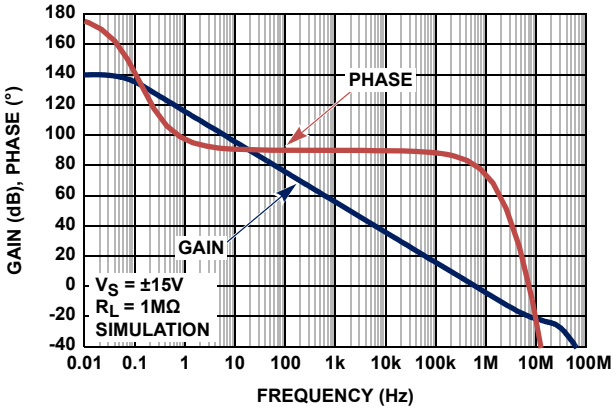


FIGURE 32. SIMULATED (DESIGN) OPEN-LOOP GAIN, PHASE vs FREQUENCY

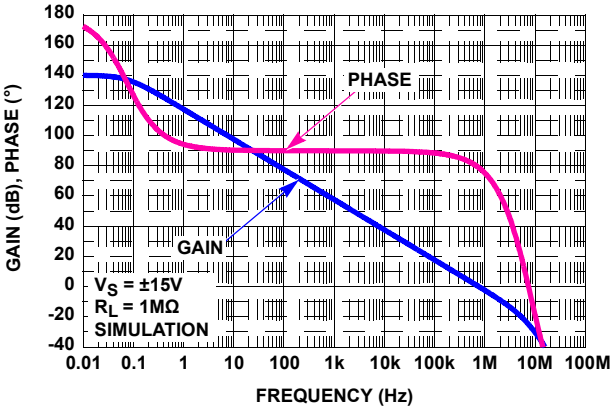


FIGURE 33. SIMULATED (SPICE) OPEN-LOOP GAIN, PHASE vs FREQUENCY

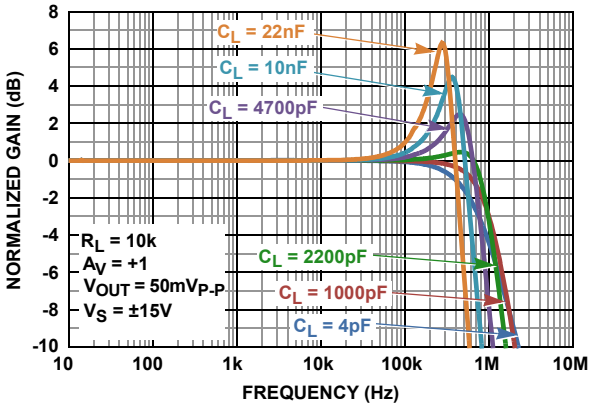


FIGURE 34. CHARACTERIZEDUNITY GAIN FREQUENCY RESPONSE vs C_L

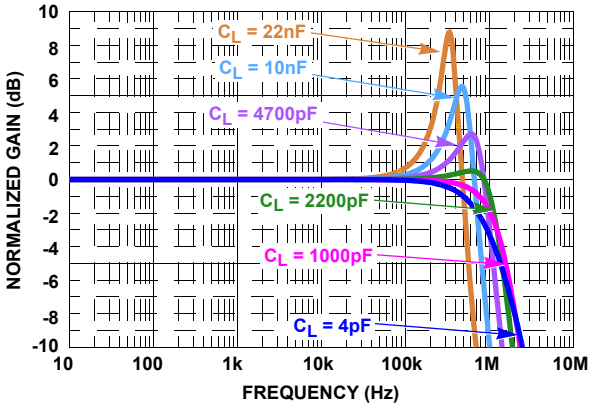


FIGURE 35. SIMULATED UNITY GAIN FREQUENCY RESPONSE vs C_L

Characterization vs Simulation Results (Continued)

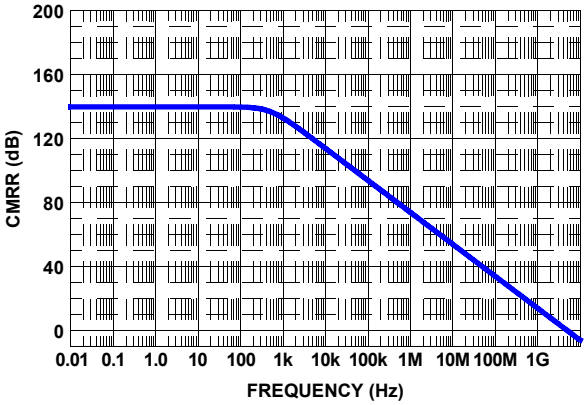


FIGURE 36. SIMULATED (SPICE) CMRR

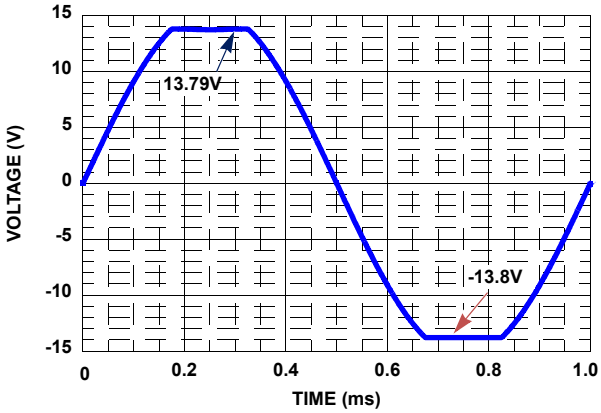


FIGURE 37. SIMULATED OUTPUT VOLTAGE SWING ±15V

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
March 29, 2012	FN7859.2	Changed Note 1 in “Ordering Information” on page 2 from: “Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.” to: “Please refer to TB347 for details on reel specifications.” Listed out tape and reel parts individually in “Ordering Information” on page 2 (ISL28177FBZ-T13, ISL28177FBZ-T7, ISL28177FBZ-T7A)
January 5, 2012	FN7859.1	Added SPICE model to data sheet. Added ESD Ratings to description on page 1.
October 31, 2011	FN7859.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28177

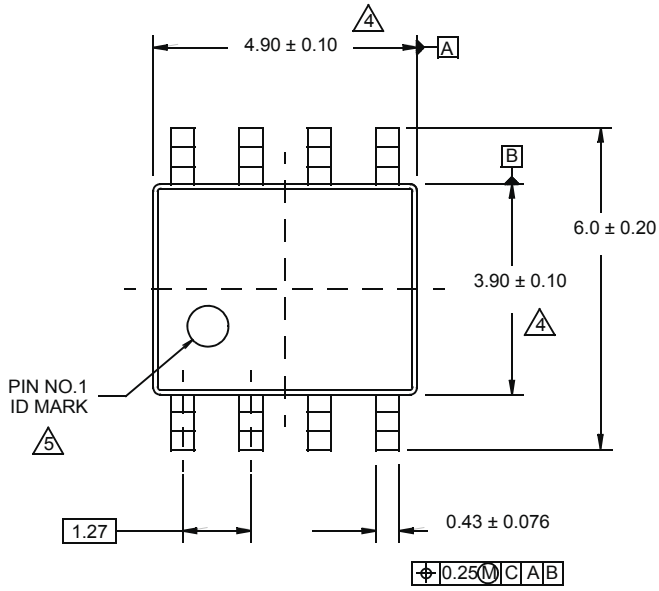
To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/sear

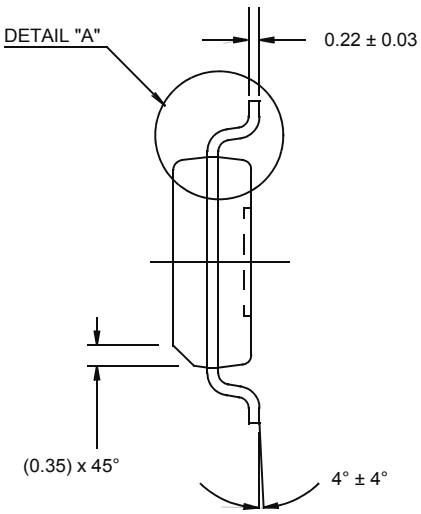
Package Outline Drawing (M8.15E)

M8.15E

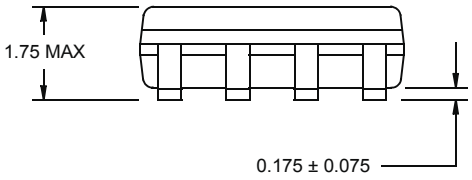
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



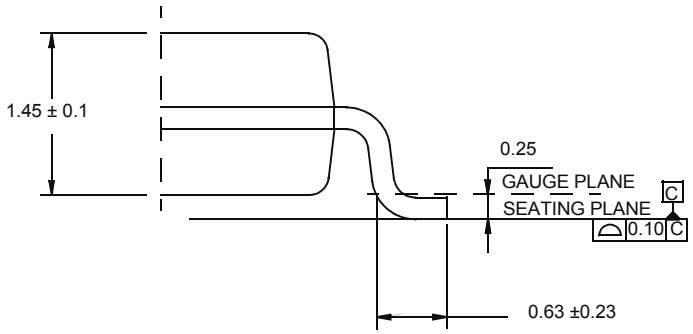
TOP VIEW



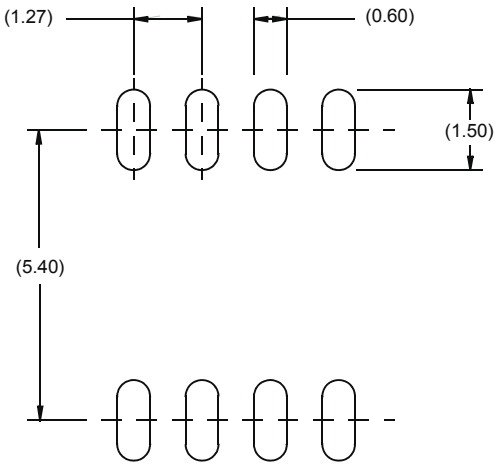
SIDE VIEW "B"



SIDE VIEW "A"



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

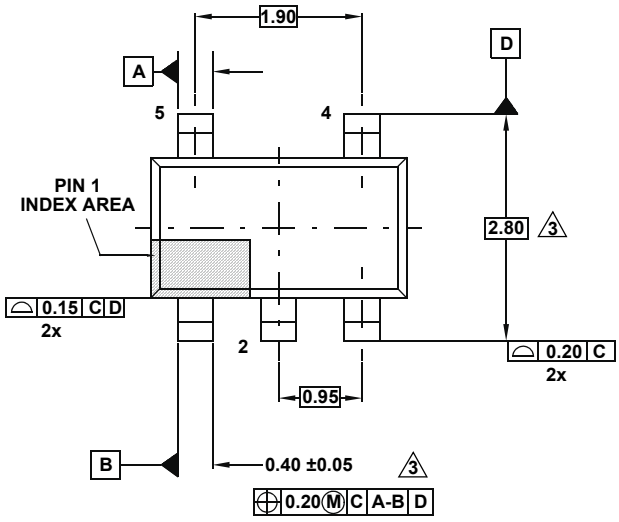
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

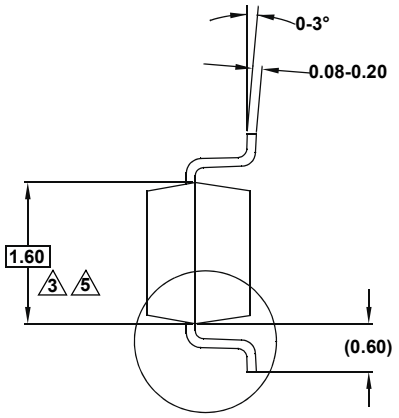
Package Outline Drawing

P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10

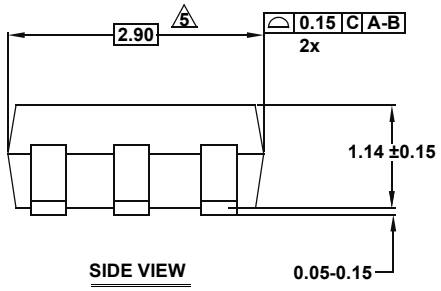


TOP VIEW

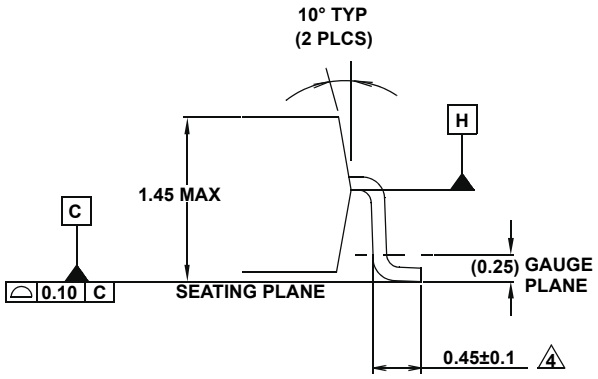


SEE DETAIL X

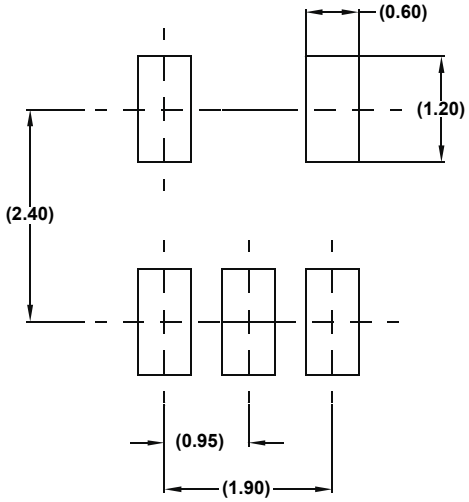
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.