NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ISL43L210

ISL43L220

Ultra Low ON-Resistance, Low Voltage, Single Supply, Dual SPDT Analog Switch

FN6093
Rev 2.00
Feb 27, 2013

The Intersil ISL43L220 device is a low ON-resistance, low voltage, bidirectional, dual single-pole/double-throw (SPDT) analog switch designed to operate from a single +1.1V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low R_{ON} (0.22Ω) and fast switching speeds (t_{ON} = 11ns, t_{OFF} = 5ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to “mux-in” additional functionality while reducing ASIC design risk. The ISL43L220 is offered in a small form factor package, alleviating board space limitations.

The ISL43L220 is a committed dual single-pole/double-throw (SPDT) that consist of two normally open (NO) and two normally closed (NC) switches. This configuration can also be used as a dual 2-to-1 multiplexer. The ISL43L220 is pin compatible with the MAX4684 and MAX4685.

TABLE 1. FEATURES AT A GLANCE

	ISL43L220
Number of Switches	2
SW	SPDT or 2-1 MUX
4.3V R_{ON}	0.22Ω
4.3V t_{ON}/t_{OFF}	11ns/5ns
3V R_{ON}	0.26Ω
3V t_{ON}/t_{OFF}	14ns/6ns
1.8V R_{ON}	0.5Ω
1.8V t_{ON}/t_{OFF}	20ns/8ns
Packages	10Ld 3x3 thin DFN

Features

- Pb-Free (RoHS Compliant)
- ON Resistance (R_{ON})
  - V+ = +4.3V 0.22Ω
  - V+ = +3.0V 0.26Ω
  - V+ = +1.8V 0.5Ω
- R_{ON} Matching Between Channels. 0.03Ω
- R_{ON} Flatness Across Signal Range 0.03Ω
- Single Supply Operation. . . . . +1.1V to +4.5V
- Low Power Consumption (PD). . . . . <0.3µW
- Fast Switching Action (V+ = +4.3V)
  - t_{ON} 11ns
  - t_{OFF} 5ns
- Guaranteed Break-Before-Make
- 1.8V Logic Compatible (+3V supply)
- Available in 10 lead 3x3 thin DFN
- ESD HBM Rating . . . . . >9kV

Applications

- Battery powered, handheld, and portable equipment
  - Cellular/mobile phones
  - Pagers
  - Laptops, notebooks, palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and video switching

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Ordering Information

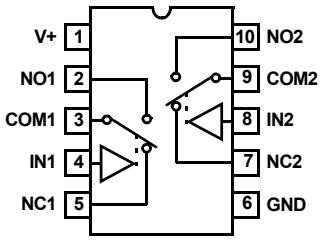
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL43L220IRZ (Notes 2, 3)	220Z	-40 to 85	10 Ld 3x3 thin DFN	L10.3x3A
ISL43L220IRZ-T (Notes 1, 2, 3)	220Z	-40 to 85	10 Ld 3x3 thin DFN Tape and Reel	L10.3x3A

NOTE:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL43L220. For more information on MSL, please see tech brief TB363.

Pinout (Note 4)

ISL43L220
(10 LD TDFN)
TOP VIEW



NOTE:

4. Switches Shown for Logic “0” Input.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.1V to +4.5V)
GND	Ground Connection
IN	Digital Control Input
COM	Analog Switch Common Pin
NO	Analog Switch Normally Open Pin
NC	Analog Switch Normally Closed Pin

Truth Table

LOGIC	PIN NC	PIN NO
0	ON	OFF
1	OFF	ON

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
NO, NC, IN (Note 5) . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
COM (Note 5) . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating:
HBM . . . . . >9kV
MM . . . . . >500V
CDM . . . . . >1kV

Thermal Information

Thermal Resistance (Typical, Notes 6, 7)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package	47	10.5

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
ISL43L220IR . . . . . -40°C to 85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Notes 8, 10), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (See Figure 5)	25	-	0.23	0.35	Ω
		Full	-	-	0.35	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max R_{ON} (Note 13)	25	-	0.03	0.06	Ω
		Full	-	-	0.06	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Note 11)	25	-	0.03	0.08	Ω
		Full	-	-	0.08	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-60	-	60	nA
		Full	-110	-	110	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-60	-	60	nA
		Full	-100	-	100	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	12	17	ns
		Full	-	-	22	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	5	10	ns
		Full	-	-	15	ns
Break-Before-Make Time Delay, t_D	V+ = 4.5V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 12)	Full	2	4	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	128	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 4)	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (See Figure 6)	25	-	-95	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.003	-	%

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.6V, V_{INL} = 0.5V (Notes 8, 10), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	115	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	224	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.1	-	4.5	V
Positive Supply Current, I+	V+ =1.1V to 4.5V, V_{IN} = 0V or V+	25	-	-	0.06	µA
		Full	-	-	1	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.6	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+ (Note 12)	Full	-0.5	-	0.5	µA

NOTES:

8. V_{IN} = input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
11. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
12. Guaranteed but not tested.
13. R_{ON} matching between channels is calculated by subtracting the channel with the highest max R_{ON} value from the channel with lowest max R_{ON} value, between NC1 and NC2 or between NO1 and NO2.

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 8, 10), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (See Figure 5, Note 12)	25	-	0.29	0.4	Ω
		Full	-	-	0.4	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC}= Voltage at max R_{ON} (Notes 12, 13)	25	-	0.03	0.06	Ω
		Full	-	-	0.06	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Notes 11, 12)	25	-	0.03	0.1	Ω
		Full	-	-	0.1	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-	1.1	-	nA
		Full	-	25	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-	1.7	-	nA
		Full	-	48	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	14	20	ns
		Full	-	-	25	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	6	12	ns
		Full	-	-	17	ns
Break-Before-Make Time Delay, t_D	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 12)	Full	2	7	-	ns

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Notes 8, 10), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	95	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 4)	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 6)	25	-	-95	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.003	-	%
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	115	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	224	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.1	-	4.5	V
Positive Supply Current, I+	V+ =1.1V to 3.6V, V_{IN} = 0V or V+	25	-	0.014	-	µA
		Full	-	0.52	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+ (Note 12)	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.8V Supply

Test Conditions: V+ = +1.65V to +2V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.4V (Notes 8, 10), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.65V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5, Note 12)	25	-	0.5	0.8	Ω
		Full	-	-	0.8	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 2.0V, V_{COM} = 0.3V, 1.8V, V_{NO} or V_{NC} = 1.8V, 0.3V	25	-	1.1	-	nA
		Full	-	25	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 2.0V, V_{COM} = 0.3V, 1.8V, or V_{NO} or V_{NC} = 0.3V, 1.8V, or Floating	25	-	1.7	-	nA
		Full	-	48	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	22	28	ns
		Full	-	-	33	ns
Turn-OFF Time, t_{OFF}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	9	15	ns
		Full	-	-	20	ns
Break-Before-Make Time Delay, t_D	V+ = 2.0V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 12)	Full	2	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (See Figure 2)	25	-	49	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 4)	25	-	68	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (See Figure 6)	25	-	-95	-	dB
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	115	-	pF

Electrical Specifications - 1.8V Supply

Test Conditions: V+ = +1.65V to +2V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.4V (Notes 8, 10), Unless Otherwise Specified **(Continued)**

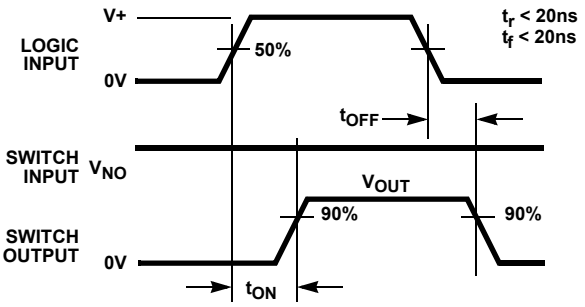
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (See Figure 7)	25	-	224	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.4	V
Input Voltage High, V_{INH}		Full	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+ (Note 12)	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.1V Supply

Test Conditions: V+ = +1.1V, GND = 0V, V_{INH} = 1.0V, V_{INL} = 0.3V (Note 4), Unless Otherwise Specified

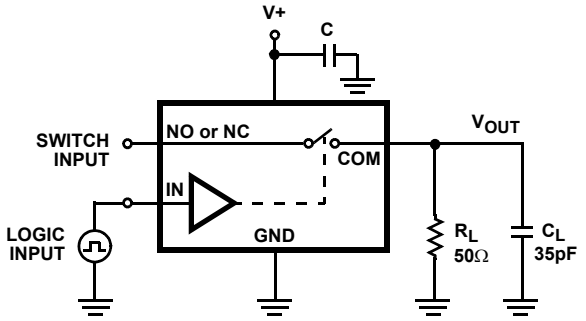
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 9) MIN	TYP	(NOTE 9) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.1V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+, (See Figure 5)	25	-	2.6	3	Ω
		Full	-	3.4	4	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.1V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	30	-	ns
		Full	-	35	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.1V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 1, Note 12)	25	-	15	-	ns
		Full	-	20	-	ns
Break-Before-Make Time Delay, t_D	V+ = 1.1V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 3, Note 12)	Full	-	4	-	ns
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	0.3	-	V
Input Voltage High, V_{INH}		Full	-	0.6	-	V
Input Current, I_{INH}, I_{INL}	V+ = 1.1V, V_{IN} = 0V or V+ (Note 12)	Full	-	0.5	-	µA

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

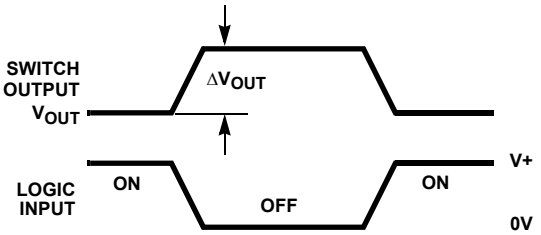


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

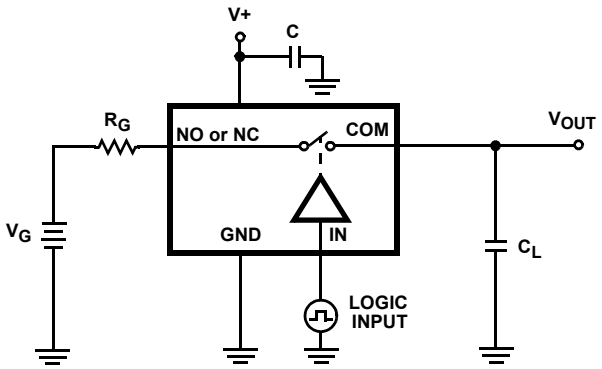
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

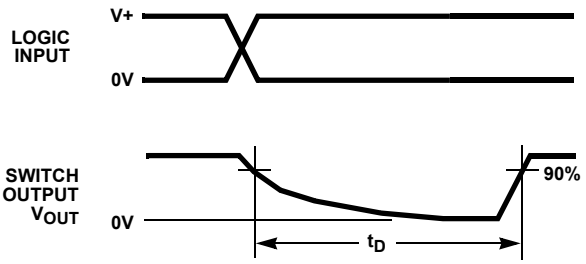
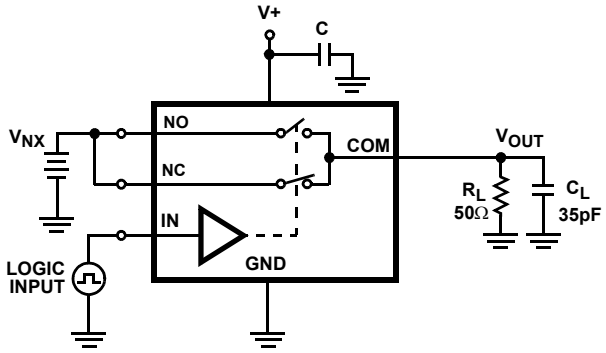


FIGURE 3A. MEASUREMENT POINTS

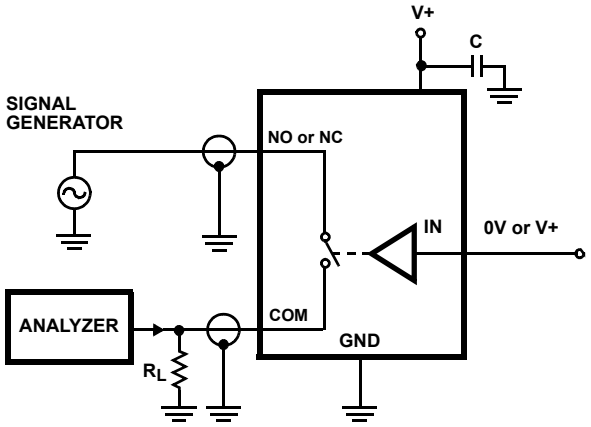


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

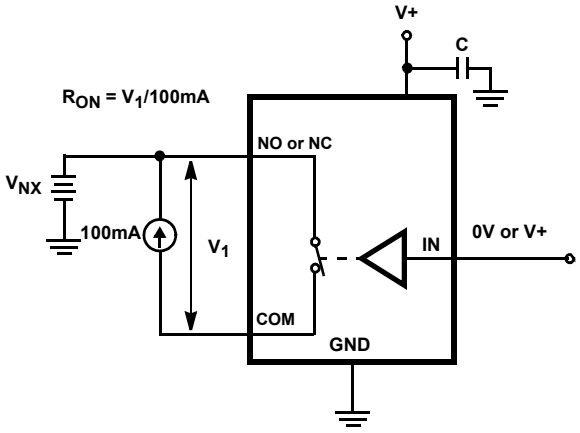
FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



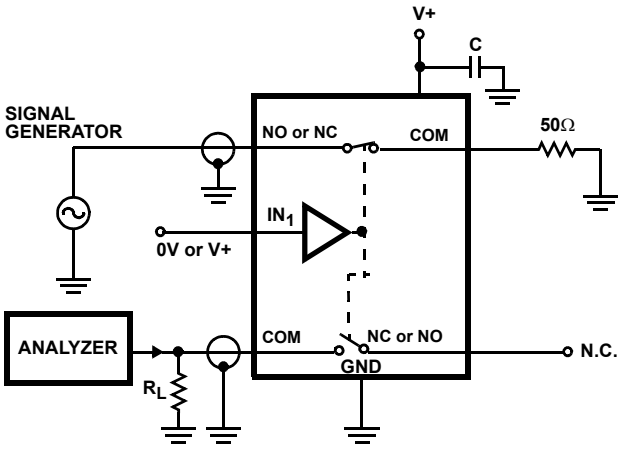
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. OFF ISOLATION TEST CIRCUIT



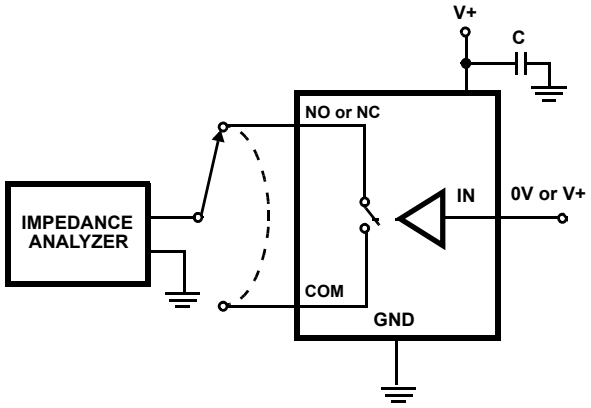
Repeat test for all switches.

FIGURE 5. R_{ON} TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43L220 is a bidirectional, dual single pole/double throw (SPDT) analog switch that offers precise switching capability from a single 1.1V to 4.5V supply with low on-resistance (0.22Ω) and high speed operation (t_{ON} = 11ns, t_{OFF} = 5ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.1V), low power consumption (4.5µW max), low leakage currents (110nA max), and the tiny DFN package. The ultra low on-resistance and Ron flatness provide very low insertion loss and distortion to applications that require signal reproduction.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage

protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch signal range is reduced and the resistance may increase, especially at low supply voltages.

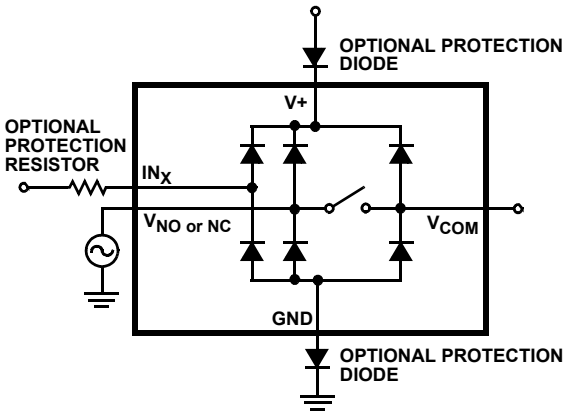


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43L220 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL43L220 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.1V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND also power the internal logic and level shifters. The level shifters convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.0V to 3.6V (see Figure 16). At 3.6V the V_{IH} level is about 1.27V. This is still below the 1.8V CMOS guaranteed high output minimum level of 1.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, the signal response is reasonably flat even past 30MHz with a -3dB bandwidth of 120MHz (see Figure 19). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this part. At 100kHz, Off Isolation is about 68dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

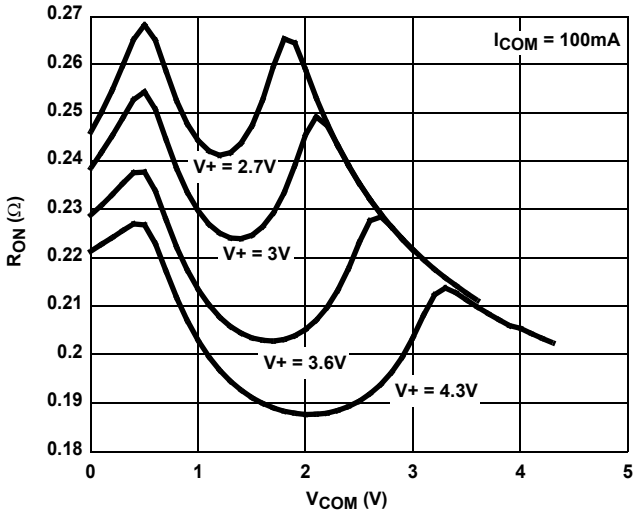


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

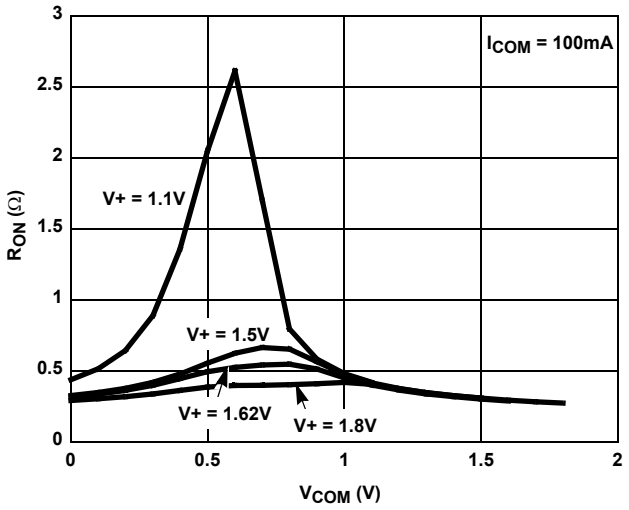


FIGURE 10. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

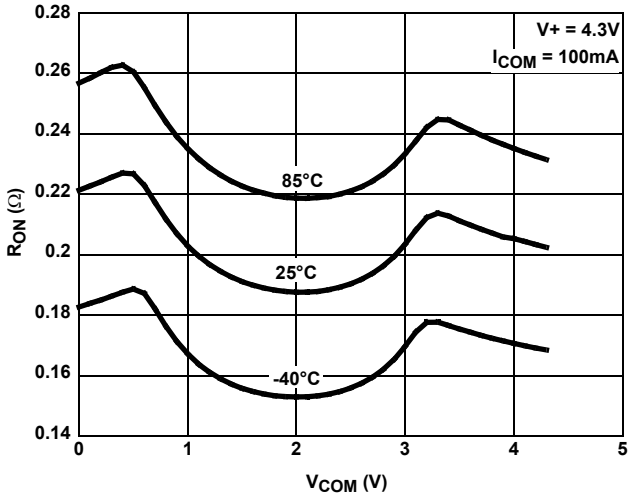


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

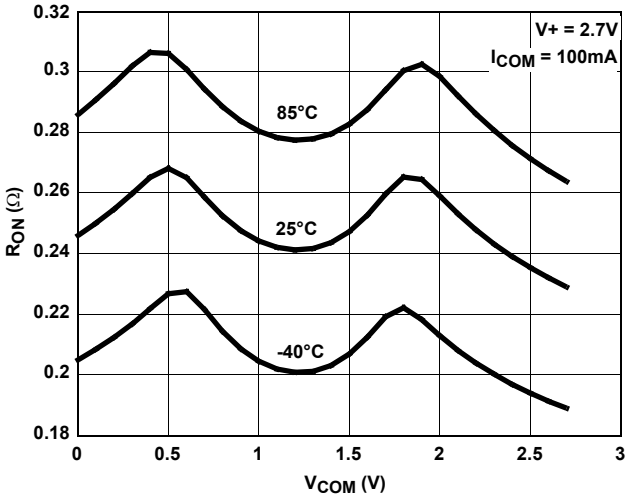


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

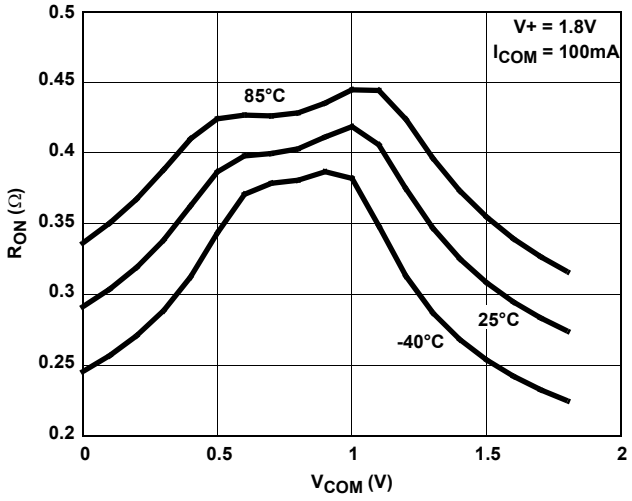


FIGURE 13. ON RESISTANCE vs SWITCH VOLTAGE

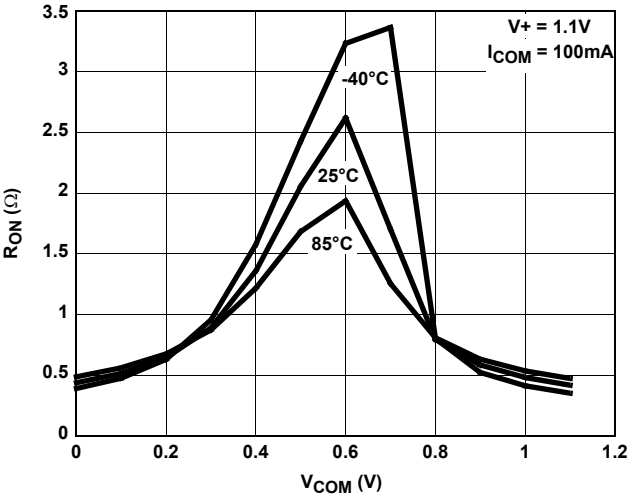


FIGURE 14. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

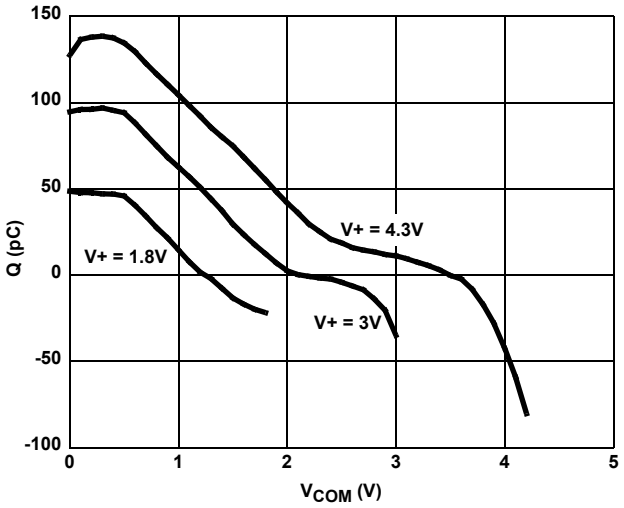


FIGURE 15. CHARGE INJECTION vs SWITCH VOLTAGE

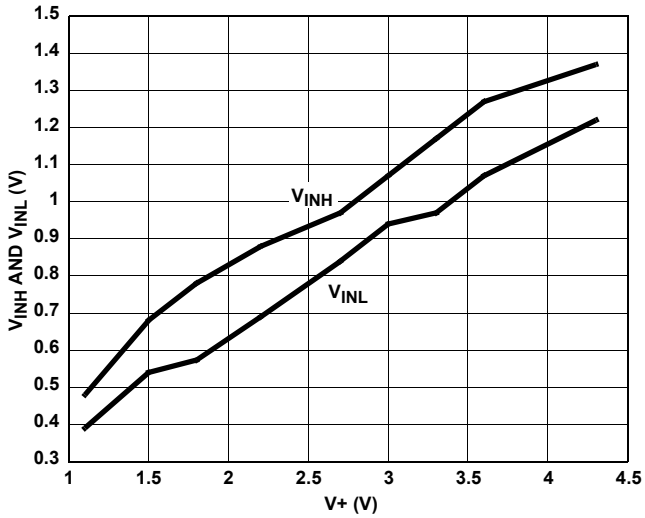


FIGURE 16. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

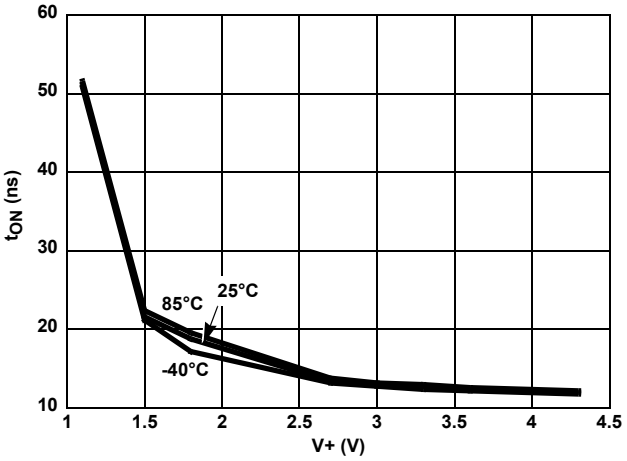


FIGURE 17. TURN - ON TIME vs SUPPLY VOLTAGE

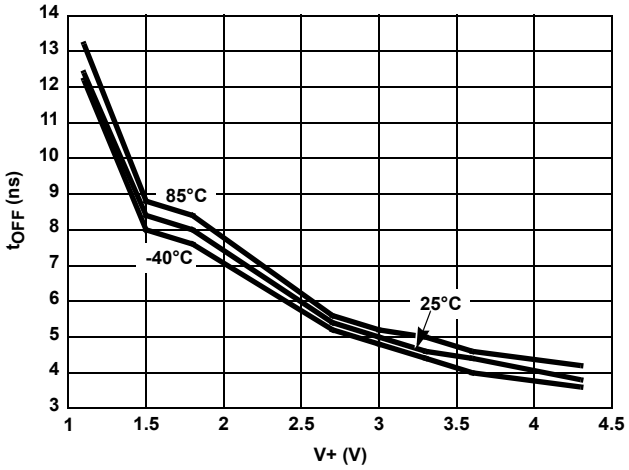


FIGURE 18. TURN - OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

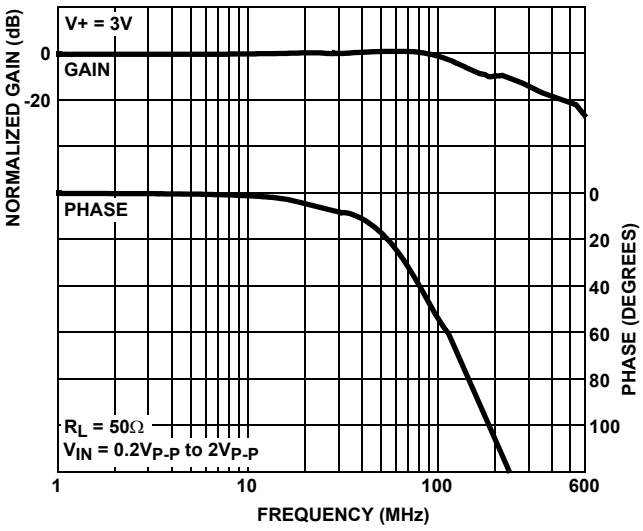


FIGURE 19. FREQUENCY RESPONSE

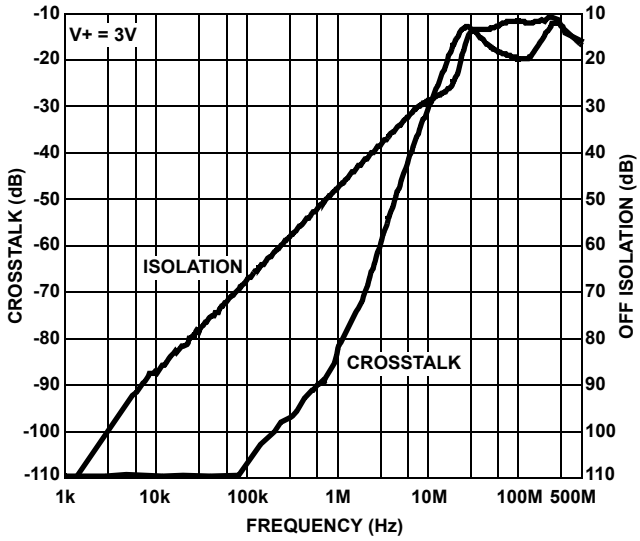


FIGURE 20. CROSSTALK AND OFF ISOLATION

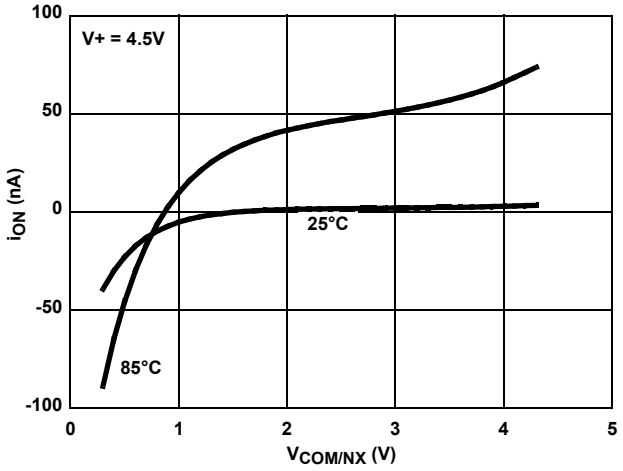


FIGURE 21. ON LEAKAGE vs SWITCH VOLTAGE

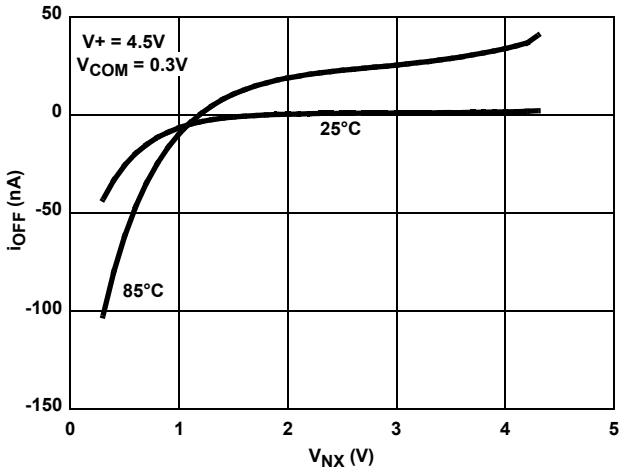


FIGURE 22. OFF LEAKAGE vs SWITCH VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

114

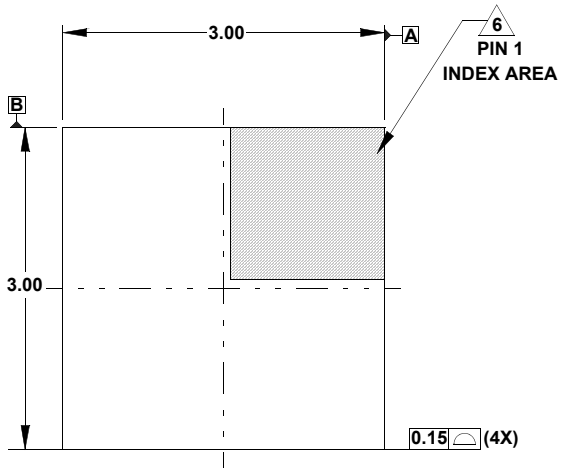
PROCESS:

Submicron CMOS

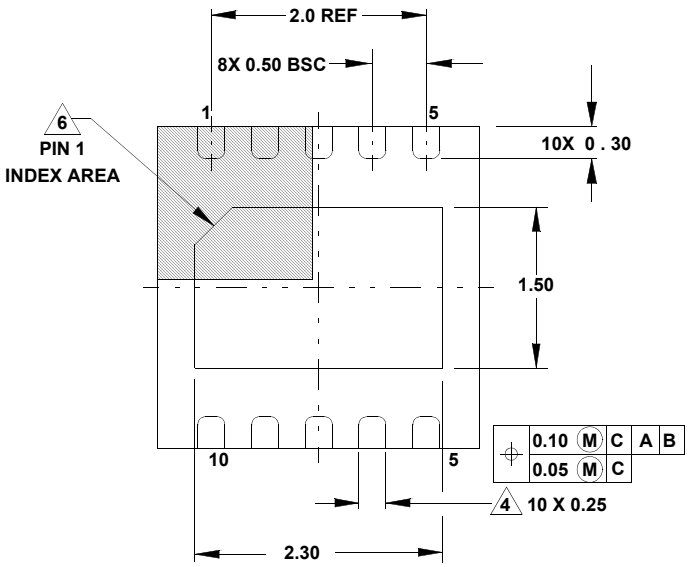
Package Outline Drawing

L10.3x3A

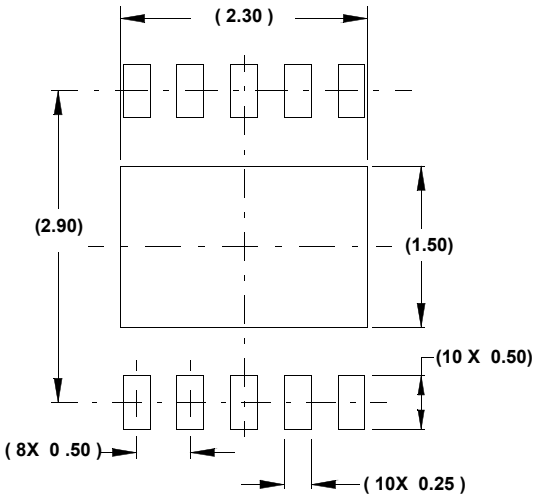
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



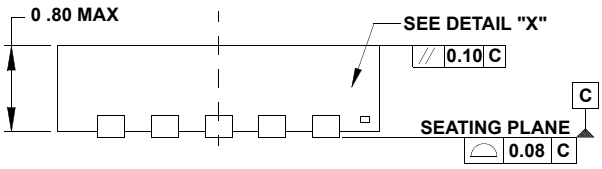
TOP VIEW



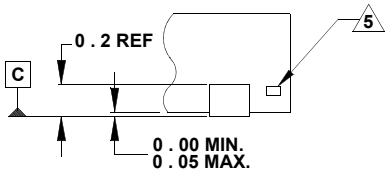
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).