ISL5961

14-Bit, +3.3V, 130/210+MSPS, High Speed D/A Converter

FN6007
Rev 4.00
Oct 7, 2015

The ISL5961 is a 14-bit, 130/210+MSPS (Mega Samples Per Second), CMOS, high speed, low power, D/A (digital to analog) converter, designed specifically for use in high performance communication systems such as base transceiver stations utilizing 2.5G or 3G cellular protocols.

This device complements the ISL5x61 family of high speed converters, which include 10, 12, and 14-bit devices.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #	CLOCK SPEED
ISL5961IBZ **(No longer available, recommended replacement: ISL5961IAZ)** (See Note)	-40 to 85	28 Ld SOIC (Pb-free)	M28.3	130MHz
ISL5961IAZ (See Note)	-40 to 85	28 Ld TSSOP (Pb-free)	M28.173	130MHz
ISL5961/2IBZ (See Note) **(No longer available, recommended replacement: ISL5961/2IAZ)**	-40 to 85	28 Ld SOIC (Pb-free)	M28.3	210MHz
ISL5961/2IAZ (See Note)	-40 to 85	28 Ld TSSOP (Pb-free)	M28.173	210MHz
ISL5961EVAL1	25	SOIC Evaluation Platform		210MHz

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

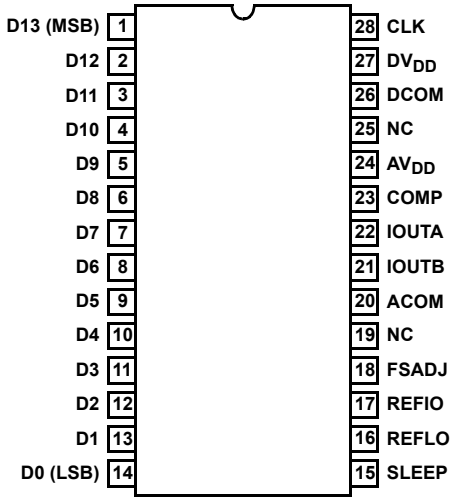
- Speed Grades . . . . . 130M and 210+MSPS
- Low Power . . . . . 103mW with 20mA Output at 130MSPS
- Adjustable Full Scale Output Current . . . . . 2mA to 20mA
- +3.3V Power Supply
- 3V LVCMOS Compatible Inputs
- Excellent Spurious Free Dynamic Range (75dBc to Nyquist, f_S = 130MSPS, f_{OUT} = 10MHz)
- UMTS Adjacent Channel Power =71dB at 19.2MHz
- EDGE/GSM SFDR = 94dBc at 11MHz in 20MHz Window
- Pin compatible, 3.3V, Lower Power Replacement For The AD9754 and HI5960
- Pb-free available

Applications

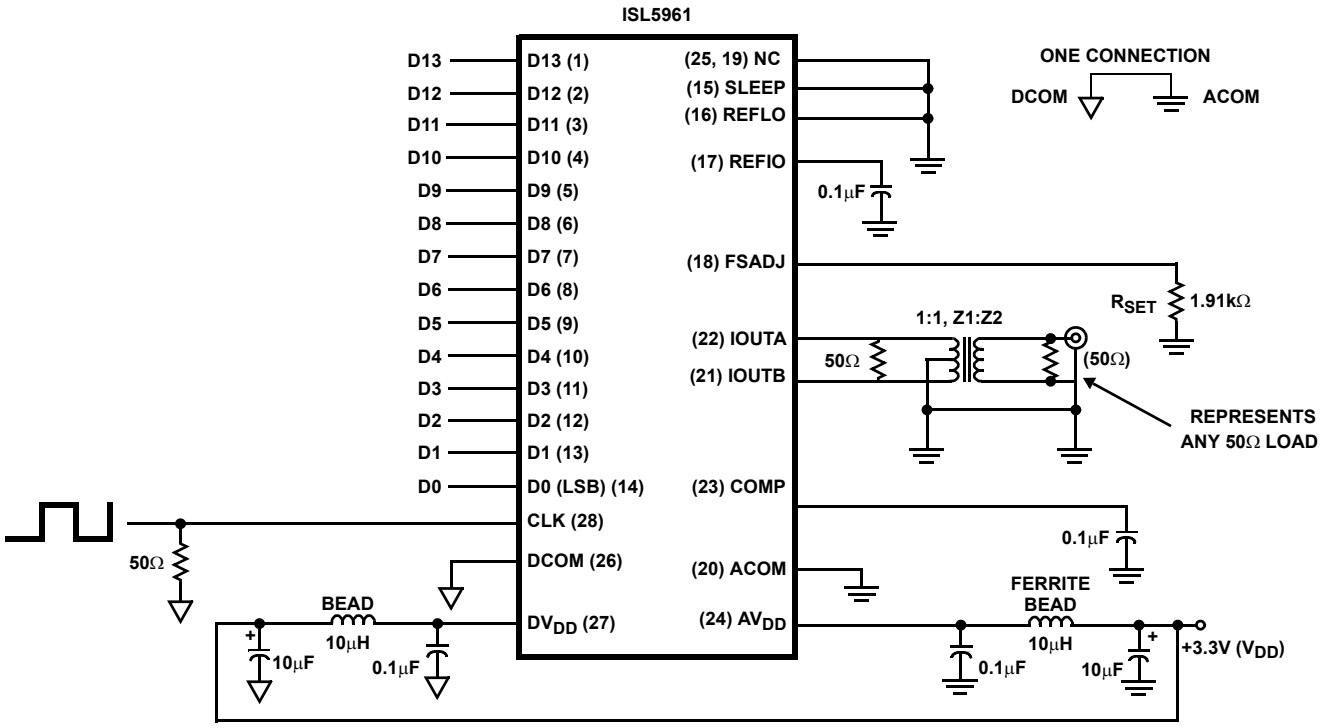
- Cellular Infrastructure - Single or Multi-Carrier: IS-136, IS-95, GSM, EDGE, CDMA2000, WCDMA, TDS-CDMA
- BWA Infrastructure
- Medical/Test Instrumentation
- Wireless Communication Systems
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

Pinout

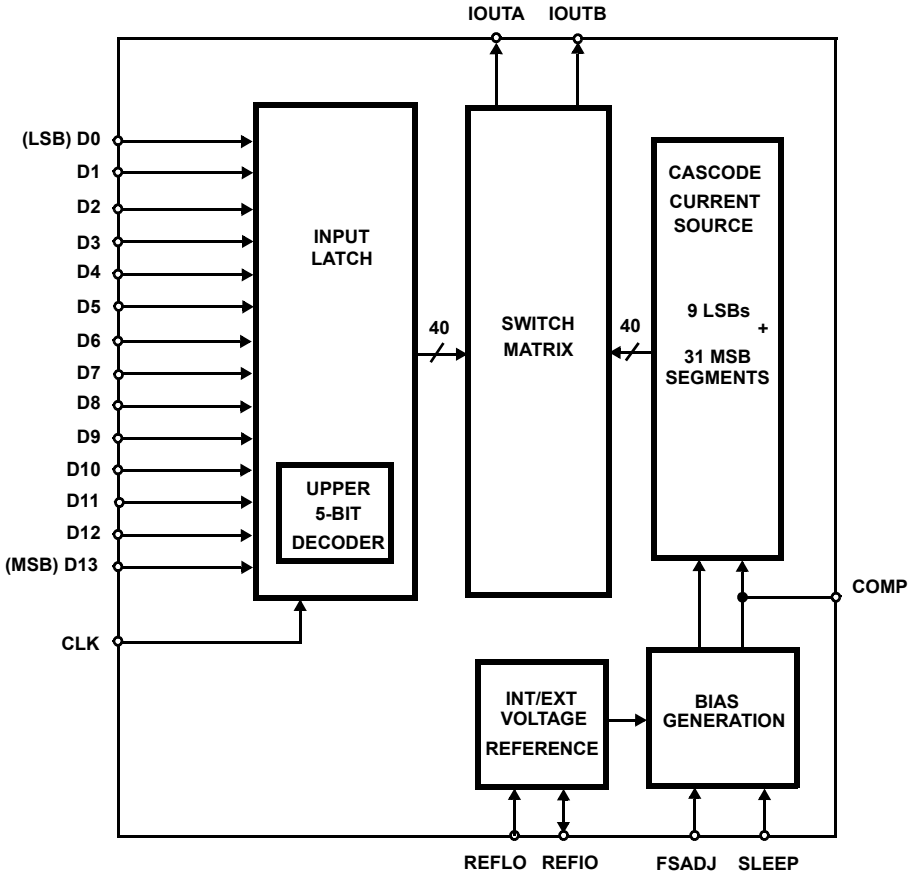
ISL5961
TOP VIEW



Typical Applications Circuit



Functional Block Diagram



Pin Descriptions

PIN NO.	PIN NAME	DESCRIPTION
1-14	D13 (MSB) Through D0 (LSB)	Digital Data Bit 13, (Most Significant Bit) through Digital Data Bit 0, (Least Significant Bit).
15	SLEEP	Control Pin for Power-Down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal 20µA active pulldown current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
18	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}.
19, 25	NC	No Connect. These should be grounded, but can be left disconnected.
21	IOUTB	The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is achieved when all input bits are set to binary 1.
23	COMP	Connect 0.1µF capacitor to ACOM.
24	AV_{DD}	Analog Supply (+2.7V to +3.6V).
20	ACOM	Connect to Analog Ground.
26	DCOM	Connect to Digital Ground.
27	DV_{DD}	Digital Supply (+2.7V to +3.6V).
28	CLK	Clock Input.

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DCOM . . . . . +3.6V
Analog Supply Voltage AV_{DD} to ACOM. . . . . +3.6V
Grounds, ACOM TO DCOM . . . . . -0.3V to +0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP). . . . . DV_{DD} + 0.3V
Reference Input Voltage Range. . . . . AV_{DD} + 0.3V
Analog Output Current (I_{OUT}) 24mA

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA}(°C/W)
SOIC Package	75
TSSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

AV_{DD} = DV_{DD} = +3.3V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		14	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line (Note 7)	-5	±2.5	+5	LSB
Differential Linearity Error, DNL	(Note 7)	-3	±1.5	+3	LSB
Offset Error, I_{OS}	IOUTA (Note 7)	-0.006		+0.006	% FSR
Offset Drift Coefficient	(Note 7)	-	0.1	-	ppm FSR/°C
Full Scale Gain Error, FSE	With External Reference (Notes 2, 7)	-3	±0.5	+3	% FSR
	With Internal Reference (Notes 2, 7)	-3	±0.5	+3	% FSR
Full Scale Gain Drift	With External Reference (Note 7)	-	±50	-	ppm FSR/°C
	With Internal Reference (Note 7)	-	±100	-	ppm FSR/°C
Full Scale Output Current, I_{FS}		2	-	20	mA
Output Voltage Compliance Range	(Note 3)	-1.0	-	1.25	V
DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	ISL5961/2IA, ISL5961/2IB	210	250	-	MHz
Maximum Clock Rate, f_{CLK}	ISL5961IA, ISL5961IB	130	150	-	MHz
Output Rise Time	Full Scale Step	-	1.5	-	ns
Output Fall Time	Full Scale Step	-	1.5	-	ns
Output Capacitance		-	10	-	pF
Output Noise	IOUTFS = 20mA	-	50	-	pA/√Hz
	IOUTFS = 2mA	-	30	-	pA/√Hz
AC CHARACTERISTICS (Using Figure 13 with R_{DIFF} = 50Ω and R_{LOAD}= 50Ω, Full Scale Output = -2.5dBm)					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 210MSPS, f_{OUT} = 80.8MHz, 30MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 210MSPS, f_{OUT} = 40.4MHz, 30MHz Span (Notes 4, 7)	-	82	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 20.2MHz, 20MHz Span (Notes 4, 7)	-	86	-	dBc

Electrical Specifications $AV_{DD} = DV_{DD} = +3.3V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
Spurious Free Dynamic Range, SFDR to Nyquist ($f_{CLK}/2$)	f_{CLK} = 210MSPS, f_{OUT} = 80.8MHz (Notes 4, 7)	-	52	-	dBc
	f_{CLK} = 210MSPS, f_{OUT} = 40.4MHz (Notes 4, 7, 9)	-	61	-	dBc
	f_{CLK} = 200MSPS, f_{OUT} = 20.2MHz, T = 25^oC (Notes 4, 7)	62	64	-	dBc
	f_{CLK} = 200MSPS, f_{OUT} = 20.2MHz, T = -40^oC to 85^oC (Notes 4, 7)	60	-	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 50.5MHz (Notes 4, 7)	-	59	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 40.4MHz (Notes 4, 7)	-	63	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 20.2MHz (Notes 4, 7)	-	70	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 10.1MHz (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.05MHz, T = 25^oC (Notes 4, 7)	72	79	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} = 5.05MHz, T = -40^oC to 85^oC (Notes 4, 7)	70	-	-	dBc
	f_{CLK} = 100MSPS, f_{OUT} = 40.4MHz (Notes 4, 7)	-	61	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 30.3MHz (Notes 4, 7)	-	65	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 20.2MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 10.1MHz (Notes 4, 7, 9)	-	71	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 5.05MHz (Notes 4, 7)	-	78	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 20.2MHz (Notes 4, 7)	-	70	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 10.1MHz (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 5.05MHz (Notes 4, 7)	-	79	-	dBc
Spurious Free Dynamic Range, SFDR in a Window with Eight Tones	f_{CLK} = 210MSPS, f_{OUT} = 28.3MHz to 45.2MHz, 2.1MHz Spacing, 50MHz Span (Notes 4, 7, 9)	-	67	-	dBc
	f_{CLK} = 130MSPS, f_{OUT} =17.5MHz to 27.9MHz, 1.3MHz Spacing, 35MHz Span (Notes 4, 7)	-	70	-	dBc
	f_{CLK} = 80MSPS, f_{OUT} = 10.8MHz to 17.2MHz, 811kHz Spacing, 15MHz Span (Notes 4, 7)	-	77	-	dBc
	f_{CLK} = 50MSPS, f_{OUT} = 6.7MHz to 10.8MHz, 490kHz Spacing, 10MHz Span (Notes 4, 7)	-	78	-	dBc
Spurious Free Dynamic Range, SFDR in a Window with EDGE or GSM	f_{CLK} = 78MSPS, f_{OUT} = 11MHz, in a 20MHz Window, RBW=30kHz (Notes 4, 7, 9)	-	94	-	dBc
Adjacent Channel Power Ratio, ACPR with UMTS	f_{CLK} = 76.8MSPS, f_{OUT} = 19.2MHz, RBW=30kHz (Notes 4, 7, 9)	-	71	-	dB
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{FSADJ}	Pin 18 Voltage with Internal Reference	1.2	1.23	1.3	V
Internal Reference Voltage Drift		-	±40	-	ppm/^oC
Internal Reference Output Current Sink/Source Capability	Reference is not intended to be externally loaded	-	0	-	µA
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 7)	-	1.0	-	MHz
DIGITAL INPUTS D13-D0, CLK					
Input Logic High Voltage with 3.3V Supply, V_{IH}	(Note 3)	2.3	3.3	-	V
Input Logic Low Voltage with 3.3V Supply, V_{IL}	(Note 3)	-	0	1.0	V
Sleep Input Current, I_{IH}		-25	-	+25	µA

Electrical Specifications $AV_{DD} = DV_{DD} = +3.3V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values **(Continued)**

PARAMETER	TEST CONDITIONS	$T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
Input Logic Current, $I_{IH, IL}$		-20	-	+20	µA
Clock Input Current, $I_{IH, IL}$		-10	-	+10	µA
Digital Input Capacitance, C_{IN}		-	5	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 15	-	1.5	-	ns
Data Hold Time, t_{HLD}	See Figure 15	-	1.5	-	ns
Propagation Delay Time, t_{PD}	See Figure 15	-	1	-	Clock Period
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 15 (Note 3)	2	-	-	ns
POWER SUPPLY CHARACTERISTICS					
AV_{DD} Power Supply	(Note 8)	2.7	3.3	3.6	V
DV_{DD} Power Supply	(Note 8)	2.7	3.3	3.6	V
Analog Supply Current (I_{AVDD})	3.3V, IOUTFS = 20mA	-	27.5	28.5	mA
	3.3V, IOUTFS = 2mA	-	10	-	mA
Digital Supply Current (I_{DVDD})	3.3V (Note 5)	-	3.7	5	mA
	3.3V (Note 6)	-	6.5	8	mA
Supply Current (I_{AVDD}) Sleep Mode	3.3V, IOUTFS = Don't Care	-	1.5	-	mA
Power Dissipation	3.3V, IOUTFS = 20mA (Note 5)	-	103	111	mW
	3.3V, IOUTFS = 20mA (Note 6)	-	110	120	mW
	3.3V, IOUTFS = 2mA (Note 5)	-	45	-	mW
Power Supply Rejection	Single Supply (Note 7)	-0.125	-	+0.125	%FSR/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential transformer coupled output and no external filtering. For multitone testing, the same pattern was used at different clock rates, producing different output frequencies but at the same ratio to the clock rate.
5. Measured with the clock at 130MSPS and the output frequency at 5MHz.
6. Measured with the clock at 200MSPS and the output frequency at 20MHz.
7. See "Definition of Specifications."
8. Recommended operation is from 3.0V to 3.6V. Operation below 3.0V is possible with some degradation in spectral performance. Reduction in analog output current may be necessary to maintain spectral performance.
9. See Typical Performance Plots.

Typical Performance (+3.3V Supply, Using Figure 13 with R_{DIFF} = 100Ω and R_{LOAD}= 50Ω)

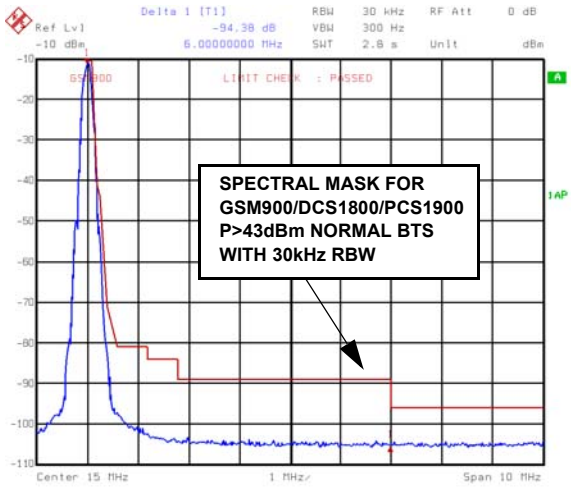


FIGURE 1. EDGE AT 11MHz, 78MSPS CLOCK (94+dBc @ Δf = +6MHz)

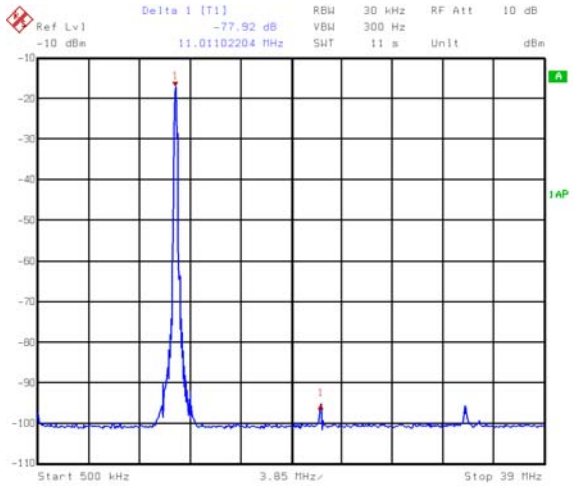


FIGURE 2. EDGE AT 11MHz, 78MSPS CLOCK (77dBc -NYQUIST, 6dB PAD)

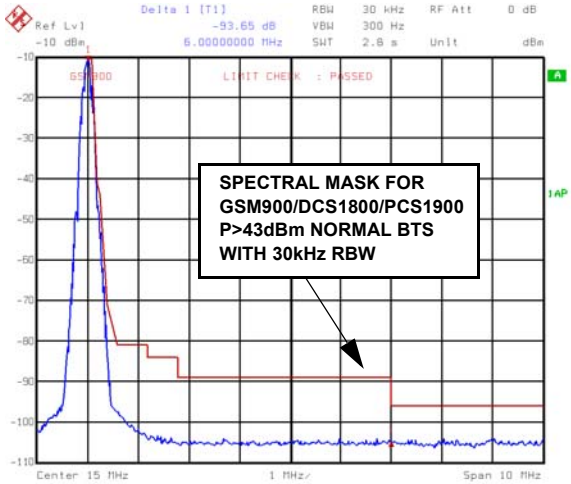


FIGURE 3. GSM AT 11MHz, 78MSPS CLOCK (94+dBc @ Δf = +6MHz, 3dB PAD)

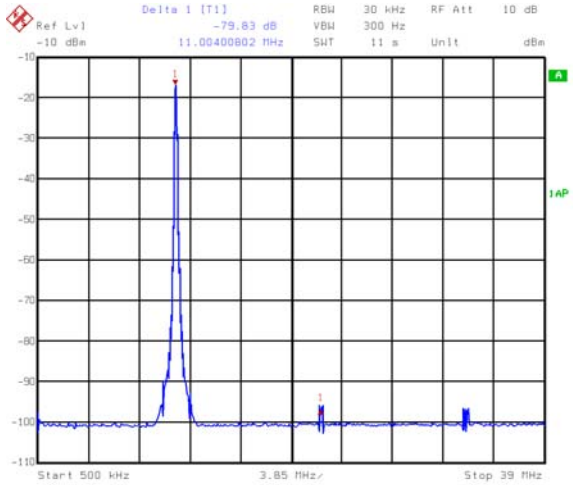


FIGURE 4. GSM AT 11MHz, 78MSPS CLOCK (79dBc - NYQUIST, 9dB PAD)

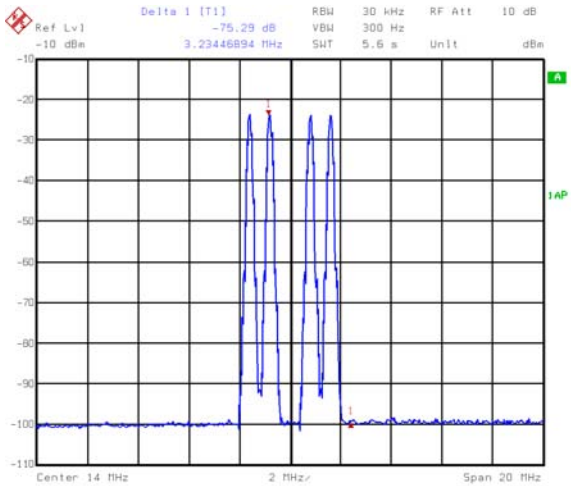


FIGURE 5. FOUR EDGE CARRIERS AT 12.4-15.6MHz, 800kHz SPACING, 78MSPS (75+dBc - 20MHz WINDOW)

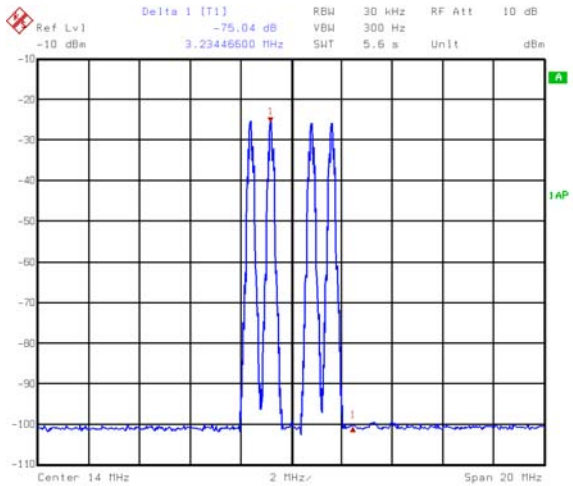


FIGURE 6. FOUR GSM CARRIERS AT 12.4-15.6MHz, 78MSPS (75+dBc - 20MHz WINDOW, 6dB PAD)

Typical Performance (+3.3V Supply, Using Figure 13 with R_{DIFF} = 100Ω and R_{LOAD}= 50Ω) **(Continued)**

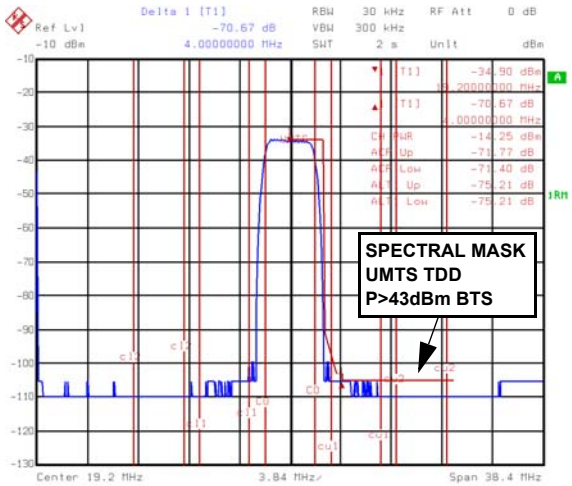


FIGURE 7. UMTS AT 19.2MHz, 76.8MSPS (71dB 1stACPR, 75dB 2ndACPR)

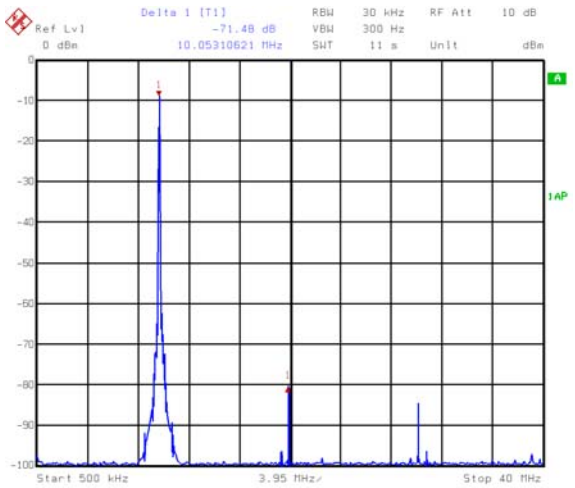


FIGURE 8. ONE TONE AT 10.1MHz, 80MSPS CLOCK (71dBc - NYQUIST, 6dB PAD)

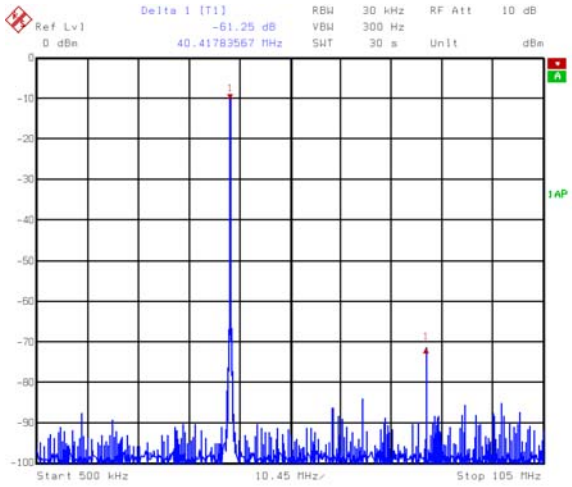


FIGURE 9. ONE TONE AT 40.4MHz, 210MSPS CLOCK (61dBc - NYQUIST, 6dB PAD)

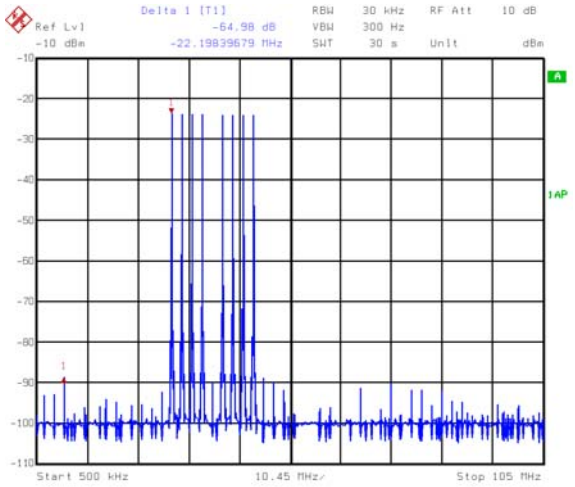


FIGURE 10. EIGHT TONES (CREST FACTOR=8.9) AT 37MHz, 210MSPS CLOCK, 2.1MHz SPACING (65dBc - NYQUIST)

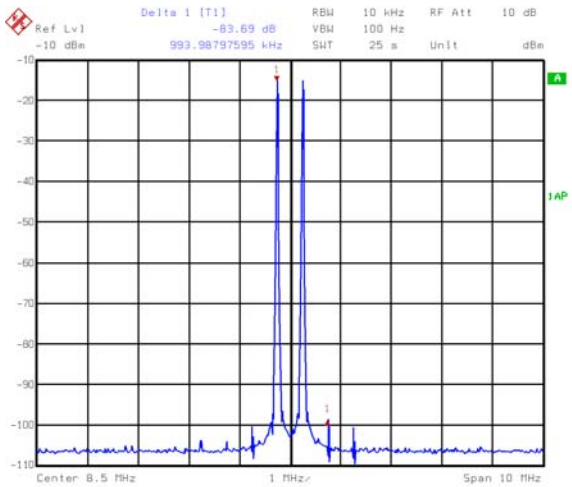


FIGURE 11. TWO TONES (CF=6) AT 8.5MHz, 50MSPS CLOCK, 500kHz SPACING (83dBc - 10MHz WINDOW, 6dB PAD)

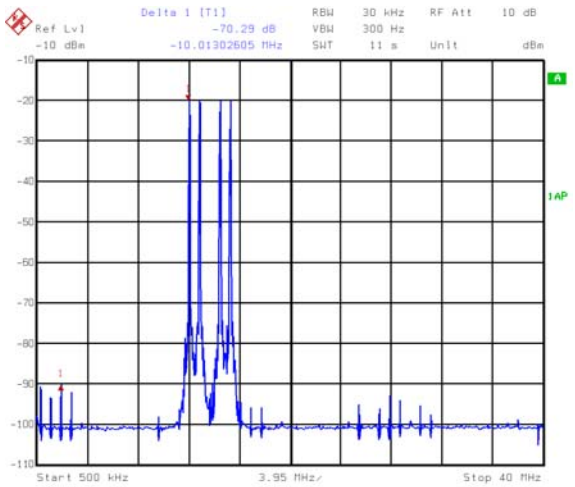


FIGURE 12. FOUR TONES (CF=8.1) AT 14MHz, 80MSPS CLOCK, 800kHz SPACING (70dBc - NYQUIST, 6dB PAD)

Definition of Specifications

Adjacent Channel Power Ratio, ACPR, is the ratio of the average power in the adjacent frequency channel (or offset) to the average power in the transmitted frequency channel.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

EDGE, Enhanced Data for Global Evolution, a TDMA standard for cellular applications which uses 200kHz BW, 8-PSK modulated carriers.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per ^{o}C.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

GSM, Global System for Mobile Communication, a TDMA standard for cellular applications which uses 200kHz BW, GMSK modulated carriers.

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per ^{o}C.

Offset Drift, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage at IOUTA through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per degree ^{o}C.

Offset Error, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage of IOUTA through a known resistance. Offset error is defined as the maximum *deviation* of the IOUTA output current from a value of 0mA.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The nominal supply voltage is varied ±10% and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Total Harmonic Distortion, THD, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

UMTS, Universal Mobile Telecommunications System, a W-CDMA standard for cellular applications which uses 3.84MHz modulated carriers.

Detailed Description

The ISL5961 is a 14-bit, current out, CMOS, digital to analog converter. The maximum update rate is at least 210+MSPS and can be powered by a single power supply in the recommended range of +3.0V to +3.6V. Operation with clock rates higher than 210MSPS is possible; please contact the factory for more information. It consumes less than 120mW of power when using a +3.3V supply, the maximum 20mA of output current, and the data switching at 210MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain, worst-case transition points such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at these major transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems, and accuracy.

Digital Inputs and Termination

The ISL5961 digital inputs are guaranteed to 3V LVCMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are long 50Ω lines, then 50Ω termination resistors should be placed as close to the converter inputs as possible connected to the digital ground plane (if separate grounds are used). These termination resistors are not likely needed as long as the digital waveform source is within a few inches of the DAC. For pattern drivers with very high speed edge rates, it is recommended that the user consider series termination (50-200Ω) prior to the DAC's inputs in order to reduce the amount of noise.

Power Supply

Separate digital and analog power supplies are recommended. The allowable supply range is +2.7V to +3.6V. The recommended supply range is +3.0 to 3.6V (nominally +3.3V) to maintain optimum SFDR. However, operation down to +2.7V is possible with some degradation in SFDR. Reducing the analog output current can help the SFDR at +2.7V. The SFDR values stated in the table of specifications were obtained with a +3.3V supply.

Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane.

Noise Reduction

To minimize power supply noise, 0.1µF capacitors should be placed as close as possible to the converter's power supply pins, AV_{DD} and DV_{DD}. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended.

Voltage Reference

The internal voltage reference of the device has a nominal value of +1.23V with a ±40ppm/^{O}C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1µF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (16) selects the reference. The internal reference can be selected if pin 16 is tied low (ground). If an external reference is desired, then pin 16 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 17. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

If the internal reference is used, V_{FSADJ} will equal approximately 1.2V (pin 18). If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT} (Full Scale) is:

$I_{OUT}(\text{Full Scale}) = (V_{FSADJ}/R_{SET})$ X 32.

If the full scale output current is set to 20mA by using the internal voltage reference (1.2V) and a 1.91kΩ R_{SET} resistor, then the input coding to output current will resemble the following:

TABLE 1. INPUT CODING vs OUTPUT CURRENT WITH INTERNAL REFERENCE AND RSET=1.91KΩ

INPUT CODE (D13-D0)	IOUTA (mA)	IOUTB (mA)
1111 11111 11111	20	0
1000 00000 00000	10	10
0000 00000 00000	0	20

Analog Output

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0V to 1.25V. R_{OUT} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$V_{OUT} = I_{OUT}$ X R_{OUT}.

The most effective method for reducing the power consumption is to reduce the analog output current, which dominates the supply current. The maximum recommended output current is 20mA.

Differential Output

IOUTA and IOUTB can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. With R_{DIFF}= 50Ω and R_{LOAD}=50Ω, the circuit in Figure 13 will provide a 500mV (-2.5dBm) signal at the output of the transformer if the full scale output current of the DAC is set to 20mA (used for the electrical specifications table). Values of R_{DIFF}= 100Ω and R_{LOAD}=50Ω were used for the typical performance curves to increase the output power and the dynamic range. The center tap in Figure 13 must be grounded.

In the circuit in Figure 14, the user is left with the option to ground or float the center tap. The DC voltage that will exist at either IOUTA or IOUTB if the center tap is floating is $IOUT_{DC}$ x (R_A//R_B) V because R_{DIFF} is DC shorted by the transformer. If the center tap is grounded, the DC voltage is 0V. Recommended values for the circuit in Figure 14 are R_A=R_B=50Ω, R_{DIFF}=100Ω, assuming R_{LOAD}=50Ω. The performance of Figure 13 and Figure 14 is basically the same, however leaving the center tap of Figure 14 floating allows the circuit to find a more balanced virtual ground, theoretically improving the even order harmonic rejection, but likely reducing the signal swing available due to the output voltage compliance range limitations.

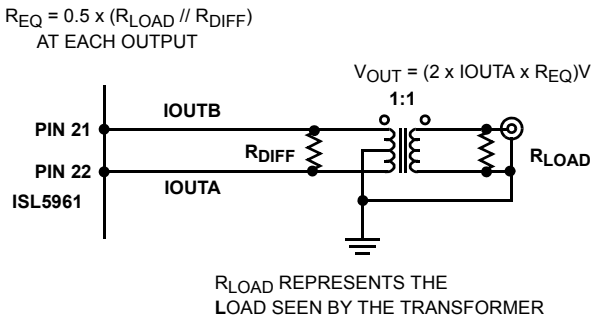


FIGURE 13. OUTPUT LOADING FOR DATASHEET MEASUREMENTS

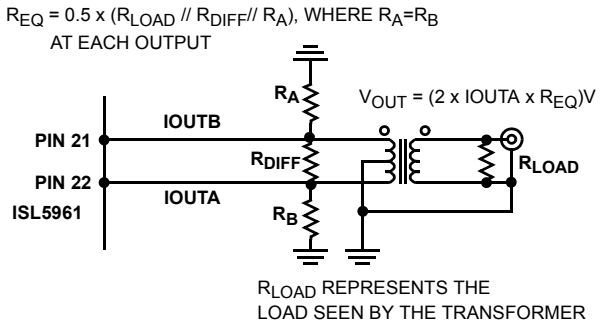


FIGURE 14. ALTERNATIVE OUTPUT LOADING

Timing Diagram

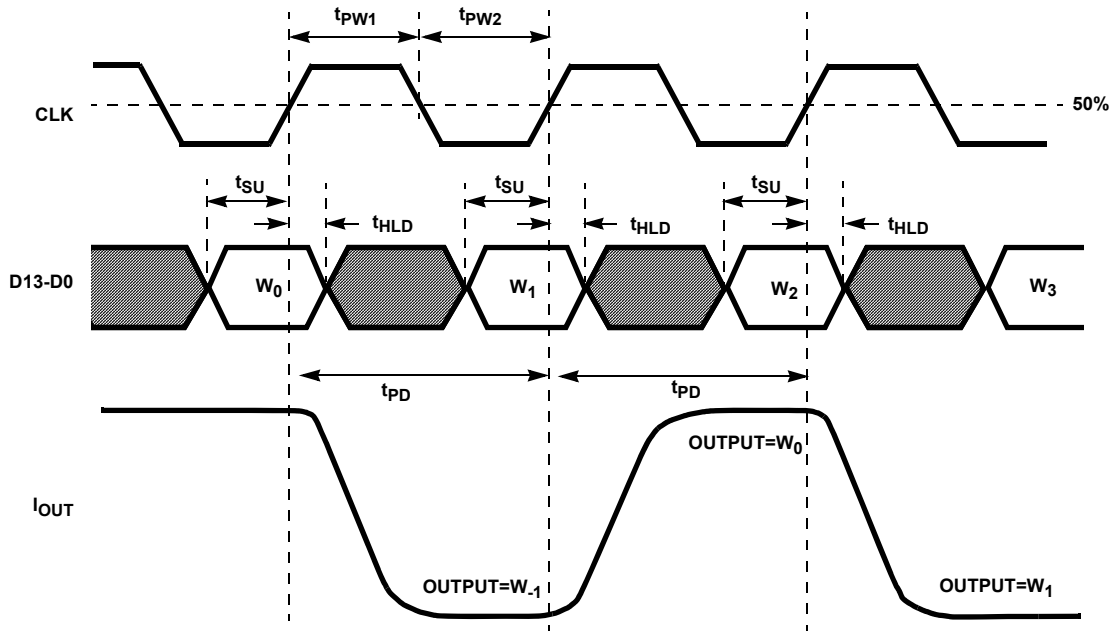


FIGURE 15. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Propagation Delay

The converter requires two clock rising edges for data to be represented at the output. Each rising edge of the clock captures the present data word and outputs the previous data. The propagation delay is therefore 1/CLK, plus <2ns of processing. See Figure 15.

Test Service

Intersil offers customer-specific testing of converters with a service called Testdrive. To submit a request, fill out the Testdrive form. The form can be found by doing an ‘entire site search’ at www.intersil.com on the words ‘DAC Testdrive’. Or, send a request to the technical support center.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
October 7, 2015	FN6007.4	- Updated Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M28.3 to latest revision changes are as follow: Added land pattern. - Updated POD M28.173 to latest revision changes are as follow: Convert to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.

About Intersil

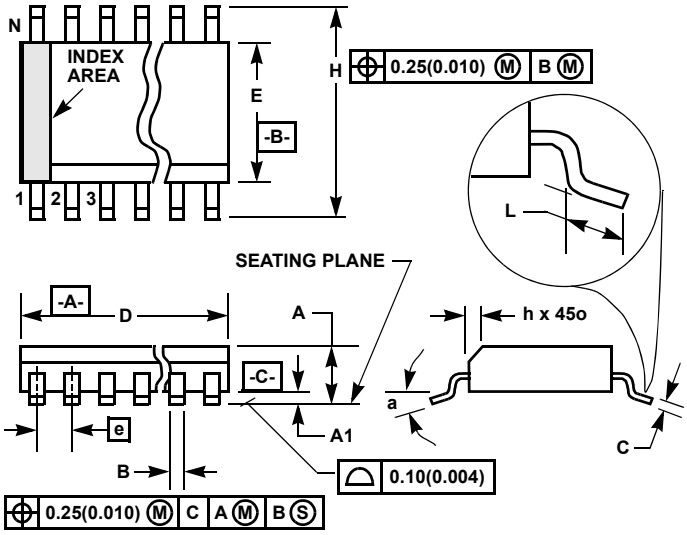
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

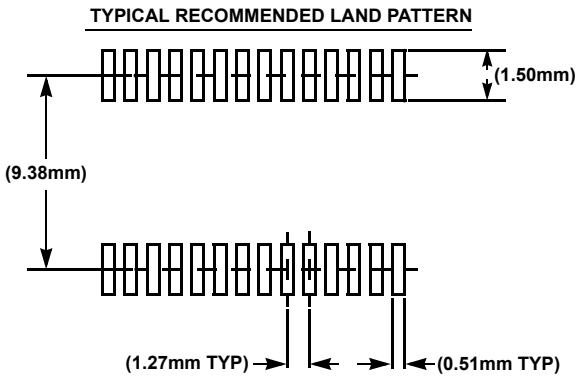
Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 1, 1/13



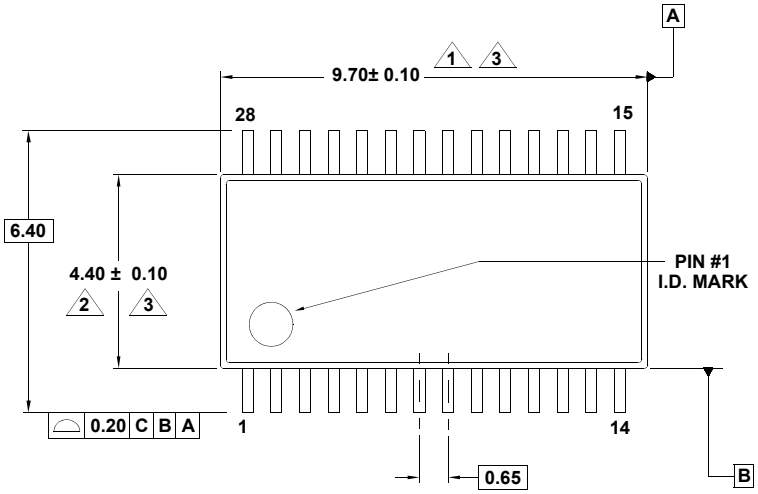
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

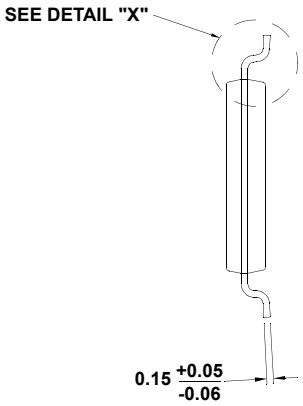
Package Outline Drawing

M28.173

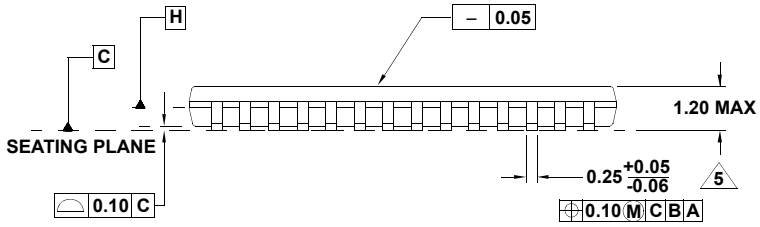
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10



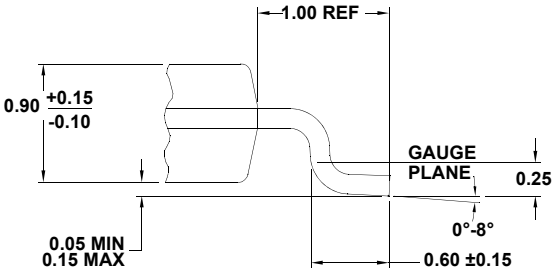
TOP VIEW



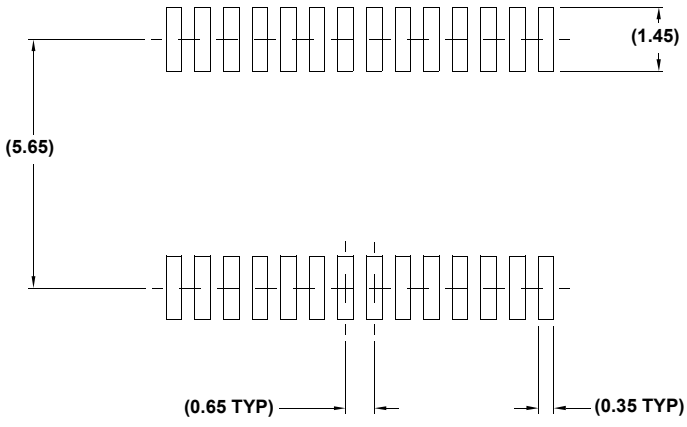
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.