ISL62776

Multiphase PWM Regulator for AMD CPUs Using SVI2

The ISL62776 is fully compliant with AMD Serial VID Interface 2.0 (SVI2) and provides a complete solution for microprocessor and graphics processor core power. The ISL62776 controller supports two Voltage Regulators (VRs) that use external drivers for maximum flexibility. The Core VR can be configured for 4-, 3-, 2-, or 1-phase operation and the SOC VR supports 1-phase operation. The two VRs share a serial control bus to communicate with the AMD CPU and achieve lower cost and smaller board area compared with two-chip solutions.

The R3™ modulator, based on the Renesas Robust Ripple Regulator (R3) technology, has many advantages compared to traditional modulators. These include faster transient settling time, variable switching frequency in response to load transients, and improved light-load efficiency due to diode emulation mode with load-dependent, low-switching frequency.

Both outputs of the ISL62776 support DC Resistance (DCR) current sensing with single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. Both outputs use remote voltage sense, adjustable switching frequency, Overcurrent Protection (OCP), and power-good.

Applications

- AMD CPU/GPU core power
- Notebook computers

Related Literature

For a full list of related documents, visit our website:

- ISL62776 device page

Features

- Supports AMD SVI 2.0 serial data bus interface
  - Serial VID clock frequency range: 100kHz to 25MHz
- Dual output controller with PWM output
- Precision voltage regulation
  - 0.5% system accuracy over-temperature
  - 0.5V to 1.55V in 6.25mV steps
  - Enhanced load-line accuracy
- Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Programmable phase operation for both Core and SOC VR outputs
- Superior noise immunity and transient response
- Output current and voltage telemetry
- Differential remote voltage sensing
- High efficiency across entire load range
- Programmable slew rate
- Programmable VID offset and droop on both outputs
- Programmable switching frequency for both outputs
- Excellent dynamic current balance between phases
- Protection: OCP/WOC, OVP, PGOOD, and thermal monitoring
- Small footprint 40 Ld 5x5 TQFN package
  - Pb-free (RoHS compliant)

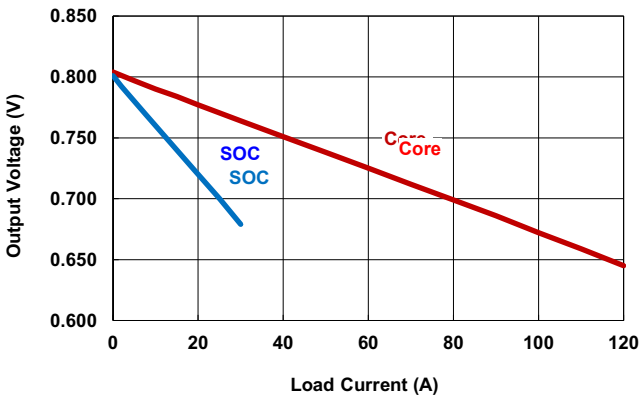


Figure 1. Output Voltage vs Load

Contents

1. Overview

1.1 Simplified Application Circuits

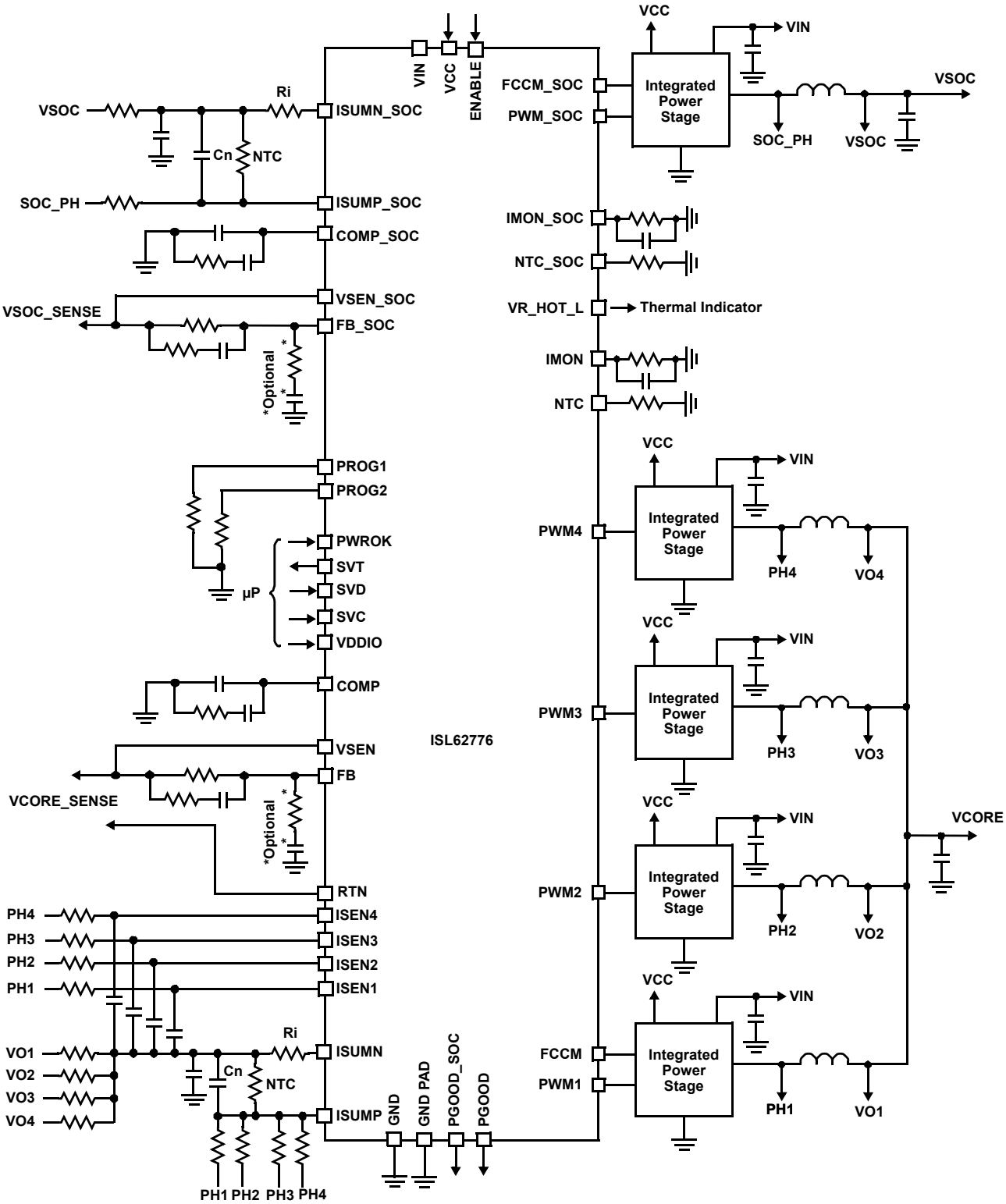


Figure 2. Typical Application Circuit for High-Power CPU Core Using Inductor DCR Sensing, 4+1

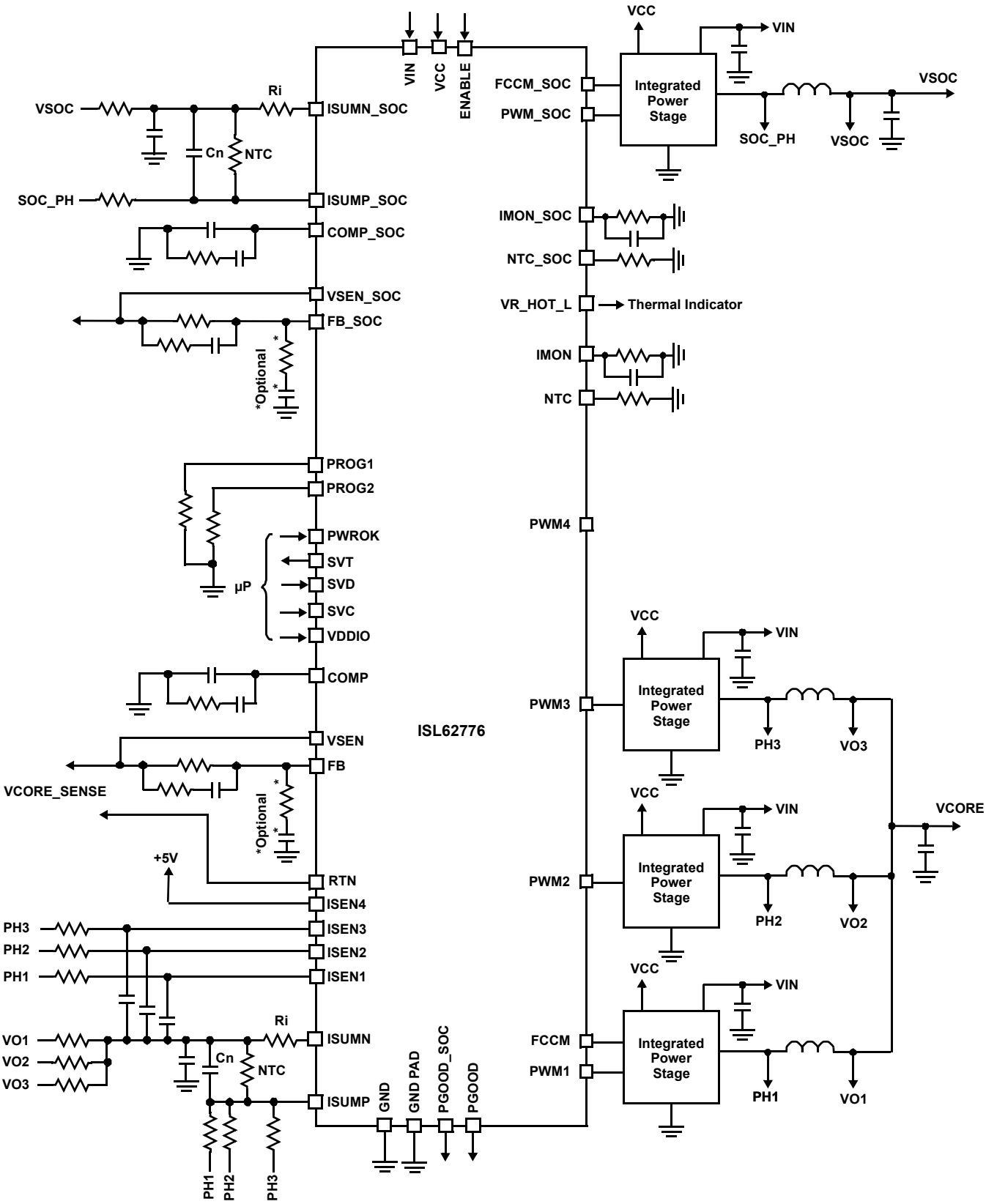


Figure 3. Typical Application Circuit for Mid-Power CPUs Using Inductor DCR Sensing, 3+1

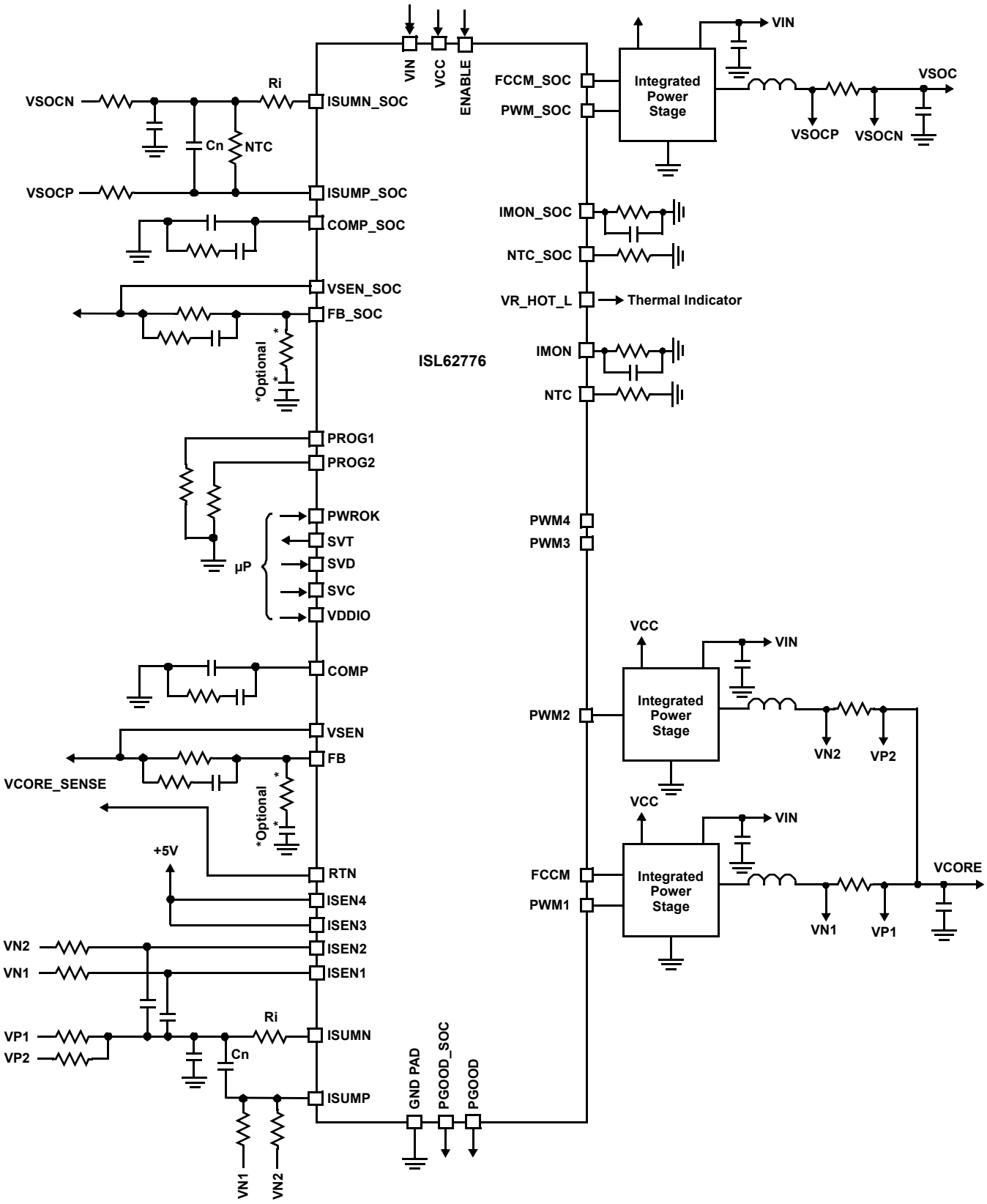


Figure 4. Typical Application Circuit for Low-Power CPUs Using Resistor Sensing, 2+1

1.2 Block Diagram

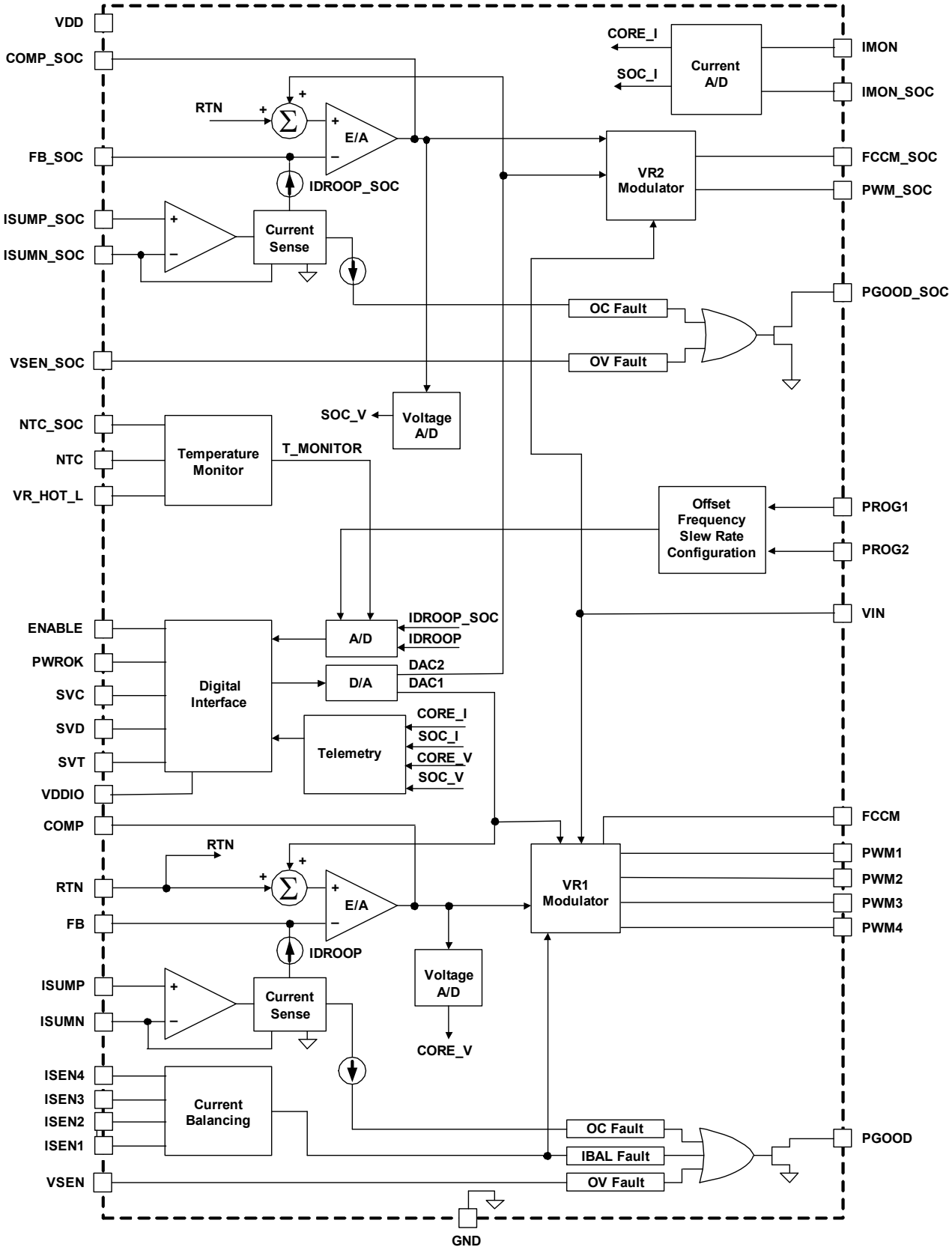


Figure 5. Block Diagram

1.3 Ordering Information

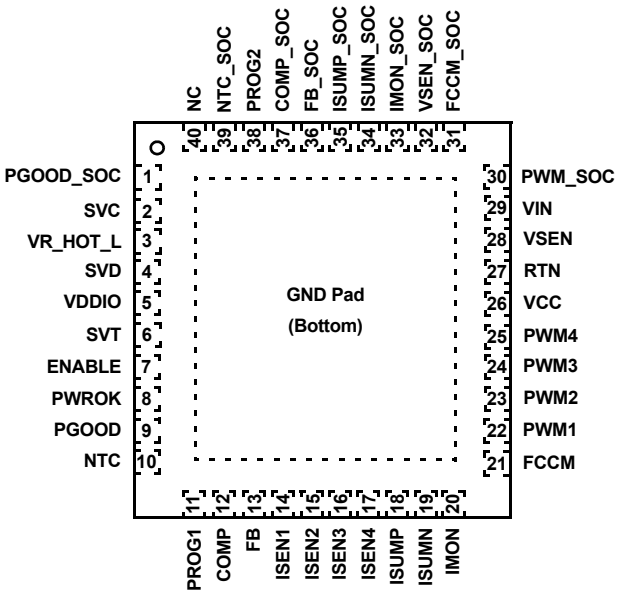
Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL62776HRTZ	62776 HRTZ	-10 to +100	-	40 Ld 5x5 TQFN	L40.5x5
ISL62776HRTZ-T	62776 HRTZ	-10 to +100	6k	40 Ld 5x5 TQFN	L40.5x5
ISL62776IRTZ	62776 IRTZ	-40 to +100	-	40 Ld 5x5 TQFN	L40.5x5
ISL62776IRTZ-T	62776 IRTZ	-40 to +100	6k	40 Ld 5x5 TQFN	L40.5x5

Notes:

1. See TB347 for details about reel specifications.
2. Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL62776 device page. For more information about MSL, see TB363.

1.4 Pin Configuration

40 Ld TQFN
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Description
1	PGOOD_SOC	Open-drain output to indicate the SOC portion of the IC is ready to supply the regulated voltage. Pull-up externally to VDDP or 3.3V through a resistor (minimum 1kΩ).
2	SVC	Serial VID clock input from the CPU processor master device.
3	VR_HOT_L	Thermal indicator signal to the AMD processor. Thermal overload open-drain output indicator active Low.
4	SVD	Serial VID data bidirectional signal from the CPU processor master device to the VR.
5	VDDIO	VDDIO is the processor memory interface power rail. This pin serves as the I/O signal level reference to the controller IC for this processor.
6	SVT	Serial VID Telemetry (SVT) data line input to the CPU from the controller IC. Telemetry and VID-on-the-fly complete signal provided from this pin.
7	ENABLE	Enable input. A high-level logic on this pin enables both VRs.
8	PWROK	System power-good input. When this pin is high, the SVI2 logic is active. While this pin is low, the SVC and SVD input states determine the pre-PWROK metal VID. This pin must be low prior to the ISL62776 PGOOD output going high, per the AMD SVI2 Controller Guidelines.

Pin Number	Pin Name	Description
9	PGOOD	Open-drain output indicates the Core portion of the IC is ready to supply the regulated voltage. Pull-up externally to VDD or 3.3V through a resistor (minimum 1kΩ).
10	NTC	Thermistor input to VR_HOT_L circuit to monitor the Core VR temperature.
11	PROG	Programming pins. See VR Offset Programming.
38	PROG2	
12	COMP	Core controller error amplifier output. See Figure 2 for general component connections.
13	FB	Output voltage feedback to the inverting input of the Core controller error amplifier. See Figure 2 for general component connections.
14	ISEN1	Individual current sensing for Channel 1 of the Core VR. If ISEN2 is tied to +5V, ISEN1 must be tied to GND through a 10kΩ resistor. If ISEN1 is tied to +5V, the Core portion of the IC is shut down.
15	ISEN2	Individual current sensing for Channel 2 of the Core VR. When ISEN2 is pulled to +5V, the controller disables Channel 2, and the Core VR runs in single-phase mode. Do not leave this pin floating.
16	ISEN3	Individual current sensing for Channel 3 of the Core VR. When ISEN3 is pulled to +5V, the controller disables Channel 3, and the Core VR runs in two-phase mode. Do not leave this pin floating.
17	ISEN4	Individual current sensing for Channel 4 of the Core VR. When ISEN4is pulled to +5V, the controller disables Channel 4, and the Core VR runs in three-phase mode. Do not leave this pin floating.
18	ISUMP	Noninverting input of the transconductance amplifier for current monitor and load line of Core output. See Inductor DCR Current-Sensing Network.
19	ISUMN	Inverting input of the transconductance amplifier for current monitor and load line of Core output. See Inductor DCR Current-Sensing Network.
20	IMON	Core output current monitor. A current proportional to the Core VR output current is sourced from this pin. Renesas recommends tying a 133kΩ resistor from IMON to GND.
21	FCCM	Diode emulation control signal for Core. When FCCM is High, continuous conduction mode is forced. When FCCM is LOW, diode emulation at the driver this pin connects to is allowed.
22, 23, 24, 25	PWM1, 2, 3, 4	PWM outputs for the Core regulator. When tri-stated, these pins are at a high impedance state.
26	VCC	5V bias power. A resistor (2Ω) and a decoupling capacitor should be used from the +5V supply. A high quality, X7R dielectric, 0.1µF minimum, MLCC capacitor is recommended.
27	RTN	Output voltage sense return pin for both Core VR and SOC VR. Connect to the -sense pin of the microprocessor die.
28	VSEN	Output voltage sense pin for the Core controller. Connect to the +sense pin of the microprocessor die.
29	VIN	Battery supply voltage, used for feed-forward and modulation.
30	PWM_SOC	PWM output for SOC regulator. When tri-stated, this pin is at a high impedance state.
31	FCCM_SOC	Diode emulation control signal for SOC. When FCCM_SOC is High, continuous conduction mode is forced. When FCCM_SOC is LOW, diode emulation at the driver this pin connects to is allowed.
32	VSEN_SOC	Output voltage sense pin for the SOC controller. Connect to the +sense pin of the microprocessor die.
33	IMON_SOC	SOC output current monitor. A current proportional to the SOC VR output current is sourced from this pin. Renesas recommends tying a 133kΩ resistor from IMON_SOC to GND.
34	ISUMN_SOC	Inverting input of the transconductance amplifier for current monitor and load line of the SOC VR. See Inductor DCR Current-Sensing Network.
35	ISUMP_SOC	Noninverting input of the transconductance amplifier for current monitor and load line of the SOC VR. See Inductor DCR Current-Sensing Network.
36	FB_SOC	Output voltage feedback to the inverting input of the SOC controller error amplifier. See Figure 2 for general component connection.
37	COMP_SOC	SOC VR error amplifier output. See Figure 2 for general component connections.
39	NTC_SOC	Thermistor input to VR_HOT_L circuit to monitor SOC VR temperature.
40	NC	No connected
-	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}	-0.3	+7	V
Battery Voltage, V_{IN}		+28	V
All Other Pins	-0.3	V_{DD} + 0.3V	V
Open-Drain Outputs, PGOOD, PGOOD_SOC, VR_HOT_L	-0.3	+7	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Charged Device Model (Tested per JS-002-2014)	1		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
40 Ld TQFN Package (Notes 4, 5)	29	3.5

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{DD}		5 ±5%	V
Battery Voltage, V_{IN}	4.5	25	V
Junction Temperature	-10	+125	°C
Ambient Temperature			
HRZ	-10	+100	°C
IRZ	-40	+100	°C

2.4 Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Input Power Supply						
+5V Supply Current	I_{VDD}	ENABLE = 4V		11	13	mA
		ENABLE = 0V			3.5	µA

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Battery Supply Current	I_{VIN}	ENABLE = 0V			1	µA
V_{IN} Input Resistance	R_{VIN}	ENABLE = 4V, V_{IN} = 15V		310		kΩ
Power-On Reset Thresholds						
V_{CC} POR Threshold	VCC_POR_r	V_{CC} rising		4.35	4.5	V
	VCC_POR_f	V_{CC} falling	4.00	4.15		V
System and References						
System Accuracy, Core	%Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V (HRZ)	-0.5		+0.5	%
		VID = 0.25V to 0.74375V (HRZ)	-10		+10	mV
	%Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V (IRZ)	-0.8		+0.8	%
		VID = 0.25V to 0.74375V (IRZ)	-12		+12	mV
System Accuracy, SOC	%Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V (HRZ)	-1		+1	%
		VID = 0.25V to 0.74375V (HRZ)	-20		+20	mV
	%Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.55V (IRZ)	-1.6		+1.6	%
		VID = 0.25V to 0.74375V (IRZ)	-24		+24	mV
Maximum Output Voltage	$V_{OUT(max)}$	VID = [00000000]		1.55		V
Minimum Output Voltage	$V_{OUT(min)}$	VID = [11111111]		0		V
Channel Frequency						
Nominal Channel Frequency	$f_{SW(nom)}$		400	450	510	kHz
			540	600	665	kHz
			680	750	810	kHz
			910	1000	1070	kHz
Amplifiers						
Current-Sense Amplifier Input Offset		I_{FB} = 0A (HRZ)	-0.2		+0.2	mV
		I_{FB} = 0A (IRZ)	-0.25		+0.25	mV
Error Amplifier DC Gain	A_{V0}			119		dB
Error Amplifier Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz
ISEN						
Input Bias Current				20		nA
Power-Good (PGOOD and PGOOD_SOC) and Protection Monitors						
PGOOD Low Voltage	V_{OL}	I_{PGOOD} = 4mA			0.4	V
PGOOD Leakage Current	I_{OH}	PGOOD = 3.3V	-1		1	µA
PWROK High Threshold				750		mV
VR_HOT_L Pull-Down				11		Ω
PWROK Leakage Current					1	µA
VR_HOT_L Leakage Current					1	µA

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), T_A = -40°C to +100°C (IRZ), f_{SW} = 300kHz, unless otherwise noted. **(Continued)**

Parameter	Symbol	Test Conditions	Min (Note 6)	Typ	Max (Note 6)	Unit
Protection						
Overvoltage Threshold	OV_H	ISUMN rising above setpoint for >1µs	275	325	375	mV
Undervoltage Threshold	UV_H	ISUMN falls below setpoint for >1µs	275	325	375	mV
Current Imbalance Threshold		One ISEN above another ISEN for >1.2ms		25		mV
Way Overcurrent Trip Threshold (IMONx Current Based Detection)	$IMONx_{WOC}$	All states, I_{DROOP} = 60µA, R_{IMON} = 135kΩ		15		µA
Overcurrent Trip Threshold (IMONx Voltage Based Detection)	V_{IMONx_OCP}	All states, I_{DROOP} = 45µA, I_{IMONx} = 11.25µA, R_{IMON} = 135kΩ	1.475	1.505	1.535	V
Logic Thresholds						
ENABLE Input Low	V_{IL}				1	V
ENABLE Input High	V_{IH}	HRZ	1.6			V
		IRZ	1.65			V
ENABLE Leakage Current	I_{ENABLE}	ENABLE = 0V	-1	0	1	µA
		ENABLE = 1V	-1	0	1	µA
SVT Impedance				50		Ω
SVC Frequency Range			0.1		21	MHz
SVC, SVD Input Low	V_{IL}	% of VDDIO			30	%
SVC, SVD Input High	V_{IH}	% of VDDIO	70			%
SVC, SVD Leakage		ENABLE = 0V; SVC, SVD = 0V and 1V	-1		1	µA
		ENABLE = 4V; SVC, SVD = 1V	-5		1	µA
		ENABLE = 4V; SVC, SVD = 0V	-35	-22	-5	µA
PWM						
PWM Output Low	V_{0L}	Sinking 5mA			1.0	V
PWM Output High	V_{0H}	Sourcing 5mA	3.5			V
PWM Tri-State Leakage		PWM = 2.5V		1		µA
Thermal Monitor						
NTC Source Current		NTC = 0.6V	27	30	33	µA
NTC Thermal Warning Voltage			610	650	690	mV
NTC Thermal Warning Voltage Hysteresis				25		mV
NTC Thermal Shutdown Voltage			550	590	630	mV
Slew Rate						
VID-on-the-Fly Slew Rate		Maximum programmed	16	20	24	mV/µs
		Minimum programmed	8	10	12	mV/µs

Note:
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Theory of Operation

3.1 Multiphase R3 Modulator

The ISL62776 is a multiphase regulator that implements two voltage regulators, Core VR and SOC VR, on one chip controlled by AMD's SVI 2.0 protocol. The Core VR can be programmed for 1-, 2-, 3-, or 4-phase operation. The SOC VR is a 1-phase regulator. Both regulators use the Renesas proprietary R3 (Robust Ripple Regulator) modulator. The R3 modulator combines the best features of PWM, such as fixed frequency and hysteretic, and eliminates many of its shortcomings. Figure 6 conceptually shows the multiphase R3 modulator circuit and Figure 7 shows the operational principles.

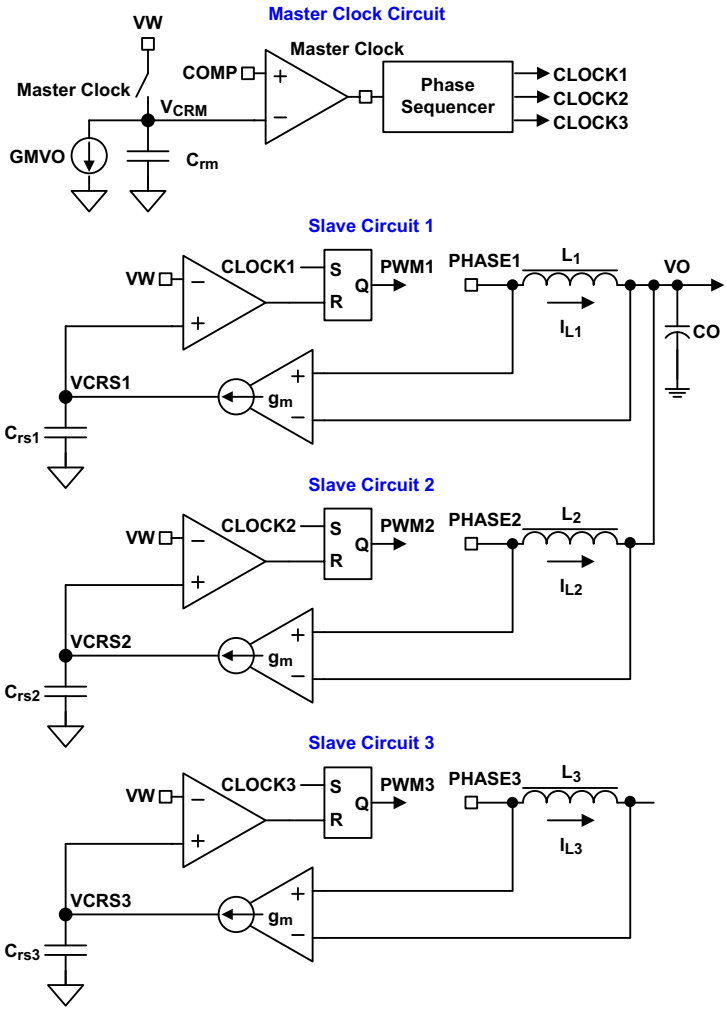


Figure 6. R3 Modulator Circuit

Inside the IC, the modulator uses the master clock circuit to generate the clocks for slave circuits. The modulator discharges the ripple capacitor C_{rm} with a current source equal to $g_m V_o$, where g_m is a gain factor. The C_{rm} voltage, V_{CRM}, is a sawtooth waveform traversing between the VW and COMP voltages. The C_{rm} voltage resets to VW when it reaches COMP and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the slave circuits.

- If the Core VR is in 3-phase mode, the master clock signal is distributed to the three phases and the Clock1 through Clock3 signals are 120 degrees out-of-phase
- If the Core VR is in 2-phase mode, the master clock signal is distributed to Phases 1 and 2 and the Clock1 and Clock2 signals are 180 degrees out-of-phase
- If the Core VR is in 1-phase mode, the master clock signal is distributed to Phase 1 only and is the Clock1 signal

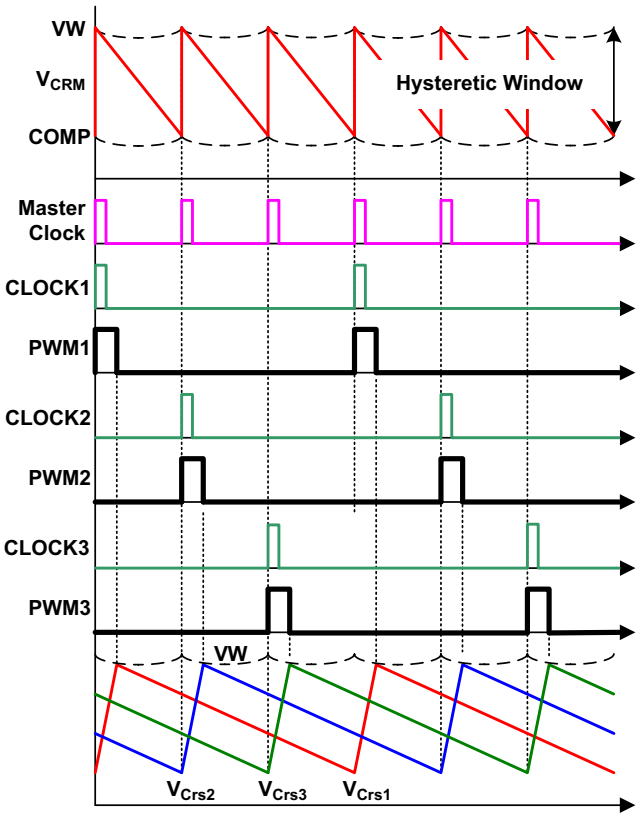


Figure 7. R3 Modulator Operational Principles in Steady State

Each slave circuit has its own ripple capacitor C_{rs}; whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage into a current source to charge and discharge C_{rs}. The slave circuit turns on its PWM pulse when it receives the clock signal and the current source charges C_{rs}. When the C_{rs} voltage V_{Crs} reaches VW, the slave circuit turns off the PWM pulse and the current source discharges C_{rs}.

Because the controller works with V_{Crs}, which is a large amplitude and noise-free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the error amplifier allows the ISL62776 to maintain a 0.5% output voltage accuracy.

Figure 8 shows the operational principles during load insertion response. The COMP voltage rises during load insertion, quickly generating the master clock signal, so the PWM pulses turn on earlier to increase the effective switching frequency, allowing for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises as the COMP voltage rises, making the PWM pulses wider. During load release response, the COMP voltage falls. The master clock circuit takes longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls as the COMP voltage falls, reducing the current PWM pulse-width. This behavior gives the ISL62776 excellent response speed.

All the phases share the same VW window voltage, ensuring excellent dynamic current balance among phases.

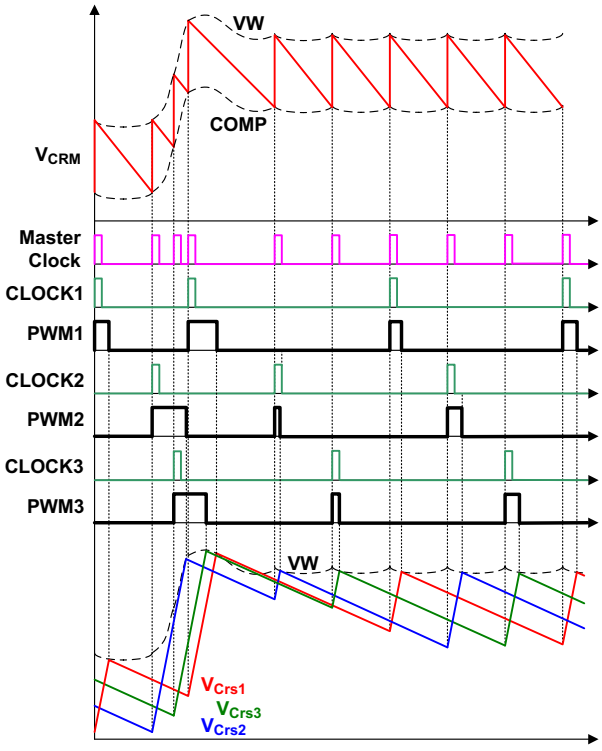


Figure 8. R3 Modulator Operational Principles in Load Insertion Response

3.2 Standard Buck Operation During Soft-Start

At startup, during the initial rise of the output voltage, the ISL62776 forces the regulator into a standard buck mode. From the initial PWM pulse until the DAC reaches approximately 480mV, the regulator operates in this mode. Once the DAC has exceeded approximately 480mV, the ISL62776 goes into synchronous buck operation. To achieve standard buck mode, the PWM signal is tri-stated (high impedance) when the upper device is turned off. In compatible drivers and power stages, both upper and lower pass devices should be turned off when they see a tri-stated PWM signal.

3.3 Diode Emulation and Period Stretching

With a compatible MOSFET driver or power stage, the regulator controlled by the ISL62776 can operate in Diode Emulation Mode (DEM). For the driver or power stage to be DEM compatible, they must be able to accept the FCCM signal from the ISL62776. For proper compatibility, the driver or power stage should also disable both upper and lower pass devices when the PWM signal they receive is tri-stated (high impedance state).

When the FCCM signal is High, the driver or power stage must be in Forced Continuous Conduction Mode, meaning that the upper pass device must be on and the lower pass device must be off when the PWM signal is High. Also, when the PWM signal is Low, the upper pass device must be off and the lower pass device must be on. When the FCCM signal is Low, the driver or power stage must operate in DEM. When the PWM signal is High, the upper pass device is on and the lower pass device is off. When the PWM signal is Low, the upper pass device must be off. The lower pass device should be on only while inductor current is greater than 0A. Once the inductor current reaches 0A, both pass devices should be off until the PWM signal goes High again. One method that is commonly utilized by drivers and power stages to be DEM compatible is to monitor the Phase voltage while the low pass element is on. As Figure 9 shows, when the Phase voltage crosses zero volts, the lower pass device turns off.

If the load current is light enough, as Figure 9 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A and the regulator is in Continuous Condution Mode (CCM) although the controller is in DEM.

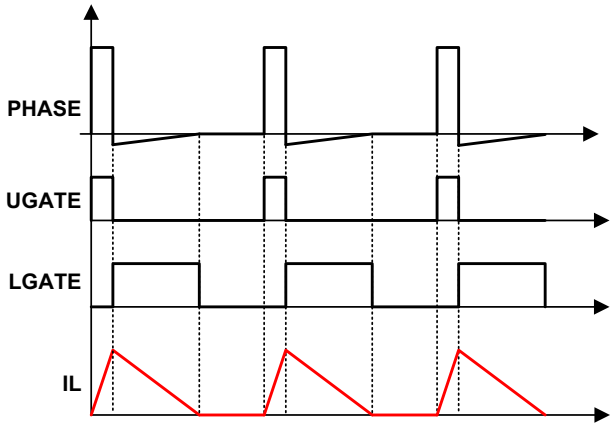


Figure 9. Diode Emulation

Figure 10 shows the operation principle in DEM at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, so the inductor current triangle is the same in the three cases. The ISL62776 clamps the ripple capacitor voltage V_{Crs} in DEM to make it mimic the inductor current. The COMP voltage takes longer to reach V_{Crs}, which naturally stretches the switching period. The inductor current triangles move farther apart, so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

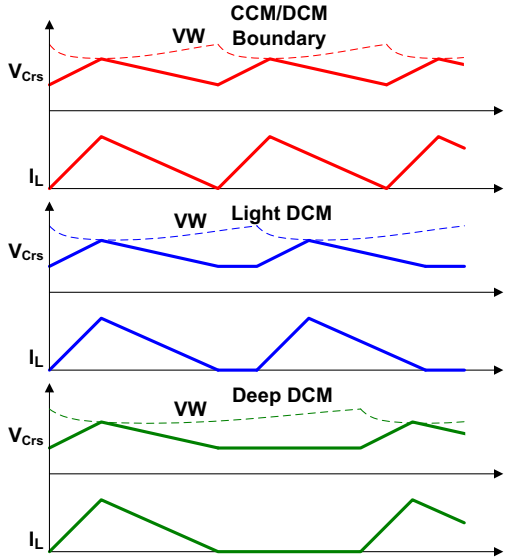


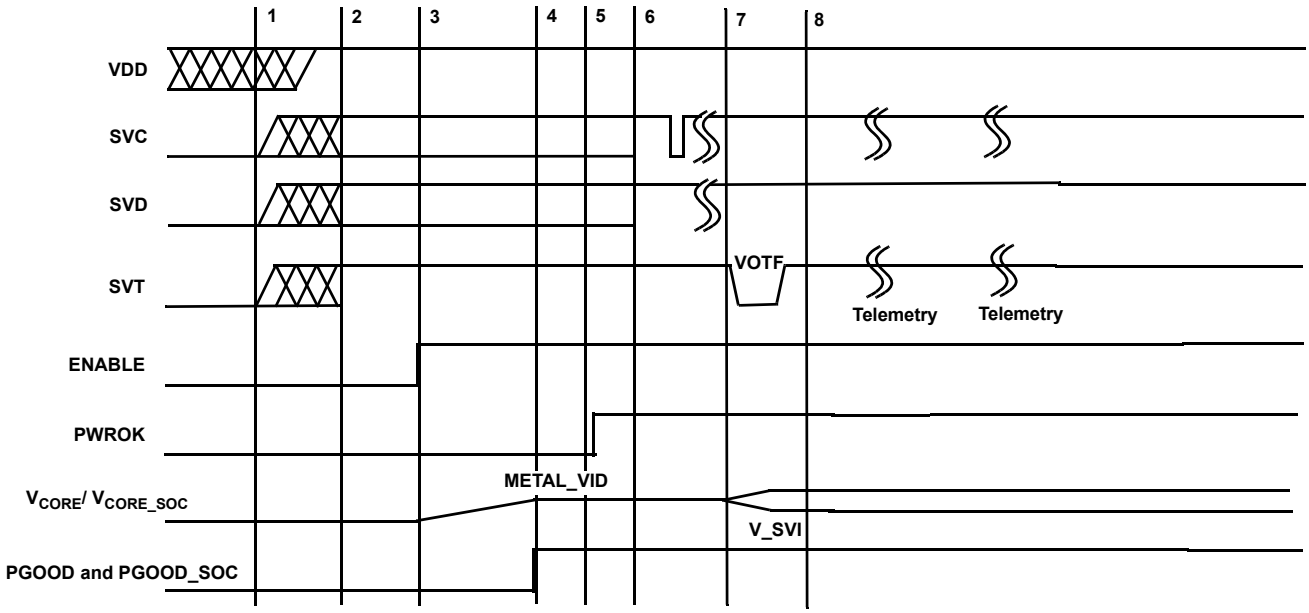
Figure 10. Period Stretching

3.4 Channel Configuration

The individual PWM channels of either VR can be disabled by connecting the ISENx pin to +5V. For example, placing the controller in a 3+1 configuration, as shown in Figure 3, requires ISEN4 of the Core VR to be tied to +5V. ISEN4 disables Channel 4 of the Core VR. Connecting ISEN1 to +5V disables the Core VR output. This feature allows debugging of individual VR outputs. The ISENx pins must not float.

3.5 Power-On Reset

The ISL62776 requires a +5V input supply tied to VDD to exceed the V_{DD} rising Power-On Reset (POR) threshold before the controller has sufficient bias to ensure proper operation. When this threshold is reached or exceeded, and ENABLE is taken high, the ISL62776 has enough bias to check the state of the SVI inputs. Hysteresis between the rising and the falling thresholds ensures the ISL62776 does not inadvertently turn off unless the bias voltage drops substantially (see Electrical Specifications on page 10). **Note:** V_{IN} must be present for the controller to drive the output voltage.



Interval 1 to 2: The ISL62776 waits to POR.

Interval 2 to 3: SVC and SVD are externally set to the pre-Metal VID code.

Interval 3 to 4: ENABLE locks the pre-Metal VID code. Both outputs soft-start to this level.

Interval 4 to 5: The PGOOD signal goes HIGH, indicating proper operation.

Interval 5 to 6: PGOOD and PGOOD_SOC high are detected and PWROK is taken high. The ISL62776 is prepared for SVI commands.

Interval 6 to 7: The SVC and SVD data lines communicate change in VID code.

Interval 7 to 8: The ISL62776 responds to VID-ON-THE-FLY code change and issues a VOTF for positive VID changes.

Post 8: Telemetry is clocked out of the ISL62776.

Figure 11. SVI Logic Timing Diagram: Typical Pre-PWROK Metal VID Start-Up

3.6 Start-Up Timing

The controller start-up sequence begins when V_{DD} is above the POR threshold and ENABLE exceeds the logic high threshold. Figure 12 shows the typical soft-start timing of the Core and SOC VRs. When the controller registers ENABLE as a high, the controller checks the state of a few programming pins during the typical 8ms delay before soft-starting the Core and SOC outputs. The pre-PWROK Metal VID is read from the state of the SVC and SVD pins and programs the DAC, and the programming resistors on PROG1 and PROG2 are read to configure switching frequency, slew rate, and output offsets. See Resistor Configuration Options for more information about the programming resistors. The ISL62776 uses a digital soft-start to ramp up the DAC to the Metal VID level programmed. PGOOD is asserted high at the end of the soft-start ramp.

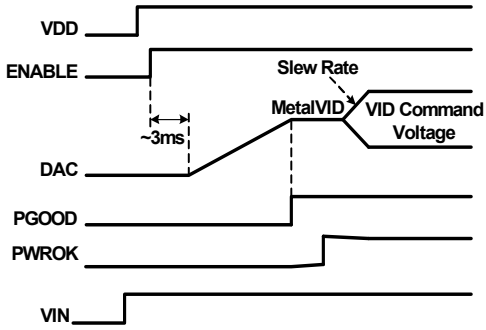


Figure 12. Typical Soft-Start Waveforms

3.7 Voltage Regulation and Load Line Implementation

After the soft-start sequence, the ISL62776 regulates the output voltages to the pre-PWROK metal VID programmed. See Table 4. The ISL62776 controls the no-load output voltage to an accuracy of ±0.5% across the range of 0.75V to 1.55V. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

As the load current increases from zero, the output voltage droops from the VID programmed value by an amount proportional to the load current to achieve the load line. The ISL62776 can sense the inductor current through the intrinsic DC Resistance (DCR) of the inductors as shown in Figures 2 and 3, or through resistors in series with the inductors as shown in Figure 4. In both methods, the capacitor C_n voltage represents the total inductor current. An internal amplifier converts the C_n voltage into an internal current source, I_{sum}, with the gain set by resistor R_i. See Equation 1.

(EQ. 1) $$I_{sum} = \frac{V_{Cn}}{R_i}$$

The I_{sum} current is used for load-line implementation, current monitoring on the IMON pins, and overcurrent protection.

Figure 13 shows the load-line implementation.

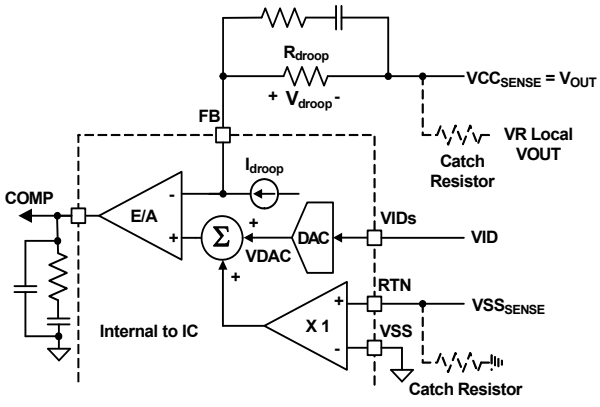


Figure 13. Differential Sensing and Load-Line Implementation

The ISL62776 drives a current source (I_{droop}) out of the FB pin, which is a ratio of the I_{sum} current, as described by Equation 2.

(EQ. 2) $$I_{droop} = \frac{5}{4} \times I_{sum} = \frac{5}{4} \times \frac{V_{Cn}}{R_i}$$

When using inductor DCR current sensing, a single NTC element compensates the positive temperature coefficient of the copper winding, sustaining the load-line accuracy with reduced cost.

I_{droop} flows through resistor R_{droop} and creates a voltage drop as shown in Equation 3.

(EQ. 3) $$V_{droop} = R_{droop} \times I_{droop}$$

V_{droop} is the droop voltage required to implement load line. Changing R_{droop} or scaling I_{droop} can change the load line slope. Because I_{sum} sets the overcurrent protection level, Renesas recommends first scaling I_{sum} based on the OCP requirement, then selecting an appropriate R_{droop} value to get the required load line slope.

3.8 Differential Sensing

Figure 13 also shows the differential voltage sensing scheme. VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. The error amplifier regulates the inverting and noninverting input voltages to be equal as shown in Equation 4:

(EQ. 4) $$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE}$$

Rewriting Equation 4 and substituting Equation 3 gives Equation 5, the exact equation required for load-line implementation.

(EQ. 5) $$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop}$$

The VCC_{SENSE} and VSS_{SENSE} signals come from the processor die. The feedback is an open circuit in the absence of the processor. Figure 13 shows the recommended catch resistor to feed the VR local output voltage back to the compensator and another catch resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, provide voltage feedback if the system is powered up without a processor installed.

3.9 Phase Current Balancing

The ISL62776 monitors individual phase average current by monitoring the ISEN1, ISEN2, and ISEN3 voltages. Figure 14 shows the recommended current balancing circuit for DCR sensing.

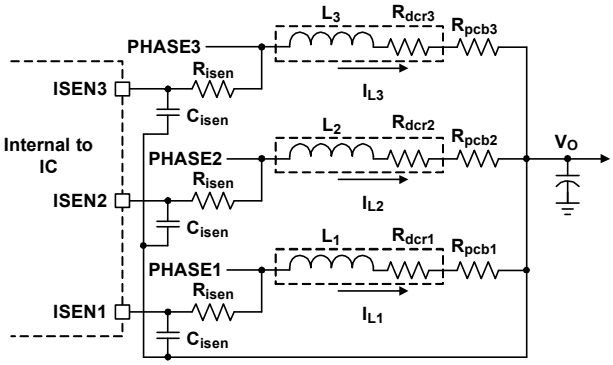


Figure 14. Current Balancing Circuit

Each phase node voltage is averaged by a low-pass filter consisting of R_{isen} and C_{isen} and is presented to the corresponding ISEN pin. Route R_{isen} to the inductor phase-node pad to eliminate the effect of phase node parasitic PCB DCR. Equations 6 through 8 give the ISEN pin voltages:

(EQ. 6) $$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1}$$

(EQ. 7) $$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2}$$

(EQ. 8) $$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3}$$

where R_{dcr1}, R_{dcr2}, and R_{dcr3} are inductor DCR; R_{pcb1}, R_{pcb2}, and R_{pcb3} are parasitic PCB DCR between the inductor output side pad and the output voltage rail; and I_{L1}, I_{L2}, and I_{L3} are inductor average currents.

The ISL62776 adjusts the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$. This adjustment yields $I_{L1} = I_{L2} = I_{L3}$ when $R_{dcr1} = R_{dcr2} = R_{dcr3}$ and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Using the same components for L1, L2, and L3 provides a good match of R_{dcr1}, R_{dcr2}, and R_{dcr3}. Board layout determines R_{pcb1}, R_{pcb2}, and R_{pcb3}. Renesas recommends a symmetrical layout for the power delivery path between each inductor and the output voltage rail so that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Symmetrical layout can be difficult to implement. For the circuit shown in Figure 14, asymmetric layout causes different R_{pcb1}, R_{pcb2}, and R_{pcb3} values, which creates a current imbalance. Figure 15 shows a differential sensing current balancing circuit recommended for ISL62776. Route the current sensing traces to the inductor pads so they pick up only the inductor DCR voltage. Each ISEN pin sees the average voltage of three sources: its own, the phase inductor phase-node pad, and the other two phase inductor output side pads.

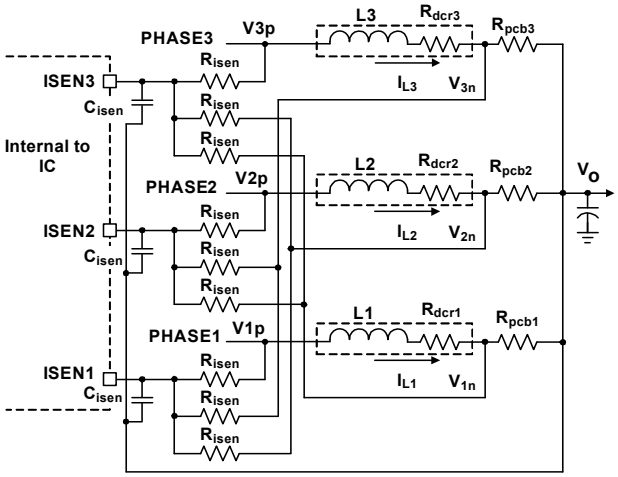


Figure 15. Differential-Sensing Current Balancing Circuit

Equation 9 through Equation 11 give the ISEN pin voltages:

(EQ. 9) $$V_{ISEN1} = V_{1p} + V_{2n} + V_{3n}$$

(EQ. 10) $$V_{ISEN2} = V_{1n} + V_{2p} + V_{3n}$$

(EQ. 11) $$V_{ISEN3} = V_{1n} + V_{2n} + V_{3p}$$

The ISL62776 makes $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$ as shown in Equation 12 and Equation 13:

(EQ. 12) $$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n}$$

(EQ. 13) $$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p}$$

Rewriting Equation 12 gives Equation 14:

(EQ. 14) $$V_{1p} - V_{1n} = V_{2p} - V_{2n}$$

Rewriting Equation 13 gives Equation 15:

(EQ. 15) $$V_{2p} - V_{2n} = V_{3p} - V_{3n}$$

Combining Equation 14 and 15 gives Equation 16:

(EQ. 16) $$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n}$$

Therefore:

(EQ. 17) $$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved when $R_{dcr1} = R_{dcr2} = R_{dcr3}$. R_{pcb1}, R_{pcb2}, and R_{pcb3} have no effect.

Because the slave ripple capacitor voltages mimic the inductor currents, the R3 modulator can naturally achieve excellent current balancing during steady state and dynamic operations. Figure 16 shows the current balancing performance of the evaluation board with a load transient of 12A/51A at different repetition rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current at a low repetition rate, but cannot keep up when the repetition rate is in the hundred-kHz range, where it is outside of the control loop bandwidth. The controller achieves excellent current balancing in all cases installed.

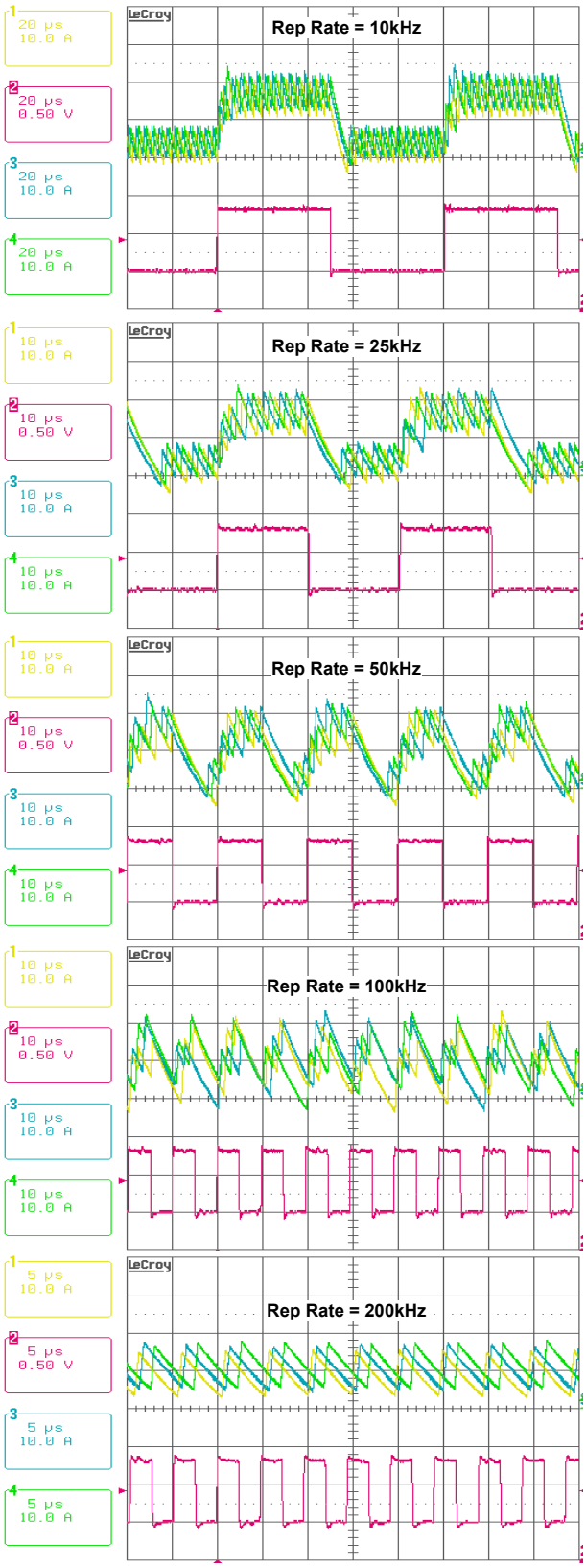


Figure 16. Current Balancing During Dynamic Operation. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

3.10 Modes of Operation

The Core VR can be configured for 4-, 3-, 2-, or 1-phase operation. Table 1 shows the Core VR configurations and operational modes, programmed by the ISEN4, ISEN3, and ISEN2 pin status and the PSL0_L and PSL1_L commands from the SVI2 interface. See Table 7 for more information about PSL0_L and PSL1_L.

Table 1. Core VR Modes of Operation

Configuration	ISEN4	ISEN3	ISEN2	PSL0_L and PSL1_L	Mode
4-Phase Core	To Power Stage	To Power Stage	To Power Stage	11	4-Phase CCM
				01	1-Phase CCM
				00	1-Phase DEM
3-Phase Core	Tied to 5V	To Power Stage	To Power Stage	11	3-Phase CCM
				01	1-Phase CCM
				00	1-Phase DEM
2-Phase Core	Tied to 5V	Tied to 5V	To Power Stage	11	2-Phase CCM
				01	1-Phase CCM
				00	1-Phase DEM
1-Phase Core	Tied to 5V	Tied to 5V	Tied to 5V	11	1-Phase CMM
				01	1-Phase CCM
				00	1-Phase DEM

In a 4-phase configuration, the Core VR operates in 4-phase CCM, with PSI0_L and PSI_L both high. If PSI0_L goes low using the SVI 2 interface, the Core VR sheds Phases 4, 3, and 2. Phase 1 operates in CCM. When both PSI0_L and PSI1_L go low, the Core VR operates in 1-phase DEM.

In a 3-phase configuration, the Core VR operates in 3-phase CCM, with PSI0_L and PSI_L both high. If PSI0_L goes low by the SVI 2 interface, the Core VR sheds Phase 2 and Phase 3. Phase 1 operates in CCM. When both PSI0_L and PSI1_L go low, the Core VR operates in 1-phase DEM. Tie the ISEN4 pin to 5V. Phases 1, 2, and 3 are active in this configuration.

In a 2-phase configuration, the Core VR operates in 2-phase CCM with PSI0_L and PSI_L both high. If PSI0_L goes low by the SVI 2 interface, the Core VR sheds Phase 2 and the Core VR operates in 1-phase CCM. When both PSI0_L and PSI1_L go low, the Core VR operates in 1-phase DEM. Tie the ISEN4 and ISEN3 pins to 5V. Phases 1 and 2 are active in this configuration.

In a 1-phase configuration, the Core VR operates in 1-phase CCM and stays in 1-phase CCM when PSI0_L goes low. When both PSI0_L and PSI1_L go low, the Core VR operates in 1-phase DEM. Tie the ISEN4, ISEN3, and ISEN2 pins to 5V. Only Phase 1 is active in this configuration.

The Core VR can be disabled by connecting ISUMN to +5V. The SOC VR operates in 1-phase CCM and stays in 1-phase CCM when PSI0_L goes low. When both PSI0_L and PSI1_L go low, the SOC VR operates in 1-phase DEM. Connect ISUMN_SOC to +5V to disable the SOC VR.

The Core and SOC VRs have an overcurrent threshold of 1.5V on IMON and IMON_SOC, respectively. This level does not vary based on channel configuration. See Overcurrent for more information.

3.11 Dynamic Operation

The Core VR and SOC VR behave the same during dynamic operation. The controller responds to VID-on-the-fly changes by slewing to the new voltage at the slew rate programmed. See Table 4 for more information. During negative VID transitions, the output voltage decays to the lower VID value at the slew rate determined by the load.

The R3 modulator intrinsically has its voltage feed-forward. The output voltage is insensitive to a fast slew-rate input voltage change.

4. Resistor Configuration Options

The PROG1 and PROG2 pins configure functionality within the IC. Resistors from these pins to GND are read during the first portion of the soft-start sequence. This section describes how to select the resistor values for each of these pins; use the values to program the output voltage offset of each output, VID-on-the-fly slew rate, and switching frequency used for both VRs.

4.1 VR Offset Programming

Program a positive or negative offset for the Core VR using a resistor to ground from the PROG1 pin. Program a positive or negative offset for the SOC VR using a resistor to ground from the PROG2 pin. Table 2 and Table 3 provide the resistor values to select the desired output voltage offset. The 1% tolerance resistor value in the table must be used to program the corresponding Core or SOC output voltage offset.

Table 2. PROG1 f_{SW} and Core Output Voltage Offset Selection

PROG1 1% Resistor Value (kΩ)	Switching Frequency (kHz)	Core Offset (mV)
5.62	450	-25
7.87		0
11.5		25
16.9		50
19.1	600	-25
24.9		0
34.0		25
41.2		50
52.3	750	-25
73.2		0
95.3		25
121		50
154	1000	-25
182		0
210		25
OPEN		50

4.2 VID-on-the-Fly Slew Rate Selection

The PROG2 resistor also selects the slew rate for VID changes commanded by the processor. See Table 3. When selected, the slew rate is locked in during soft-start and is not adjustable during operation. The lowest slew rate that can be selected is 10mV/µs, which is above the minimum of 7.5mV/µs required by the SVI 2.0 specification. The slew rate selected sets the slew rate for both Core and the SOC VRs; they cannot be independently selected.

4.3 CCM Switching Frequency

The programming resistor on the PROG1 pin sets the Core and SOC VR switching frequency. When the ISL62776 is in CCM, the switching frequency is not absolutely constant due to the nature of the R3 modulator. As explained in Multiphase R3 Modulator, the effective switching frequency increases during load insertion and decreases during load release to achieve fast response. Thus, the switching frequency is relatively constant at steady state. Variation is expected when the power stage condition, such as input voltage, output voltage, or load changes. The variation is usually less than 10% and does not have any significant effect on output voltage ripple magnitude. Table 3 defines the switching frequency based on the resistor value that programs the FCCM pin.

Table 3. PROG2 VOTF Slew Rate and SOC Output Voltage Offset Selection

PROG2 1% Resistor Value (kΩ)	VOTF Slew Rate (mV/µs)	SOC Offset (mV)
5.62	10	-25
7.87		0
11.5		25
16.9		50
19.1	12.5	-25
24.9		0
34.0		25
41.2		50
52.3	15	-25
73.2		0
95.3		25
121		50
154	20	-25
182		0
210		25
OPEN		50

The controller monitors SVI commands to determine when to enter power-saving mode, implement dynamic VID changes, and shut down individual outputs.

5. AMD Serial VID Interface 2.0

The on-board SVI2 interface circuitry allows the AMD processor to directly control the Core and SOC voltage reference levels within the ISL62776. When the PWROK signal goes high, the IC begins monitoring the SVC and SVD pins for instructions. The ISL62776 uses a Digital-to-Analog Converter (DAC) to generate a reference voltage based on the decoded SVI value. See Figure 11 for a simple SVI interface timing diagram.

5.1 Pre-PWROK Metal VID

Typical motherboard start-up begins with the controller decoding the SVC and SVD inputs to determine the pre-PWROK Metal VID setting (see Table 4). When the ENABLE input exceeds the rising threshold, the ISL62776 decodes and locks the decoded value into an onboard hold register.

Table 4. Pre-PWROK Metal VID Codes

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

When the programming pins are read, the internal DAC circuitry begins to ramp the Core and SOC VRs to the decoded pre-PWROK Metal VID output level. The digital soft-start circuitry ramps the internal reference to the target gradually at a fixed rate of approximately 5mV/µs until the output voltage reaches ~250mV, and then at the programmed slew rate. The controlled ramp of all output voltage planes reduces inrush current during the soft-start interval. At the end of the soft-start interval, the PGOOD and PGOOD_SOC outputs transition high to indicate that both output planes are within regulation limits.

If the ENABLE input falls below the enable falling threshold, the ISL62776 tri-states both outputs. PGOOD and PGOOD_SOC are pulled low with the loss of ENABLE. The Core and SOC VR output voltages decay based on output capacitance and load leakage resistance. If bias to V_{DD} falls below the POR level, the ISL62776 responds in the manner previously described. When V_{DD} and ENABLE rise above their respective rising thresholds, the internal DAC circuitry reacquires a pre-PWROK metal VID code and the controller soft-starts.

5.2 SVI Interface Active

When the Core and SOC VRs successfully soft-start and the PGOOD and PGOOD_SOC signals transition high, PWROK can be asserted externally to the ISL62776. When PWROK is asserted to the IC, SVI instructions can begin as the controller actively monitors the SVI interface. Details about the SVI Bus protocol are provided in the “AMD Serial VID Interface 2.0 (SVI 2.0) Specification”. See AMD publication #48022.

When a VID change command is received, the ISL62776 decodes the information to determine which VR is affected. The VID target is determined by the byte combinations in Table 5. The internal DAC circuitry steps the output voltage of the VR commanded to the new VID level. During this time, one or more of the VR outputs can be targeted. If either VR is commanded to power off by serial VID commands, the PGOOD signal remains asserted.

If the PWROK input is deasserted, the controller steps both the Core and the SOC VRs back to the stored pre-PWROK metal VID level in the holding register from initial soft-start. No attempt is made to read the SVC and SVD inputs during this time. If PWROK is reasserted, the ISL62776 SVI interface waits for instructions.

If ENABLE goes low during normal operation, all external MOSFETs are tri-stated and both PGOOD and PGOOD_SOC are pulled low. This event clears the pre-PWROK metal VID code, forces the controller to check SVC and SVD upon restart, and stores the pre-PWROK metal VID code found on restart.

A POR event on either VCC or VIN during normal operation shuts down both regulators and pulls both PGOOD outputs low. The pre-PWROK metal VID code is not retained. Loss of VIN during operation typically causes the controller to enter a fault condition on one or both outputs. The controller shuts down both Core and SOC VRs and latches off. The pre-PWROK metal VID code is not retained during the process of cycling ENABLE to reset the fault latch and restart the controller.

5.3 VID-on-the-Fly Transition

When PWROK is high, the ISL62776 detects this flag and begins monitoring the SVC and SVD pins for SVI instructions. The microprocessor follows the protocol outlined in the following sections to send instructions for VID-on-the-fly transitions. The ISL62776 decodes the instruction and acknowledges the new VID code. For VID codes higher than the current VID level, the ISL62776 begins stepping the commanded VR outputs to the new VID target at the programmed slew rate; see Table 3. When the DAC ramps to the new VID code, a VID-on-the-fly Complete (VOTFC) request is sent on the SVI lines.

When the VID codes are lower than the current VID level, the ISL62776 checks the state of the power state bits in the SVI command. If the power state bits are not active, the controller begins stepping the regulator output to the new VID target. If the power state bits are active, the controller allows the output voltage to decay and slowly steps the DAC down with the natural decay of the output. This decay allows the controller to quickly recover and move to a high VID code if commanded. The controller issues a VOTFC code on the SVI lines when the SVI command is decoded and before reaching the final output voltage.

VOTFC requests do not take priority over telemetry per the AMD SVI 2.0 specification.

5.4 SVI Data Communication Protocol

The SVI WIRE protocol is based on the I^2C bus concept. The Serial Clock (SVC) and Serial Data (SVD) wires carry information between the AMD processor (master) and VR controller (slave) on the bus. The master initiates and terminates SVI transactions and drives the clock (SVC) during a transaction. The AMD processor is always the master and the voltage regulators are the slaves. The slave receives the SVI transactions and acts accordingly. Mobile SVI WIRE protocol timing is based on high-speed mode I^2C. See AMD publication #48022 for more information.

Table 5. Serial VID Codes

SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)
0000_0000	1.55000	0010_0000	1.35000	0100_0000	1.15000	0110_0000	0.95000
0000_0001	1.54375	0010_0001	1.34375	0100_0001	1.14375	0110_0001	0.94375
0000_0010	1.53750	0010_0010	1.33750	0100_0010	1.13750	0110_0010	0.93750
0000_0011	1.53125	0010_0011	1.33125	0100_0011	1.13125	0110_0011	0.93125
0000_0100	1.52500	0010_0100	1.32500	0100_0100	1.12500	0110_0100	0.92500
0000_0101	1.51875	0010_0101	1.31875	0100_0101	1.11875	0110_0101	0.91875
0000_0110	1.51250	0010_0110	1.31250	0100_0110	1.11250	0110_0110	0.91250
0000_0111	1.50625	0010_0111	1.30625	0100_0111	1.10625	0110_0111	0.90625
0000_1000	1.50000	0010_1000	1.30000	0100_1000	1.10000	0110_1000	0.90000
0000_1001	1.49375	0010_1001	1.29375	0100_1001	1.09375	0110_1001	0.89375
0000_1010	1.48750	0010_1010	1.28750	0100_1010	1.08750	0110_1010	0.88750
0000_1011	1.48125	0010_1011	1.28125	0100_1011	1.08125	0110_1011	0.88125
0000_1100	1.47500	0010_1100	1.27500	0100_1100	1.07500	0110_1100	0.87500
0000_1101	1.46875	0010_1101	1.26875	0100_1101	1.06875	0110_1101	0.86875
0000_1110	1.46250	0010_1110	1.26250	0100_1110	1.06250	0110_1110	0.86250
0000_1111	1.45625	0010_1111	1.25625	0100_1111	1.05625	0110_1111	0.85625
0001_0000	1.45000	0011_0000	1.25000	0101_0000	1.05000	0111_0000	0.85000
0001_0001	1.44375	0011_0001	1.24375	0101_0001	1.04375	0111_0001	0.84375
0001_0010	1.43750	0011_0010	1.23750	0101_0010	1.03750	0111_0010	0.83750
0001_0011	1.43125	0011_0011	1.23125	0101_0011	1.03125	0111_0011	0.83125
0001_0100	1.42500	0011_0100	1.22500	0101_0100	1.02500	0111_0100	0.82500
0001_0101	1.41875	0011_0101	1.21875	0101_0101	1.01875	0111_0101	0.81875

Table 5. Serial VID Codes (Continued)

SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)
0001_0110	1.41250	0011_0110	1.21250	0101_0110	1.01250	0111_0110	0.81250
0001_0111	1.40625	0011_0111	1.20625	0101_0111	1.00625	0111_0111	0.80625
0001_1000	1.40000	0011_1000	1.20000	0101_1000	1.00000	0111_1000	0.80000
0001_1001	1.39375	0011_1001	1.19375	0101_1001	0.99375	0111_1001	0.79375
0001_1010	1.38750	0011_1010	1.18750	0101_1010	0.98750	0111_1010	0.78750
0001_1011	1.38125	0011_1011	1.18125	0101_1011	0.98125	0111_1011	0.78125
0001_1100	1.37500	0011_1100	1.17500	0101_1100	0.97500	0111_1100	0.77500
0001_1101	1.36875	0011_1101	1.16875	0101_1101	0.96875	0111_1101	0.76875
0001_1110	1.36250	0011_1110	1.16250	0101_1110	0.96250	0111_1110	0.76250
0001_1111	1.35625	0011_1111	1.15625	0101_1111	0.95625	0111_1111	0.75625
1000_0000	0.75000	1010_0000	0.55000 (Note 7)	1100_0000	0.35000 (Note 7)	1110_0000	0.15000 (Note 7)
1000_0001	0.74375	1010_0001	0.54375 (Note 7)	1100_0001	0.34375 (Note 7)	1110_0001	0.14375 (Note 7)
1000_0010	0.73750	1010_0010	0.53750 (Note 7)	1100_0010	0.33750 (Note 7)	1110_0010	0.13750 (Note 7)
1000_0011	0.73125	1010_0011	0.53125 (Note 7)	1100_0011	0.33125 (Note 7)	1110_0011	0.13125 (Note 7)
1000_0100	0.72500	1010_0100	0.52500 (Note 7)	1100_0100	0.32500 (Note 7)	1110_0100	0.12500 (Note 7)
1000_0101	0.71875	1010_0101	0.51875 (Note 7)	1100_0101	0.31875 (Note 7)	1110_0101	0.11875 (Note 7)
1000_0110	0.71250	1010_0110	0.51250 (Note 7)	1100_0110	0.31250 (Note 7)	1110_0110	0.11250 (Note 7)
1000_0111	0.70625	1010_0111	0.50625 (Note 7)	1100_0111	0.30625 (Note 7)	1110_0111	0.10625 (Note 7)
1000_1000	0.70000	1010_1000	0.50000 (Note 7)	1100_1000	0.30000 (Note 7)	1110_1000	0.10000 (Note 7)
1000_1001	0.69375	1010_1001	0.49375 (Note 7)	1100_1001	0.29375 (Note 7)	1110_1001	0.09375 (Note 7)
1000_1010	0.68750	1010_1010	0.48750 (Note 7)	1100_1010	0.28750 (Note 7)	1110_1010	0.08750 (Note 7)
1000_1011	0.68125	1010_1011	0.48125 (Note 7)	1100_1011	0.28125 (Note 7)	1110_1011	0.08125 (Note 7)
1000_1100	0.67500	1010_1100	0.47500 (Note 7)	1100_1100	0.27500 (Note 7)	1110_1100	0.07500 (Note 7)
1000_1101	0.66875	1010_1101	0.46875 (Note 7)	1100_1101	0.26875 (Note 7)	1110_1101	0.06875 (Note 7)
1000_1110	0.66250	1010_1110	0.46250 (Note 7)	1100_1110	0.26250 (Note 7)	1110_1110	0.06250 (Note 7)
1000_1111	0.65625	1010_1111	0.45625 (Note 7)	1100_1111	0.25625 (Note 7)	1110_1111	0.05625 (Note 7)
1001_0000	0.65000	1011_0000	0.45000 (Note 7)	1101_0000	0.25000 (Note 7)	1111_0000	0.05000 (Note 7)
1001_0001	0.64375	1011_0001	0.44375 (Note 7)	1101_0001	0.24375 (Note 7)	1111_0001	0.04375 (Note 7)
1001_0010	0.63750	1011_0010	0.43750 (Note 7)	1101_0010	0.23750 (Note 7)	1111_0010	0.03750 (Note 7)

Table 5. Serial VID Codes (Continued)

SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)	SVID[7:0]	Voltage (V)
1001_0011	0.63125	1011_0011	0.43125 (Note 7)	1101_0011	0.23125 (Note 7)	1111_0011	0.03125 (Note 7)
1001_0100	0.62500	1011_0100	0.42500 (Note 7)	1101_0100	0.22500 (Note 7)	1111_0100	0.02500 (Note 7)
1001_0101	0.61875	1011_0101	0.41875 (Note 7)	1101_0101	0.21875 (Note 7)	1111_0101	0.01875 (Note 7)
1001_0110	0.61250	1011_0110	0.41250 (Note 7)	1101_0110	0.21250 (Note 7)	1111_0110	0.01250 (Note 7)
1001_0111	0.60625	1011_0111	0.40625 (Note 7)	1101_0111 (Note 7)	0.20625 (Note 7)	1111_0111	0.00625 (Note 7)
1001_1000	0.60000 (Note 7)	1011_1000	0.40000 (Note 7)	1101_1000	0.20000 (Note 7)	1111_1000	OFF (Note 7)
1001_1001	0.59375 (Note 7)	1011_1001	0.39375 (Note 7)	1101_1001	0.19375 (Note 7)	1111_1001	OFF (Note 7)
1001_1010	0.58750 (Note 7)	1011_1010	0.38750 (Note 7)	1101_1010	0.18750 (Note 7)	1111_1010	OFF (Note 7)
1001_1011	0.58125 (Note 7)	1011_1011	0.38125 (Note 7)	1101_1011	0.18125 (Note 7)	1111_1011	OFF (Note 7)
1001_1100	0.57500 (Note 7)	1011_1100	0.37500 (Note 7)	1101_1100	0.17500 (Note 7)	1111_1100	OFF (Note 7)
1001_1101	0.56875 (Note 7)	1011_1101	0.36875 (Note 7)	1101_1101	0.16875 (Note 7)	1111_1101	OFF (Note 7)
1001_1110	0.56250 (Note 7)	1011_1110	0.36250 (Note 7)	1101_1110	0.16250 (Note 7)	1111_1110	OFF (Note 7)
1001_1111	0.55625 (Note 7)	1011_1111	0.35625 (Note 7)	1101_1111	0.15625 (Note 7)	1111_1111	OFF (Note 7)

Note:
7. VID not required for AMD Family 10h processors. AMD processor requirements are loosened at these levels.

5.5 SVI Bus Protocol

The AMD processor bus protocol is compliant with the SMBus send byte protocol for VID transactions. Figure 17 shows the AMD SVD packet structure.

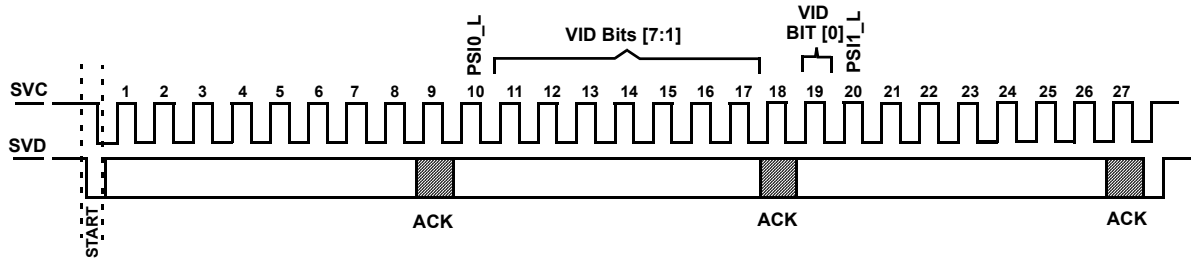


Figure 17. SVD Packet Structure

Table 6 contains the descriptions of each bit of the three bytes that make up the SVI command. During a transaction, the processor sends the start sequence followed by each of the three bytes, which end with an optional Acknowledge (ACK) bit. The ISL62776 does not drive the SVD line during the ACK bit. Finally, the processor sends the stop sequence. After the ISL62776 detects the stop, it can proceed with the commanded action from the transaction.

Table 6. SVD Data Packet

Bits	Description
1:5	Always 11000b
6	Core domain selector bit. If set, the following data byte contains the VID, power state, telemetry control, load line trim, and offset trim to apply to the Core VR.
7	SOC domain selector bit. If set, the following data byte contains the VID, power state, telemetry control, load line trim, and offset trim to apply to the SOC VR.
8	Always 0b
9	ACK bit
10	PSI0_L
11:17	VID code bits [7:1]
18	ACK bit
19	VID code bit [0]
20	PSI1_L
21	TFN (Telemetry Functionality)
22:24	Load line slope trim
25:26	Offset trim [1:0]
27	ACK bit

5.6 Power States

SVI 2.0 defines two power state indicator levels, PSI0_L and PSI1L. See Table 7 for information about these power state indicators. As processor current consumption is reduced, the power state indicator level changes to improve VR efficiency under low power conditions.

Table 7. PSI0_L and PSI1_L Definition

Function	Bit	Description
PSI0_L	10	Power State Indicate Level 0. When this signal is asserted (active Low), the processor is in a low enough power state for the ISL62776 to boost efficiency by dropping phases and entering 1-Phase CCM.
PSI1_L	20	Power State Indicate Level 1. When this signal is asserted (active Low), the processor is in a low enough power state for the ISL62776 to boost efficiency by dropping phases and entering 1-Phase DEM.

When the Core VR is operating in 3-phase mode and PSI0_L is asserted, Channels 2 and 3 are tri-stated and Channel 1 remains active in CCM mode. When PSI1_L is asserted, Channel 1 enters into enters Diode Emulation Mode (DEM) to boost efficiency.

When PSI0_L is asserted for the SOC VR, the SOC regulator remains in Continuous Conduction Mode (CCM). When PSI1_L is asserted, the SOC VR transitions to DEM to boost efficiency.

The processor can assert or deassert PSI0_L and PSI1_L out of order. PSI0_L takes priority over PSI1_L. If PSI0_L is deasserted while PSI1_L is still asserted, the ISL62776 returns the selected VR back to full channel CCM operation.

5.7 Dynamic Load Line Slope Trim

The ISL62776 supports the SVI 2.0 ability for the processor to manipulate the load line slope of the Core and SOC VRs independently using the serial VID interface. The slope manipulation applies to the initial load line slope. A load line slope trim typically coincides with a VOTF change. See Table 8 for more information about the load line slope trim feature.

Table 8. Load Line Slope Trim Definition

Load Line Slope Trim [2:0]	Description
000	Disable LL
001	-40% mΩ change
010	-20% mΩ change
011	No change
100	+20% mΩ change
101	+40% mΩ change
110	+60% mΩ change
111	+80% mΩ change

5.8 Dynamic Offset Trim

The ISL62776 supports the SVI 2.0 ability for the processor to manipulate the output voltage offset of the Core and SOC VRs. See Table 9 for offset values. This offset is in addition to any output voltage offset set from the COMP resistor reader. The dynamic offset trim can disable the COMP resistor programmed offset of either output when **Disable All Offset** is selected.

Table 9. Offset Trim Definition

Offset Trim [1:0]	Description
00	Disable All Offset
01	-25mV change
10	0mV change
11	+25mV change

6. Telemetry

The ISL62776 can provide voltage and current information to the AMD processor through the telemetry system outlined by the AMD SVI 2.0 specification. The telemetry data is transmitted through the SVC and SVT lines of the SVI 2.0 interface.

Current telemetry is based on a voltage generated across the recommended 133kΩ resistor placed from the IMON pin to GND. The current flowing out of the IMON pin is proportional to the load current in the VR. The I_{sum} current defined in Voltage Regulation and Load Line Implementation provides the base conversion from the load current to the I_{sum} current created by the internal amplifier. The I_{sum} current is then divided down by a factor of 4 to create the IMON current, which flows out of the IMON pin. The I_{sum} current measures 36µA when the load current is at full load based on a droop current designed for 45µA at the same load current. The difference between the I_{sum} current and the droop current is provided in Equation 2. The IMON current measures 11.25µA at full load current for the VR and the IMON voltage is 1.2V. The load percentage reported by the IC is based on the this voltage. When the load is 25% of the full load, the voltage on the IMON pin is 25% of 1.2V or 0.3V.

The SVI interface allows the selection of no telemetry, voltage only, or voltage and current telemetry on either or both of the VR outputs. The processor uses the TFN bit and the Core and SOC domain selector bits to change the telemetry functionality. See Table 10 for more information.

Table 10. TFN Truth Table

TFN, Core, SOC Bits [21, 6, 7]	Description
1, 0, 1	Telemetry is in voltage and current mode, so the voltage and current are sent for the VDD and VDDSOC domains by the controller.
1, 0, 0	Telemetry is in voltage mode only. The controller sends only the voltage of VDD and VDDSOC domains.
1, 1, 0	Telemetry is disabled.
1, 1, 1	Reserved

7. Protection Features

The Core VR and SOC VR both provide overcurrent, current-balance, undervoltage, and overvoltage fault protections. The controller provides over-temperature protection.

7.1 Overcurrent

You can use the IMON voltage to determine the load current at any moment in time. The Overcurrent Protection (OCP) circuitry monitors the IMON voltage to determine when a fault occurs. Based on the description in Voltage Regulation and Load Line Implementation, the current that flows out of the IMON pin is proportional to the I_{sum} current. The I_{sum} current is created from the sensed voltage across Cn, which is a measure of the load current based upon the sensing element selected. The IMON current is generated internally and is 1/4 of the I_{sum} current. The EDC or IDDspike current value for the AMD CPU load sets the maximum current level for droop and the IMON voltage of 1.2V, which indicates 100% loading for telemetry. The I_{sum} current level at maximum load, or IDDspike, is 36µA, which translates to an IMON current level of 9µA. The IMON resistor is 133kΩ and the 9µA flowing through the IMON resistor results in a 1.2V level at maximum loading of the VR.

The overcurrent threshold is 1.5V on the IMON pin. Based on a 1.2V IMON voltage equating to 100% loading, the additional 0.3V provided above this level equates to a 25% increase in load current before an OCP fault is detected. The EDC or IDDspike current is sets the 1.2V on IMON for full load current, so the OCP level is 1.25 times the EDC or IDDspike current level. This additional margin above the EDC or IDDspike current allows the AMD CPU to enter and exit the IDDspike performance mode without issue unless the load current is out of line with the IDDspike expectation, thus the need for overcurrent protection.

When the voltage on the IMON pin meets the overcurrent threshold of 1.5V, an OCP event occurs. Within 2µs of detecting an OCP event, the controller asserts VR_HOT_L low to communicate to the AMD CPU to throttle back. A fault timer begins counting while IMON is at or above the 1.5V threshold. The fault timer lasts 7.5µs to 11µs, then flags an OCP fault. The controller then tri-states the active channels and goes into shutdown. PGOOD goes low and a fault flag from this VR is sent to the other VR, which is shut down within 10µs. If the IMON voltage drops below the 1.5V threshold before the fault timer count finishes, the fault timer is cleared and VR_HOT_L is taken high.

The ISL62776 also features a Way-Overcurrent (WOC) feature that immediately takes the controller into shutdown. This protection is also referred to as fast overcurrent protection for short-circuit protection. If the IMON current reaches 15µA, WOC is triggered, active channels are tri-stated, the controller is placed in shutdown, and PGOOD is pulled low. There is no fault timer on the WOC fault; the controller takes immediate action. The other controller output is also shut down within 10µs.

7.2 Current Balance

The controller monitors the ISENx pin voltages to determine current balance protection. If the ISENx pin voltage difference is greater than 9mV for 1ms, the controller declares a fault and latches off.

7.3 Undervoltage

If the VSEN pin voltage falls below the output voltage VID value plus any programmed offsets by -325mV, the controller declares an undervoltage fault. The controller deasserts PGOOD and tri-states the power MOSFETs.

7.4 Overvoltage

If the VSEN pin voltage exceeds the output voltage VID value plus any programmed offsets by +325mV, the controller declares an overvoltage fault. The controller deasserts PGOOD and turns on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value. When the output voltage is below this level, the lower gate is tri-stated. If the output voltage rises above the overvoltage threshold again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing output ringing below ground.

7.5 Thermal Monitor (NTC, NTC_SOC)

The ISL62776 has two thermal monitors that use an external resistor network, which includes an NTC thermistor, to monitor motherboard temperature and alert the AMD CPU of a thermal issue. Figure 18 shows the basic thermal monitor circuit on the Core VR NTC pin. The SOC VR features the same thermal monitor. The controller drives a 30µA current out of the NTC pin and monitors the voltage at the pin. The current flowing out of the NTC pin creates a voltage that is compared to a warning threshold of 660mV. When the voltage at the NTC pin falls to this warning threshold or below, the controller asserts VR_HOT_L to alert the AMD CPU to throttle back load current to stabilize the motherboard temperature. A thermal fault counter begins counting toward a minimum shutdown time of 100µs. The thermal fault counter is an up/down counter, so if the voltage at the NTC pin rises above the warning threshold, it counts down and extends the time for a thermal fault to occur. The warning threshold has 20mV of hysteresis.

If the voltage at the NTC pin continues to fall down to the shutdown threshold of 600mV or below, the controller goes into shutdown and triggers a thermal fault. The PGOOD pin is pulled low and tri-states the power MOSFETs. A fault on either side shuts down both VRs.

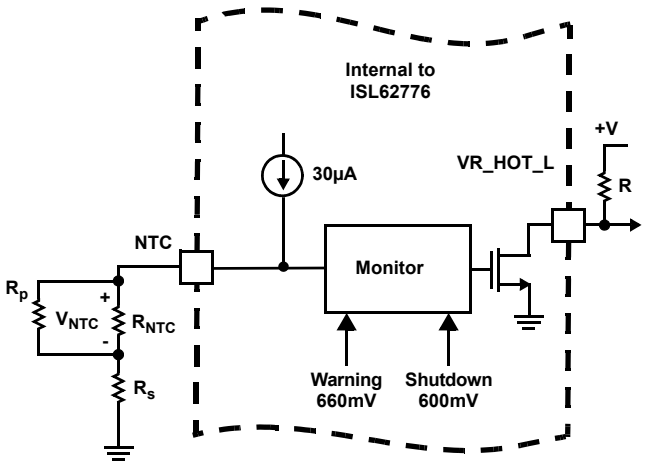


Figure 18. Circuitry Associated With the Thermal Monitor Feature of the ISL62776

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the over-temperature trip threshold, VR_HOT is pulled low. The VR_HOT signal changes the CPU operation and decreases power consumption. When the CPU power consumption decreases, the board temperature decreases and the NTC thermistor voltage rises. When the over-temperature threshold is tripped and VR_HOT goes low, the over-temperature threshold changes to the reset level. The addition of hysteresis to the over-temperature threshold prevents nuisance trips. When both pin voltages exceed the over-temperature reset threshold, the pull-down on VR_HOT is released. The signal changes state, the CPU resumes normal operation, and the over-temperature threshold returns to the trip level.

Table 11 summarizes the fault protections.

Table 11. Fault Protection Summary

Fault Type	Fault Duration Before Protection	Protection Action	Fault Reset
Overcurrent	7.5µs to 11.5µs	PWM tri-state, PGOOD latched low	ENABLE toggle or VDD toggle
Phase Current Unbalance	1ms		
Way-Overcurrent (1.5xOC)	Immediately		
Undervoltage -325mV		PWM tri-state, PGOOD latched low	
Overvoltage +325mV		PGOOD latched low. Actively pulls the output voltage to below VID value, then tri-states.	
NTC Thermal	100µs minimum	PWM tri-state, PGOOD latched low	

7.6 Fault Recovery

All of the fault conditions can be reset by bringing ENABLE low or by bringing VDD below the POR threshold. When ENABLE and VDD return to their high operating levels, the controller resets the faults and soft-start occurs.

7.7 Interface Pin Protection

When removing power to VDD and VDDIO but leaving power applied to the SVC and SVD pins, the SVC and SVD protection diodes must be considered. Figure 19 shows the basic protection on the pins. If SVC and/or SVD are powered but VDD is not, leakage current flows from these pins to VDD.

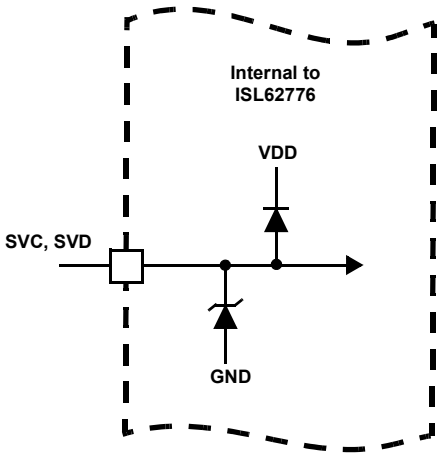


Figure 19. Protection Diodes on the SVC and SVD Pins

8. Selecting Key Components

8.1 Inductor DCR Current-Sensing Network

Figure 20 shows the inductor DCR current-sensing network for a 3-phase solution. An inductor current flows through the DCR and creates a voltage drop. Each inductor has two resistors in R_{sum} and R_o connected to the pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc}, and R_p) and capacitor C_n. R_{ntc} is a negative temperature coefficient (NTC) thermistor that temperature-compensates the inductor DCR change.

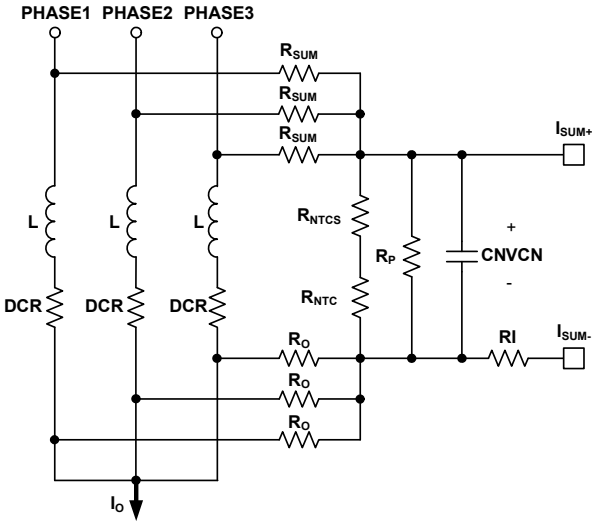


Figure 20. DCR Current-Sensing Network

The inductor output side pads are electrically shorted in the schematic but have some parasitic impedance in actual board layout, so they cannot be shorted together for the current-sensing summing network. Renesas recommends using 1Ω~10Ω R_o to create quality signals. Because the R_o value is much smaller than the rest of the current sensing circuit, the following analysis ignores it.

The summed inductor current information is presented to the capacitor C_n. Equations 18 through Equation 22 describe the frequency domain relationship between the inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

(EQ. 18) $$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s)$$

(EQ. 19) $$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p}$$

(EQ. 20) $$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}}$$

(EQ. 21) $$\omega_L = \frac{DCR}{L}$$

(EQ. 22) $$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n}$$

where N is the number of phases.

Transfer function $A_{cs}(s)$ always has unity gain at DC. The inductor DCR value increases as the winding temperature increases, causing a higher reading of the inductor DC current. The NTC R_{ntc} value decrease as its temperature decreases. Proper selection of R_{sum}, R_{ntcs}, R_p, and R_{ntc} parameters ensures that V_{Cn} represents the inductor total DC current over the temperature range of interest.

Many sets of parameters can properly temperature-compensate the DCR change. Because the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. Renesas recommends using a higher ratio of V_{cn} to the inductor DCR voltage so the droop circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, and R_{ntc} = 10kΩ (ERT-J1VR103J). The NTC network parameters may need to be fine tuned on actual boards. Apply full load DC current and record the output voltage reading immediately, then record the output voltage reading again when the board reaches the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. Renesas recommends following the evaluation board layout and current sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ needs to represent real-time $I_o(s)$ for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ has a pole w_{sns} and a zero w_L. Match w_L and w_{sns} so $A_{cs}(s)$ is unity gain at all frequencies. By forcing w_L equal to w_{sns} and solving for the solution, Equation 23 gives C_n.

(EQ. 23) $$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, and L = 0.36µH, Equation 23 gives C_n = 0.406µF.

Assuming the compensator design is correct, Figure 21 shows the expected load transient response waveforms if C_n is correctly selected. When the load current I_{core} has a square change, the output voltage V_{core} also has a square response.

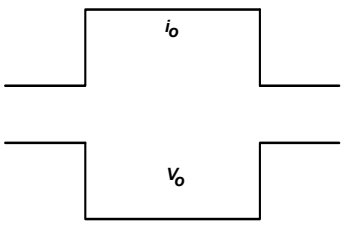


Figure 21. Desired Load Transient Response Waveforms

If C_n is too large or too small, $V_{Cn}(s)$ does not accurately represent real-time $I_o(s)$ and worsens the transient response. Figure 22 shows the load transient response when C_n is too small. V_{core} sags excessively upon load insertion and can create a system failure. Figure 23 shows the transient response when C_n is too large. V_{core} is sluggish in drooping to its final value. There is excessive overshoot if load insertion occurs during this time, which can negatively affect the CPU reliability.

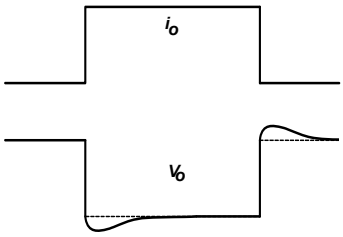


Figure 22. Load Transient Response When C_n is Too Small

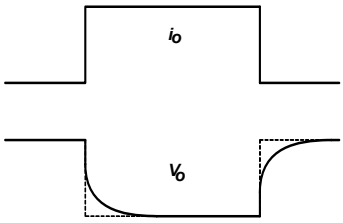


Figure 23. Load Transient Response When C_n is Too Large

Figure 24 shows the output voltage ringback problem during load transient response. The load current i_o has a fast step change but the inductor current i_L cannot accurately follow. Instead, i_L responds in first-order system fashion due to the nature of the current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_o dip quickly upon load current change. However, the controller regulates V_o according to the droop current i_{droop}, which is a real-time representation of i_L; therefore, it pulls V_o back to the level dictated by i_L, causing ringback. Ringback does not occur if the output capacitor has very low ESR and ESL, as is the case with all ceramic capacitors.

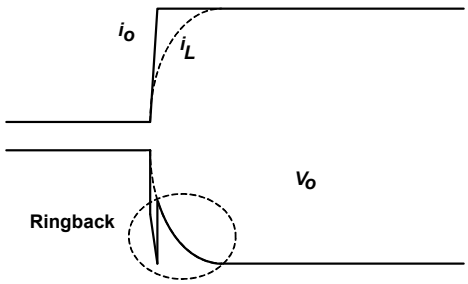


Figure 24. Output Voltage Ringback Problem

Figure 25 shows two optional circuits for ringback reduction. C_n is the capacitor used to match the inductor time constant. Usually, two or more parallel capacitors are required to get the desired value. Figure 25 shows that two capacitors ($C_{n.1}$ and $C_{n.2}$) are in parallel. Resistor R_n is an optional component to reduce the V_o ringback. At steady state, $C_{n.1}$ + $C_{n.2}$ provides the desired C_n capacitance. At the beginning of the i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 22 shows, V_o tends to dip when C_n is too small. This effect reduces the V_o ringback. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$ and when R_n is large. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. Renesas recommends keeping $C_{n.2}$ greater than 2200pF. The R_n value is usually a few Ω. Determine the $C_{n.1}$, $C_{n.2}$, and R_n values by tuning the load transient response waveforms on an actual board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of the i_o change. R_{ip} and C_{ip} do not have any effect at steady state. By properly selecting the R_{ip} and C_{ip} values, i_{droop} can resemble i_o rather than i_L and V_o does not ring back. The recommended value for R_{ip} is 100Ω. Determine C_{ip} by tuning the load transient response waveforms on an actual board. The recommended range for C_{ip} is 100pF~2000pF. However, the R_{ip} - C_{ip} branch may distort the i_{droop} waveform. Instead of being triangular like the real inductor current, i_{droop} may have sharp spikes, which can adversely affect i_{droop} average value detection and therefore can affect OCP accuracy. User discretion is advised.

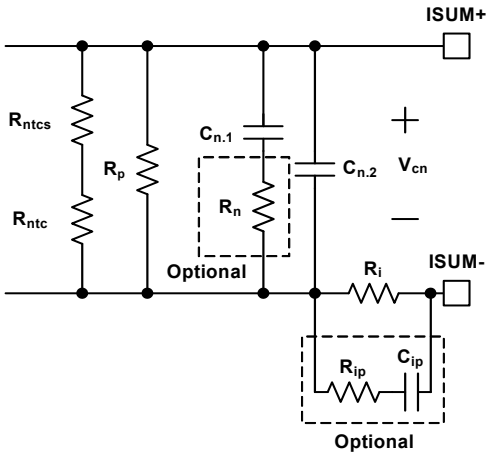


Figure 25. Optional Circuits for Ringback Reduction

8.2 Resistor Current-Sensing Network

Figure 26 shows the resistor current-sensing network for a 3-phase solution.

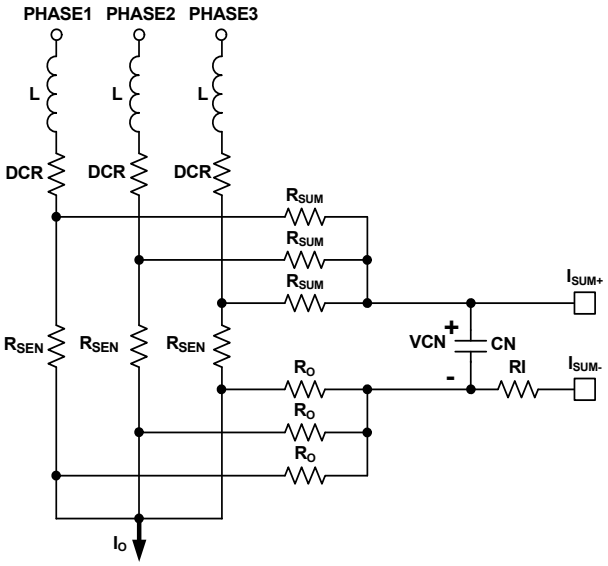


Figure 26. Resistor Current-Sensing Network

Each inductor has a series current sensing resistor, R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equation 24 through Equation 26 give the $V_{Cn}(s)$ expression.

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_o(s) \times A_{Rsen}(s) \quad \text{(EQ. 24)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 25)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 26)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. The current-sensing resistor R_{sen} value does not have significant variation over-temperature, so the NTC network is not needed.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

8.3 Overcurrent Protection

Resistor R_i sets the I_{sum} current which is proportional to droop current and IMON current. See Equation 2 and Figures 20, 24, and 26. Table 1 and Table 2 show the internal OCP threshold based on the IMON pin voltage. Because the R_i resistor impacts both the droop current and the IMON current, fine adjustments to I_{droop} requires changing the R_{comp} resistor.

For example, the OCP threshold is 1.5V on the IMON pin, which equates to an IMON current of 11.25µA using a 133kΩ IMON resistor. The corresponding I_{sum} is 45µA, resulting in an I_{droop} of 56.25µA. At full load current, I_{omax}, the I_{sum} current is 36µA and the resulting I_{droop} is 45µA. The ratio of I_{sum} at OCP relative to full load current is 1.25. Therefore, the OCP current trip level is 25% higher than the full load current.

For inductor DCR sensing, Equation 27 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$:

$$V_{Cn} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o \quad \text{(EQ. 27)}$$

Substituting Equation 27 into Equation 2 gives Equation 28:

$$I_{droop} = \frac{5}{4} \times \frac{1}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \times I_o \quad \text{(EQ. 28)}$$

Therefore:

$$R_i = \frac{5}{4} \times \frac{R_{ntcnet} \times DCR \times I_o}{N \times \left(R_{ntcnet} + \frac{R_{sum}}{N} \right) \times I_{droop}} \quad \text{(EQ. 29)}$$

Substituting Equation 19 and applying the OCP condition in Equation 29 gives Equation 30:

$$R_i = \frac{5}{4} \times \frac{\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \times DCR \times I_{omax}}{N \times \left(\frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} + \frac{R_{sum}}{N} \right) \times I_{droopmax}} \quad \text{(EQ. 30)}$$

where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current.

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.88mΩ, I_{omax} = 65A, and $I_{droopmax}$ = 45µA, Equation 30 gives R_i = 439Ω.

For resistor sensing, Equation 31 gives the DC relationship of $V_{cn}(s)$ and $I_o(s)$.

$$V_{Cn} = \frac{R_{sen}}{N} \times I_o \quad \text{(EQ. 31)}$$

Substituting Equation 31 into Equation 2 gives Equation 32:

(EQ. 32) $$I_{droop} = \frac{5}{4} \times \frac{1}{R_i} \times \frac{R_{sen}}{N} \times I_o$$

Therefore:

(EQ. 33) $$R_i = \frac{5}{4} \times \frac{R_{sen} \times I_o}{N \times I_{droop}}$$

Substituting Equation 33 and applying the OCP condition in Equation 29 gives Equation 34:

(EQ. 34) $$R_i = \frac{5}{4} \times \frac{R_{sen} \times I_{omax}}{N \times I_{droopmax}}$$

where I_{omax} is the full load current and $I_{droopmax}$ is the corresponding droop current.

For example, given N = 3, R_{sen} = 1mΩ, I_{omax} = 65A, and $I_{droopmax}$ = 45µA, Equation 34 gives R_i = 602Ω.

8.4 Load-Line Slope

See Figure 13 for load-line implementation.

For inductor DCR sensing, substituting Equation 28 into Equation 3 gives the load line slope expression:

(EQ. 35) $$LL = \frac{V_{droop}}{I_o} = \frac{5}{4} \times \frac{R_{droop}}{R_i} \times \frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N}$$

For resistor sensing, substituting Equation 32 into Equation 3 gives the load line slope expression.

(EQ. 36) $$LL = \frac{V_{droop}}{I_o} = \frac{5}{4} \times \frac{R_{sen} \times R_{droop}}{N \times R_i}$$

Substituting Equation 29 and rewriting Equation 35, or substituting Equation 33 and rewriting Equation 36, gives the same result as in Equation 37:

(EQ. 37) $$R_{droop} = \frac{I_o}{I_{droop}} \times LL$$

Use the full-load condition to calculate R_{droop}. For example, given I_{omax} = 65A, $I_{droopmax}$ = 45µA, and LL = 2.1mΩ, Equation 37 gives R_{droop} = 3.03kΩ.

Renesas recommends starting with the R_{droop} value calculated by Equation 37 and fine-tuning it on the actual board to get accurate load line slope. Record the output voltage readings at no load and at full load for load-line slope calculation. Reading the output voltage at lighter load instead of full load increases the measurement error.

8.5 Compensator

Figure 21 shows the desired load transient response waveforms. Figure 27 shows the equivalent circuit of a voltage regulator (VR) with the droop function. A VR is equivalent to a voltage source (= VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load-line slope LL (that is, a constant output impedance), V_o has a square response when i_o has a square change in the entire frequency range.

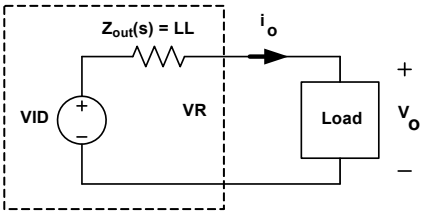


Figure 27. Voltage Regulator Equivalent Circuit

Renesas provides a Microsoft® Excel-®based spreadsheet to help design the compensator and the current sensing network so the VR achieves constant output impedance as a stable system.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 28 conceptually shows T1(s) measurement setup, and Figure 29 conceptually shows T2(s) measurement setup. The VR senses the inductor current, multiplies it by a gain of the load-line slope, adds it on top of the sensed output voltage, and feeds it to the compensator. T1 is measured after the summing node and T2 is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) can actually be measured on an ISL62776 regulator.

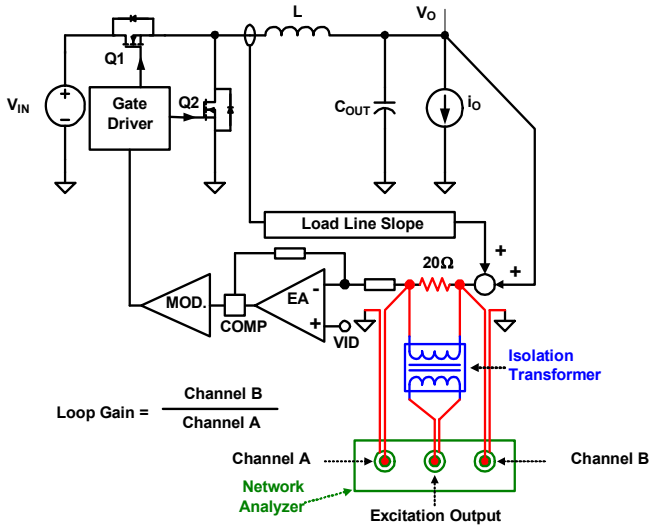


Figure 28. Loop Gain T1(s) Measurement Setup

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s), so it has a higher impact on system stability.

T2(s) is the voltage loop gain with closed droop loop, so it has a higher impact on output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin and an output impedance equal to or smaller than the load-line slope.

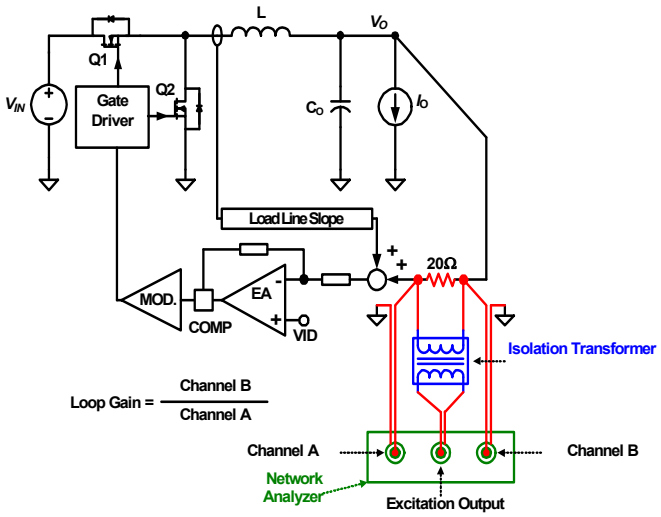


Figure 29. Loop Gain T2(s) Measurement Setup

8.6 Current Balancing

See Figure 14 through Figure 20 for information about current balancing. The ISL62776 achieves current balancing by matching the ISEN pin voltages. R_{isen} and C_{isen} form filters to remove the switching ripple of the phase node voltages. Renesas recommends using a long $R_{isen}C_{isen}$ time constant so that the ISEN voltages have minimal ripple and represent the DC current flowing through the inductors. The recommended values are R_s = 10kΩ and C_s = 0.22µF.

8.7 Thermal Monitor Component Selection

The ISL62776's NTC and NTC_SOC pins monitor the motherboard temperature and alert the AMD CPU if a thermal issue arises. The basic function of this circuitry is described in Thermal Monitor (NTC, NTC_SOC). Figure 30 shows the basic configuration of the NTC resistor, R_{NTC}, and offset resistor, R_S, used to generate the warning and shutdown voltages at the NTC pin.

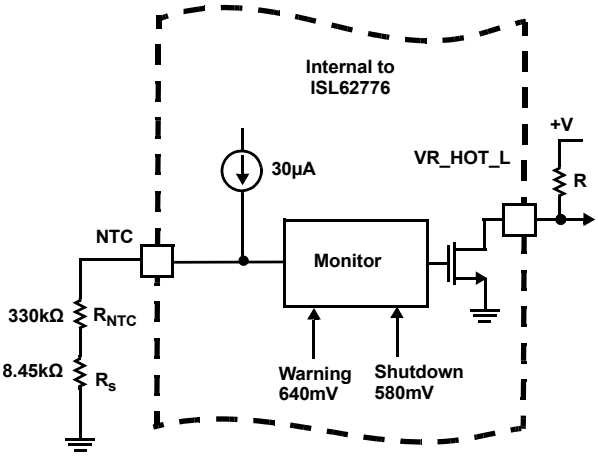


Figure 30. Thermal Monitor Feature of the ISL62776

As the board temperature rises, the NTC thermistor resistance decreases and the voltage at the NTC pin drops. When the voltage on the NTC pin drops below the thermal warning threshold of 0.640V, VR_HOT_L is pulled low. When the AMD CPU detects VR_HOT_L has gone low, it begins throttling back load current on both outputs to reduce the board temperature.

If the board temperature continues to rise, the NTC thermistor resistance drops further and the voltage at the NTC pin could drop below the thermal shutdown threshold of 0.580V. When this threshold is reached, the ISL62776

shuts down both the Core and SOC VRs, indicating a thermal fault occurred before the thermal fault counter triggered a fault.

NTC thermistor selection can vary depending on the resistor network configuration. The equivalent resistance at the typical thermal warning threshold voltage of 0.64V is defined in Equation 38.

$$\frac{0.64V}{30\mu A} = 21.3k\Omega \quad \text{(EQ. 38)}$$

The equivalent resistance at the typical thermal shutdown threshold voltage of 0.58V required to shutdown both outputs is defined in Equation 39.

$$\frac{0.58V}{30\mu A} = 19.3k\Omega \quad \text{(EQ. 39)}$$

The NTC thermistor value correlates to the resistance change between the warning and shutdown thresholds and the required temperature change. If the warning level is designed to occur at a board temperature of +100°C and the thermal shutdown level at a board temperature of +105°C, the thermistor resistance change can be calculated. For example, a Panasonic NTC thermistor with B = 4700 has a resistance ratio of 0.03939 of its nominal value at +100°C and 0.03308 of its nominal value at +105°C. Dividing the required resistance change between the thermal warning threshold and the shutdown threshold by the change in resistance ratio of the NTC thermistor at the two temperatures of interest provides the required NTC resistance is defined (see Equation 40).

$$\frac{(21.3k\Omega - 19.3k\Omega)}{(0.03939 - 0.03308)} = 317k\Omega \quad \text{(EQ. 40)}$$

The closest standard thermistor to the value calculated with B = 4700 is 330kΩ. The NTC thermistor part number is ERTJ0EV334J. The actual resistance change of this standard thermistor value between the warning threshold and the shutdown threshold is calculated in Equation 41.

$$(330k\Omega \cdot 0.03939) - (330k\Omega \cdot 0.03308) = 2.082k\Omega \quad \text{(EQ. 41)}$$

Because the NTC thermistor resistance at +105°C is less than the required resistance from Equation 39, additional resistance in series with the thermistor is required to make up the difference. A standard resistor, 1% tolerance, added in series with the thermistor increases the voltage seen at the NTC pin. The additional resistance required is calculated in Equation 42.

$$19.3k\Omega - 10.916k\Omega = 8.384k\Omega \quad \text{(EQ. 42)}$$

The closest standard 1% tolerance resistor is 8.45kΩ. The NTC thermistor is placed in a hot spot on the board, typically near the upper MOSFET of Channel 1 of the respective output. The standard resistor is placed next to the controller.

8.8 Bootstrap Capacitor Selection

The external drivers feature an internal bootstrap Schottky diode. Add an external capacitor across the BOOT and PHASE pins to complete the bootstrap circuit. The bootstrap capacitor must have a maximum voltage rating above VDDP + 4V and its capacitance value can be chosen from Equation 43:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 43)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet PVCC}{V_{GS1}} \bullet N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs.

The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

9. Layout Guidelines

9.1 PCB Layout Considerations

9.1.1 Power and Signal Layers Placement on the PCB

Generally, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground-plane layer should be adjacent to the signal layer to provide shielding.

9.1.2 Component Placement

The two critical sets of components in a DC/DC converter are the power components and the small signal components. The power components are the most critical because they switch large amounts of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

Place the power components first (see Figure 31). The power components include MOSFETs, input and output capacitors, and the inductor. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each power train. Symmetrical layout allows heat to be dissipated equally across all power trains. Keeping a minimum distance between the power train and the control IC helps keep the gate drive traces short. The drive signals include LGATE, UGATE, PGND, PHASE, and BOOT.

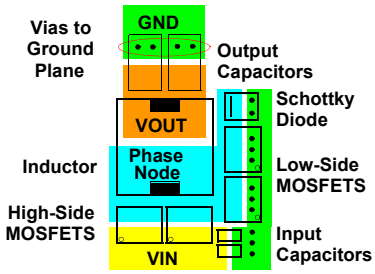


Figure 31. Typical Power Component Placement

When placing MOSFETs, keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible. Place input high-frequency capacitors close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. Place high-frequency output decoupling capacitors (ceramic) as close as possible to the decoupling target (microprocessor), making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has fewer noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Table 12 shows pin layout considerations for the ISL62776 controller.

Table 12. Layout Guidelines

ISL62776 Pin	Symbol	Layout Guidelines
Bottom Pad	GND	Connect this ground pad to the ground plane through a low-impedance path. A minimum of five vias are recommended to connect this pad to the internal ground plane layers of the PCB.
1	PGOOD_SOC	No special considerations.
2	SVC	Use good signal integrity practices and follow AMD processor recommendations.
3	VR_HOT_L	Follow AMD processor recommendations. Place the pull-up resistor near the IC.
4 5 6	SVD VDDIO SVT	Use good signal integrity practices and follow AMD processor recommendations.
7	ENABLE	No special considerations.
8	PWROK	Use good signal integrity practices and follow AMD processor recommendations.
9	PGOOD	No special considerations.

Table 12. Layout Guidelines (Continued)

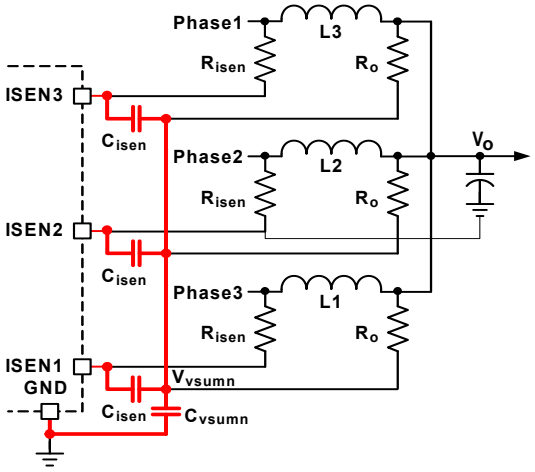
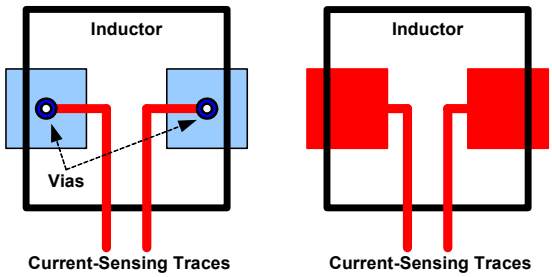
ISL62776 Pin	Symbol	Layout Guidelines
10	NTC	Place the NTC thermistor close to the thermal source that is monitored to determine core thermal throttling. Placement at the hottest spot of the Core VR is recommended. Place additional standard resistors in the resistor network on this pin near the IC.
11	PROG1	Place the PROG1 resistor close to this pin and keep a tight GND connection.
12 13	COMP FB	Place the compensation components in the general proximity of the controller.
14 15 16 17	ISEN1 ISEN2 ISEN3 ISEN4	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN and through another capacitor (C_{vsumn}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: Any ISEN pin to another ISEN pin Any ISEN pin to GND The red traces in the following drawing show the loops to be minimized. 
18 19	ISUMP ISUMN	Place the current-sensing circuit in the general proximity of the controller. Place capacitor Cn very close to the controller. Place the NTC thermistor next to the Core VR Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of VSUMP and VSUMN signals to the controller. Run these two signals traces in parallel fashion with sufficient width (>20 mil). **IMPORTANT:** To sense the inductor current, route the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current-sensing traces. 
20	IMON	Place the IMON resistor close to this pin and keep a tight GND connection.
21	FCCM	No special considerations.
22 23 24 25	PWM1 PWM2 PWM3 PWM4	No special considerations.

Table 12. Layout Guidelines (Continued)

ISL62776 Pin	Symbol	Layout Guidelines
26	VCC	A high-quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin with the filter resistor nearby the IC.
27	RTN	Use signal integrity best practices.
28	GND	Connect this ground pad to the ground plane through a low-impedance path.
29	VIN	Place the decoupling capacitor in close proximity to the pin with a short connection to the internal GND plane.
30	PWM_SOC	No special considerations.
31	FCCM_SOC	No special considerations.
32	GND	Connect this ground pad to the ground plane through a low-impedance path.
33	IMON_SOC	Place the IMON_SOC resistor close to this pin and keep a tight GND connection.
34 35	ISUMN_SOC ISUMP_SOC	Use the same guidelines as the outline for Pins 18 and 19 (ISUMP and ISUMN).
36 37	FB_SOC COMP_SOC	Place the compensation components in the general proximity of the controller.
38	PROG2	No special considerations.
39	NTC_SOC	Place the NTC_SOC thermistor close to the thermal source that is monitored to determine SOC thermal throttling. Placement at the hottest spot of the SOC VR is recommended. Place additional standard resistors in the resistor network on this pin near the IC.
40	GND	Connect this ground pad to the ground plane through a low-impedance path.

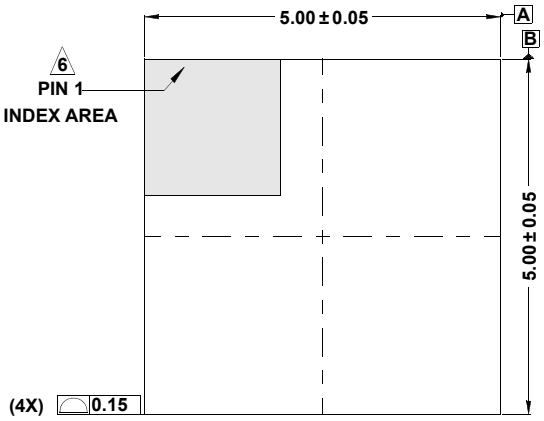
10. Revision History

Rev.	Date	Description
2.00	Oct.8.20	SVC Frequency Range maximum value increased.
1.00	Oct.22.19	Initial release

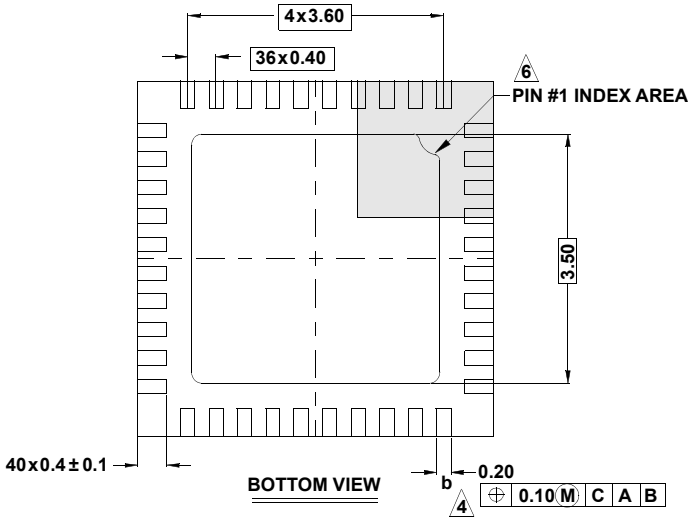
11. Package Outline Drawing

For the most recent package outline drawing, see L40.5x5.

L40.5x5
40 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 7/14

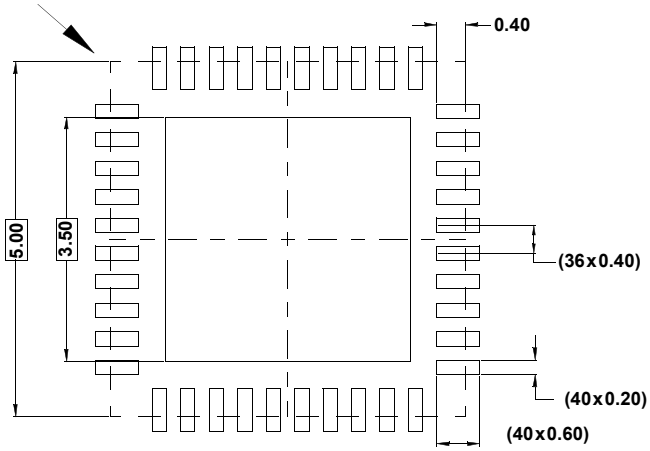


TOP VIEW

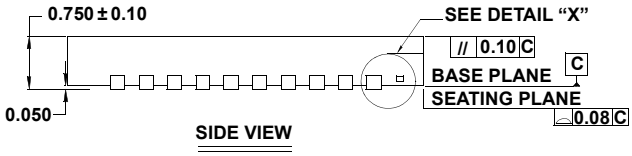


BOTTOM VIEW

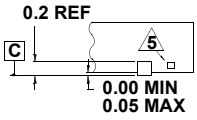
PACKAGE OUTLINE



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.27mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220WHHE-1

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