ISL6625A

Synchronous Rectified Buck MOSFET Drivers

FN7978
Rev 0.00
September 19, 2012

The ISL6625A is a high frequency MOSFET driver designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology.

In ISL6625A, the upper and lower gates are both driven to an externally applied voltage. This provides the capability to optimize applications involving trade-offs between gate charge and conduction losses.

An advanced adaptive shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The ISL6625A has a 10kΩ integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt.

This driver also has an overvoltage protection feature, which is operational while VCC is below the POR threshold. The PHASE node is connected to the gate of the low-side MOSFET (LGATE) via a 30kΩ resistor, limiting the output voltage of the converter close to the gate threshold of the low-side MOSFET. This is dependent on the current being shunted, which provides some protection to the load should the upper MOSFET(s) become shorted.

Applications

- High light load efficiency voltage regulators
- Core regulators for advanced microprocessors
- High current DC/DC converters

Features

- Dual MOSFET drives for synchronous rectified bridge
- Advanced adaptive zero shoot-through protection
  - PHASE detection
  - LGATE detection
  - Auto-Zero of $r_{DS(ON)}$ conduction offset effect
- Low standby bias current
- 36V internal bootstrap switcher
- Bootstrap capacitor overcharging prevention
- Integrated high-side gate-to-source resistor to prevent from self turn-on due to high input bus dV/dt
- Pre-POR overvoltage protection for start-up and shutdown
- Power rails undervoltage protection
- Expandable bottom copper pad for enhanced heat sinking
- Dual flat no-lead (DFN) package
  - Near chip-scale package footprint; improves PCB efficiency and thinner in profile
- Pb-Free (RoHS compliant)

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB417 “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators”

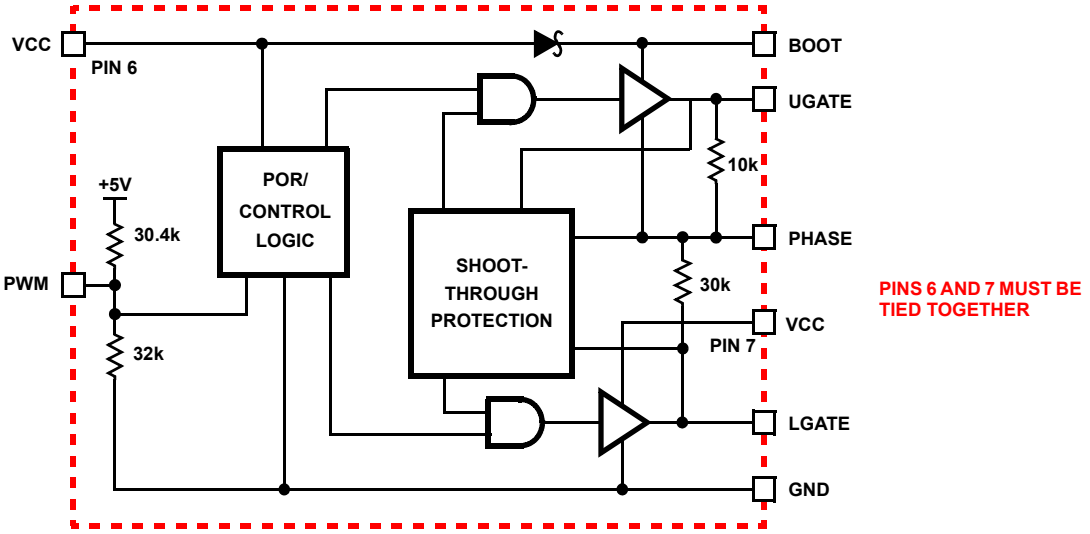


FIGURE 1. BLOCK DIAGRAM

Ordering Information

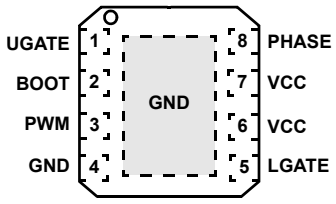
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6625ACRZ-T	5AZ	0 to +70	8 Ld 2x2 DFN	L8.2x2D
ISL6625AIRZ-T	25A	-40 to +85	8 Ld 2x2 DFN	L8.2x2D

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6625A. For more information on MSL please see tech brief TB363

Pin Configuration

ISL6625A
(8 LD 2x2 DFN)
TOP VIEW



Functional Pin Descriptions

PIN #	PIN SYMBOL	FUNCTION
1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Internal Bootstrap Device” on page 6 for guidance in choosing the capacitor value.
3	PWM	The PWM signal is the control input for the driver. The PWM signal can enter three distinct states during operation, see the three-state PWM Input section for further details. Connect this pin to the PWM output of the controller.
4	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
5	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
6,7	VCC	These two pins must tie to each other. Connect them to 12V bias supply. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
-	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Absolute Maximum Ratings

Supply Voltage (VCC) 15V
BOOT Voltage ($V_{BOOT - GND}$) 36V
Input Voltage (V_{PWM}) . . . . . GND - 0.3V to 7V
UGATE. . . . . V_{PHASE} - 0.3V_{DC} to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
LGATE . . . . . GND - 0.3V_{DC} to V_{CC} + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to V_{CC} + 0.3V
PHASE . . . . . GND - 0.3V_{DC} to 25V_{DC}
GND - 8V (<400ns, 20µJ) to 30V (<200ns, $V_{BOOT - GND}$<36V)
ESD Rating
Human Body Model (Tested per Class I JEDEC STD) 2.5kV
Machine Model 250V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x2 DFN Package (Notes 4, 5)	90	25

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Temperature Range (ISL6625AIRZ). . . . . -40°C to +85°C
Ambient Temperature Range (ISL6625ACRZ) . . . . . 0°C to +70°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5.5V to 13.2V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended operating conditions, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
VCC SUPPLY CURRENT (Note 6)						
No Load Switching Supply Current	I_{VCC}	V_{VCC} = 12V, F_{PWM} = 300kHz	-	7.56	-	mA
	I_{VCC}	V_{VCC} = 12V, PWM = 2.5V	-	0.72	-	mA
POWER-ON RESET						
VCC Rising Threshold			-	4.64	-	V
VCC Falling Threshold			-	4.17	-	V
PWM INPUT (See "TIMING DIAGRAM" on page 4)						
Input Current	I_{PWM}	V_{PWM} = 5V	-	124	-	µA
		V_{PWM} = 0V	-	-141	-	µA
Three-State Upper Gate Rising Threshold		VCC = 12V	-	2.77	-	V
Three-State Upper Gate Falling Threshold		VCC = 12V	-	3.23	-	V
Three-State Lower Gate Rising Threshold		VCC = 12V	-	1.20	-	V
Three-State Lower Gate Falling Threshold		VCC = 12V	-	1.50	-	V
UGATE Rise Time	t_{RU}	V_{VCC} = 12V, 3nF Load, 10% to 90%	-	31	-	ns
LGATE Rise Time	t_{RL}	V_{VCC} = 12V, 3nF Load, 10% to 90%	-	28	-	ns
UGATE Fall Time	t_{FU}	V_{VCC} = 12V, 3nF Load, 90% to 10%	-	18	-	ns
LGATE Fall Time	t_{FL}	V_{VCC} = 12V, 3nF Load, 90% to 10%	-	16	-	ns
UGATE Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 12V, 3nF Load, Adaptive	-	16	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 12V, 3nF Load, Adaptive	-	38	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 12V, 3nF Load	-	21	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 12V, 3nF Load	-	23	-	ns

Electrical Specifications Recommended operating conditions, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
OUTPUT						
Upper Drive Source Impedance	R_{U_SOURCE}	20mA Source Current	-	3.9	-	Ω
Upper Drive Sink Impedance	R_{U_SINK}	20mA Sink Current	-	1.4	-	Ω
Lower Drive Source Impedance	R_{L_SOURCE}	20mA Source Current	-	2.7	-	Ω
Lower Drive Sink Impedance	R_{L_SINK}	20mA Sink Current	-	0.9	-	Ω

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

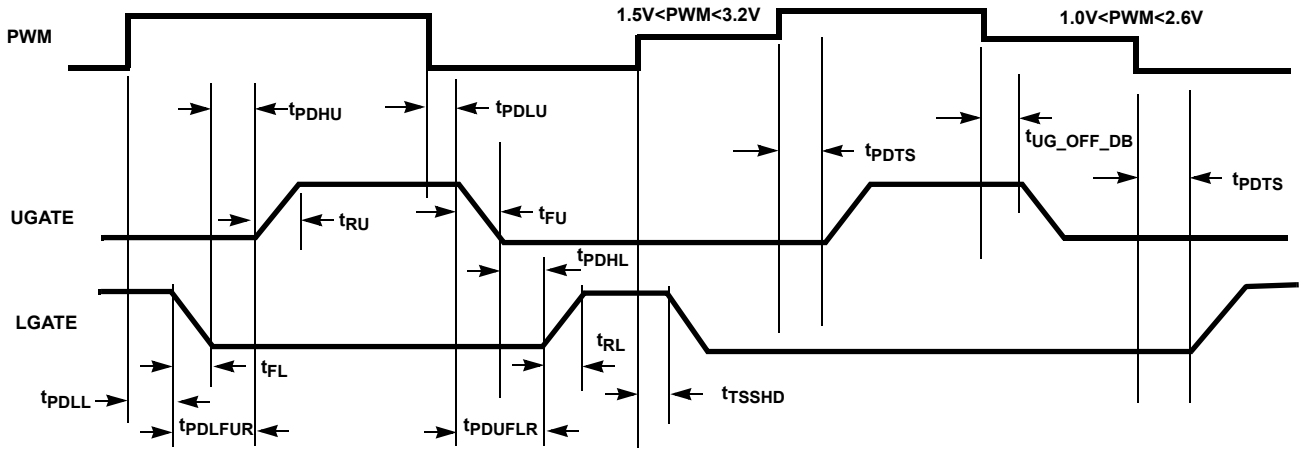
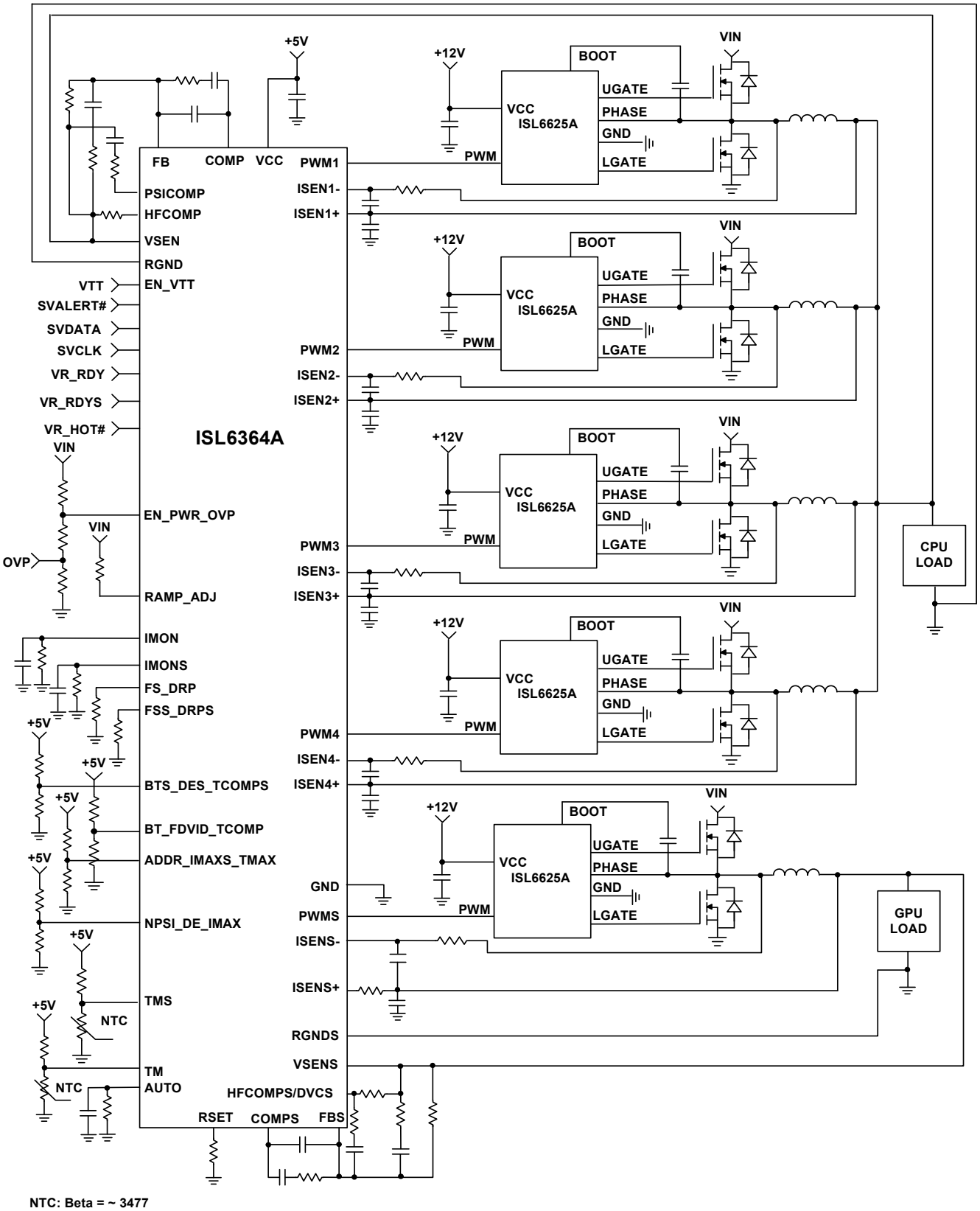


FIGURE 2. TIMING DIAGRAM

Typical Application Circuit



NTC: Beta = ~ 3477

Description

Operation and Adaptive Shoot-through Protection

Designed for high speed switching, the ISL6625A MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Figure 2). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall time [t_{FL}] is provided in the "Electrical Specifications" on page 3. Following a 25ns blanking period, adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1.75V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [t_{PDHL}] after the upper MOSFET's PHASE voltage drops below +0.8V or 40ns after the upper MOSFET's gate voltage [UGATE-PHASE] drops below ~1.75V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.8Ω ON-resistance and 3A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Three-State PWM Input

A unique feature of ISL6625A and other Intersil drivers is the addition of a three-state shutdown window to the PWM input. If the PWM signal enters and remains within the shutdown window for a set holdoff time, the driver outputs are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. Otherwise, the PWM rising and falling thresholds outlined in the "Electrical Specifications" on page 3 determine when the lower and upper gates are enabled. This feature helps prevent a negative transient on the output voltage when the output is shut down, eliminating the Schottky diode that is used in some systems for protecting the load from reversed output voltage events.

Power-On Reset (POR) Function

During initial start-up, the VCC voltage rise is monitored. Once the rising VCC voltage exceeds rising POR threshold, operation of the driver is enabled and the PWM input signal takes control of the gate drives. If VCC drops below the POR falling threshold, operation of the driver is disabled.

Pre-POR Overvoltage Protection

While VCC is below its POR level, the upper gate is held low and LGATE is connected to the PHASE pin via an internal 30kΩ (typically) resistor. By connecting the PHASE node to the gate of the low side MOSFET, the driver offers some passive protection to the load if the upper MOSFET(s) is or becomes shorted. If the PHASE node goes higher than the gate threshold of the lower MOSFET, it results in the progressive turn-on of the device and the effective clamping of the PHASE node's rise. The actual PHASE node clamping level depends on the lower MOSFET's electrical characteristics, as well as the characteristics of the input supply and the path connecting it to the respective PHASE node.

Internal Bootstrap Device

The ISL6625A features an internal bootstrap Schottky diode equivalent circuit implemented by swichers with typical on resistance of 40Ω and no typical diode forward voltage drop. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node. This reduces the voltage stress on the BOOT to PHASE pins.

The bootstrap capacitor must have a maximum voltage rating well above the maximum voltage intended for UVCC. Its minimum capacitance value can be estimated from Equation 1:

$$C_{BOOT\_CAP} \geq \frac{Q_{UGATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 1)}$$

$$Q_{UGATE} = \frac{Q_{G1} \bullet UVCC}{V_{GS1}} \bullet N_{Q1}$$

Where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 4.

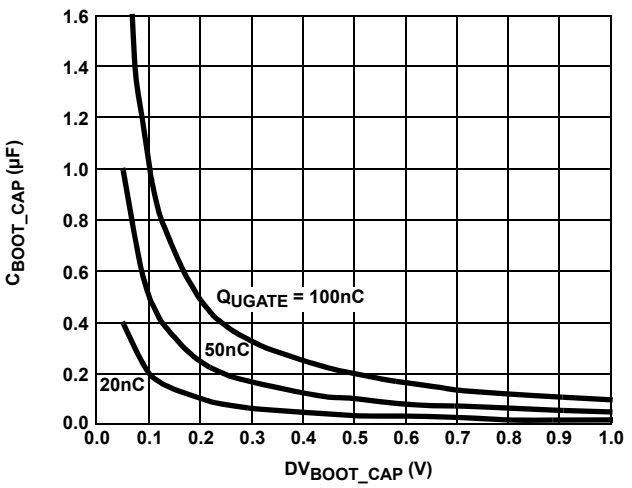


FIGURE 3. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the layout resistance, and the selected MOSFET's internal gate resistance and total gate charge (Q_G). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level may push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 8 for thermal impedance improvement suggestions. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated using Equations 2 and 3, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC \quad \text{(EQ. 2)}$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \quad \text{(EQ. 3)}$$

Where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The I_Q*VCC product is the quiescent power of the driver without a load.

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 4 and 5 show the typical upper and lower gate drives turn-on current paths.

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC \quad \text{(EQ. 4)}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

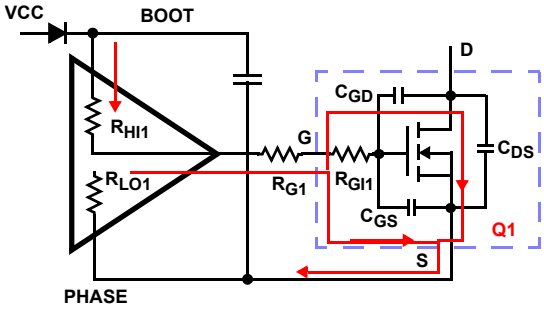


FIGURE 4. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

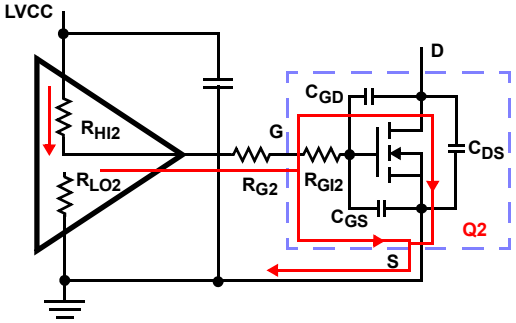


FIGURE 5. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

Layout Considerations

During switching of the devices, the parasitic inductances of the PCB and the power devices' packaging (both upper and lower MOSFETs) leads to ringing, possibly in excess of the absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

- Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially low-impedance lines: all power traces (UGATE, PHASE, LGATE, GND) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node: ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the input current loop: connect the source of the lower MOSFET to ground as close to the transistor pin as feasible; input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

In addition, for improved heat dissipation, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended surface copper islands, and buried planes combine to allow the IC and the power switches to achieve their full thermal potential.

Upper MOSFET Self Turn-On Effect at Start-up

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self-coupling via the internal C_{GD} of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not affecting normal performance and efficiency.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. Figure 6 provides a visual reference for this phenomenon and its potential solution.

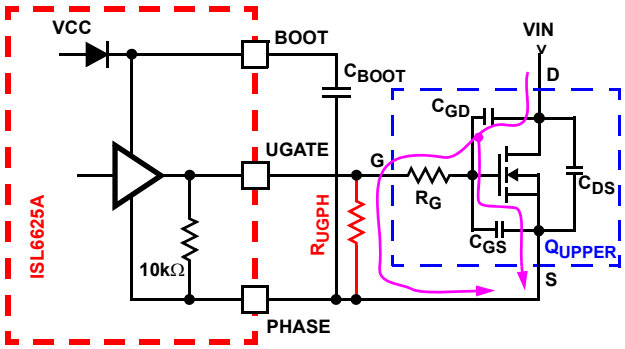


FIGURE 6. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 19, 2012	FN7978.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL6625A

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

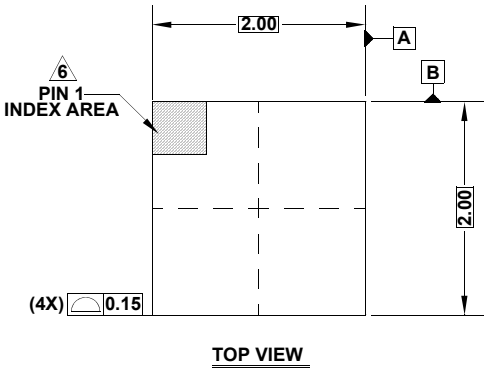
FITs are available from our website at: http://rel.intersil.com/reports/sear

Package Outline Drawing

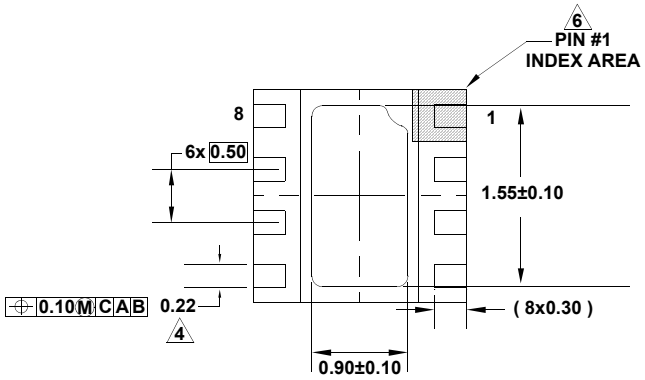
L8.2x2D

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH EXPOSED PAD

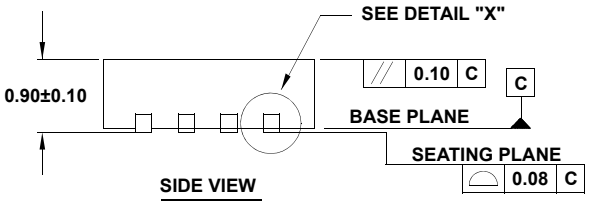
Rev 0, 3/11



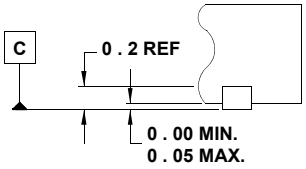
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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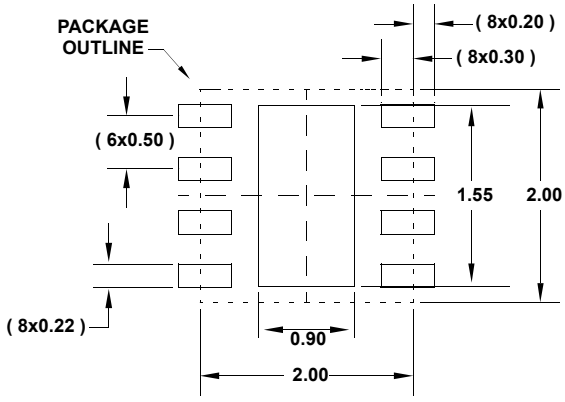

TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.