

ISL68227

Digital Single Output, 12-Phase PWM Controller

The [ISL68227](#) is a digital multiphase ($X \leq 12$) PWM controller with PMBus V1.3 compatibility. The digital multiphase controller can be configured to support any phase assignment up to a maximum of 12 phases. Increased power density, combined with support for PMBus V1.3 allows the ISL68227 to support any demanding power supply requirements.

The ISL68227 uses the proprietary Renesas digital synthetic current modulation scheme to achieve the industry-best combination of transient response, ease of tuning, and efficiency across the full load range. Diode emulation and automatic phase add/drop features allow you to extract maximum efficiency from the converter regardless of load conditions. You can use the intuitive Renesas PowerNavigator™ software to configure and monitor the device.

With minimal external components, easy configuration, robust fault management, and highly accurate regulation capability, implementing a high-performance, multiphase regulator has never been easier.

Applications

- Network equipment
- Server/storage equipment
- Telecom/datacom equipment
- Point-of-load power supply (memory, DSP, ASIC, FPGA)
- Artificial intelligence/accelerator cards (FPGA, ASIC)
- DDR memory solutions

Related Literature

For a full list of related documents, visit our website:

- [ISL68227](#) device page

Features

- Advanced linear digital modulation scheme
 - Auto phase add/drop with PFM mode for excellent load vs efficiency profile
 - Dual edge modulation with optional diode braking for faster transient response
 - Excellent V_{OUT} transition performance
 - Zero latency synthetic current control for excellent high frequency current balance
- Flexible phase assignment from 1 to 12 phases
- Up to 2MHz switching frequency operation for high density designs
- Differential remote voltage sensing supports $\pm 0.5\%$ closed-loop system accuracy over load, line, and temperature
- Highly accurate current sensing for excellent load-line regulation and accurate OCP
 - Supports the full range of Renesas Smart Power Stage (SPS) devices
- Comprehensive fault management enables high reliability systems
 - Pulse-by-pulse (per phase) and total output current limiting
 - Black Box status recording capability with first fault indicator
- Intuitive configuration using [PowerNavigator](#)
- SMBus/PMBus V1.3 compatible
- Up to 16 user configurations stored in device Non-Volatile Memory (NVM)

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1. Overview

1.1 Typical Applications

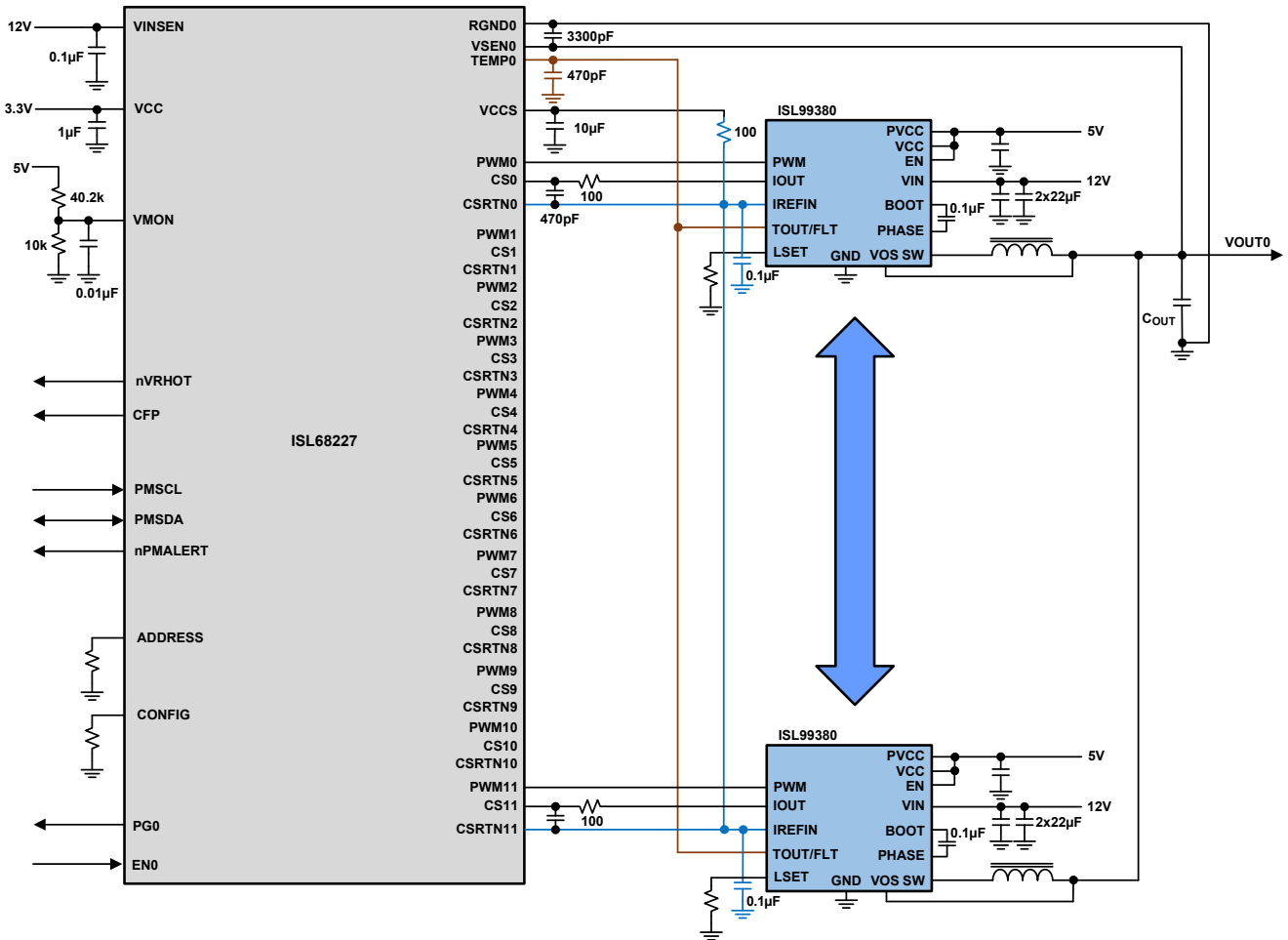


Figure 1. 12-Phase Smart Power Stage (ISL99380)

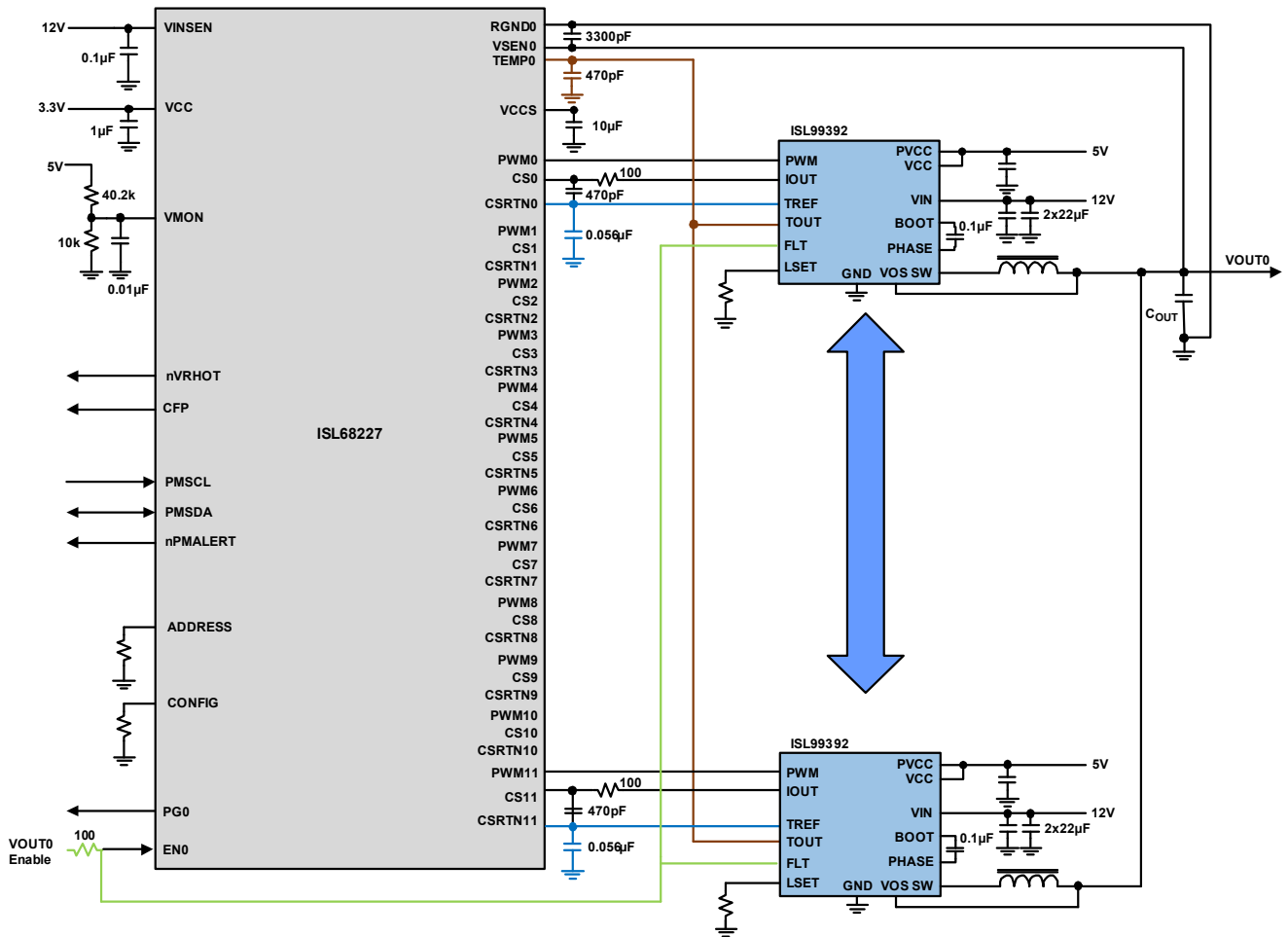


Figure 2. 12-Phase Smart Power Stage (ISL99392)

1.2 Internal Block Diagram

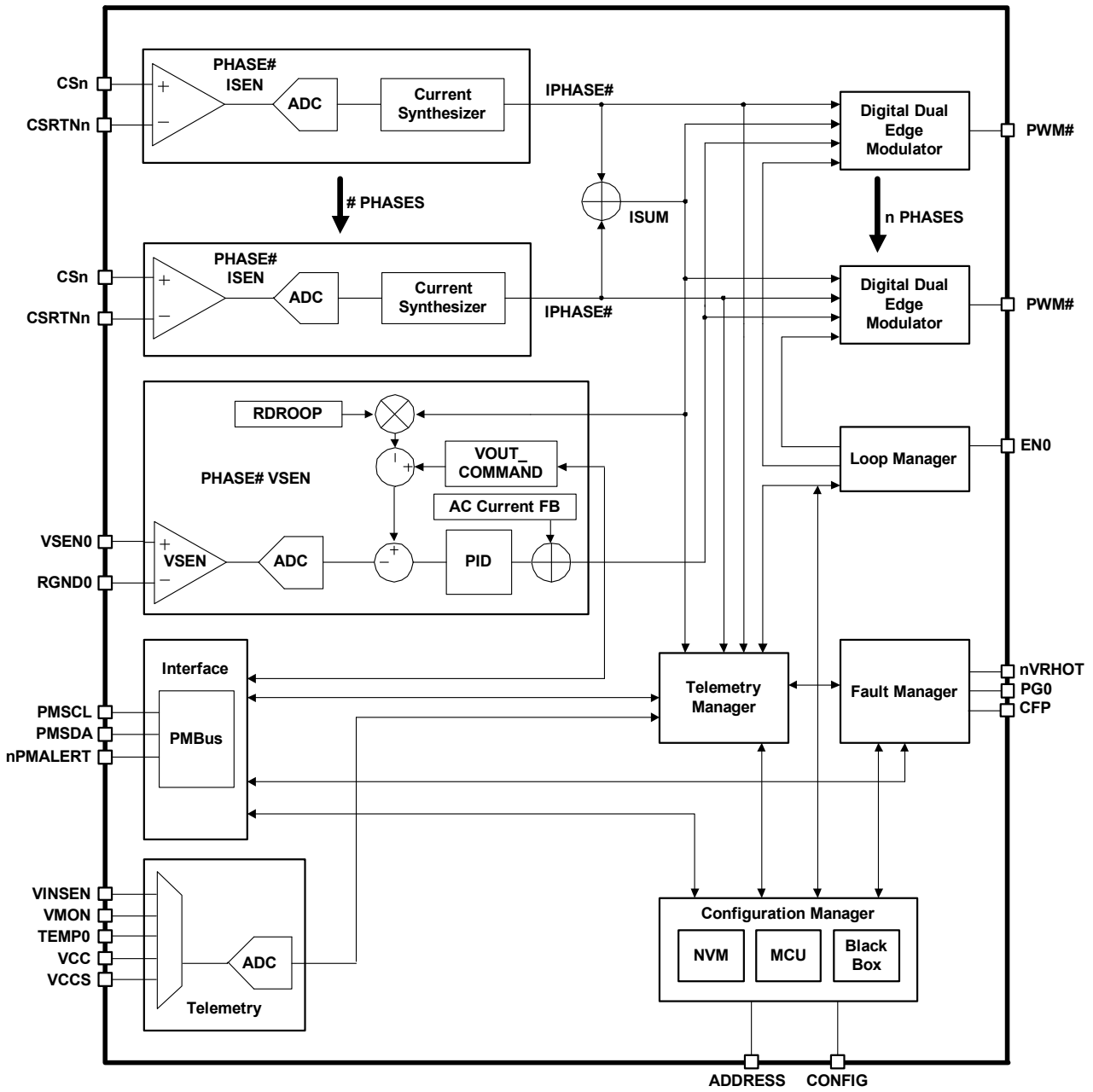


Figure 3. Internal Block Diagram

1.3 Ordering Information

| Part Number (Notes 2, 3) | Part Marking | Junction Temperature (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|-----------------------------|--------------|---------------------------|-----------------------------------|-----------------------------|----------------|
| ISL68227IRAZ | ISL68227 IRZ | -40 to +125 | - | 60 Ld 7x7 QFN | L60.7x7 |
| ISL68227IRAZ-T | ISL68227 IRZ | -40 to +125 | 6k | 60 Ld 7x7 QFN | L60.7x7 |

Notes:

- See [TB347](#) for details about reel specifications.
- These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
- For Moisture Sensitivity Level (MSL), see the [ISL68227](#) device page. For more information about MSL, see [TB363](#).

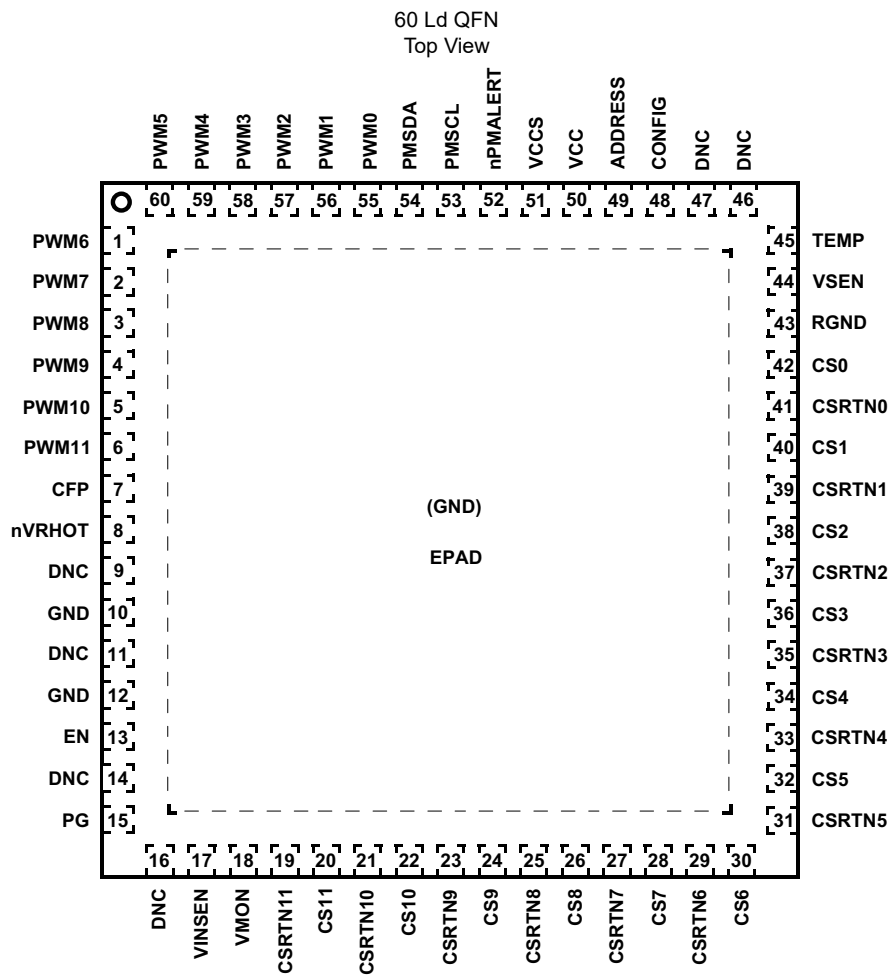
Table 1. Key Differences Between Family of Parts

| Part Number | Phase Configuration Output X/Output Y/Output Z | High Speed Bus Specification Supported | Package |
|-------------|---|---|------------------|
| ISL68227 | $X \leq 12$ | PMBus | QFN 60 Ld, 7x7mm |
| ISL68239 | $X+Y+Z \leq 12$ | AVSBus/PMBus | QFN 68 Ld, 8x8mm |
| ISL68236 | $X+Y \leq 9$ | AVSBus/PMBus | QFN 52 Ld, 6x6mm |
| ISL68229 | $X+Y+Z \leq 12$ | PMBus | QFN 68 Ld, 8x8mm |
| ISL68226 | $X+Y+Z \leq 8$ | PMBus | QFN 60 Ld, 7x7mm |
| ISL68225 | $X+Y \leq 9$ | PMBus | QFN 52 Ld, 6x6mm |
| ISL68224 | $X+Y+Z \leq 6$ | PMBus | QFN 52 Ld, 6x6mm |
| ISL68233 | $X+Y \leq 5$ | AVSBus/PMBus | QFN 40 Ld, 5x5mm |
| ISL68223 | $X+Y \leq 4$ | PMBus | QFN 40 Ld, 5x5mm |
| ISL68222 | $X+Y \leq 5$ | PMBus | QFN 40 Ld, 5x5mm |
| ISL68221 | $X+Y+Z \leq 3$ | PMBus | QFN 40 Ld, 5x5mm |
| ISL68220 | $X+Y \leq 2$ | PMBus | QFN 32 Ld, 4x4mm |

Table 2. Power Stage Recommendations

| Part Number | Rating (A) | Type | TOUT | TREF | REFIN | FAULT# | Package Dwg. # | Pin-to-Pin Compatible | Typically Used With |
|------------------------------------|------------|------|------|------|-------|--------|----------------|-----------------------|--|
| 5.0V PWM Power Stage Family | | | | | | | | | |
| ISL99227B | 60 | SPS | Yes | No | Yes | Yes | L32.5x5V | N/A | Phase Doublers: ISL6617A |
| ISL99360B | 60 | SPS | Yes | No | Yes | Yes | L32.5x5W | N/A | |
| 3.3V PWM Power Stage Family | | | | | | | | | |
| ISL99227 | 60 | SPS | Yes | No | Yes | Yes | L32.5x5V | N/A | Full Digital Controllers: ISL68/69xxx |
| ISL99360 | 60 | SPS | Yes | No | Yes | Yes | L32.5x5W | N/A | |
| ISL99380 | 80 | SPS | Yes | No | Yes | No | L39.5x6A | ISL99390 | |
| ISL99390 | 90 | SPS | Yes | No | Yes | No | L39.5x6A | ISL99380 | |
| ISL99392 | 90 | SPS | Yes | Yes | No | Yes | L39.5X6A | N/A | ISL682xx/692xx controllers that support low power state PWM protocol |

1.4 Pin Configuration



1.5 Functional Pin Descriptions

See [Table 5 on page 30](#) for design layout considerations.

| Pin Number | Pin Name | Description |
|--|--------------|---|
| 1, 2, 3, 4, 5, 6, 55, 56, 57, 58, 59, 60 | PWM [11:0] | Pulse-Width Modulation (PWM) outputs. Connect these pins to the PWM input pins of 3.3V logic-compatible, smart power stages, driver ICs, or DrMOS. |
| 7 | CFP | Thermal warning indicator. This open-drain output is pulled low if a sensed over-temperature occurs at the TEMP pins. |
| 8 | nVRHOT | Indicator of high VR temperature. This open-drain output is pulled low in the event of a sensed over-temperature. |
| 9, 11, 14, 16, 46, 47 | DNC | Do not connect to these pins. |
| 10, 12 | GND | Connect to ground. |
| 13 | EN | Input pin used for enable control of the output. Connect to ground if not used. |
| 15 | PG | Open-drain, power-good indicator for the output. |
| 17 | VINSEN | Input voltage sense pin for the V_{IN} supply voltage. |
| 18 | VMON | Input voltage sense pin for the driver supply voltage. |
| 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39, 41 | CSRTN [11:0] | The CS and CSRTN pins are current-sense inputs to individual phase differential amplifiers. Unused phases should have their respective current-sense inputs grounded. The CS and CSRTN pins support smart power stage, DCR, and resistor sensing. Connection details depend on the current-sense method chosen. |
| 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42 | CS [11:0] | |
| 43 | RGND | Negative differential voltage sense input for the output. Connect to the negative remote sensing point. Place a 3300pF capacitor across the pair at the pins. |
| 44 | VSEN | Positive differential voltage sense input for the outputs. Connect to the positive remote sensing point. Place a 3300pF capacitor across the pair at the pins. |
| 45 | TEMP | Input pin for sensing external temperature measurement at the outputs. Supports NTC-based temperature sensing and smart power stage sensing. Connect to ground if not used. |
| 48 | CONFIG | Configuration ID selection pin. Attach a resistor from this pin to GND. |
| 49 | ADDRESS | SMBus/PMBus address selection pin. Attach a resistor from this pin to GND. |
| 50 | VCC | Chip primary bias input. Connect this pin directly to a +3.3V supply with a 1 μ F or greater MLCC bypass capacitor. |
| 51 | VCCS | Internally generated 1.2V LDO logic supply from VCC. Decouple with a 4.7 μ F or greater MLCC (X5R or better). |
| 52 | nPMALERT | Open-drain output pin for alerting the SMBus host. |
| 53 | PMSCL | Serial clock signal pin for the SMBus interface. |
| 54 | PMSDA | Serial data signal pin for the SMBus interface. |
| EPAD | GND | The package pad serves as the GND return for all IC functions. Connect directly to the system GND plane with multiple vias. |

2. Specifications

2.1 Absolute Maximum Ratings

| Parameter | Pins | Minimum | Maximum | Unit |
|--|----------------|-----------|----------------|------|
| Input Voltage Range | VCC | | +4.3 | V |
| | VCCS | | +1.6 | V |
| | VINSEN | GND - 0.3 | 18 | V |
| | All Other Pins | GND - 0.3 | $V_{CC} + 0.3$ | V |
| ESD Rating | Pins | Value | | Unit |
| Human Body Model (Tested per JS-001-2017) | All Pins | 2 | | kV |
| Charged Device Model (Tested per JS-002-2014) | All Pins | 750 | | V |
| Latch-Up (Tested per JESD-78E; Class 2, Level A) | All Pins | 100 | | mA |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
|--|----------------------|----------------------|
| 60 Ld 7x7 QFN Package (Notes 4, 5) | 26 | 2.5 |

Notes:

- θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See [TB379](#).
- For θ_{JC} , the case temperature location is the center of the exposed metal pad on the package underside.

| Parameter | Minimum | Maximum | Unit |
|-----------------------------------|---------------------------|---------|------|
| Maximum Junction Temperature | | +150 | °C |
| Maximum Storage Temperature Range | -65 | +150 | °C |
| Pb-Free Reflow Profile | see TB493 | | |

2.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|--------------------------|---------|---------|------|
| Supply Voltage, V_{CC} | 3.135 | 3.465 | V |
| Junction Temperature | -40 | +125 | °C |
| Output Voltage | 0 | 3.05 | V |

2.4 Electrical Specifications

Recommended operating conditions, $V_{CC} = 3.3V$, unless otherwise specified. **Boldface limits apply across the operating ambient temperature range $-40^{\circ}C$ to $+85^{\circ}C$.**

| Parameter | Test Conditions | Min (Note 7) | Typ | Max (Note 7) | Unit |
|--|---|-----------------|----------------|-----------------|------------|
| V_{CC} Supply Current | | | | | |
| Nominal Supply Current | $V_{CC} = 3.3V_{DC}$; $ENx = V_{IH}$, all rails and phases operating, $f_{SW} = 600kHz$ | | 61 | | mA |
| Shutdown Supply Current | $V_{CC} = 3.3V_{DC}$; $EN0 = 0V$, no switching | | 8 | | mA |
| VCCS LDO Supply | | | | | |
| Output Voltage | | | 1.22 | | V |
| Maximum Current Capability | Excluding internal load | | 20 | | mA |
| Power-On Reset (POR) | | | | | |
| V_{CC} Brownout Threshold | | | 2.95 | | V |
| VCCS Rising POR Threshold | | | 1 | | V |
| VCCS Falling POR Threshold | | | 0.9 | | V |
| Enable Input High Level | | 2.0 | | | V |
| Enable Input Low Level | | | | 0.8 | V |
| Configurations Stored in Memory | | | | | |
| Number of Configuration Write Slots | | 28 | | | |
| Number of Unique Configurations Stored | | 16 | | | |
| POR to Initialization | | | | | |
| POR to Initialization Complete Time | | | 15 | | ms |
| Output Voltage Characteristics | | | | | |
| System Accuracy | Note 6, closed loop V_{OUT} set-point = 1.00V to 3.05V | -0.5 | | 0.5 | % |
| | Note 6, closed loop V_{OUT} set-point = 0.8V to 0.999V | -5 | | 5 | mV |
| | Note 6, closed loop V_{OUT} set-point = 0.25V to 0.799V | -8 | | +8 | mV |
| Voltage Sense Amplifier | | | | | |
| Open Sense Current | Only at VSEN open detection during initialization period | | 220 | | μA |
| Input Impedance (VSEN - RGND) | | | 140 | | k Ω |
| Maximum Common-Mode Input | | | $V_{CC} - 0.2$ | | V |
| Differential Input Range (VSEN - RGND) | | | | 3.05 | V |
| Output Current-Sense and Overcurrent Protection | | | | | |
| Current Sense Accuracy | SPS configuration | -1 | | 1 | % |
| Average Overcurrent Threshold Resolution | | | 0.1 | | A |
| Cycle-by-Cycle Current Limiting Threshold Resolution | | | 0.4 | | A |
| Digital Droop | | | | | |
| Droop Resolution | | | 0.01 | | mV/A |
| Oscillators | | | | | |
| Accuracy of Switching Frequency Setting | | | ± 2 | | % |
| Switching Frequency Range | | 0.2 | | 2.0 | MHz |

Recommended operating conditions, $V_{CC} = 3.3V$, unless otherwise specified. **Boldface limits apply across the operating ambient temperature range -40°C to +85°C. (Continued)**

| Parameter | Test Conditions | Min (Note 7) | Typ | Max (Note 7) | Unit |
|---|---|----------------------------------|-----------|-----------------|-------------|
| Soft-Start Rate and V_{OUT} Transition Rate | | | | | |
| Minimum Soft-Start Ramp Rate | Programmable minimum rate | | 0.01 | | mV/ μ s |
| Maximum Soft-Start Ramp Rate | Programmable maximum rate | | 100 | | mV/ μ s |
| Soft-Start Ramp Rate Accuracy | | | ± 2 | | % |
| Minimum Dynamic V_{OUT} Transition Rate | | | 0.01 | | mV/ μ s |
| Maximum Fast Dynamic V_{OUT} Transition Rate | | | 100 | | mV/ μ s |
| Dynamic V_{OUT} Transition Rate Accuracy | | -4 | | 4 | % |
| PWM Output (PWM[11:0]) | | | | | |
| PWMx Output High Level | $I_{OUT} = 4mA$ | $V_{CC} - 0.4$ | | | V |
| PWMx Output Low Level | $I_{OUT} = 4mA$ | | | 0.4 | V |
| PWM Tri-State Leakage (pin forced high) | $V_{PWM} = V_{CC}$ | | | 1 | μA |
| PWM Tri-State Leakage (pin forced low) | $V_{PWM} = 0V$ | -1 | | | μA |
| Thermal Monitoring and Protection | | | | | |
| Temperature Sensor Range | | -50 | | 150 | $^{\circ}C$ |
| Temperature Sensor Accuracy | SPS configuration | | ± 4.5 | | % |
| nVRHOT Output Low Impedance | | | 9 | | Ω |
| Power-Good and Protection Monitors | | | | | |
| PG Output Low Voltage | $I_{OUT} = 4mA$ load | | | 0.2 | V |
| PG Leakage Current | With a pull-up resistor externally connected to VCC | | 5 | | μA |
| Overvoltage Protection Threshold Resolution | | | 1 | | mV |
| Undervoltage Protection Threshold Resolution | | | 1 | | mV |
| Input Voltage-Sense and Catastrophic Failure Protection (CFP) Output | | | | | |
| Input Voltage Accuracy | VINSEN to ADC accuracy | | ± 2.5 | | % |
| Input Overvoltage Threshold Resolution | | | 16 | | mV |
| CFP Output High Voltage | $I_{OUT} = 8mA$ | $V_{CC} - 0.4$ | | | V |
| CFP Output Low Voltage | $I_{OUT} = 8mA$ | | | 0.4 | V |
| SMBus/PMBus | | | | | |
| nPMALERT, PMSDA Output Low Level | $I_{OUT} = 20mA$ | | | 0.4 | V |
| PMSCL, PMSDA Input High Level | | 1.35 | | | V |
| PMSCL, PMSDA Input Low Level | | | | 0.8 | V |
| PMSCL, PMSDA Input Hysteresis | | | 80 | | mV |
| PMSCL Frequency Range | | 0.01 | | 2.00 | MHz |

Notes:

- These parts are designed and adjusted for accuracy with all errors in the voltage loop included. Verified by design and/or characterization.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Initializing the Device

3.1 Power-On Reset (POR)

ISL68227 initialization begins after V_{CC} crosses its rising POR threshold. When POR conditions are met, basic digital subsystem integrity checks begin. During this process, the controller starts the telemetry subsystem, configures its PMBus address according to the ADDRESS pin resistor value, loads the selected user configuration from NVM as indicated by the CONFIG pin resistor value, checks fault status, and prepares for regulation. The PWM pins are held in tri-state until the device is commanded to regulate. [Figure 4](#) shows the device initialization sequence.

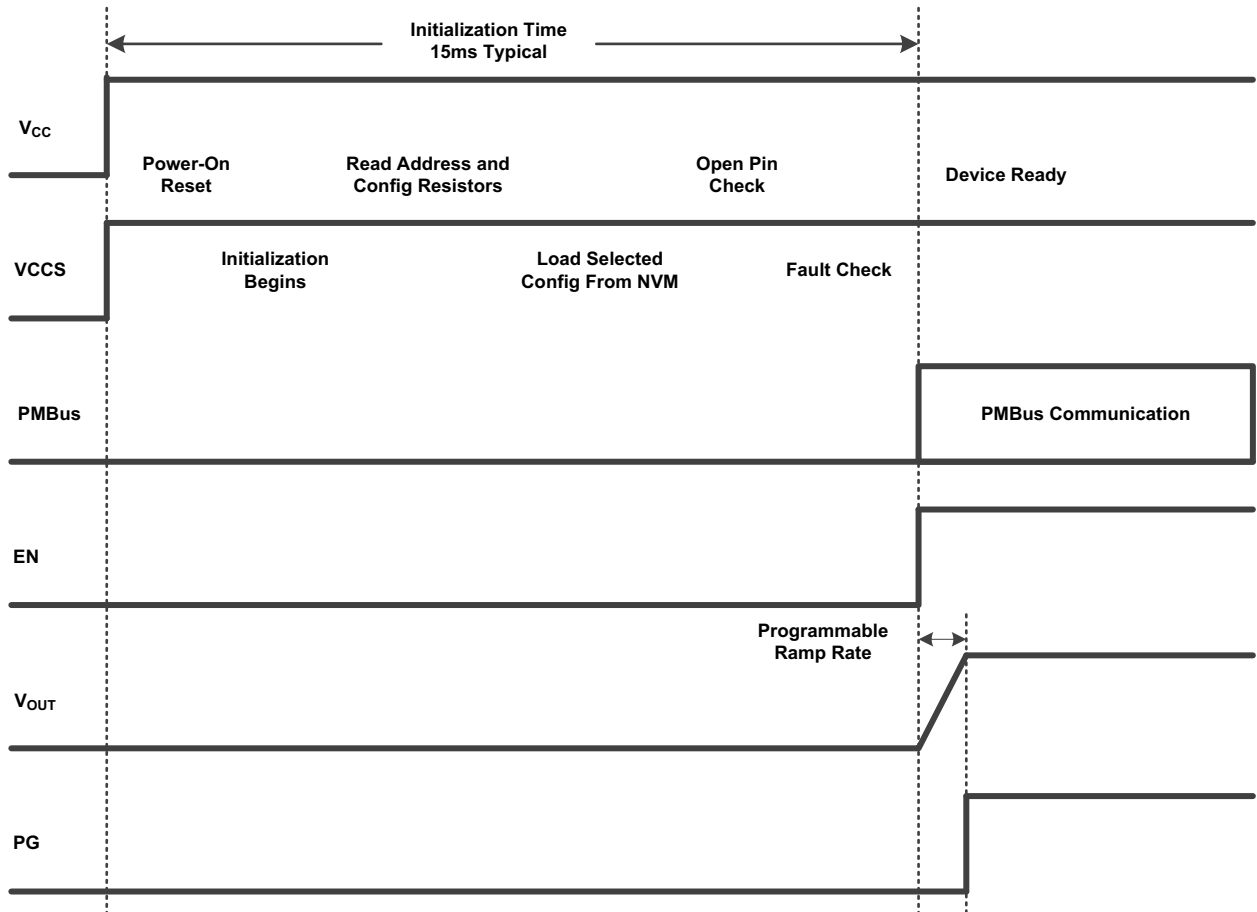


Figure 4. Simplified PMBus Initialization Timing Diagram

3.2 Selecting the PMBus Address

A resistor reader selects the PMBus slave address. The ADDRESS pin reads the value of a resistor connected to GND to determine the PMBus address to use during host communication. [Table 3](#) shows the $R_{ADDRESS}$ values to specify the PMBus slave addresses (7-bit).

Table 3. Resistor Value to PMBus Address Map

| R Value (Ω) | PMBus Address | R Value (Ω) | PMBus Address |
|----------------------|---------------|----------------------|---------------|
| 0 | 60 | 5230 | 51 |
| 162 | 61 | 5900 | 52 |
| 316 | 62 | 6650 | 53 |
| 487 | 63 | 7500 | 54 |
| 681 | 64 | 8450 | 55 |
| 887 | 65 | 9530 | 56 |
| 1130 | 66 | 10700 | 57 |
| 1370 | 67 | 12100 | 58 |
| 1650 | 45 | 13700 | 59 |
| 1960 | 46 | 15400 | 5A |
| 2320 | 47 | 17400 | 5B |
| 2670 | 4C | 19600 | 5C |
| 3090 | 4D | 22100 | 5D |
| 3570 | 4E | 24300 | 5E |
| 4120 | 4F | 27400 | 5F |
| 4640 | 50 | 30100 | 68 |

3.3 Selecting the User Configurations

A user configuration is loaded for operation at power-up. The CONFIG pin reads the value of a resistor connected to GND to determine which user configuration is loaded. The ISL68227 supports 16 distinct configuration identifiers. [Table 4](#) provides the R_{CONFIG} value corresponding to each configuration identifier. A total of 28 one-time programmable non-volatile memory locations are available to store new user configurations or overwrite existing ones. With this flexibility, all 16 unique configurations can be written with 12 available overwrites, one configuration ID can be written up to 28 times, or any combination of configuration IDs can be written until the 28 write limit is reached. Only the most recent configuration for a given configuration ID can be loaded. When all 28 memory locations have been written, the ISL68227 no longer accepts attempts to write to NVM. PowerNavigator provides a simple interface to store and load configurations.

Table 4. Resistor Value to CONFIG ID Map

| R Value (Ω) | Configuration ID | R Value (Ω) | Configuration ID |
|----------------------|------------------|----------------------|------------------|
| 0 | 0 | 1650 | 8 |
| 162 | 1 | 1960 | 9 |
| 316 | 2 | 2320 | 10 |
| 487 | 3 | 2670 | 11 |
| 681 | 4 | 3090 | 12 |
| 887 | 5 | 3570 | 13 |
| 1130 | 6 | 4120 | 14 |
| 1370 | 7 | 4640 | 15 |

3.4 Configuring the Device

Configure the ISL68227 by generate a configuration file using PowerNavigator to either directly load the device RAM or program the device NVM. During device initialization, the ISL68227 attempts to load a configuration from NVM. If no configuration is found, the device remains in a wait state with the PWM pins tri-stated. The device ignores attempts to enable and waits until a configuration is directly loaded using PowerNavigator. The ISL68227 features and functions described in this datasheet are all configured using PowerNavigator. This datasheet provides fundamental understanding of device behavior and design information. Additional detail regarding the configuration process is provided in PowerNavigator.

4. Operating the Device

After the ISL68227 initializes and a configuration is loaded, it is ready for operation.

The ISL68227 has several performance enhancing features that enable it to meet the most stringent voltage regulation and efficiency demands. The synthetic current modulator provides excellent transient response to support the latest generation of ASICs and CPUs. Automatic phase dropping, diode emulation, and PFM operation improve efficiency across the load range. The ISL68227 supports Smart Power Stage (SPS) current sense in addition to DCR/resistor current sense to enable optimal design. The device also supports a full complement of high resolution telemetry, including per phase temperature sense when paired with select Renesas SPS devices. The following sections provide more detail about using these features.

4.1 Input Voltage Sensing

Input voltage is monitored using the VINSEN pin. Connect the VINSEN pin as shown in [Figure 5](#).

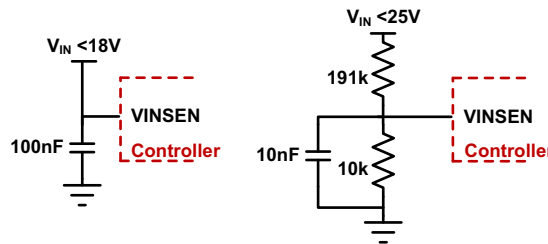


Figure 5. Input Voltage Sense Configuration

Input voltage is monitored continuously, and regulation is stopped anytime the sensed input voltage falls outside the boundaries established by configuration settings associated with the parameters $V_{IN\ ON}$, $V_{IN\ OFF}$, $V_{IN\ Overvoltage\ Fault\ Limit}$, and $V_{IN\ Undervoltage\ Fault\ Limit}$.

4.2 Lossless Input Current and Power Sensing

Input current telemetry is provided per rail using an input current synthesizer. By using the ability of the ISL68227 to precisely determine its operational conditions, the input current can be synthesized to a high degree of accuracy without the need for a lossy sense resistor. With a precise knowledge of the input current and voltage, the input power can be computed.

4.3 VMON Voltage Sensing

The VMON input pin provides a secondary input voltage sense with several selectable voltage ranges. The VMON input pin can be used to inhibit rail operation when the sensed voltage falls outside the boundary established by the configuration settings that are associated with the parameters $VMON_ON$ and $VMON_OFF$. If a rail is prevented from operating due to a VMON excursion, the rail restarts if the sensed voltage returns to the specified range. Use of this feature is optional for each rail. A typical use case for this voltage sensing feature is monitoring the bias supply voltage associated with the power stages and preventing operation if this voltage is below the configured range. Connection of the VMON pin for sensing the 5V SPS bias voltage is shown in [Figure 6](#).

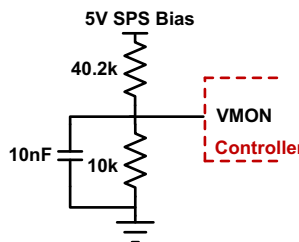


Figure 6. VMON Configuration

4.4 Enabling and Soft-Starting the Device

The ISL68227 outputs can be enabled using the enable pin or PMBus. Enable method selection is configured in PowerNavigator on a per rail basis. The ISL68227 begins its soft-start sequence when it is commanded to regulate an output. Soft-start moves V_{OUT} smoothly to the programmed $V_{OUT_COMMAND}$. Soft-start timing is programmed using the [TON_DELAY \(60h\)](#) and [TON_RISE \(61h\)](#) PMBus commands.

If a pre-existing voltage bias exists on the output, the PWM signals are held in tri-state until the soft-start ramp reaches the prebias level. The tri-state prevents the converter from sinking current and pulling the prebias down. No special configuration is required to enable this operation.

4.5 Disabling the Device

Similar to the enabling process, outputs can be disabled using the enable pin or PMBus on a per rail basis. The ISL68227 can be configured to disable in two ways:

- **Immediate OFF:** Immediately ceases regulation and tri-state the PWM pins
- **Soft OFF:** Actively ramps the output voltage down to 0V before ceasing activity as programmed in the [TOFF_DELAY \(64h\)](#) and [TOFF_FALL \(65h\)](#) PMBus commands.

4.6 Phase Configuration and Automatic Phase Dropping

The ISL68227 supports three regulated outputs that control its twelve phases. Each rail is capable of controlling up to twelve phases, but the rails can be configured for fewer phases. Unused phases should have their CS and CSRTN pins grounded.

The ISL68227 supports Automatic Phase Dropping (APD) to optimize efficiency across the load range. [Figure 7](#) shows the typical characteristics of efficiency vs load current as the phase count is varied. The diagram shows that optimal efficiency is achieved by using fewer phases as the load current decreases.

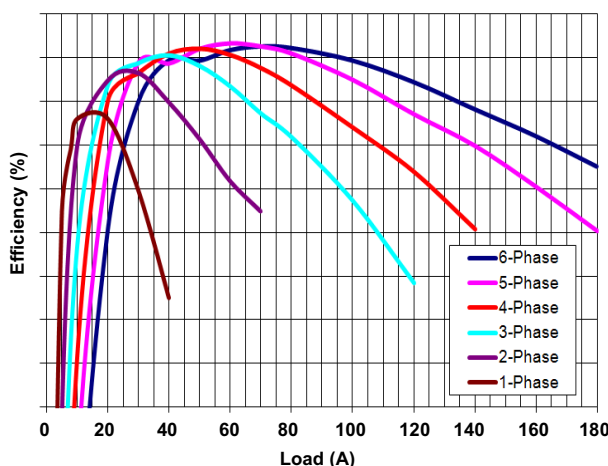


Figure 7. Efficiency vs Phase Number

The ISL68227 continuously monitors output current, and if APD is enabled, the device drops or adds phases from use as the load current varies.

Phases are dropped one at a time with a user-programmed delay between drop events. For example, if the delay is set to 1ms, six phases are active, and the load suddenly drops to a level needing only one phase; the ISL68227 begins by dropping a single phase after 1ms. An additional phase is dropped each millisecond until only one phase remains active. On Rail 0, phases are dropped beginning with the highest assigned phase.

Phases are automatically returned to service when load conditions require more phases. The phases are returned to service in the opposite order they were dropped. Conditions that result in phase adding include increased load current, rapid change sensed on the output voltage, and V_{OUT} transition events. When rapid change is sensed on the output voltage, the Fast Phase Add function prepares all dropped phases for activation so there is no delay if all phases are needed to support a load transient.

Any command to change the output voltage set point uses all phases, including V_{OUT} transition events. After the output voltage change is complete, phases begin dropping as configured.

To ensure dropped phases have sufficient bootstrap capacitor charge to turn on the high-side MOSFET after a long period of inactivity, a bootstrap refresh function periodically turns on the low-side MOSFET of each dropped phase to refresh the bootstrap capacitor.

To produce the most optimal efficiency across a wide range of output loading, the modulator supports automatic dropping or adding of phases and diode emulation (in a single-phase state). Use of APD and diode emulation are optional. If automatic phase dropping is enabled, the number of active phases at anytime is determined only by load current.

4.7 Diode Emulation and PFM Operation

As described in [Phase Configuration and Automatic Phase Dropping](#), the ISL68227 supports APD to optimize phase usage as load demand decreases. When the regulator drops to 1-phase operation, it supports diode emulation and Pulse Frequency Modulation (PFM) operation to further maximize efficiency performance. Traditionally, use of such efficiency boosting techniques has come at the expense of transient response, but the ISL68227 is able to meet all transient demands directly from diode emulation/PFM operation.

Diode emulation and PFM operation are supported when a single phase is active. If constant frequency operation is needed at light loads, the feature can be disabled. If enabled, the low-side MOSFET conducts when the current is flowing from source-to-drain and does not allow a reverse current, emulating an ideal diode. As [Figure 8](#) shows, when the inductor current is positive, the LGATE is held on and allows current to flow in the low resistance channel of the LFET. When current reaches zero, the LFET is turned off to prevent a reverse current in the inductor. The controller modulates the LFET state through the PWM pin of the respective regulator channel by tri-stating the PWM when the load current reaches zero, which commands the MOSFET driver to turn off both the HFET and LFET.

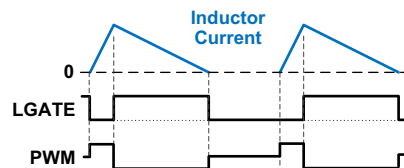


Figure 8. Diode Emulation PWM Signaling

In single-phase diode emulation operation, the IC delivers inductor current pulses with a user programmed pulse width. By programming the pulse width, the output voltage ripple can be tuned to meet expectations for any system type. Pulse frequency is then modulated to maintain output voltage regulation, which is shown in [Figure 9](#). The transition from single phase PFM to multiphase constant frequency operation is managed seamlessly by the IC.

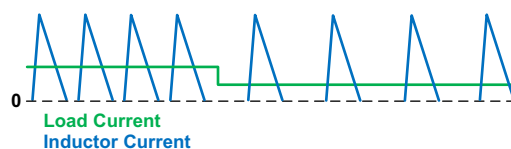


Figure 9. Single Phase Light Load PFM Operation

4.8 Diode Braking

Applications that support loads with large transient current demands often have significant output voltage overshoot when the load current demand drops suddenly. In some cases, diode braking may allow overshoot reduction at the expense of thermal dissipation in the low-side MOSFET.

4.9 Switching Frequency

Switching frequency is independently programmable on each rail from 200kHz to 2MHz.

4.10 Output Current Sensing

The ISL68227 supports DCR, resistor, and smart power stage current sensing. Use the differential input CS and CSRTN pins to connect to the various sense elements.

4.10.1 SPS Current Sensing

In applications using Smart Power Stage (SPS), the SPS IMON output is connected to the corresponding ISL68227 CSn input. The CSRTNn pins are connected to the SPS current sense reference voltage. For connection details, see the typical application diagram shown in [Figure 1 on page 6](#).

4.10.2 Inductor DCR Sensing

Inductor windings have a resistive component (DCR) that drops a voltage proportional to the inductor current. [Figure 10](#) shows that the DCR is treated as a lumped element with one terminal inaccessible for measurement. Fortunately, a simple R-C network as shown in [Figure 10](#) can reproduce the hidden DCR voltage. By matching the R-C time constant to the L divided by DCR time constant, it is possible to precisely recreate the DCR voltage across the capacitor, so that $V_{DCR}(t) = V_C(t)$, preserving even the switching frequency characteristic of the DCR voltage.

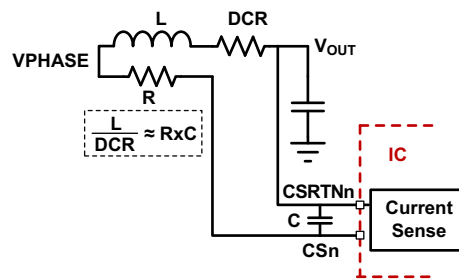


Figure 10. DCR Sensing Configuration

Modern inductors often have such low DCR values that the resulting signal is <10mV. To avoid noise problems, care must be taken in the PCB layout to properly place the R-C components and route the differential lines between controller and inductor. [Figure 10](#) shows one PCB design method that places the R component near the inductor VPHASE and the C component very close to the IC pins. The design method maintains isolation of the noisy VPHASE node and maximizes filtering near the IC. Route the lines as a pair on a single layer directly to the controller. Avoid routing the pair near any switching signals such as Phase and PWM. This is the method used by Renesas on evaluation board designs. **Note:** The R component should be 0603 or greater size to limit the effects of voltage coefficient of resistance in the resistor.

Because the DCR is actually the resistance of a metal winding, the DCR value increases with rising temperature. The increase must be compensated or the sensed (and reported) current increases with temperature. To compensate the temperature effect, the ISL68227 provides temperature sensing options and an internal methodology to apply the correction.

4.10.3 Resistive Sensing

For more accurate current sensing, a dedicated current-sense resistor, R_{SENSE} , in series with each output inductor, can serve as the current-sense element. However, this technique reduces the overall converter efficiency due to the additional power loss on the current-sense element, R_{SENSE} .

A current-sensing resistor has a distributed parasitic inductance known as Equivalent Series Inductance (ESL), which is typically less than 4nH. Consider the ESL as a separate lumped quantity, as shown in [Figure 11 on page 22](#). The phase current, I_L , flowing through the inductor, also passes through the ESL. Similar to DCR sensing described in [Inductor DCR Sensing](#), a simple R-C network across the current-sense resistor extracts the R_{SENSE} voltage. Match the ESL/R_{SENSE} time constant to the R-C time constant.

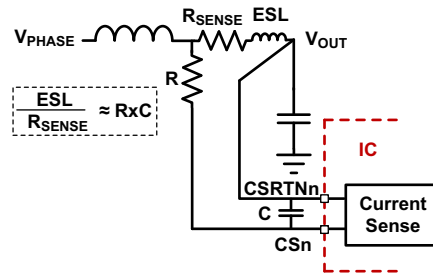


Figure 11. Sense Resistor in Series with Inductor

[Figure 12](#) shows the sensed waveforms with and without matching RC when using resistive sense. PCB layout for resistive sense should follow the guidance described in [“Inductor DCR Sensing” on page 21](#).

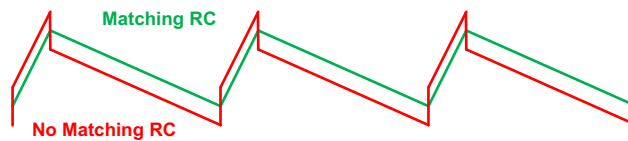


Figure 12. Voltage Across R with and without RC

4.10.4 L/DCR or ESL/R_{SEN} Matching

Assuming the compensator design is correct, [Figure 13](#) shows the expected load transient response waveforms if L/DCR or ESL/R_{SEN} is matching the R-C time constant for a droop application. When the load current I_{OUT} has a square change, the output voltage V_{OUT} also has a square response except for the potential overshoot at load release. However, there is always some uncertainty in the true parameter values involved in the time constant matching, so fine-tuning is generally required.

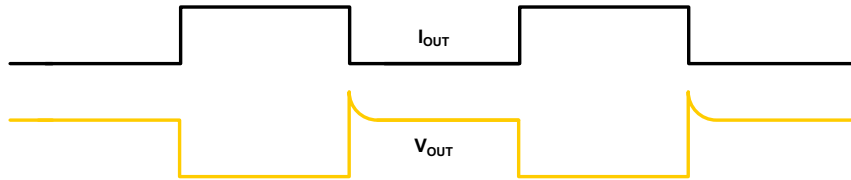


Figure 13. Desired Load Transient Response Waveforms

If the R-C time constant is too large or too small, V_C(t) does not accurately represent real-time I_{OUT}(t) and worsens the transient response. [Figure 14](#) shows the load transient response when the R-C time constant is too small. In this condition, V_{OUT} sags excessively on load insertion and can create a system failure or early overcurrent trip.

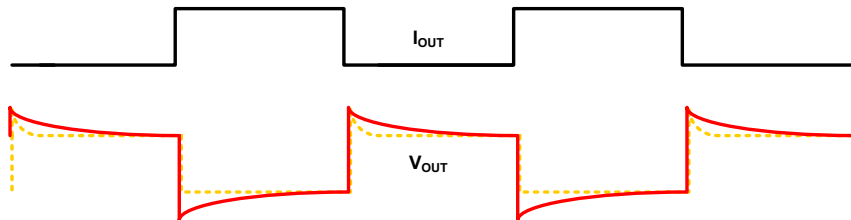


Figure 14. Load Transient Response when R-C Time Constant is Too Small

[Figure 15](#) shows the transient response when the R-C time constant is too large. V_{OUT} is sluggish in drooping to its final value. Use these general guides if fine-tuning is needed.

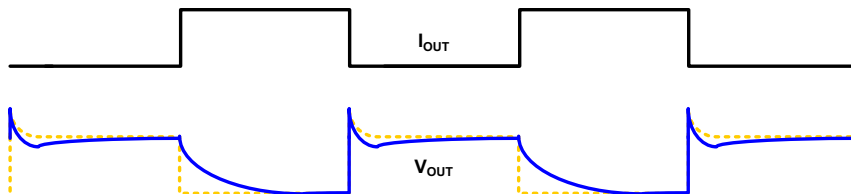


Figure 15. Load Transient Response when R-C Time Constant is Too Large

5. Temperature Sensing

The ISL68227 monitors internal die temperature and supports external per-rail SPS or NTC resistor temperature sense using the TEMPn pins. The controller also offers per-phase temperature sense using the CS and CSRTN pins when paired with select Renesas SPS devices.

5.1 SPS Temperature Sensing

The ISL68227 can be configured to sense SPS temperature on a per-rail or per-phase basis. To configure for per-rail temperature sense, connect the TOUT/FLT pin of each SPS in the rail together and tie the net to the ISL68227 TEMPn pin. Select SPS devices also have current sense reference voltage outputs (TREF) that are proportional to temperature. The ISL68227 can be configured to accept this signal and report individual phase temperature. When configured for per-phase temperature sense, the SPS TOUT/FLT pins should remain connected to the ISL68227 TEMPn pin, because the SPS devices report internal fault conditions through the TOUT/FLT pin. See the typical application diagram ([Figure 1 on page 6](#)) for a detailed connection overview of per-rail temperature sense.

5.2 NTC Temperature Sensing

NTC temperature sensing is used in conjunction with inductor DCR output current sensing to sense the inductor temperature. In this configuration, the specified NTC is connected to the IC as shown in [Figure 16](#). To avoid noise problems, the PCB traces leading to the NTC should be routed differentially and kept away from noise sources.

Note: Use the component values shown.

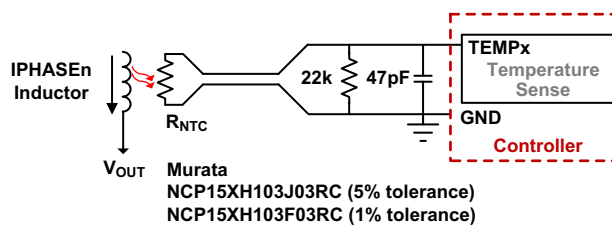


Figure 16. NTC Temperature Sense Connection

When automatic phase dropping is used in a multiphase design, position the NTC close to the phase that runs in single-phase operation. For Rail 0, the correct phase is the lowest phase number assigned to the rail as shown in [Figure 17](#).

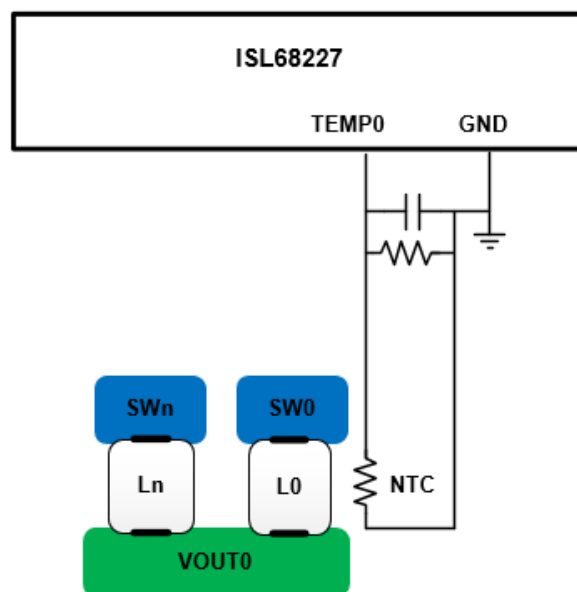


Figure 17. NTC Placement

5.3 Temperature Compensation

The ISL68227 supports temperature compensation to improve the DCR current sense accuracy. Copper wire used to form inductors has a resistivity temperature coefficient of 0.39%/°C. Because the voltage across the inductor is sensed for the output current information, the sensed signal has the same positive temperature coefficient as the inductor DCR.

Compensating current sense for temperature variation requires that the current-sensing element temperature and temperature coefficient are known. Although the temperature coefficient is easily obtained, actual current-sense element temperature is difficult to measure directly. Instead, an NTC temperature sensor placed near an inductor is measured, and the compensation is applied based on this sensed temperature.

The sensed temperature and the actual temperature are different, because the temperature sensor is not perfectly coupled to the inductor winding. To accommodate this difference, the ISL68227 allows you to fine-tune temperature compensation for optimal current sense accuracy. For applications requiring the highest current sense accuracy, use SPS current sense.

6. Fault Monitoring and Protection

The ISL68227 includes an extensive fault management system that integrates with high performance host controllers, supporting unprecedented remote system management and debugging capability. If a fault condition occurs, the IC deasserts the PG pin associated with the faulted rail and alerts the host using the PMAAlert pin. You can optionally configure the CFP (Catastrophic Failure Protection) to assert on select faults for additional protection measures at the system level. The ISL68227 also provides Black Box, a recorder with extensive fault logging to support system level debug.

Fault controls are independently enabled and associated fault responses are user configurable. Response type is independently configurable by fault type. Response types supported are:

- **Alert only:** The rail continues to operate.
- **Shut down immediately:** The rail is latched off until commanded on.
- **Shut down and retry with variable retry delay:** The rail attempts to retry indefinitely until the condition clears or the rail is commanded off.

When a fault condition has been declared, clear the fault by issuing a CLEAR_FAULTS command or by cycling the EN pin of the faulted rail.

6.1 Power-Good Signals

The PG pins are open-drain, power-good outputs that indicate completion of the soft-start sequence and output voltage of the associated rail within the expected regulation range. If a fault occurs, the PG pin of the associated rail is pulled low. PG is also pulled low immediately on a rail disable.

6.2 Overvoltage/Undervoltage Protection

Output voltage is measured at the load sensing points differentially for regulation, and the same measurement is used for OVP and UVP. [Figure 18](#) shows a simplified OVP/UVP block diagram. The output voltage comparisons are done in the digital domain.

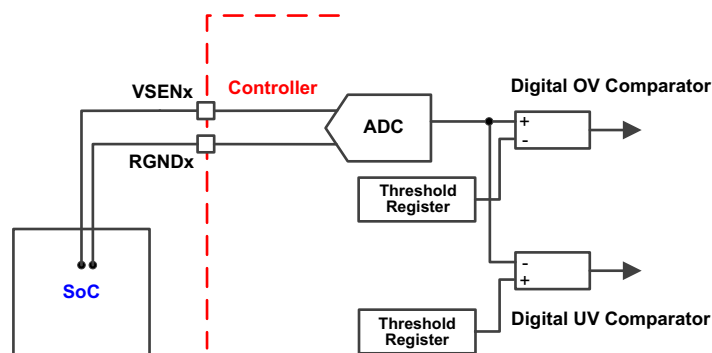


Figure 18. OV/UV Comparators

The device responds to an output overvoltage condition by disabling the output, declaring a fault, setting the PMAAlert pin, pulling the PG pin low, and pulsing the LFET until the output voltage drops below the threshold. Similarly, the device responds to an output undervoltage condition by disabling the output, declaring a fault, setting the PMAAlert pin, and pulling the PG pin low. The output does not restart until the EN pin is cycled (unless the device is configured to retry).

The ISL68227 also features open pin sensing protection to detect an open of the output voltage sensing circuit. When this condition is detected, controller operation is suspended.

6.3 Output Overcurrent Protection

The ISL68227 provides a comprehensive overcurrent protection scheme that monitors the total output current, peak phase current, and the valley phase current. The scheme allows you to eliminate inductor saturation and limit the total output current. The ISL68227 supports shutdown and retry response types for OC faults. The response configuration applies to all output current fault mechanisms such as phase peak overcurrent and total output overcurrent.

Figure 19 shows the block diagram of the output overcurrent protection scheme.

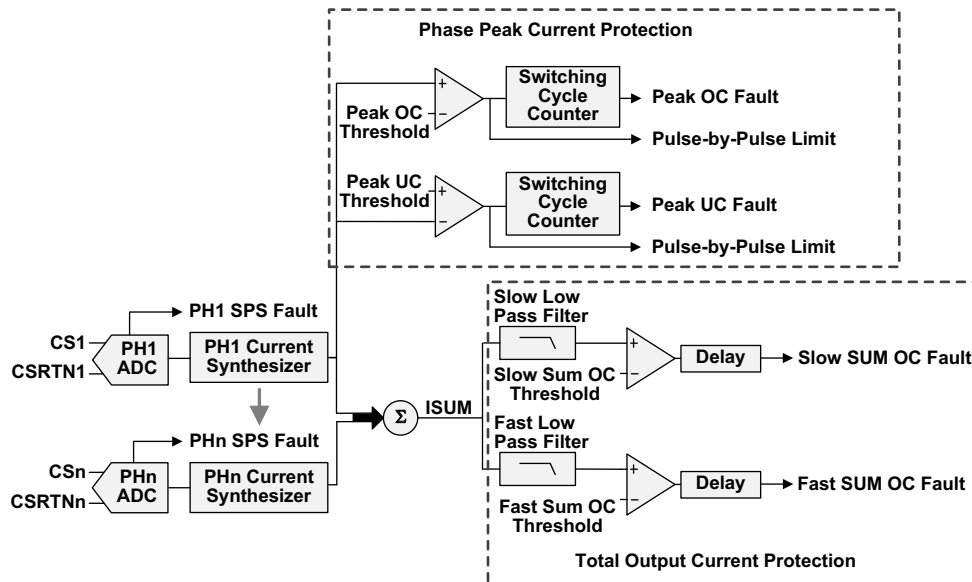


Figure 19. OCP Functional Diagram

Phases are protected from both overcurrent and undercurrent using a pulse-by-pulse scheme that acts instantly on a PWM signal if a detected phase current reaches its threshold. Thresholds for overcurrent and undercurrent allow you to precisely limit phase currents so the inductors never saturate. Phase current limiting behavior can be configured to either shut down the device after a user-determined number of consecutive events or continue indefinitely. If configured to continue indefinitely, the converter behaves much like a current source. Figures 20 and 21 show per-phase current limiting when the device is configured to shut down after a user-determined number of consecutive events.

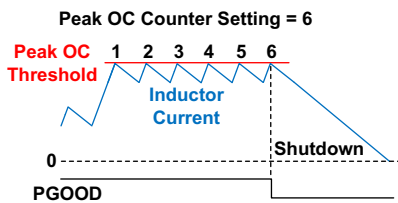


Figure 20. Peak OC Operation

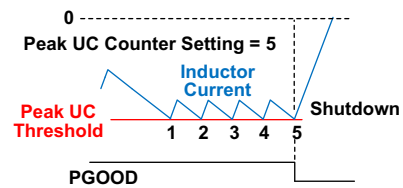


Figure 21. Peak UC Operation

The device also supports total output current limits that have user adjustable response delay. The two sum current limits, fast and slow, allow you to permit high maximum output current for a shorter period of time and lower output current for a longer period. The response delay for the limiting mechanisms is also adjustable. These mechanisms do not restrict the maximum output current until the current has exceeded a threshold for the response delay time. For example, suppose the device is configured with a Fast Sum OC limit of 350A, a response delay of 50μs, and a shutdown response type. Next, suppose a 400A load is then placed on the regulator. 400A is supplied to the load for 50μs, and the device shuts down as shown in Figure 22.

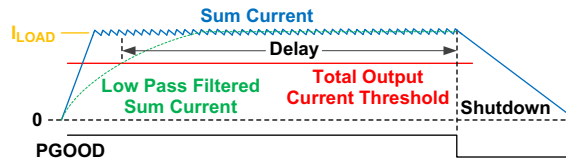


Figure 22. Total Output Current Protection

6.4 Smart Power Stage OC Fault Detect

Renesas Smart Power Stage (SPS) devices output a large signal on their IMON lines if peak current exceeds their preprogrammed threshold; for more details about this functionality, see the relevant SPS datasheet. The ISL68227 detects this fault flag by sensing signals that exceed the current-sense ADC full scale range and immediately shuts down.

SPS devices that conform to the industry common footprint, such as the ISL99380, do not use the IOUT pin for signaling overcurrent faults. All faults are signaled using their TOUT/FLT pins, and the ISL68227 provides a detector on each TEMP pin to support this method.

6.5 Thermal Protection and nVRHOT

The ISL68227 supports a comprehensive scheme for thermal alerting and protection. Regardless of temperature sense method, the device supports over-temperature or under-temperature faults in addition to over-temperature warning. When configured for per phase temperature telemetry, temperature faults are triggered based on the hottest reported phase. For example, if a 3-phase rail with an over-temperature threshold of +110°C reports phase temperatures of +100°C, +102°C, and +111°C, the device declares a fault because the hottest phase at +111°C exceeds the +110°C fault threshold. When configured for per-phase temperature sense, the SPS TOUT/FLT pins should remain connected to the ISL68227 TEMP pins.

IC die temperature is monitored to support telemetry and thermal shutdown. Shutdown occurs at approximately +130°C.

The nVRHOT pin is used at the system level to inform the powered device to reduce its power consumption. nVRHOT is an open-drain output; an external pull-up resistor is required. This signal is valid only after the controller is enabled. nVRHOT is pulled low when the sensed temperature for any rail reaches the PMBus OT_WARN threshold, providing the powered device with an advance warning of the thermal status of the IC.

Figure 23 shows the behavior of nVRHOT and an over-temperature fault shutdown.

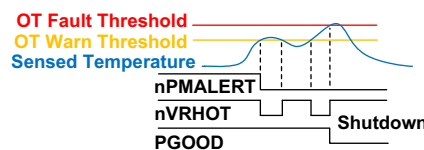


Figure 23. nVRHOT and Over-Temperature Shutdown

6.6 Catastrophic Failure Protection

The CFP pin supports Catastrophic Failure Protection (CFP) functionality. The pin can be configured to activate in the event of a catastrophic fault detection. The function is typically used to immediately disable the input supply to protect the entire system. The CFP function can be configured to respond to output overvoltage, input overvoltage, and/or output overcurrent faults.

6.7 Black Box Recorder

Black Box is a powerful diagnostic tool that captures all telemetry and status information when any fault occurs. The ISL68227 continuously monitors all rail and phase information along with the time duration that the rail has been regulating, and the tool captures that data when a fault is registered. Next, the tool reports the first fault bit that occurred to cause the shutdown. This diagnostic data is stored in RAM, and Black Box can be configured to additionally write to NVM for retrieval when the system loses input power as a fault occurs. The RAM record is updated every time a fault occurs. Black Box can write to NVM up to 10 times and provides an option to limit NVM writing to once per power cycle to avoid filling up the available NVM space inadvertently.

7. Layout and Design Considerations

The following layout and design strategies help minimize noise coupling and the impact of board parasitic impedances on converter performance, and they optimize the heat dissipating capabilities of the Printed Circuit Board (PCB). Follow these practices during the layout and design process.

7.1 Pin Noise Sensitivity, Design, and Layout Consideration

[Table 5](#) provides general guidance on best practices related to pin noise sensitivity. Use of good engineering judgment is required to implement designs based on criteria specific to the situation.

Table 5. Pin Design and/or Layout Consideration

| Pin Name | Noise Sensitive | Description |
|------------------------------|-----------------|---|
| VINSEN | Yes | Filter VINSEN with 100nF capacitor when sensing VIN directly. Use 10nF when using a resistor divider. |
| RGNDx VSENx | Yes | Treat each of the remote voltage sense pairs as differential signals in the PCB layout. Route them side by side on the same layer. Do not route them in proximity to noisy signals like PWM or Phase. Place a 3.3nF capacitor across the signals directly at the pins on the top layer. |
| PGx | No | Open-drain. Avoid setting its pull-up higher than VCC. Tie it to ground when not used. |
| PMSCL, PMSDA, nPMALERT | Yes | 50kHz to 2MHz signals should pair up with nPMALERT and be routed carefully between devices and back to the host. Provide 20 mils of spacing within PMSDA, nPMALERT, and PMSCL, and more than 30 mils to all other signals. See the SMBus design guidelines and place proper terminated (pull-up) resistance for impedance matching. Tie to ground when not used. Pull up to 3.3V max. |
| TEMPx | Yes | While using SPS, place a filter capacitor no greater than 500pF between each TEMP pin and ground near the IC. While using NTC, place a 47pF capacitor and a 22k resistor near the IC and route a differential signal pair from there to the remote NTC. Use Murata NCP15XH103J03RC (5% tolerance) or NCP15XH103F03RC (1% tolerance). Tie to ground if not used. |
| nVRHOT | No | Open drain. Avoid setting its pull-up rail higher than VCC. |
| VCC | Yes | Place a 1μF MLCC decoupling capacitor (X5R or better) directly at the pin. |
| VCCS | Yes | Place a 4.7μF MLCC decoupling capacitor (X5R or better) directly at the pin. |
| PWMx | No | Avoid routing near noise sensitive analog lines such as current sense or voltage sense. Leave floating if not used. |
| CSx CSRTNx | Yes | Treat each of the current sense pairs as differential signals in the PCB layout. Route them side by side on the same layer. Do not route them in close proximity to noisy signals like PWM or Phase. Proper routing of current sense is perhaps the most critical of all the layout tasks. Place the R-C filter between CSx and CSRTNx at the controller for SPS configuration. |
| GND | Yes | This EPAD is the ground for all IC signals. Use four or more vias to directly connect the EPAD to the ground plane. Never use only a single via or a 0Ω resistor connection to the power ground plane. Split ground planes are not advised. |
| General Comments | | The layer next to the top or bottom layer should be a ground layer. The signal layers should be sandwiched between the ground layers if possible. |

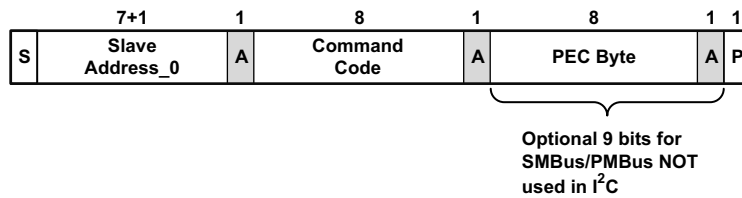
8. PMBus Protocol

The PMBus Protocol includes the Send Byte, the Write Byte/Word, Read Byte/Word, Group Command, and Alert Response Address protocols.

PMBus Protocol Legend

- S: Start Condition
- A: Acknowledge ("0")
- N: Not Acknowledge ("1")
- W: Write ("0")
- RS: Repeated Start Condition
- R: Read ("1")
- PEC: Packet Error Checking
- P: Stop Condition
- Acknowledge or DATA from Slave, Controller

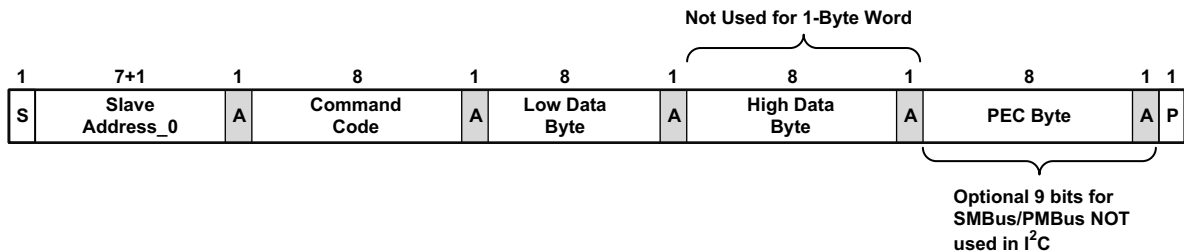
8.1 Send Byte Protocol



Example command: 03h Clear Faults
 (This clears all of the bits in Status Byte for the selected rail)

Figure 24. Send Byte Protocol

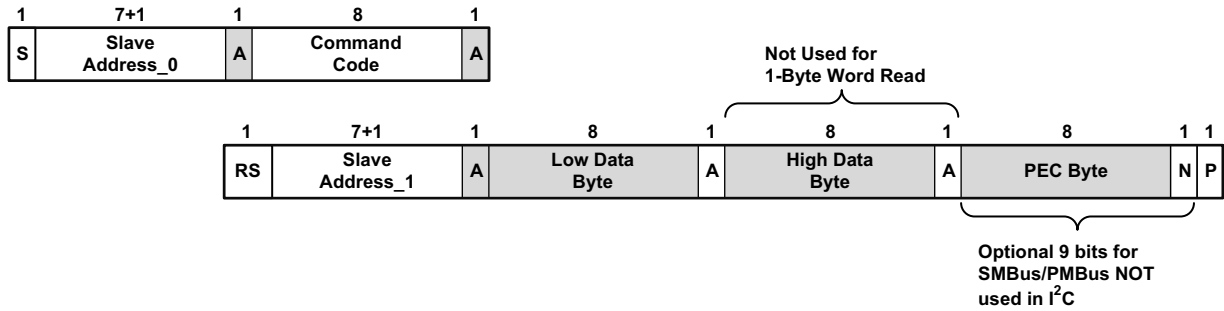
8.2 Write Byte/Word Protocol



Example command: 21h VOUT_COMMAND

Figure 25. Write Byte/Word Protocol

8.3 Read Byte/Word Protocol

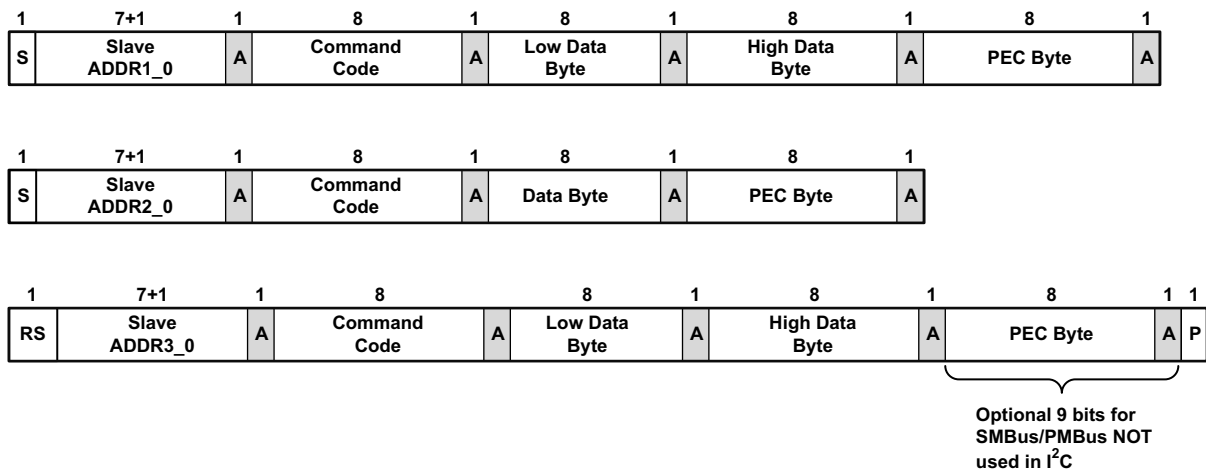


Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

Note: The STOP (P) bit is NOT allowed before the repeated START condition when reading contents of a register.

Figure 26. Read Byte/Word Protocol

8.4 Group Command Protocol



Note: No more than one command can be sent to the same Address

Figure 27. Group Command Protocol

8.5 Alert Response Address

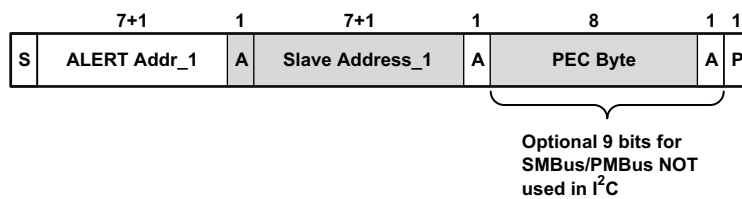


Figure 28. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus

9. PMBus Commands Summary

| Code | Command Name | Description | Type | Data Format | Default Value | Default Setting |
|------|--|--|-------------------------------|-------------|---------------|--|
| 00h | PAGE (00h) | Rail selector | R/W | Bit | 00h | Page 0 |
| 01h | OPERATION (01h) | Enable/disable, V_{OUT} source | R/W | Bit | 08h | Immediate off, Act on fault |
| 02h | ON_OFF_CONFIG (02h) | On/off configuration settings | R/W | Bit | 17h | ENABLE pin control, active high, immediate off |
| 03h | CLEAR_FAULTS (03h) | Clears all fault bits in all registers and releases the nPMALERT pin | Write | N/A | N/A | N/A |
| 04h | PHASE (04h) | Phase selector | R/W | Direct | 00h | Phase 0 |
| 05h | PAGE_PLUS_WRITE (05h) | Allows page and command write in single transaction | Block Write | Bit | N/A | N/A |
| 06h | PAGE_PLUS_READ (06h) | Allows page and command read in single transaction | Block Write/read/process call | Bit | N/A | N/A |
| 10h | WRITE_PROTECT (10h) | Write protection to sets of commands | R/W | Bit | 00h | No write protection |
| 19h | CAPABILITY (19h) | Reports PMBus capability | Read | Bit | D0h | See detail |
| 1Bh | SMBALERT_MASK (1Bh) | Mask status bits from SMBALERT signal | Block R/W | Bit | 00h | No bits masked |
| 20h | VOUT_MODE (20h) | Defines format for output voltage related commands | Read | Bit | 40h | Direct format |
| 21h | VOUT_COMMAND (21h) | Output voltage set by PMBus | R/W | Direct | 0384h | 900mV |
| 22h | VOUT_TRIM (22h) | Applies trim voltage to V_{OUT} set-point | R/W | Direct | 0000h | 0mV |
| 23h | VOUT_CAL_OFFSET (23h) | Applies offset voltage to V_{OUT} set-point | R/W | Direct | 0000h | 0mV |
| 24h | VOUT_MAX (24h) | Absolute maximum voltage setting | R/W | Direct | 0BEAh | 3050mV |
| 25h | VOUT_MARGIN_HIGH (25h) | Sets voltage target during margin high | R/W | Direct | 03B1 | 945mV |
| 26h | VOUT_MARGIN_LOW (26h) | Sets voltage target during margin low | R/W | Direct | 0357 | 855mV |
| 27h | VOUT_TRANSITION_RATE (27h) | Slew rate setting for V_{OUT} ramp | R/W | Direct | 09C4h | 25mV/ μ s |
| 28h | VOUT_DROOP (28h) | Sets the load-line (V/I slope) resistance for the output | R/W | Direct | 0000h | 0 μ V/A |
| 2Bh | VOUT_MIN (2Bh) | Absolute minimum voltage setting | R/W | Direct | 0000h | 0mV |
| 33h | FREQUENCY_SWITCH (33h) | Sets PWM switching frequency | R/W | Direct | 0258h | 600kHz |
| 34h | POWER_MODE (34h) | Sets power conversion mode | R/W | Bit | 03h | Maximum power |
| 35h | VIN_ON (35h) | Sets the V_{IN} startup threshold | R/W | Direct | 02BCh | 7V |
| 36h | VIN_OFF (36h) | Sets the V_{IN} shutdown threshold | R/W | Direct | 01F4h | 5V |
| 40h | VOUT_OV_FAULT_LIMIT (40h) | Sets the V_{OUT} OV fault limit while disabled | R/W | Direct | 0C1Ch | 3100mV |
| 41h | VOUT_OV_FAULT_RESPONSE (41h) | Configures the V_{OUT} OV fault response | R/W | Bit | 84h | Latch off |

| Code | Command Name | Description | Type | Data Format | Default Value | Default Setting |
|------|--|---|------|-------------|---------------|-----------------|
| 44h | VOUT_UV_FAULT_LIMIT (44h) | Sets the V_{OUT} UV fault limit | R/W | Direct | 0000h | 0V |
| 45h | VOUT_UV_FAULT_RESPONSE (45h) | Configures the V_{OUT} UV fault response | R/W | Bit | 84h | Latch off |
| 46h | IOUT_OC_FAULT_LIMIT (46h) | Sets the I_{OUT} OC fault limit | R/W | Direct | 1388h | 50A |
| 47h | IOUT_OC_FAULT_RESPONSE (47h) | Configures the I_{OUT} OC fault response | R/W | Bit | C4h | Latch off |
| 4Fh | OT_FAULT_LIMIT (4Fh) | Sets the OT fault limit | R/W | Direct | 007Dh | 125°C |
| 50h | OT_FAULT_RESPONSE (50h) | Configures the OT fault response | R/W | Bit | 84h | Latch off |
| 51h | OT_WARN_LIMIT (51h) | Sets the OT warning limit | R/W | Direct | 006Eh | 110°C |
| 53h | UT_FAULT_LIMIT (53h) | Sets the UT fault limit | R/W | Direct | FFD8h | -40°C |
| 54h | UT_FAULT_RESPONSE (54h) | Configures the UT fault response | R/W | Bit | 80h | Latch off |
| 55h | VIN_OV_FAULT_LIMIT (55h) | Sets the V_{IN} OV fault limit | R/W | Direct | 0640h | 16V |
| 56h | VIN_OV_FAULT_RESPONSE (56h) | Configures the V_{IN} OV fault response | R/W | Bit | 84h | Latch off |
| 57h | VIN_OV_WARN_LIMIT (57h) | Sets the V_{IN} OV warning limit | R/W | Direct | 0708h | 18V |
| 58h | VIN_UV_WARN_LIMIT (58h) | Sets the V_{IN} UV warning limit | R/W | Direct | 0000h | 0mV |
| 59h | VIN_UV_FAULT_LIMIT (59h) | Sets the V_{IN} UV fault limit | R/W | Direct | 0000h | 0mV |
| 5Ah | VIN_UV_FAULT_RESPONSE (5Ah) | Configures the V_{IN} UV fault response | R/W | Bit | 84h | Latch off |
| 5Bh | IIN_OC_FAULT_LIMIT (5Bh) | Sets the I_{IN} OC fault limit | R/W | Direct | 1388h | 50A |
| 5Ch | IIN_OC_FAULT_RESPONSE (5Ch) | Configures the I_{IN} OC fault response | R/W | Bit | 04h | Ignore |
| 5Dh | IIN_OC_WARN_LIMIT (5Dh) | Sets the I_{IN} OC warning limit | R/W | Direct | 3A98h | 150A |
| 60h | TON_DELAY (60h) | Sets turn-on delay time | R/W | Direct | 0000h | 0 μ s |
| 61h | TON_RISE (61h) | Sets turn-on rise time | R/W | Direct | 01F4h | 500 μ s |
| 64h | TOFF_DELAY (64h) | Sets turn-off delay time | R/W | Direct | 0000h | 0 μ s |
| 65h | TOFF_FALL (65h) | Sets turn-off fall time | R/W | Direct | 01F4h | 500 μ s |
| 78h | STATUS_BYTE (78h) | First byte of STATUS_WORD | Read | Bit | N/A | N/A |
| 79h | STATUS_WORD (79h) | Summary of critical faults | Read | Bit | N/A | N/A |
| 7Ah | STATUS_VOUT (7Ah) | Reports V_{OUT} warnings/faults | Read | Bit | N/A | N/A |
| 7Bh | STATUS_IOUT (7Bh) | Reports I_{OUT} warnings/faults | Read | Bit | N/A | N/A |
| 7Ch | STATUS_INPUT (7Ch) | Reports input warnings/faults | Read | Bit | N/A | N/A |
| 7Dh | STATUS_TEMPERATURE (7Dh) | Reports temperature warnings/faults | Read | Bit | N/A | N/A |
| 7Eh | STATUS_CML (7Eh) | Reports communication, memory, logic errors | Read | Bit | N/A | N/A |
| 80h | STATUS_MFR_SPECIFIC (80h) | Reports other specific faults | Read | Bit | N/A | N/A |
| 88h | READ_VIN (88h) | Reports input voltage measurement | Read | Direct | N/A | mV |
| 89h | READ_IIN (89h) | Reports input current measurement | Read | Direct | N/A | A |
| 8Bh | READ_VOUT (8Bh) | Reports output voltage measurement | Read | Direct | N/A | mV |

| Code | Command Name | Description | Type | Data Format | Default Value | Default Setting |
|------|--|---|------------|-------------|---------------|------------------------------------|
| 8Ch | READ_IOUT (8Ch) | Reports output current measurement | Read | Direct | N/A | A |
| 8Dh | READ_TEMPERATURE_1 (8Dh) | Reports power stage temperature measurement | Read | Direct | N/A | °C |
| 8Eh | READ_TEMPERATURE_2 (8Eh) | Reports internal temperature measurement | Read | Direct | N/A | °C |
| 8Fh | READ_TEMPERATURE_3 (8Fh) | Reports TEMP pin temperature measurement | Read | Direct | N/A | °C |
| 96h | READ_POUT (96h) | Reports output power | Read | Direct | N/A | W |
| 97h | READ_PIN (97h) | Reports input power | Read | Direct | N/A | W |
| 98h | PMBUS_REVISION (98h) | Reports the PMBus revision used | Read | Bit | 33h | P1 R1.3, P2 R1.3 |
| 99h | MFR_ID (99h) | Stores Inventory Information | Block R/W | Bit | 00000000h | Empty |
| 9Ah | MFR_MODEL (9Ah) | Stores Inventory Information | Block R/W | Bit | 00000000h | Empty |
| 9Bh | MFR_REVISION (9Bh) | Stores Inventory Information | Block R/W | Bit | 00000000h | Empty |
| 9Dh | MFR_DATE (9Dh) | Stores Inventory Information | Block R/W | Bit | 00000000h | Empty |
| ADh | IC_DEVICE_ID (ADh) | Reports device identification information | Block Read | Bit | 49D24F00h | 49D24F00h |
| A Eh | IC_DEVICE_REV (A Eh) | Reports device revision information | Block Read | Bit | | Release revision |
| C5h | DMAFIX (C5h) | Fixed DMA transactions | R/W | Bit | 0000h | 0 |
| C6h | DMASEQ (C6h) | Sequential DMA transaction | R/W | Bit | 0000h | 0 |
| C7h | DMAADDR (C7h) | Sets the address for DMA transactions | R/W | Bit | 0000h | 0 |
| CDh | PEAK_OC_LIMIT (CDh) | Sets peak per-phase OC limit | R/W | Direct | 258h | 60A |
| CEh | PEAK_UC_LIMIT (CEh) | Sets peak per-phase UC limit | R/W | Direct | FDA8 | -60A |
| D0h | VMON_ON (D0h) | Sets the VMON startup threshold | R/W | Direct | 1C2h | 4500mV |
| D1h | VMON_OFF (D1h) | Sets the VMON shutdown threshold | R/W | Direct | 190h | 4000mV |
| DDh | COMPPROP (DDh) | Configures proportional gain | R/W | Bit | D90907C4 | See detail |
| DEh | COMPINTEG (DEh) | Configures integral gain | R/W | Bit | A9h | See detail |
| DFh | COMPIDFF (DFh) | Configures differential gain | R/W | Bit | 0h | See detail |
| E0h | COMPCFB (E0h) | Configures AC current feedback | R/W | Bit | 560h | See detail |
| E3h | HS_BUS_CURRENT_SCALE (E3h) | Sets the high speed bus current scaling | R/W | Direct | 4000h | 1.0 |
| E4h | PHASE_CURRENT (E4h) | Reports per-phase current | Read | Direct | N/A | A |
| E5h | PHASE_TEMPERATURE (E5h) | Reports per-phase temperature | Read | Direct | N/A | °C |
| E9h | PEAK_OCUC_COUNT (E9h) | Sets the count limit before fault | R/W | Bit | 0606h | 6 cycles for OC & UC |
| E Ah | SLOW_IOUT_OC_LIMIT (E Ah) | Sets the slow I _{OUT} OC limit | R/W | Direct | C8h | 20A |
| EBh | FAST_OC_FILT_COUNT (EBh) | Configures the fast OC filter | R/W | Bit | 0696h | Filter = 10.6µs, Delay = 100µs |
| ECh | SLOW_OC_FILT_COUNT (ECh) | Configures the slow OC filter | R/W | Bit | 606h | Filter = 10.6µs, Delay = 1024µs |
| F0h | LOOPCFG (F0h) | Defines loop operating configuration | R/W | Bit | 102031F6h | See detail |

| Code | Command Name | Description | Type | Data Format | Default Value | Default Setting |
|------|-----------------------------------|--|------|-------------|---------------|-----------------|
| F2h | RESTORE_CFG (F2h) | Identifies configuration to be restored from NVM | R/W | Bit | 00h | |

9.1 PMBus Use Guidelines

All commands can be read at any time.

9.2 PMBus Data Formats

9.2.1 Direct

The Direct data format is a 2-byte binary integer.

9.2.2 Linear 16 Unsigned (L16U)

The L16u data format uses a fixed exponent (hard-coded to $N = -9h$) and a 16-bit unsigned integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

9.2.3 Linear 16 Signed (L16S)

The L16S data format uses a fixed exponent (hard-coded to $N = -9h$) and a 16-bit signed integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-9}$.

9.2.4 Linear 11 (L11)

The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent the real world decimal value (X).

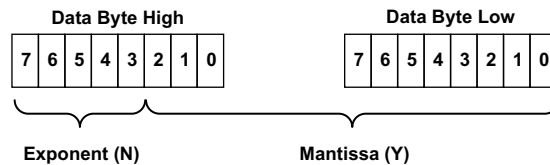


Figure 29. Linear 11 Data Format

The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^N$.

9.2.5 Bit Field (Bit)

A description of Bit Field is provided in the [“PMBus Command Detail” on page 37](#).

9.2.6 Custom (Cus)

Custom format

10. PMBus Command Detail

10.1 PAGE (00h)

Definition: Selects the communication path to Rail 0 or individual phases. All paged commands following this command are received and acted on by the selected destination path. Paged commands that can be written can be written globally, but can only be read on a specific page unless otherwise specified. Global commands remain global regardless of the value of this command. Individual phase access is available by setting this command to 80h and setting the individual phase value using the PHASE command.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

| Command | PAGE (00h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Value | Setting |
|-----------|---|
| 00h | Page 0 (Rail 0) |
| 80h | Individual phase (set by the PHASE command) |
| FFh | Global (All Rails) |

10.2 OPERATION (01h)

Definition: Sets Enable state when configured for PMBus enable. Sets the source of the target V_{OUT} . The table below reflects the valid settings for the device.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: Default Value: 08h (Immediate off, Act on fault)

| Command | OPERATION (01h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| Bit Number | Purpose | Bit Value | Meaning |
|------------|-----------------------|-----------|--|
| 7 | Enable/Disable Output | 0 | Disable |
| | | 1 | Enable |
| 6 | Disable Behavior | 0 | Immediate off (decay with PWM tri-state) |
| | | 1 | Soft off (Use TOFF_DELAY and TOFF_FALL) |
| 5:4 | V_{OUT} Source | 00 | $V_{OUT_COMMAND}$ |
| | | 01 | $V_{OUT_MARGIN_LOW}$ |
| | | 10 | $V_{OUT_MARGIN_HIGH}$ |
| | | 11 | Not used |
| 3:2 | Margin Response | 01 | Ignore V_{OUT} OV, UV faults when margined |
| | | 10 | Act on V_{OUT} OV, UV faults when margined |
| 1 | Not Supported | 0 | Not supported |
| 0 | Not Supported | X | Not supported |

10.3 ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 17h (ENABLE pin control)

Default Setting: ENABLE pin control, active high, immediate off

| Command | ON_OFF_CONFIG (02h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

| Bit Number | Purpose | Bit Value | Meaning |
|------------|--|-----------|---|
| 7:5 | Not Supported | 000 | Not supported |
| 4:2 | Sets the source of enable | 0XX | Output enables any time power is present regardless of pin or OPERATION command state. |
| | | 101 | Output enables from the enable pin only |
| | | 110 | Output enables from the OPERATION command only. |
| | | 111 | Output enables from the enable pin AND the OPERATION command. Both must be set to enable. |
| 1 | Polarity of ENABLE pin | 0 | Active low |
| | | 1 | Active high |
| 0 | ENABLE pin action when commanding the unit to turn off | 0 | Use the configured TOFF_DELAY and TOFF_FALL settings. |
| | | 1 | Turn off the output immediately (decay with PWM tri-state). |

10.4 CLEAR_FAULTS (03h)

Definition: Clears all fault status bits in all registers and releases the nPMALERT pin (if asserted) simultaneously. If a fault condition still exists, the bit(s) reasserts immediately. This command does not restart a device if it is shut down, it only clears the faults.

Access: Paged

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

10.5 PHASE (04h)

Definition: Sets the individual phase address for reading from PHASE_CURRENT (E4h) and PHASE_TEMPERATURE (E5h). The PAGE command must also be set to access phase information.

Access: Global

Data Length in Bytes: 1

Data Format: Direct

Type: R/W

Default Value: 00h (phase 0)

Equation: PHASE = (direct value)

Range: Phase 0 to 11

| Command | PHASE (04h) | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.6 PAGE_PLUS_WRITE (05h)

Definition: Sets the page within a device, sends a command, and sends the data for the command in one packet.

Access: Global

Data Format: Bit Field

Type: Block Write

The PAGE_PLUS_WRITE command uses the WRITE BLOCK protocol.

Figure 30 shows an example of the PAGE_PLUS command being used to send a command that has two data bytes to be written and a PEC byte.

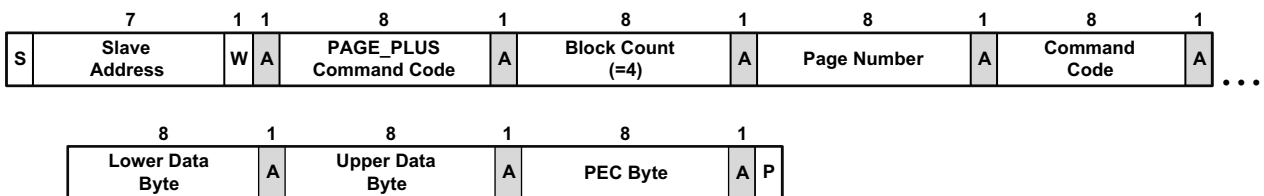


Figure 30. PAGE_PLUS_WRITE Command with a PEC Byte

10.7 PAGE_PLUS_READ (06h)

Definition: Sets the page within a device, sends a command, and reads the data returned by the command in one packet.

Access: Paged

Data Format: Bit Field

Type: Block Read

The PAGE_PLUS_READ command uses the BLOCK WRITE – BLOCK READ PROCESS CALL protocol.

Figure 31 shows an example of the PAGE_PLUS command being used to send a command that has two data bytes to be read and a PEC byte.

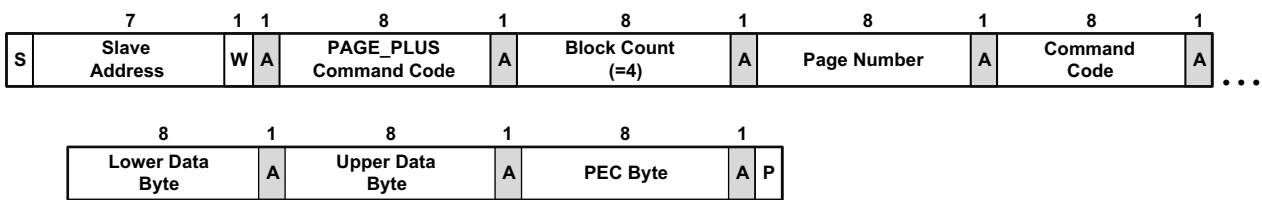


Figure 31. PAGE_PLUS_READ Command with a PEC Byte

10.8 WRITE_PROTECT (10h)

Definition: Sets the write protection of certain configuration commands.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h (enable all writes)

| Command | WRITE_PROTECT (10h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits 7:0 | Protection |
|-----------|--|
| 1000 0000 | Disable all writes except to WRITE_PROTECT command. |
| 0100 0000 | Disable all writes except to WRITE_PROTECT, OPERATION, and PAGE. |
| 0010 0000 | Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND. |
| 0000 0010 | Disable all writes except to WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, VOUT_COMMAND, and DMA. |
| 0000 0000 | Enable all writes |

Note: Any settings other than the five shown results in an invalid data fault.

10.9 CAPABILITY (19h)

Definition: Reports PMBus capabilities of the device.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: D0h (PEC supported, bus speed 1MHz, SMBALERT supported, Linear/Direct numeric data)

| Command | CAPABILITY (19h) | | | | | | | |
|---------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bit Number | Purpose | Bit Value | Meaning |
|------------|-------------------|-----------|---|
| 7 | PEC Support | 1 | PEC supported |
| | | 0 | PEC not supported |
| 6:5 | Maximum Bus Speed | 11 | Not supported |
| | | 10 | 1MHz |
| | | 01 | 400kHz |
| | | 00 | 100kHz |
| 4 | SMBALERT Support | 1 | SMBALERT pin and response protocol is supported. |
| | | 0 | SMBALERT pin and response protocol is not supported. |
| 3 | Numeric Format | 1 | Numeric data, IEEE half precision floating point format |
| | | 0 | Numeric data, Linear/Direct |
| 2 | Not Supported | 0 | Not supported |
| 1:0 | Not Supported | 00 | Not supported |

10.10 SMBALERT_MASK (1Bh)

Definition: Prevents a warning or fault condition from asserting the SMBALERT# signal. Can be used on the following PMBus status commands: STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, and STATUS_MFR_SPECIFIC.

Access: Paged

Data Format: Bit Field

Type: Block R/W

The command format used to block a status bit or bits from causing the SMBALERT# signal to be asserted is shown in [Figures 32](#) and [33](#). The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command code were sent with the mask byte 0100000b, an over-temperature warning condition would be blocked from asserting SMBALERT#.

Note: [Figure 32](#) shows the command format used by the host to determine the SMBALERT_MASK setting for a given status register.

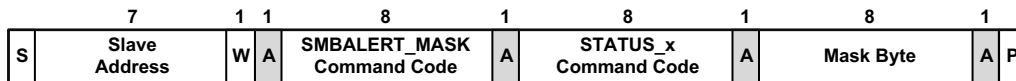


Figure 32. SMBALERT_MASK Command Packet Format

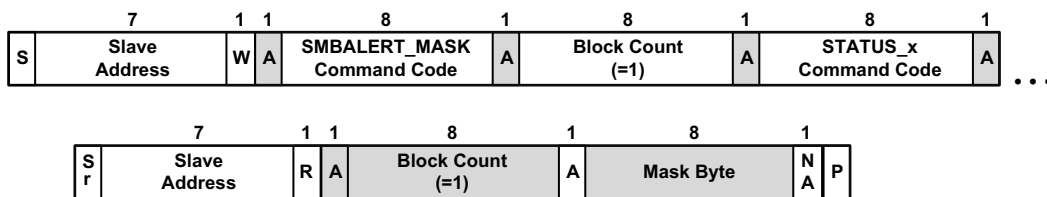


Figure 33. Retrieving the SMBALERT_MASK Setting for a Given Status Register

10.11 VOUT_MODE (20h)

Definition: Returns the supported V_{OUT} mode. Direct mode, 1mV per LSB.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 40h

| Command | VOUT_MODE (20h) | | | | | | | |
|---------------|-----------------|-----|-----|-----|----------|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Mode | | | | Exponent | | | |
| Default Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

10.12 VOUT_COMMAND (21h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for PMBus nominal operation. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0384h (900mV)

Units: mV

Equation: V_{OUT} Command = (Direct value)

Range: 0mV to 3050mV

| Command | VOUT_COMMAND (21h) | | | | | | | | | | | | | | | | |
|---------------|--------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

10.13 VOUT_TRIM (22h)

Definition: Applies a fixed trim voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: V_{OUT} Trim = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and V_{OUT_MAX}

| Command | VOUT_TRIM (22h) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.14 VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: V_{OUT} Cal Offset = (Direct value)

Range: Any value that results in the V_{OUT} target being between 0V and V_{OUT_MAX}

| Command | VOUT_CAL_OFFSET (23h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.15 VOUT_MAX (24h)

Definition: Sets the absolute maximum V_{OUT} regulation value regardless of any other commands or combinations. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0BEAh (3050mV)

Units: mV

Equation: V_{OUT} Max = (Direct value)

Range: 0mV to 3050mV

| Command | VOUT_MAX (24h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

10.16 VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin high. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 3B1h (945mV)

Units: mV

Equation: V_{OUT} Margin High = (Direct value)

Range: 0mV to 3050mV

| Command | VOUT_MARGIN_HIGH (25h) | | | | | | | | | | | | | | | | |
|---------------|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

10.17 VOUT_MARGIN_LOW (26h)

Definition: Sets the value of V_{OUT} when the OPERATION command is configured for margin low. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 357h (855mV)

Units: mV

Equation: V_{OUT} Margin Low = (Direct value)

Range: 0mV to 3050mV

| Command | VOUT_MARGIN_LOW (26h) | | | | | | | | | | | | | | | | |
|---------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |

10.18 VOUT_TRANSITION_RATE (27h)

Definition: Defines the output voltage rate of change during regulation. 0.01mV/μs per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 9C4h (25mV/μs)

Units: mV/μs

Equation: V_{OUT} Transition Rate = (Direct value) /100

Range: 10μV/μs to 100mV/μs

| Command | VOUT_TRANSITION_RATE (27h) | | | | | | | | | | | | | | | |
|---------------|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

10.19 VOUT_DROOP (28h)

Definition: Sets the rate at which output voltage changes relative to output current during regulation. 10μV/A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0μV/A)

Units: μV/A

Equation: V_{OUT} Droop = (Direct value) x 10

Range: 0μV/A to 16000μV/A

| Command | VOUT_DROOP (28h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.20 VOUT_MIN (2Bh)

Definition: Sets the absolute minimum voltage that is delivered to the output during regulation. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h

Units: mV

Equation: $V_{OUT\ Min} = (\text{Direct value})$

Range: 0mV to 3050mV

| Command | VOUT_MIN (2Bh) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.21 FREQUENCY_SWITCH (33h)

Definition: Sets the PWM switching frequency during regulation. 1kHz per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0258h (600kHz)

Units: kHz

Equation: Frequency Switch = (Direct value)

Range: 200kHz to 2MHz

| Command | FREQUENCY_SWITCH (33h) | | | | | | | | | | | | | | | |
|---------------|------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

10.22 POWER_MODE (34h)

Definition: Sets the power conversion mode.

- Maximum Efficiency Mode (0):
 - Voltage down transitions happen immediately with decay (PWM tri-state)
 - Phase dropping is enabled irrespective of the APD setting in the LOOPCFG command.
 - Diode emulation can be enabled using LOOPCFG[6].
- Maximum Power Mode (3) defaults:
 - Voltage down transitions happen as programmed in the TOFF_DELAY and TOFF_FALL commands.
 - Phase automatic add/drop is enabled using LOOPCFG[0].
 - Diode emulation can be enabled using LOOPCFG[28].
- MFR Defined (4) defaults:
 - Voltage down transitions happen immediately with decay (PWM tri-state).
 - Phase automatic is enabled irrespective of the APD setting in the LOOPCFG command.
 - Diode emulation can be enabled using LOOPCFG[6] and LOOPCFG[28].

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 03h, Maximum Power

| Command | POWER_MODE (34h) | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| Bit Value | Setting |
|-----------|--------------------|
| 04h | MFR defined |
| 03h | Maximum Power |
| 00h | Maximum Efficiency |

10.23 VIN_ON (35h)

Definition: Sets the input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 02BCh (7000mV)

Units: mV

Equation: $V_{IN\ On} = (\text{Direct value}) \times 10$

Range: -327680mV to 327670mV

| Command | VIN_ON (35h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

10.24 VIN_OFF (36h)

Definition: Sets the input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4 (5000mV)

Units: mV

Equation: $V_{IN\ Off} = (\text{Direct value}) \times 10$

Range: -327680mV to 327670mV

| Command | VIN_OFF (36h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

10.25 VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the disabled rail overvoltage threshold. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0C1Ch (3100mV)

Units: mV

Equation: $V_{OUT\ OV\ Fault\ Limit} = (\text{Direct value})$

Range: 0mV to 3050mV

| Command | VOUT_OV_FAULT_LIMIT (40h) | | | | | | | | | | | | | | | |
|---------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

10.26 VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the output overvoltage fault response. For a fault to be considered cleared, the output must drop by 100mV.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | VOUT_OV_FAULT_RESPONSE (41h) | | | | | | | |
|---------------|------------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the rail is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | 0ms delay (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.27 VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the output under voltage fault threshold. 1mV per LSB. This fault is masked during ramp or when disabled.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0V

Units: mV

Equation: V_{OUT} UV Fault Limit = (Direct value)

Range: 0V to 3.05V

| Command | VOUT_UV_FAULT_LIMIT (44h) | | | | | | | | | | | | | | | |
|---------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.28 VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the output undervoltage fault response. This fault is masked during ramp or when disabled.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | VOUT_UV_FAULT_RESPONSE (45h) | | | | | | | |
|---------------|------------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the rail is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.29 IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the fast sum output overcurrent fault threshold. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 12Ch (30A)

Units: A

Equation: $I_{OUT\ OC\ Fault\ Limit} = (Direct\ value)/10$

Range: 0A to 3276.7A

| Command | IOUT_OC_FAULT_LIMIT (46h) | | | | | | | | | | | | | | | | |
|---------------|---------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

10.30 UT_OC_FAULT_RESPONSE (47h)

Definition: Configures the output overcurrent fault response for all IOUT OC detection methods. This response setting is also applied to output undercurrent faults.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: C4h (latch off)

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01-10 | Not supported |
| | | 11 | Disable and retry as set in Bits [5:3] |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the rail is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.31 OT_FAULT_LIMIT (4Fh)

Definition: Sets the power stage over-temperature fault limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 007Dh (125°C)

Units: °C

Equation: OT Fault Limit = (Direct value)

Range: 0°C to +150°C

| Command | OT_FAULT_LIMIT (4Fh) | | | | | | | | | | | | | | | | |
|---------------|----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

10.32 OT_FAULT_RESPONSE (50h)

Definition: Configures the power stage over-temperature fault response. For a fault to be considered cleared, the temperature must drop 5°C below the OT fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | OT_FAULT_RESPONSE (50h) | | | | | | | |
|---------------|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the rail is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.33 OT_WARN_LIMIT (51h)

Definition: Sets the power stage over-temperature warning limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 006Eh (110°C)

Units: °C

Equation: OT Warn Limit = (Direct value)

Range: 0°C to 150°C

| Command | OT_WARN_LIMIT (51h) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

10.34 UT_FAULT_LIMIT (53h)

Definition: Sets the power stage under-temperature fault limit. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: FFD8h (-40°C)

Units: °C

Equation: UT Fault Limit = (Direct value)

Range: -50°C to 150°C

| Command | UT_FAULT_LIMIT (53h) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

10.35 UT_FAULT_RESPONSE (54h)

Definition: Configures the power stage under-temperature fault response. For the fault to be considered cleared, the temperature must rise 5°C above the UT fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | UT_FAULT_RESPONSE (54h) | | | | | | | |
|---------------|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the device is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously without limitation until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.36 VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0640h (16000mV)

Units: mV

Equation: V_{IN} OV Fault Limit = (Direct value) x 10

Range: -327680mV to 327670mV

| Command | VIN_OV_FAULT_LIMIT (55h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

10.37 VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the input overvoltage fault response. For a fault to be considered cleared, the input voltage must drop by 1/16th of the OV fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | VIN_OV_FAULT_RESPONSE (56h) | | | | | | | |
|---------------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the device is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously without limitation until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.38 VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} undervoltage fault threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 708h (18000mV)

Units: mV

Equation: V_{IN} OV Warn Limit = (Direct value) *10

Range: 0mV to 327670mV

| Command | VIN_OV_WARN_LIMIT (57h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

10.39 VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0V)

Units: mV

Equation: V_{IN} UV Warn Limit = (Direct value) *10

Range: 0mV to 327670mV

| Command | VIN_UV_WARN_LIMIT (58h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.40 VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold. 10mV per LSB. If using VIN_ON and VIN_OFF commands, this command should be set to 0V.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0V)

Units: mV

Equation: V_{IN} UV Fault Limit = (Direct value) x 10

Range: -327680mV to 327670mV

| Command | VIN_UV_FAULT_LIMIT (59h) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.41 VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the input undervoltage fault response. For a fault to be considered cleared, the input voltage must rise by 1/16th of the UV fault threshold value.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 84h (latch off)

| Command | VIN_UV_FAULT_RESPONSE (5Ah) | | | | | | | |
|---------------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01 | Not supported |
| | | 10 | Disable and retry according to the setting in Bits [5:3]. |
| | | 11 | Not supported |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the device is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.42 IIN_OC_FAULT_LIMIT (5Bh)

Definition: Sets the input overcurrent fault threshold for the synthesized input current reading at READ_IIN. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1388h (50A)

Units: A

Equation: $I_{IN} \text{ OC Fault Limit} = (\text{Direct value})/100$

Range: -327.68A to 327.67A

| Command | IIN_OC_FAULT_LIMIT (5Bh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

10.43 IIN_OC_FAULT_RESPONSE (5Ch)

Definition: Configures the input overcurrent fault response for the synthesized input current reading at READ_IIN.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 04h (ignore)

| Command | IIN_OC_FAULT_RESPONSE (5Ch) | | | | | | | |
|---------------|-----------------------------|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit | Field Name | Value | Description |
|-----|---|---------|---|
| 7:6 | Response Behavior During a fault, the device: <ul style="list-style-type: none"> • Pulls PMALRT low • Sets the related fault bit in the status registers. | 00 | Continue without interruption. |
| | | 01-10 | Not supported |
| | | 11 | Disable and retry as set in Bits [5:3]. |
| 5:3 | Retry Setting | 000 | No retry. The output remains disabled until the device is restarted. |
| | | 001-110 | Not supported |
| | | 111 | Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down. The time between retries is set by Bits [2:0]. |
| 2:0 | Delay Time before Retry | 000 | Delay 0ms (not recommended) |
| | | 001-110 | Delay 25ms per LSB |
| | | 111 | Delay 175ms |

10.44 IIN_OC_WARN_LIMIT (5Dh)

Definition: Sets the input overcurrent warning threshold. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 3A98h (150A)

Units: A

Equation: $I_{IN} \text{ OC Warn Limit} = (\text{Direct value})/100$

Range:

| Command | IIN_OC_WARN_LIMIT (5Dh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

10.45 TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise. 10 μ s per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0 μ s)

Units: μ s

Equation: $t_{ON} \text{ Delay} = (\text{Direct value}) \times 10$

Range: 0 μ s to 655534 μ s

| Command | TON_DELAY (60h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.46 TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} during enable. 1 μ s per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (500 μ s)

Units: μ s

Equation: t_{ON} Rise = (Direct value)

Range: 0 μ s to 10000 μ s

| Command | TON_RISE (61h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

10.47 TOFF_DELAY (64h)

Definition: Sets the delay time of V_{OUT} during disable when configured for soft off. 10 μ s per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 0000h (0 μ s)

Units: μ s

Equation: t_{OFF} Delay = (Direct value) x 10

Range: 0 μ s to 655534 μ s

| Command | TOFF_DELAY (64h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.48 TOFF_FALL (65h)

Definition: Sets the fall time of V_{OUT} during disable when configured for soft off. 1 μ s per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 01F4h (500 μ s)

Units: μ s

Equation: t_{OFF} Fall = (Direct value)

Range: 0 μ s to 10000 μ s

| Command | TOFF_FALL (65h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |

10.49 STATUS_BYTE (78h)

Definition: Returns a summary of the device status. Based on the information in this byte, the host can get more information by reading the appropriate status registers. Depending on the setting of the PAGE command, this command returns information about individual rails or a global summary of all rail statuses.

Access: Paged and Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

| Command | STATUS_BYTE (78h) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|-------------------|--|
| 7 | BUSY | A fault was declared because the device was busy and unable to respond. |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault occurred. |
| 2 | TEMPERATURE | A temperature fault or warning occurred. |
| 1 | CML | A communications, memory, or logic fault occurred. |
| 0 | None of the Above | A fault other than those listed above occurred. |

10.50 STATUS_WORD (79h)

Definition: Returns a summary of the device status. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. Depending on the setting of the PAGE command, this command returns information about individual rails or a global summary of all rail statuses. The low byte of the STATUS_WORD is the same as the STATUS_BYTE (78h) command.

Access: Paged and Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

| Command | STATUS_WORD (79h) | | | | | | | | | | | | | | | |
|--------------|---------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | | | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|-------------------|--|
| 15 | V _{OUT} | An output voltage fault or warning occurred. |
| 14 | I _{OUT} | An output current fault occurred. |
| 13 | INPUT | An input voltage fault or warning occurred. |
| 12 | MFR_SPECIFIC | A manufacturer specific fault or warning occurred. |
| 11 | POWER_GOOD # | The POWER_GOOD signal is negated (Note 8) |
| 10:9 | Not Supported | Not supported |
| 8 | Unknown | A fault other than those described in Bits[15:9] occurred. |
| 7 | Busy | Device busy and unable to respond |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault occurred. |
| 2 | TEMPERATURE | A temperature fault or warning occurred. |
| 1 | CML | A communications, memory, or logic fault occurred. |
| 0 | None of the Above | A status change other than those listed above occurred. |

Note:

8. If the POWER_GOOD# Bit is set, this indicates that the POWER_GOOD signal is signaling that the output power is not good.

10.51 STATUS_VOUT (7Ah)

Definition: Returns a summary of output voltage status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_VOUT (7Ah) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|------------------|---|
| 7 | VOUT_OV_FAULT | Indicates an output overvoltage fault occurred. |
| 6:5 | Not Supported | Not supported |
| 4 | VOUT_UV_FAULT | Indicates an output undervoltage fault occurred. |
| 3 | VOUT_MAX Warning | Indicates an output voltage maximum warning occurred. |
| 2:0 | Not Supported | Not supported |

10.52 STATUS_IOUT (7Bh)

Definition: Returns a summary of output current status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_IOUT (7Bh) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|---------------------|--|
| 7 | IOUT_OC_FAULT | An output overcurrent fault occurred. |
| 6 | Not Supported | Not supported |
| 5 | Not supported | Not supported |
| 4 | IOUT_UC_FAULT | An output undercurrent fault occurred. |
| 3 | Current Share Fault | A current share fault occurred. |
| 2:0 | Not Supported | Not supported |

10.53 STATUS_INPUT (7Ch)

Definition: Returns a summary of input status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_INPUT (7Ch) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|--|
| 7 | VIN_OV_FAULT | An input overvoltage fault occurred. |
| 6 | VIN_OV_WARN | An input overvoltage warning occurred. |
| 5 | VIN_UV_WARN | An input undervoltage warning occurred. |
| 4 | VIN_UV_FAULT | An input undervoltage fault occurred. |
| 3 | VIN_ON/OFF | Disabled due to insufficient input voltage. This could be VIN or VMON. |
| 2 | IIN_OC_FAULT | An input overcurrent fault occurred. |
| 1 | IIN_OC_WARN | An input overcurrent warning occurred. |
| 0 | Not Supported | Not supported |

10.54 STATUS_TEMPERATURE (7Dh)

Definition: Returns a summary of temperature status.

Access: Paged

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_TEMPERATURE (7Dh) | | | | | | | |
|--------------|--------------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|---------------------------------------|
| 7 | OT_FAULT | An over-temperature fault occurred. |
| 6 | OT_WARN | An over-temperature warning occurred. |
| 5 | Not Supported | Not supported |
| 4 | UT_FAULT | An under-temperature fault occurred. |
| 3:0 | Not Supported | Not supported |

10.55 STATUS_CML (7Eh)

Definition: Returns a summary of any communications, logic, and/or memory errors.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_CML (7Eh) | | | | | | | |
|--------------|---------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|---|
| 7 | IUCR | Invalid or unsupported PMBus command was received. This bit sets during device discovery when using PowerNavigator. |
| 6 | IUDR | The PMBus command was sent with invalid or unsupported data. |
| 5 | PECF | A packet error check failure was detected in the PMBus command. |
| 4 | MFD | Memory fault detected. This bit sets if the selected NVM config location is empty or invalid. |
| 3 | PFD | Processor fault detected. |
| 2 | Not Supported | Not supported |
| 1 | OCF | A communication fault other than the ones listed in this table occurred. |
| 0 | OMLF | A memory or logical fault not listed previously was detected. |

10.56 STATUS_MFR_SPECIFIC (80h)

Definition: Returns a summary of the manufacturer specific status.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

| Command | STATUS_MFR_SPECIFIC (80h) | | | | | | | |
|--------------|---------------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| Bit | Status Bit Name | Meaning |
|-----|----------------------------|--|
| 7 | ADCUNLOCK | ADC clock unlock detected |
| 6 | Not Supported | Not supported |
| 5 | CFP Fault | A CFP fault occurred |
| 4 | Internal Temperature Fault | The controller internal temp exceeded 130 °C. |
| 3 | BBEVENT | A Black Box event occurred. |
| 2 | LMSEvent | A Last Man Standing event occurred. |
| 1 | SPSFault | An SPS overcurrent and/or over-temperature event occurred. |
| 0 | Not Supported | Not supported |

10.57 READ_VIN (88h)

Definition: Returns the input voltage reading. Scaled as 10mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read $V_{IN} = (\text{Direct value}) \times 10$

| Command | READ_VIN (88h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.58 READ_IIN (89h)

Definition: Returns the synthesized input current reading. 10mA per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read $I_{IN} = (\text{Direct value})/100$

| Command | READ_IIN (89h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.59 READ_VOUT (8Bh)

Definition: Returns the output voltage reading. 1mV per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: mV

Equation: Read $V_{OUT} = (\text{Direct value})$

| Command | READ_VOUT (8Bh) | | | | | | | | | | | | | | | |
|--------------|------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |

10.60 READ_IOUT (8Ch)

Definition: Returns the output current reading. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Read $I_{OUT} = (\text{Direct value})/10$

| Command | READ_IOUT (8Ch) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.61 READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading of the hottest power stage per configured rail. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 1 = (Direct value)

| Command | READ_TEMPERATURE_1 (8Dh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.62 READ_TEMPERATURE_2 (8Eh)

Definition: Returns the internal controller temperature reading. 1°C per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 2 = (Direct value)

| Command | READ_TEMPERATURE_2 (8Eh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.63 READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the TEMP pins. 1°C per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Read Temperature 3 = (Direct value)

| Command | READ_TEMPERATURE_3 (8Fh) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.64 READ_POUT (96h)**Definition:** Returns the output power. 1W per LSB.**Access:** Paged**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Units:** W**Equation:** Read P_{OUT} = (Direct value)

| Command | READ_POUT (96h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.65 READ_PIN (97h)**Definition:** Returns the input power. 1W per LSB.**Access:** Paged**Data Length in Bytes:** 2**Data Format:** Direct**Type:** Read Only**Units:** W**Equation:** READ_PIN = (Direct value)

| Command | READ_PIN (97h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.66 PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus specification to which the device is compliant.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Default Value: 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

| Command | PMBUS_REVISION (98h) | | | | | | | |
|---------------|----------------------|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

| Bits 7:4 | Part 1 Revision | Bits 3:0 | Part 2 Revision |
|----------|-----------------|----------|-----------------|
| 0000 | 1.0 | 0000 | 1.0 |
| 0001 | 1.1 | 0001 | 1.1 |
| 0010 | 1.2 | 0010 | 1.2 |
| 0011 | 1.3 | 0011 | 1.3 |

10.67 MFR_ID (99h)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

10.68 MFR_MODEL (9Ah)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

10.69 MFR_REVISION (9Bh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

10.70 MFR_DATE (9Dh)

Definition: Stores inventory information during manufacturing of end products. 4 bytes of space with no defined format.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block R/W

Default Value: 00000000h (empty)

10.71 IC_DEVICE_ID (ADh)

Definition: Reports device identification information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: 49D24F00h

| Command | IC_DEVICE_ID (ADh) | | | |
|---------------|--------------------|--------------|-------------|----------|
| Format | Bit Field | | | |
| Byte Position | 3 | 2 | 1 | 0 |
| Function | MFR Code | ID High Byte | ID Low Byte | Reserved |
| Default Value | 49h | D2h | 4Fh | 00h |

10.72 IC_DEVICE_REV (AEh)

Definition: Reports device revision information.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: Block Read

Default Value: Based on the revision released

| Command | IC_DEVICE_REV (AEh) | | |
|--------------|---------------------|----------|-------------------|
| Format | Bit Field | | |
| Bit Position | 31:24 | 23:8 | 7:0 |
| Function | Hardware Revision | Reserved | Firmware Revision |

10.73 DMAFIX (C5h)

Definition: Location for DMA access when performing a fixed address memory access. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

10.74 DMASEQ (C6h)

Definition: Location for DMA access when performing a auto-increment address memory access. A series of reads or writes accesses sequential memory locations, with the value of DMAADDR incremented with each access. The reads or writes can be singular 32-bit transfers or unlimited bursts. There is no physical storage for this register.

Access: Global

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

10.75 DMAADDR (C7h)

Definition: Specifies the target address of a DMA read or write to system memory. This command is used for indirect access to any system memory.

Access: Global

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0000h

Units: N/A

| Command | DMAADDR (C7h) | | | | | | | | | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | Field Name | Meaning |
|-------|------------|---------------------------|
| 15:13 | REGION | 000 - RAM |
| 12:0 | DMAADDR | The 13-bit target address |

10.76 PEAK_OC_LIMIT (CDh)

Definition: Sets the peak overcurrent limit thresholds for each phase within a rail. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase OC Limit = (Direct value)/10

Units: A

Default Value: 0258h (60A)

Range: Depends on configuration

| Command | PEAK_OC_LIMIT (CDh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

10.77 PEAK_UC_LIMIT (CEh)

Definition: Sets the peak undercurrent limit thresholds for each phase within a rail. 0.1A per LSB.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Equation: Peak Phase UC Limit = (Direct value)/10

Units: A

Default Value: FDA8 (-60A)

Range: Depends on configuration

| Command | PEAK_UC_LIMIT (CEh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |

10.78 VMON_ON (D0h)

Definition: Sets the VMON pin input voltage rising threshold at which the output can be enabled. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 1C2h (4.5V)

Units: mV

Equation: VMON On = (Direct value) x 10

Range: 0mV to 32767mV

| Command | VMON_ON (D0h) | | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Unsigned Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

10.79 VMON_OFF (D1h)

Definition: Sets the VMON pin input voltage falling threshold at which the output disables. 10mV per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 190h (4V)

Units: mV

Equation: VMON_OFF = (Direct value) x 10

Range: 0mV to 32767mV

| Command | VMON_OFF (D1h) | | | | | | | | | | | | | | | |
|---------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

10.80 COMPPROP (DDh)

Definition: Sets the proportional gain of the compensation loop.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: D90907C4h

| Command | COMPPROP (DDh) | | | | | | | | | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit Position | Function |
|--------------|---|
| 31:28 | Proportional gain mantissa >8 phase override, use normal P gain if value = 0 and shift = 0 |
| 27:25 | Proportional gain exponent >8 phase override, use normal P gain if value = 0 and shift = 0 |
| 24:21 | Proportional gain mantissa 2-phase override, use normal P gain if value = 0 and shift = 0 |
| 20 | Not Used |
| 19:17 | Proportional gain exponent 2-phase override, use normal P gain if value = 0 and shift = 0 |
| 16:13 | Proportional gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0 |
| 12 | Not Used |
| 11:9 | Proportional gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0 |
| 8 | FIR filter length, 0 = None or 1 = ON Must be set if using D term for PID, optional if not using D term |
| 7:4 | Proportional gain mantissa is (value/8), all phase counts, if value = 0 gain is 0 |
| 3 | Not Used |
| 2:0 | Proportional gain exponent is $2^{(\text{shift}-3)}$, all phase counts, if value = 0 and shift = 0 gain is 0 |

10.81 COMPINTEG (DEh)

Definition: Sets the integral gain of the compensation loop.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 00A9h

| Command | COMPINTEG (DEh) | | | | | | | | | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

| Bit Position | Function |
|--------------|---|
| 31:16 | Not used |
| 15:12 | Delay time for stepping down gain towards shift. Dcm when in DCM, in 16*clkTs per gain step |
| 11:8 | Gain when in DCM for a while |
| 7:4 | Max gain used when Integral movement detected Gain is $2^{(-shift-1)}$ |
| 3:0 | Gain is $2^{(-shift-1)}$ |

10.82 COMPIDFF (DFh)

Definition: Sets the differential gain of the compensation loop.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0000h

| Command | COMPIDFF (DFh) | | | | | | | | | | | | | | | |
|---------------|---------------------|----|-----|-----|----|----|-----|-----|---|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R/W | R/W | R | R | R/W | R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Setting |
|------------|---|
| 15:13 | Reserved |
| 12 | FIR filter length 0 or 1 |
| 11:8 | Diff gain mantissa 1-phase override, use normal P gain if value = 0 and shift = 0 |
| 7:6 | Diff gain exponent 1-phase override, use normal P gain if value = 0 and shift = 0 |
| 5:2 | Differentiator gain mantissa (value/8) |
| 1:0 | Differentiator gain exponent $2^{(\text{shift}+1 + \text{P-shift})}$ range 0:3 |

10.83 COMPCFB (E0h)

Definition: Sets the AC current feedback gain of the compensation loop.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0560h

| Command | COMPCFB (E0h) | | | | | | | | | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Function |
|------------|---|
| 15:8 | High-pass filter coefficient for current feedback |
| 7:0 | Current feedback gain, low droop cases |

10.84 HS_BUS_CURRENT_SCALE (E3h)

Definition: Sets the scaling value for the high speed bus output current reporting. 16 bits with 14 fractional bits. A value of 0x4000 is a scale factor of 1.0. A value of 0x0000 is also interpreted as a scale factor of 1.0.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: 4000h (1.0)

Units: Scale Factor

Equation: HS Bus Current Scale = (Direct value) * 2⁻¹⁴

Range: 0 to 4.0

| Command | HS_BUS_CURRENT_SCALE (E3h) | | | | | | | | | | | | | | | |
|---------------|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

10.85 PHASE_CURRENT (E4h)

Definition: Returns the individual phase current reading for the phase selected in PHASE (04h). 0.1A per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: A

Equation: Phase current = (Direct value) / 10

| Command | PHASE_CURRENT (E4h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.86 PHASE_TEMPERATURE (E5h)

Definition: Returns the individual phase temperature reading for the phase selected in PHASE (04h). 1°C per LSB.

Access: Global

Data Length in Bytes: 2

Data Format: Direct

Type: Read Only

Units: °C

Equation: Phase Temperature = (Direct value)

| Command | PHASE_TEMPERATURE (E5h) | | | | | | | | | | | | | | | |
|--------------|--------------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

10.87 PEAK_OCUC_COUNT (E9h)

Definition: Sets the number of consecutive switch cycles that can exceed the peak per-phase overcurrent limit threshold before generating a fault within a rail. A value of 0 disables the fault shutdown and produces a constant current effect.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Equation: Peak UC Count = (Direct value [15:8]), Peak OC Count = (Direct value [7:0])

Units: Cycles

Default Value: 0606h (6 cycles OC and 6 cycles UC)

Range: 1 cycle to 255 cycles

| Command | PEAK_OCUC_COUNT (E9h) | | | | | | | | | | | | | | | |
|---------------|-----------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit Number | Meaning |
|------------|--|
| 15:8 | Number of consecutive switch cycles exceeding peak UC limit before fault |
| 7:0 | Number of consecutive switch cycles exceeding peak OC limit before fault |

10.88 SLOW_IOUT_OC_LIMIT (EAh)

Definition: Sets the slow sum output overcurrent fault threshold. 100mA per LSB. A value of 0 disables this function.

Access: Paged

Data Length in Bytes: 2

Data Format: Direct

Type: R/W

Default Value: C8h (20A)

Units: A

Equation: Slow I_{OUT} OC Limit = (Direct value) / 10

Range: 0A to 3276A

| Command | SLOW_IOUT_OC_LIMIT (EAh) | | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Format | Direct | | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

10.89 FAST_OC_FILT_COUNT (EBh)

Definition: Sets the fast sum output overcurrent fault filter settings.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 0696h (Filter = 10.6µs, Delay = 100µs)

| Command | FAST_OC_FILT_COUNT (EBh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

| Bit Number | Purpose | Setting |
|------------|----------------|--|
| 15:12 | Not Used | Not used |
| 11:8 | Filter Setting | Time constant = 166.7ns * 2 ^{direct value} . Range is 167ns to 5.46ms. |
| 7:0 | Delay Setting | Delay 0.667µs * direct value before a fault is generated. Range is 0µs to 170µs. |

10.90 SLOW_OC_FILT_COUNT (ECh)

Definition: Sets the slow sum output overcurrent fault filter settings.

Access: Paged

Data Length in Bytes: 2

Data Format: Bit Field

Type: R/W

Default Value: 606h (Filter = 10.6µs, Delay = 1024µs)

| Command | SLOW_OC_FILT_COUNT (ECh) | | | | | | | | | | | | | | | |
|---------------|--------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| Bit Number | Purpose | Setting |
|------------|----------------|---|
| 15:12 | Not Used | Not used |
| 11:8 | Filter Setting | Time constant = 166.7ns * 2 ^{direct value} . Range is 167ns to 5.46ms |
| 7:0 | Delay Setting | Delay 170.7µs * direct value before a fault is generated. Range is 0µs to 43.5ms. |

10.91 LOOPCFG (F0h)

Definition: Configures various rail settings. To make a change, read the value, modify only the desired bits, and write the value while preserving the bit settings.

Access: Paged

Data Length in Bytes: 4

Data Format: Bit Field

Type: R/W

Default Value: 102031F6h

| Command | LOOPCFG (F0h) | | | | | | | | | | | | | | | |
|---------------|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

| Bit Position | Field | Function |
|--------------|------------------------|---|
| 31 | Not Used | Not used |
| 30:29 | Reserved | Reserved |
| 28 | Diode Emulation Mode | 1 = Enable diode emulation for power_mode 3 |
| 27:12 | Reserved | Reserved |
| 11:8 | Minimum Phase Count | Minimum phase count, 0-12 |
| 7 | Reserved | Reserved |
| 6 | Diode Emulation Enable | 1 = Enable diode emulation |
| 5:4 | Reserved | Reserved |
| 3:1 | Reserved | Reserved |
| 0 | APD enable | 1 = Enable auto phase add/drop |

10.92 RESTORE_CFG (F2h)

Definition: Identifies the user configuration ID to be restored from NVM and loads the store settings into the active memory of the device. This command should only be used while all outputs are disabled. Restore takes 3ms to complete.

Access: Global

Data Length in Bytes: 1

Data Format: Bit Field

Type: R/W

Default Value: 00h

| Command | RESTORE_CFG (F2h) | | | | | | | |
|---------------|---------------------|---|---|---|-----|-----|-----|-----|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit Number | Status Bit Name | Meaning |
|------------|-----------------|--|
| 7:4 | Reserved | Reserved |
| 3:0 | CONFIG | Selected user configuration ID to restore, 0-15. |

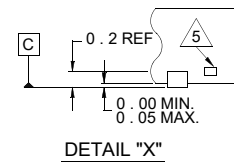
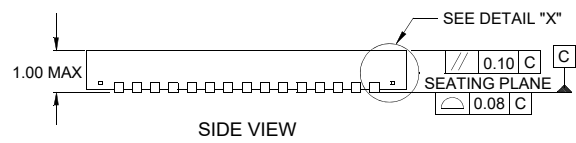
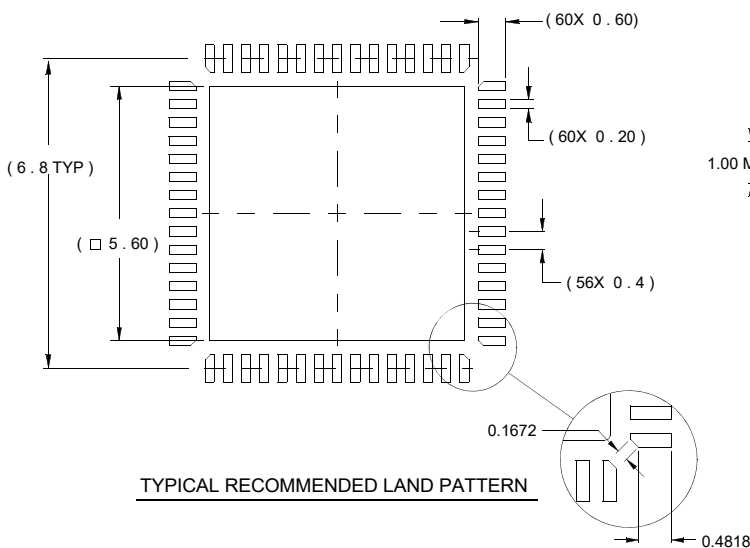
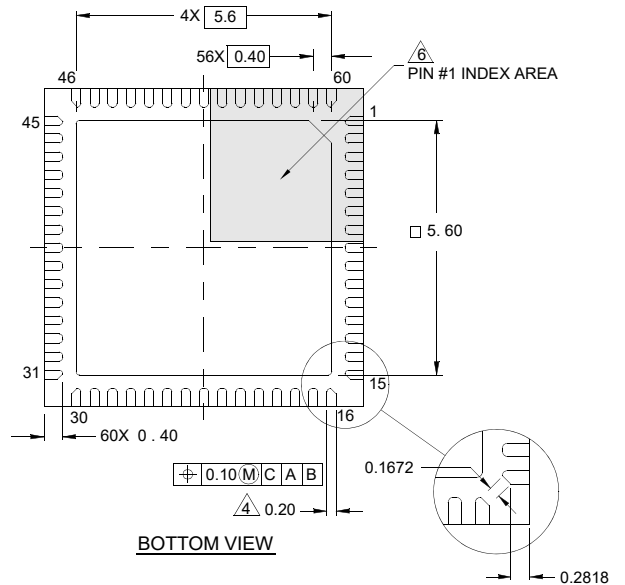
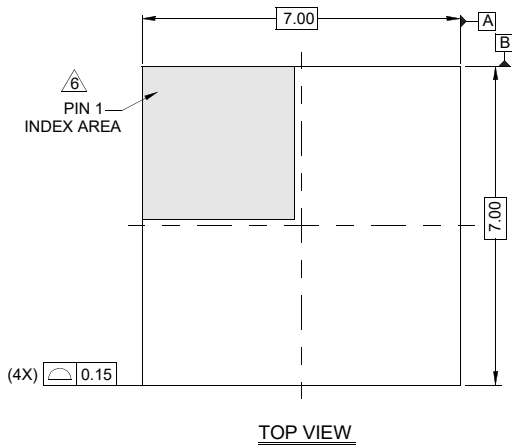
11. Revision History

| Rev. | Date | Description |
|------|----------|-----------------|
| 1.00 | Oct.1.20 | Initial release |

12. Package Outline Drawing

For the most recent package outline drawing, see [L60.7x7](#).

L60.7x7
 60 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
 Rev 1, 2/10



NOTES:

1. Dimensions are in millimeters.
 Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.10
 Angular $\pm 2.50^\circ$
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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