ISL70100SEH, ISL73100SEH

Radiation Hardened 40V Current Sense Amplifiers

The ISL70100SEH and ISL73100SEH are radiation hardened 40V current sense amplifiers built on the Renesas proprietary PR40 SOI process. These devices have a wide power supply range of 2.7V to 40V. The input common-mode voltage is independent of the supply voltage and extends from -0.3V to 40.0V, making them ideal to use in both high-side and low-side applications.

The ISL70100SEH and ISL73100SEH are trans-conductance amplifiers that monitor current using an external sense resistor and output a current proportional to the sensed voltage. The overall voltage gain is adjustable with a single resistor from the output to ground.

These amplifiers have an extremely low offset voltage and input bias currents, making them ideal for precision sensing applications. They have a minimum bandwidth of 500kHz with a slew rate of 500µA/µs that make them useful for current feedback in telemetry applications. When the parts are powered down (V+ = V- = 0V), the sense pins (RS+, RS-) are high impedance to avoid loading the monitored circuit.

The parts are available in a hermetically sealed 10 Ld ceramic flat-pack package or die form and operate across the full-range military temperature of -55°C to +125°C.

Related Literature

For a full list of related documents, visit our website:

ISL70100SEH and ISL73100SEH product pages

Features

- Power supply range: 2.7V to 40V
- Input common-mode range: -0.3V to 40V
- Transconductance: 2µA/mV (typical)
  - ±1% accuracy (T_A = 25°C)
  - ±1.5% accuracy (T_A = -55°C, 125°C)
- Voltage offset: 10µV (typical), V+ = 12V
- Adjustable gain with a single resistor
- Radiation acceptance testing - ISL70100SEH
  - HDR (50-300rad(Si)/s): 100krad(Si)
  - LDR (<10mrad(Si)/s): 75krad(Si)
- Radiation acceptance testing - ISL73100SEH
  - LDR (<10mrad(Si)/s): 75krad(Si)
- SEE hardness (see SEE report for details)
  - No SEB (V+ = 35V): 86.4MeV•cm^2/mg
  - No SEB (V+ = 42V): 43.0MeV•cm^2/mg
- Electrically Screened to SMD 5962-20212

Applications

- High-side or low-side current sensing
- Battery monitoring
- Power management
- Motor control
- Command, telemetry, and control systems

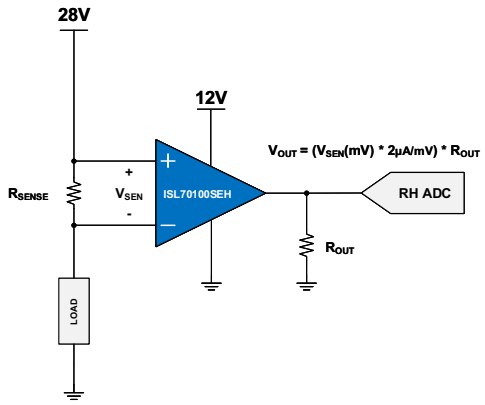


Figure 1. Typical Application: High-Side Current Sense for 28V Supply Rail

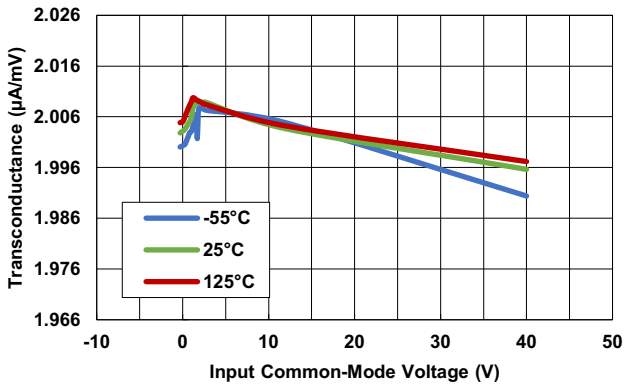


Figure 2. Transconductance, V+ = 12V

Contents

1. Overview

1.1 Block Diagram

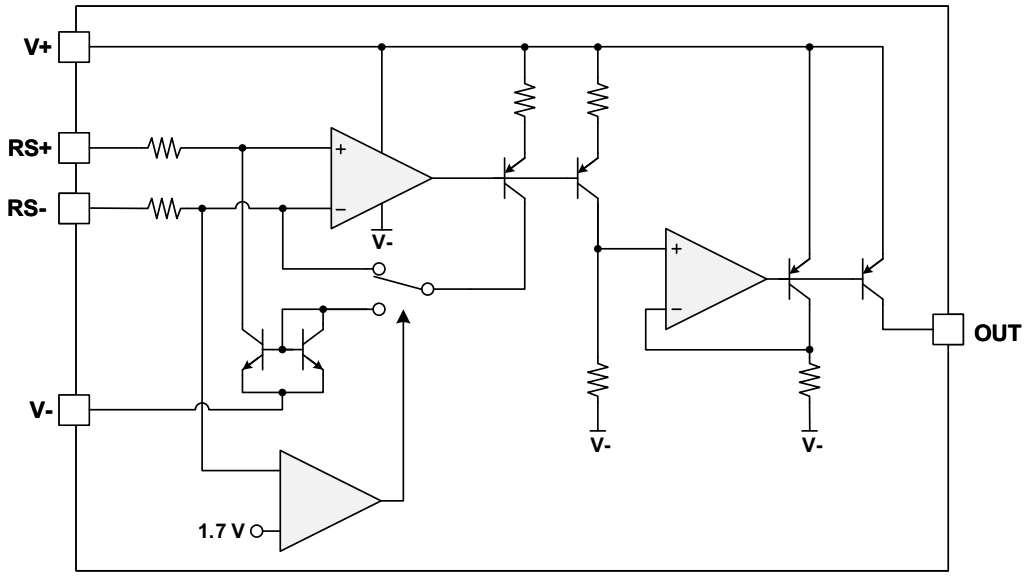


Figure 3. ISL70100SEH Block Diagram

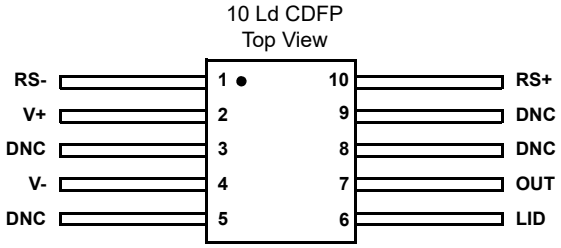
1.2 Ordering Information

Ordering SMD Number (Note 1)	Part Number (Note 2)	Radiation Hardness (Total Ionizing Dose)	Temp Range (°C)	Package (RoHS Compliant)	Package Drawing
5962R2021201VXC	ISL70100SEHVF	HDR to 100krad(Si), LDR to 75krad(Si)	-55 to +125	10 Ld FP	K10.A
5962R2021201V9A	ISL70100SEHVX (Note 3)		-55 to +125	Die	N/A
5962L2021202VXC	ISL73100SEHVF	LDR to 75krad(Si)	-55 to +125	10 Ld FP	K10.A
5962L2021202V9A	ISL73100SEHVX (Note 3)		-55 to +125	Die	N/A
N/A	ISL70100SEHF/PROTO (Note 4)	N/A	-55 to +125	10 Ld FP	K10.A
N/A	ISL70100SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	N/A
N/A	ISL73100SEHF/PROTO (Note 4)	N/A	-55 to +125	10 Ld FP	K10.A
N/A	ISL73100SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	N/A
N/A	ISL73100SEHEV1Z (Note 5)	Evaluation Board with ISL73100SEHF/PROTO			

Notes:

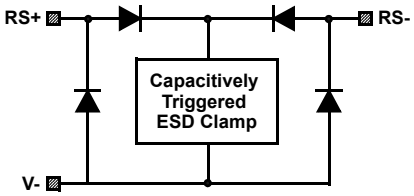
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 6.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. The evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

1.3 Pin Configurations

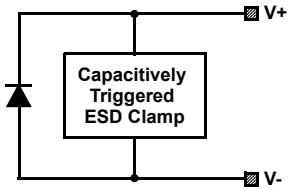


1.4 Pin Descriptions

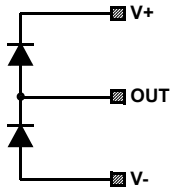
Pin Number	Pin Name	ESD Circuit	Description
1	RS-	1	Negative sense input of current sense amplifier
2	V+	2	Positive power supply
3	DNC	-	Do not connect, leave floating. This pin leaks to V-.
4	V-	-	Negative power supply
5	DNC	-	Do not connect, leave floating. This pin leaks to V-.
6	LID	-	This pin is electrically connected to the lid, connect this pin to V- to avoid floating metal. This pin does not connect to the die.
7	OUT	3	Output of the transconductance amplifier
8	DNC	-	Do not connect, leave floating. This pin leaks to V-.
9	DNC	-	Do not connect, leave floating. This pin leaks to V-.
10	RS+	1	Positive sense input of current sense amplifier



Circuit 1



Circuit 2



Circuit 3

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V+ to V-	-	42	V
Input Common Mode Voltage Range (VRS+, VRS-)	-0.3	42	V
Maximum Input Voltage Differential (RS+ to RS-)	-42	42	V
V+ to V- (Note 6)	-	35	V
Input Voltage Range (VRS+, VRS-) (Note 6)	-0.3	35	V
Maximum Input Voltage Differential (RS+ to RS-) (Note 6)	-35	35	V
V+ to V- (Note 7)	-	42	V
Input Voltage Range (VRS+, VRS-) (Note 7)	-0.3	42	V
Maximum Input Voltage Differential (RS+ to RS-) (Note 7)	-42	42	V
Maximum Differential Input Current	-	4	mA
Maximum Power Supply Ramp Rate	-	10	V/µs
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	4		kV
Charged Device Model (Tested per JS-002-2014)	2		kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Notes:

6. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg at +125°C (T_C).
7. Tested in a heavy ion environment at LET = 43MeV•cm^2/mg at +125°C (T_C).

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld CDFP Package (Notes 8, 9)	39	7

Notes:

8. θ_{JA} is measured in free air with the component mounted to a high-effective thermal conductivity test board with direct attach features. See TB379.
9. For θ_{JC}, the case temperature location is taken at the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V+ to V-	2.7	40	V
Input Common-Mode Voltage Range (from V-)	-0.3	40	V
Input Voltage Differential (RS+ to RS-)	0	150	mV
Temperature	-55	+125	°C

2.4 Electrical Specifications

2.4.1 V+ = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C.**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**		**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.966		2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.009	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930		2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.009	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-700		700	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-400	-20	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-800		700	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-400	-50	400	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV		12	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8		µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV	**-1**		**1**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-1**		**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 12V	**-0.8**		**0.8**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106		dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV			**20**	mV
Maximum Output Voltage	V_{OH}	A_V = 100, V_{SEN} = 120mV	**10.0**	10.7	**11.4**	V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**10**			V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Short-Circuit Current		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Power Supply Specifications						
Power Supply Range	V+	Assured by PSRR Test	**2.7**		**40**	V
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+		250	**400**	µA
Power Supply Rejection Ratio	PSRR	V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V	90	96		dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, Post Radiation	90	95		dB
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	**-3**	-0.17		dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)		0.8		µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output		0.32	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.25	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.90	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.80	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.25	2.50	mA/µs

2.4.2 V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified.**Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C.**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**		**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.976		2.036	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.013	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930		2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.013	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-300	400	1000	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-600		1300	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-300	320	1000	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-300	250	900	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-700		1300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-300	100	900	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV		11	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8		µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**		**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 2.7V	**-1**		**1**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106		dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV		-	**14**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 100, V_{SEN} = 27mV	**0.7**	1.4	**2.1**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = Open	**0.7**	-		V

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified.**Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω	**300**	600	**1100**	µA
Short-Circuit Current		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω	**300**	600	**1100**	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+		240	**400**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	**-3**	-0.20		dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)		0.8		µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output		0.4	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.2	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.75	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.1	2.50	mA/µs

2.4.3 V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C.**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**		**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.960		2.020	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.011	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930		2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.011	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-1200	-515	300	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-1500		600	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-1200	-650	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-1100	-365	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-1600		600	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-1100	-635	300	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV		15	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-9		µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**		**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 40V	**-0.8**		**0.8**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106		dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85			dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106		dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV			**4**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 400, V_{SEN} = 100mV	**38**	38.7	**39.4**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**38**			V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range from -55°C to +125°C; over a Total Ionizing Dose (TID) of 100krad(Si) with an exposure rate of 50-300rad(Si)/s at 25°C (ISL70100SEH only); or over a TID of 75krad(Si) with an exposure rate of <10mrad(Si)/s at 25°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 11)	Typ (Note 10)	Max (Note 11)	Unit
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Short-Circuit Current	I_{SC}	V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+		280	**420**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	**-3**	-0.21		dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)		0.8		µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output			**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.3	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.9	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.3	2.50	mA/µs

Notes:

10. Typical values shown are not guaranteed.
11. Parameters with MIN and/or MAX limits are 100% tested at -55C, +25°C and +125°C, unless otherwise specified.
12. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Curves

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified.

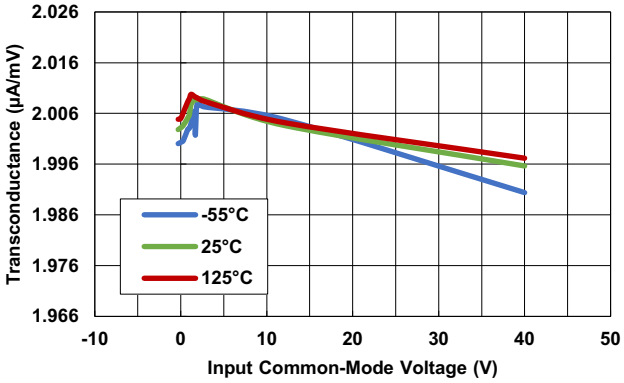


Figure 4. Transconductance, V+ = 12V

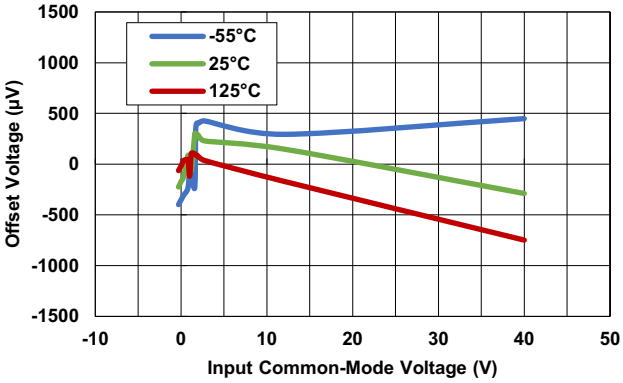


Figure 5. Common-Mode Voltage vs V_{OS}, V+ = 12V

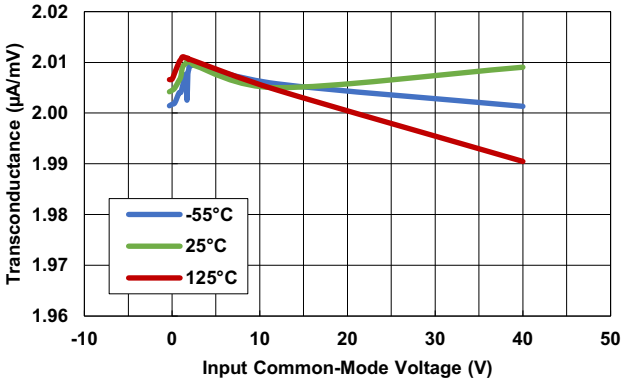


Figure 6. Transconductance, V+ = 40V

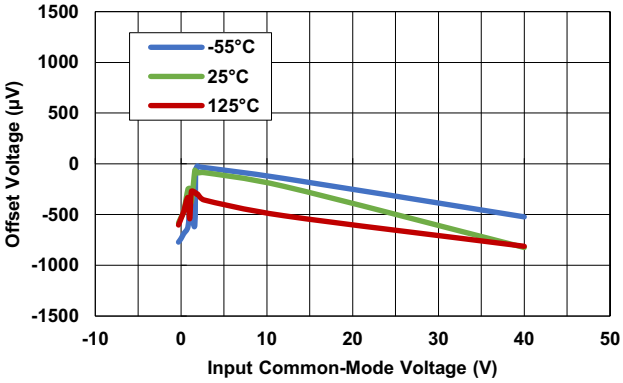


Figure 7. Common-Mode Voltage vs V_{OS}, V+ = 40V

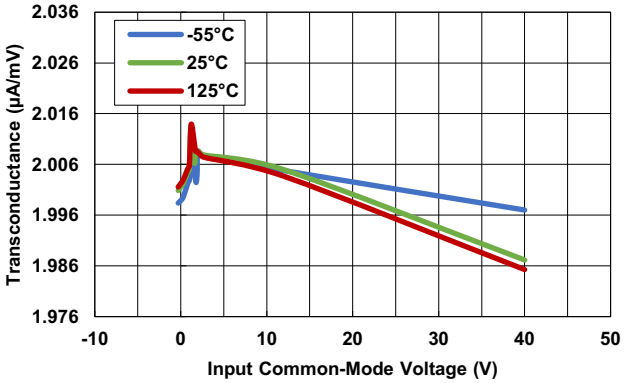


Figure 8. Transconductance, V+ = 2.7V

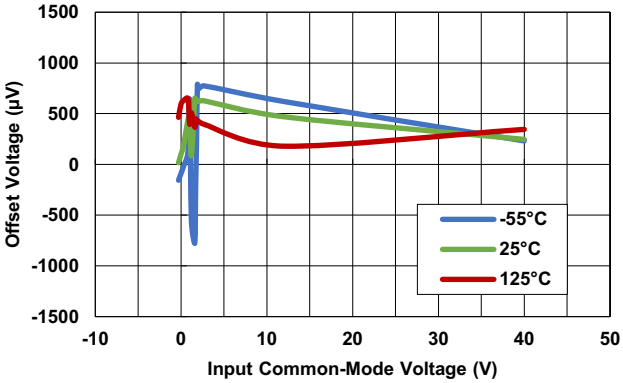


Figure 9. Common-Mode Voltage vs V_{OS}, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

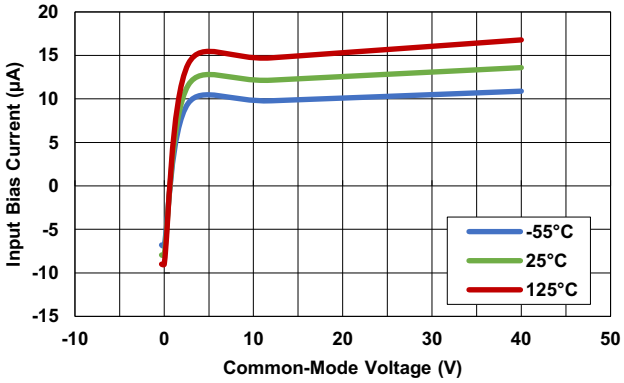


Figure 10. Input Bias Current vs VCM, V+ = 12V

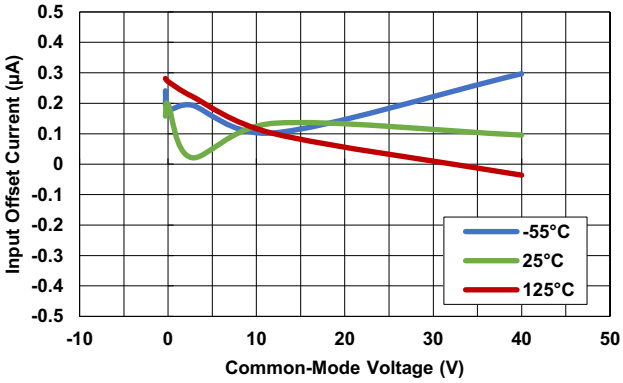


Figure 11. Input Offset Current vs VCM, V+ = 12V

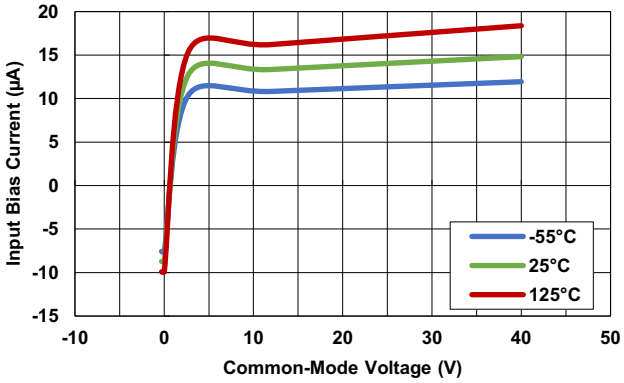


Figure 12. Input Bias Current vs VCM, V+ = 40V

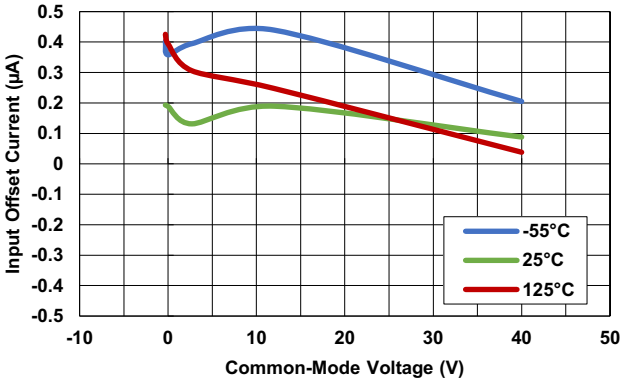


Figure 13. Input Offset Current vs VCM, V+ = 40V

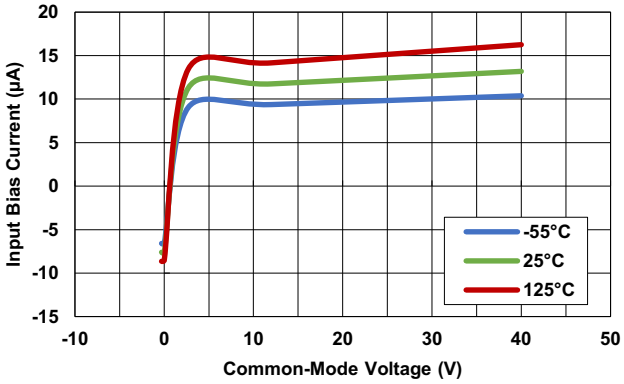


Figure 14. Input Bias Current vs VCM, V+ = 2.7V

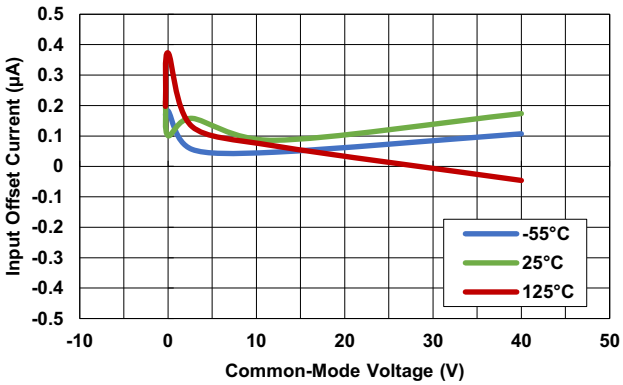


Figure 15. Input Offset Current vs VCM, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

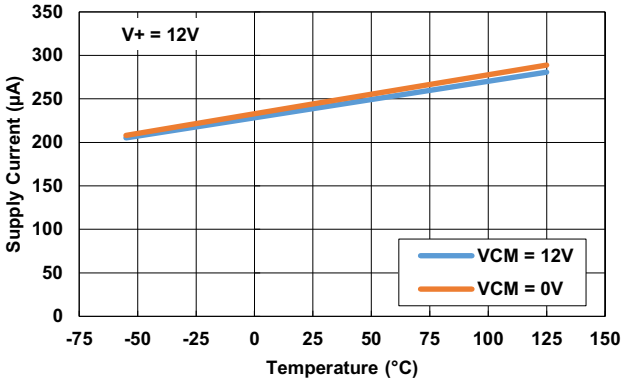


Figure 16. Supply Current, V+ = 12V

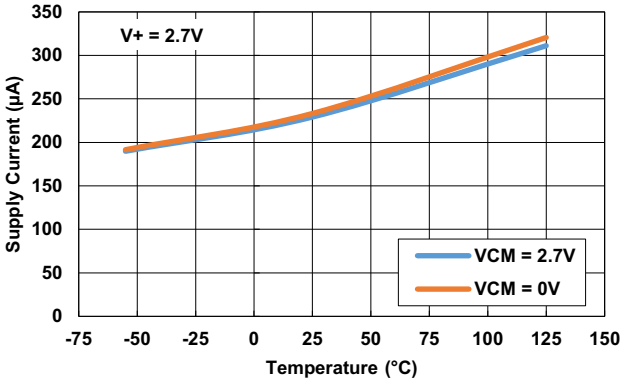


Figure 17. Supply Current, V+ = 2.7V

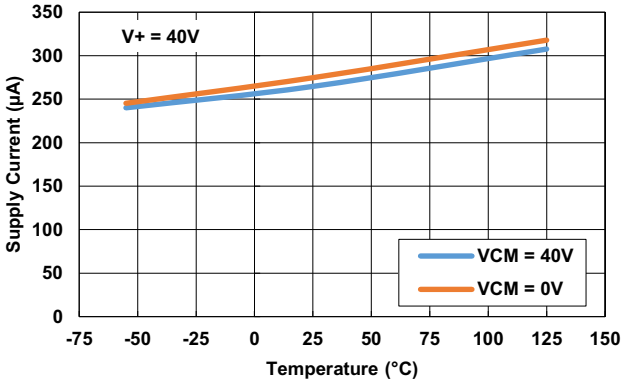


Figure 18. Supply Current, V+ = 40V

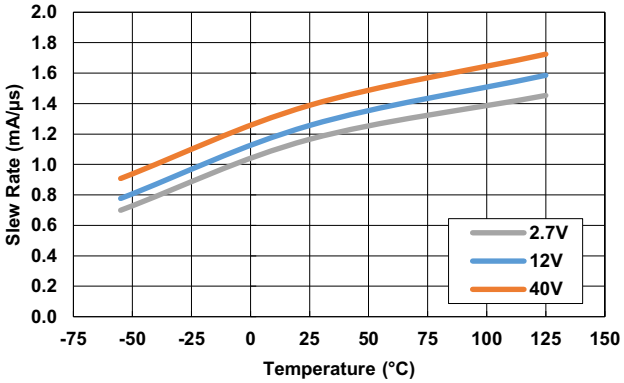


Figure 19. Slew Rate

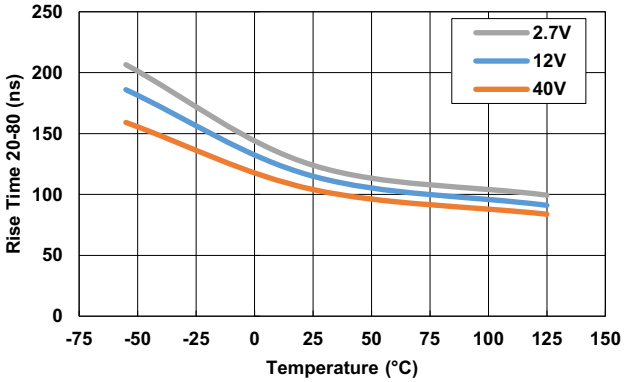


Figure 20. Rise Time

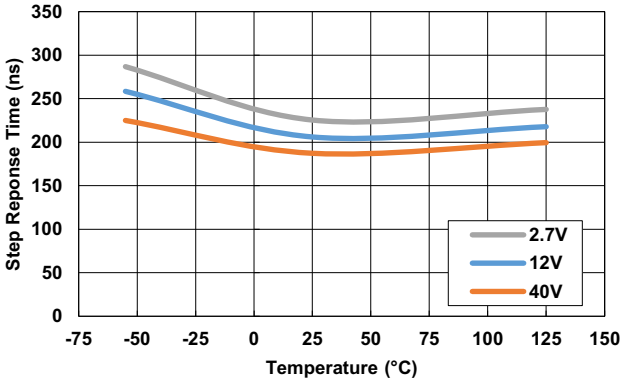


Figure 21. Step Response Time

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

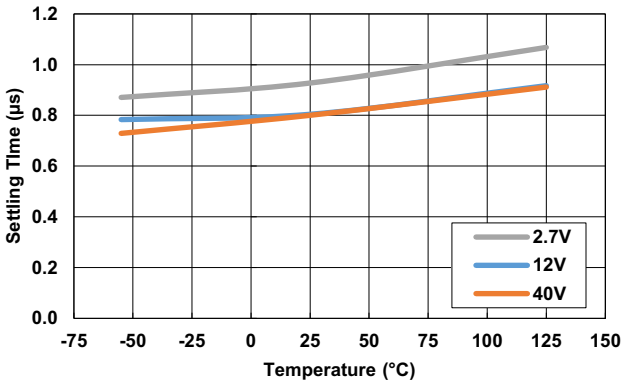


Figure 22. Settling Time

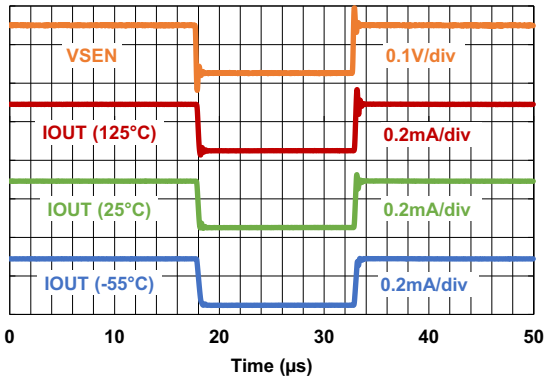


Figure 23. Input Step Response

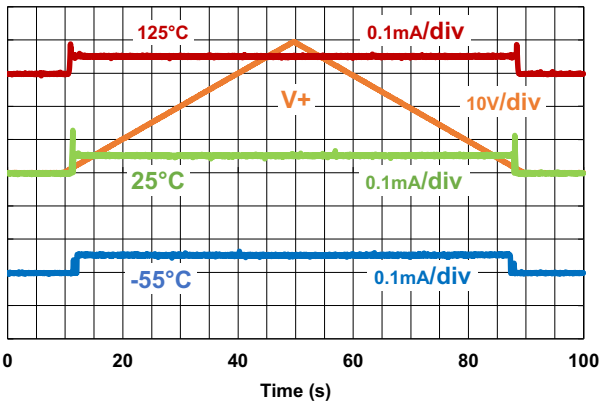


Figure 24. Power Supply Ramp at 1V/s

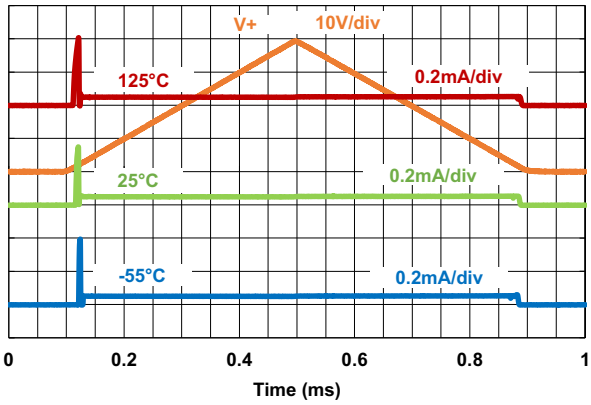


Figure 25. Power Supply Ramp at 1V/10µs

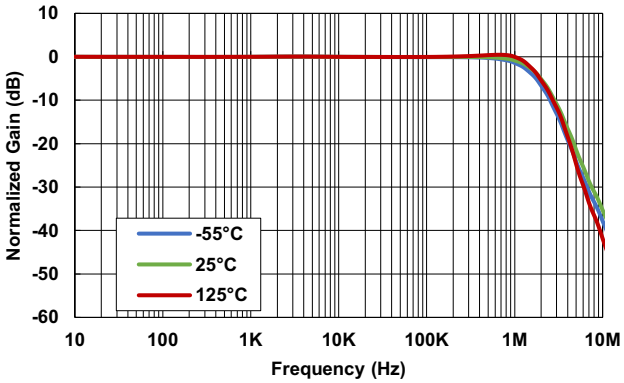


Figure 26. Normalized Gain, V+ = 12V

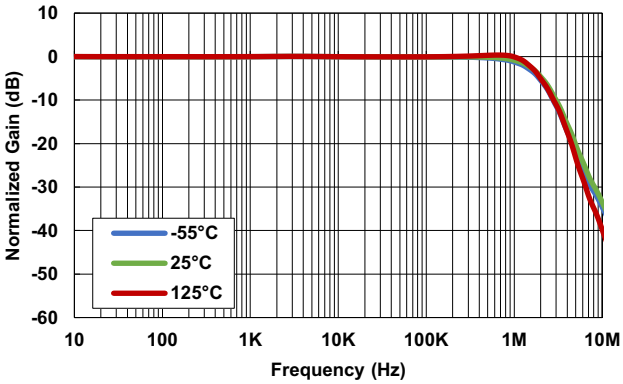


Figure 27. Normalized Gain, V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

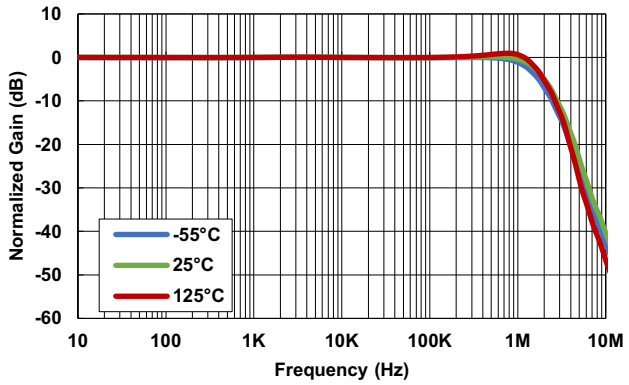


Figure 28. Normalized Gain, V+ = 2.7V

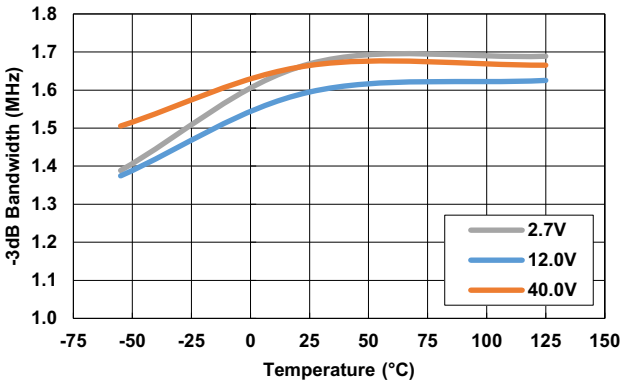


Figure 29. Bandwidth vs Temperature

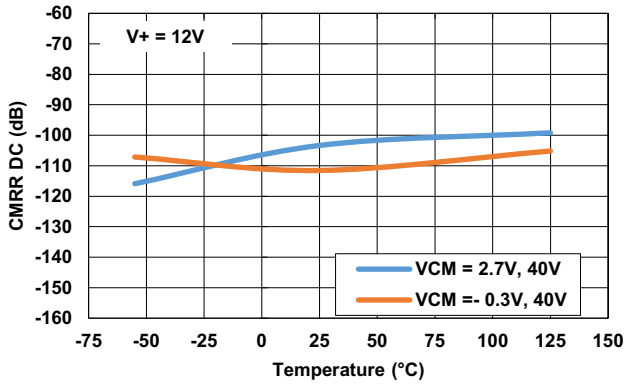


Figure 30. CMRR DC, V+ = 12V

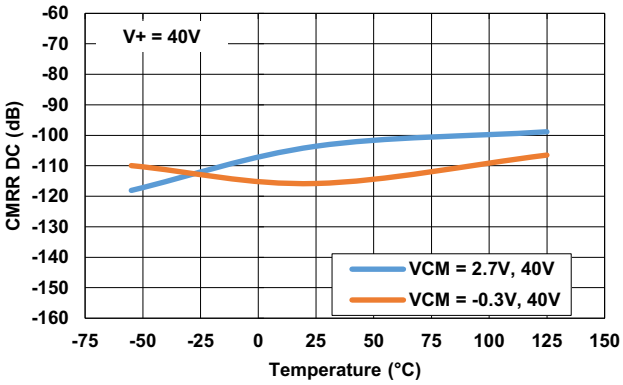


Figure 31. CMRR DC, V+ = 40V

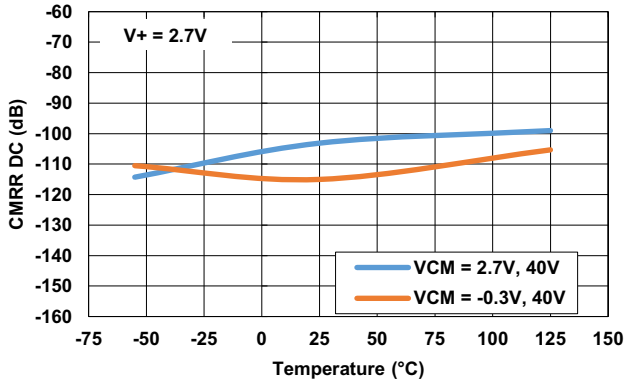


Figure 32. CMRR DC, V+ = 2.7V

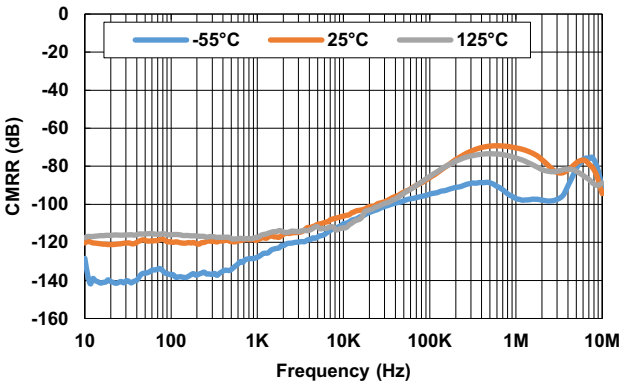


Figure 33. CMRR vs Frequency, V+ = 12V, V_{CM} = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

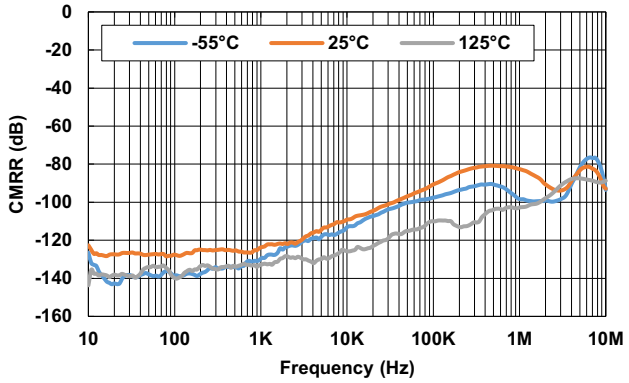


Figure 34. CMRR vs Frequency, V+ = 12V, V_{CM} = 12V

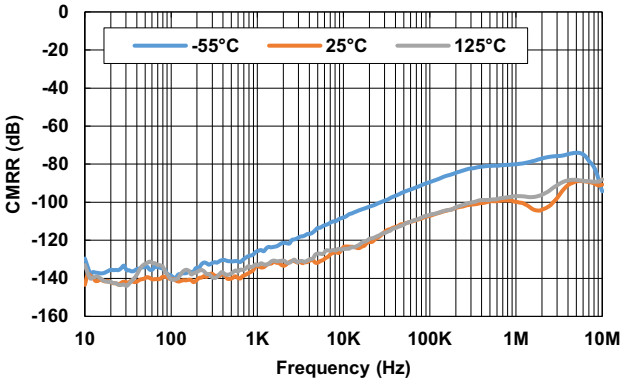


Figure 35. CMRR vs Frequency, V+ = 12V, V_{CM} = 40V

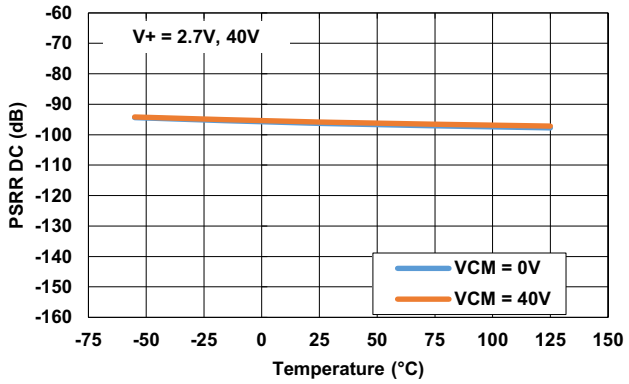


Figure 36. PSRR DC

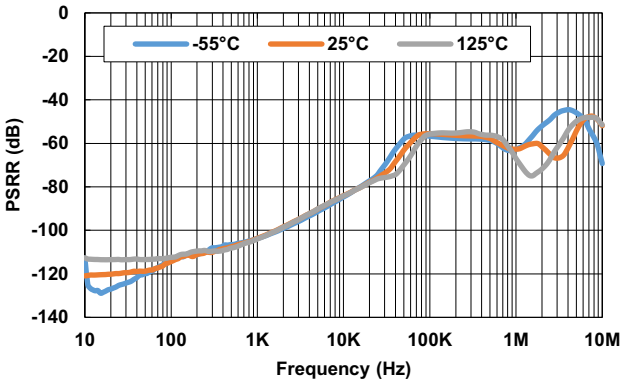


Figure 37. PSRR vs Frequency, V+ = 2.7V, V_{CM} = 12V

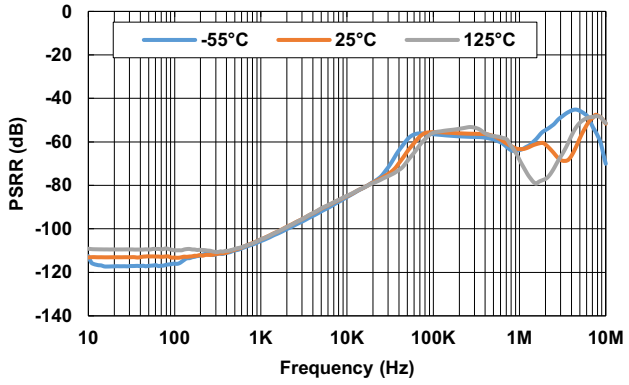


Figure 38. PSRR vs Frequency, V+ = 12V, V_{CM} = 12V

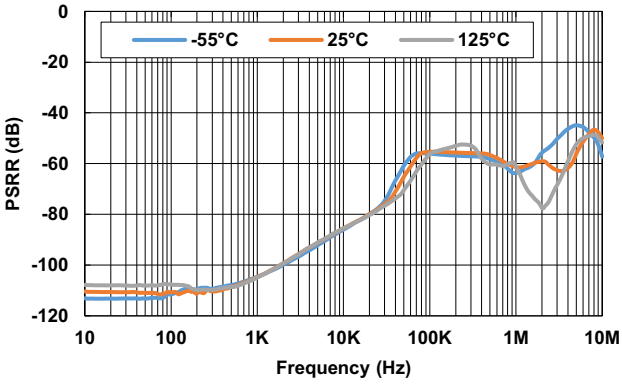


Figure 39. PSRR vs Frequency, V+ = 40V, V_{CM} = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **(Continued)**

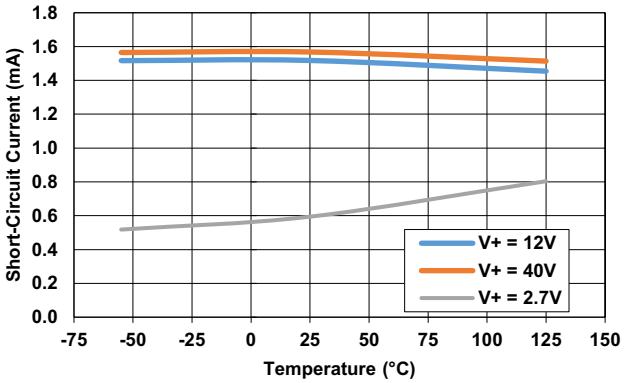


Figure 40. Short-Circuit Current

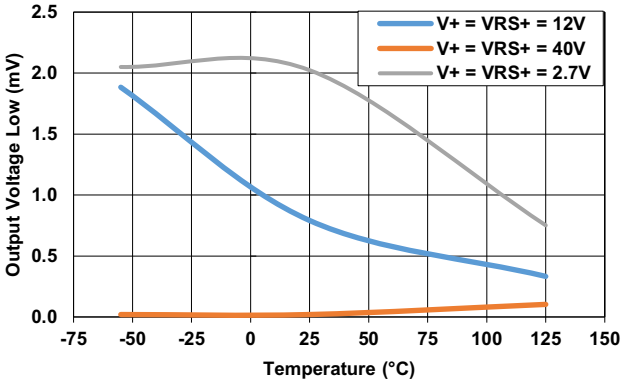


Figure 41. Output Voltage Low

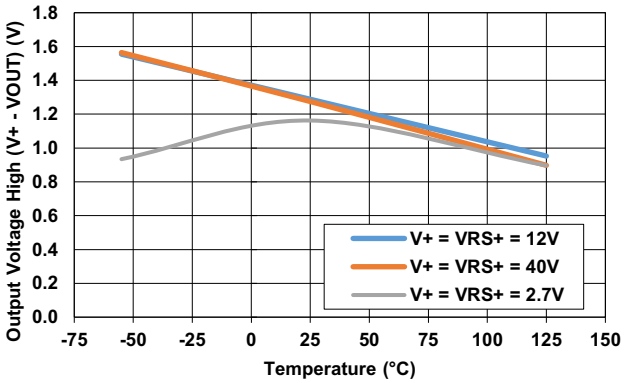


Figure 42. Output Voltage High (Referred to V+)

4. Functional Description

The ISL70100SEH is a transconductance current sense amplifier with a power supply range of 2.7V to 40V. Its input common-mode range extends from -0.3V to 40V, which makes it ideal for use in both low-side and high-side applications. The input common-mode voltage is independent of the power supply such that the ISL70100SEH can be powered of a 5V rail but sense a 40V common mode. The ISL70100SEH level shifts in the sensed voltage from the sensed power supply to a ground-referenced output. The output gain of the ISL70100SEH can be easily configured with a single resistor on the output. It outputs a current proportional to the input voltage differential and the output resistor sets the voltage gain seen by downstream devices.

The ISL7x100SEH can be driven with bi-polar supplies with the positive voltage on V+ and the negative voltage on V-. The same voltage differentials should still be between 2.7V and 40V from V+ to V-. The output of the amplifier is referenced to V- so any downstream device will need to be able to handle a bipolar input.

4.1 Output Signal Range

The output range of these amplifiers is limited on the low end by the input offset voltage and the saturation voltage of the output transistors on the top end. The maximum voltage is always about 2V below the voltage on V+. If the application calls for a large gain, the supply voltage may need to be increased to accommodate the full output voltage range. For example, if the supply voltage is 2.7V, the output can only get up to 0.7V before the output is saturated; this sets the maximum gain with 2.7V supply to 4.67 with a maximum sensing voltage of 150mV. If the sensing voltage range is reduced, higher gains can be used.

(EQ. 1) $$A_{CSA(MAX)} = \frac{(V+) - V_{OH}}{V_{SEN(MAX)}}$$

where:

- $A_{CSA(MAX)}$ is the maximum output gain given the maximum input differential
- V+ is the power supply voltage of the ISL7x100SEH in volts
- V_{OH} is output high saturation voltage referred to V+ from the electrical specifications table in volts
- $V_{SEN(MAX)}$ is the maximum input differential that the application calls for in volts

Typically, the output of the ISL7x100SEH is connected to the input of an Analog-to-Digital Converter (ADC), which has limited input voltage ranges. Ensure that the output voltage ($I_{OUT(MAX)} \bullet R_{OUT}$) does not exceed the input voltage range of the downstream ADC.

4.2 Input Common-Mode Range

The input common-mode range of the ISL70100SEH and ISL73100SEH ranges from -0.3V to 40V regardless of the voltage on V+. The electrical specifications table shows that the offset voltage of these amplifiers changes very slightly over the full common-mode range. The inputs are also capable of either RS+ or RS- dropping to 0V without damaging the amplifier, this is particularly useful in monitoring protection fuse circuits where the output goes to the positive rail if the fuse is blown. If the inputs differential is reversed (RS- goes above RS+), the output does not phase invert, it will simply remain at the output low voltage specified in the electrical specifications table.

4.3 Crossover Region

The ISL7x100SEH accomplishes the wide input common-mode range using multiple input paths that are selected based on the common-mode voltage. The transition point between the high-side and low-side is typically 1.7V but can range from 1.5V to 2.0V across temperature. When the common-mode voltage has reached the transition point, there is a soft switchover from the low-side to the high-side.

4.4 Sources of Error

4.4.1 Input Impedance of Downstream Devices

The value of the output resistance is not critical if the circuit that is being driven has a high input impedance. If the driven circuit has a low input impedance, the accuracy of V_{OUT} is reduced. Using an example where the input impedance is 100 times larger than the output resistance. It can be seen that the accuracy drops by 1%.

(EQ. 2) $$V_{OUT} = I_{OUT} \times \frac{R_{OUT} \times R_{IN}}{R_{OUT} + R_{IN}} = I_{OUT} \times \frac{100}{101} = I_{OUT} \times R_{OUT} \times 0.99$$

where:

- V_{OUT} is the output voltage in volts
- I_{OUT} is the output current in amps
- R_{OUT} is output resistance loading the output of the ISL7x100SEH in ohms
- R_{IN} is the input impedance of the downstream device in ohms

4.4.2 Input Offset Voltage

The dynamic range of the ISL7x100SEH is inversely proportional to the input offset voltage. The dynamic range can be thought of as the maximum sense voltage divided by V_{OS}. These amplifiers have an offset voltage of 10µV typically. The electrical specification table shows how the offset voltage can vary across various operating points.

4.4.3 Input Bias and Offset Current

A typical current sense amplifier has the ability to change its transconductance by changing the input resistors. In this case, the input bias currents and offset currents can induce more error on top of the offset voltage. The ISL7x100SEH gets around this by internalizing these input resistors and trimming out the error associated with them during production.

4.4.4 Sensed Current Error

The effective current error can be determined with Equation 3. It shows the amount of current that the current-sense amplifier is blind to.

(EQ. 3) $$I_{ERROR} = \frac{V_{OS}}{R_{SENSE}}$$

where:

- V_{OS} is the offset voltage in µV.
- R_{SENSE} is the sense resistor in mΩ.
- I_{ERROR} is the current error in mA.

The R_{SENSE} can be increased to lower the current error, but this reduces the maximum current that can be sensed and increases power dissipation. Careful consideration must be made to balance power dissipation and accuracy.

5. Applications Information

5.1 Selection of the External Current-Sense Resistor

To pick the current-sense resistor value, a decision has to be made between power dissipation and measurement accuracy. As a general rule for all applications, the sense resistor should be as small as possible while still providing adequate input dynamic range across the operating range. The minimum accurately sensed input voltage is primarily limited by the offset voltage of the ISL70100SEH.

The sense resistor value can be calculated once the maximum sensed load current is determined. The maximum recommended sense voltage for the ISL70100SEH is 150mV, so dividing that by the maximum load current provides the sense resistor value.

$$R_{SENSE} = \frac{150mV}{I_{OUT(MAX)}} \quad \text{(EQ. 4)}$$

where:

- R_{SENSE} is the sense resistor in mΩ.
- $I_{OUT(MAX)}$ is the maximum expected load current to be sensed in amps.

5.2 Gain Setting

The gain on the ISL70100SEH can be adjusted using a single resistor on the output. The ISL70100SEH outputs 2µA for every 1mV of differential across the inputs. Equation 5 can be used to calculate the output load resistance to get a specific gain:

$$R_{OUT} = \frac{A_{CSA}}{g_m} \quad \text{(EQ. 5)}$$

where:

- R_{OUT} is the output load resistance in kΩ.
- A_{CSA} is desired voltage gain.
- g_m is the transconductance of the ISL70100SEH which is 2µA/mV (typical).

5.3 Selection of Output Resistor

The output signal is a current conducted through the output resistor to generate a voltage. With a maximum input range of 150mV, the output current is 300µA. The voltage gain should be determined based on the input voltage range of the downstream device. For example, if there is a 5V ADC on the output of the ISL7x100SEH, the output resistance should be 16.6kΩ to ensure that V_{OUT} stays under 5V. This also means that the minimum power supply voltage has to be 7V to achieve 5V on the output. Renesas recommends using resistors that have a low temperature coefficient on the output as it adds error to the measurement.

5.4 Output Filtering

Because the output of these amplifiers is a current source, filtering is straight forward. A capacitor can be placed in parallel to the output resistance to create a pole based on Equation 6:

$$f_{-3dB} = \frac{1}{2 \times \pi \times R_{OUT} \times C_{OUT}} \quad \text{(EQ. 6)}$$

where:

- f_{-3dB} is frequency location of the pole in hertz
- R_{OUT} is the output resistance in ohms
- C_{OUT} is the output capacitance in parallel with R_{OUT} in farads

5.5 Response Time

The ISL7x100SEH is designed to provide fast response time for circuit protection or signal transmission. The delay and speed of the response depend on the starting point of the step. If the sensed current is very low (near zero) before the transient, there may be an increased delay time to see the output react. If fast reaction times are required, increase the sense resistance such that there are a few millivolts (1-5mV) of differential across the inputs under the lowest current condition. The higher the differential is for the lowest current condition, the faster the response time is, but that results in increased DC power losses.

Figures 43 and 44 show the step response difference from starting with a 0mV differential versus starting with a 25mV differential. For most applications the 40-50ns faster reaction time may not warrant the resulting power loss.

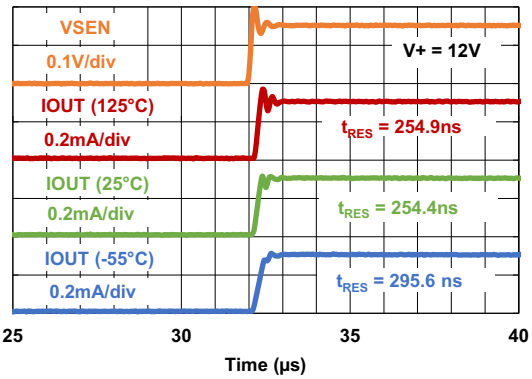


Figure 43. 0mV to 150mV Step Response

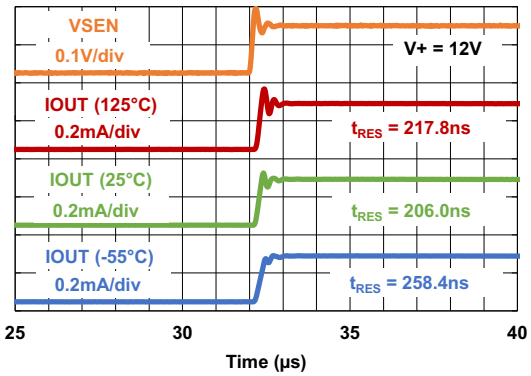


Figure 44. 25mV to 150mV Step Response

6. Die Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2413µm x 3302µm (95 mils x 130 mils) Thickness: 483µm ± 25µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: 15kÅ Nitrox
Top Metallization	Type: 30kÅ AlCu (99.5%/0.5%)
Backside Finish	Silicon
Process	PR40
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	$<2 \times 10^5 A/cm^2$
Transistor Count	560
Weight of Packaged Device	0.3916 grams
Lid Characteristics	Finish: Gold Potential: Tied to package Pin 6 (Lid)

6.1 Metallization Mask Layout

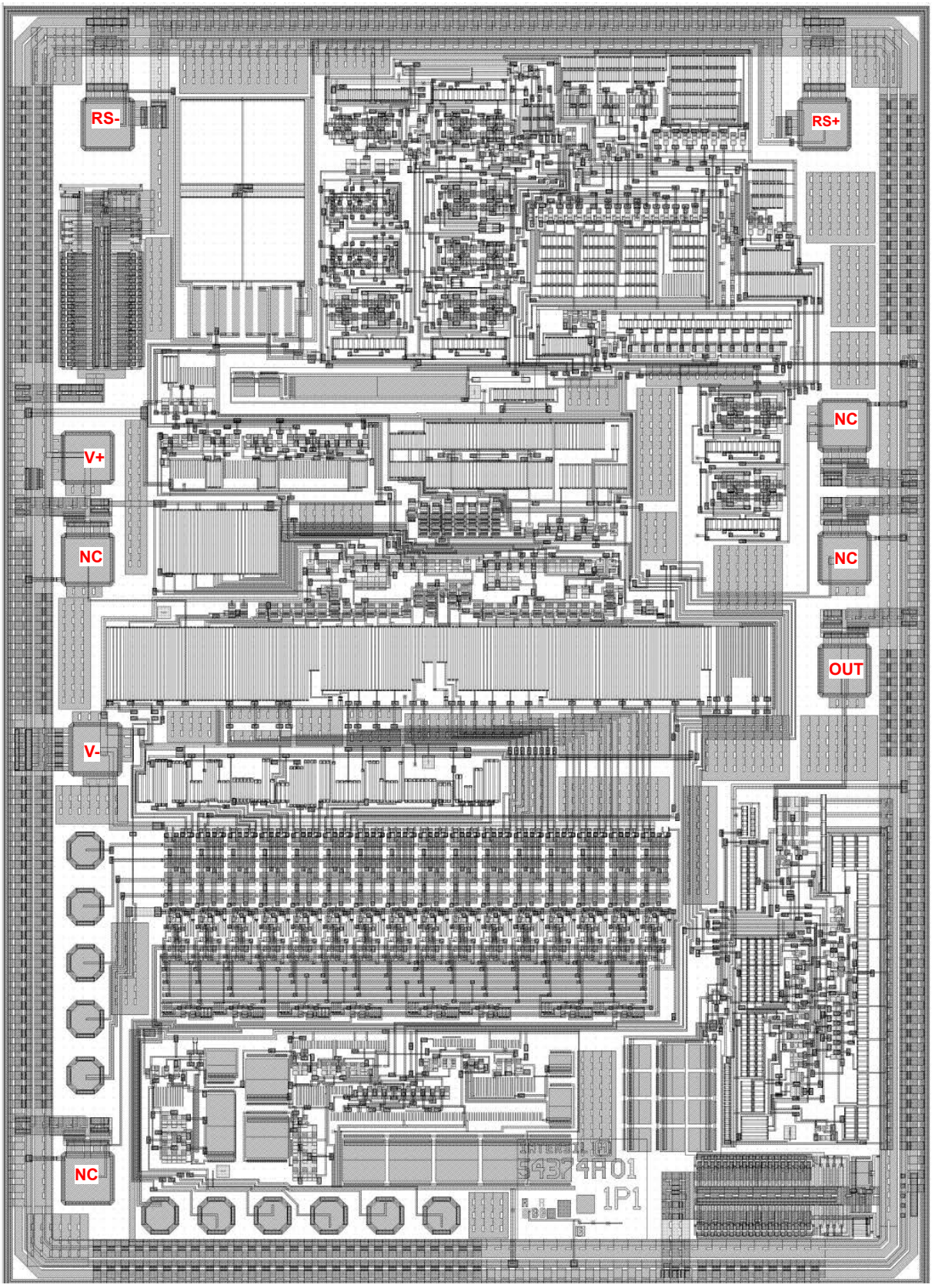


Table 2. Die Layout X-Y Coordinates

Pad Name	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
RS-	110	110	-891.0	1302.5
V+	110	110	-941.0	472.5
NC	110	110	-941.0	219.5
V-	110	110	-921.5	-252.5
NC	110	110	-941.0	-1320.5
OUT	110	110	941.0	-57.0
NC	110	110	941.0	223.0
NC	110	110	941.0	553.0
RS+	110	110	891.0	1302.5

Note: Origin of coordinates is the center of the die.

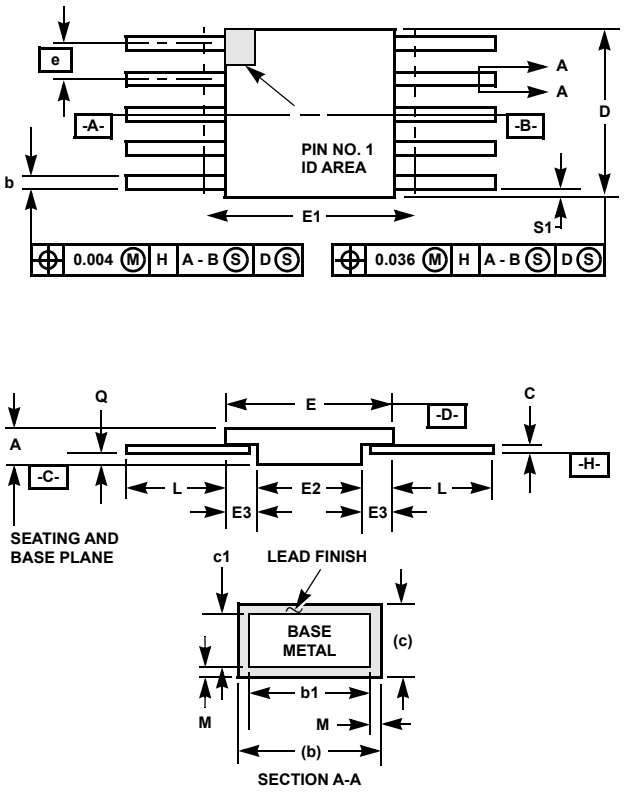
7. Revision History

Rev.	Date	Description
1.01	Jul.10.20	Updated the Maximum Input Voltage Differential minimum specifications in the Absolute Maximum Ratings section to align with SMD.
1.00	Jun.3.20	Initial release

8. Package Outline Drawing

For the most recent package outline drawing, see K10.A.

K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

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Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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