ISL71043M, ISL71041M

Radiation Tolerant Single-Ended Current Mode PWM Controllers

The ISL71043M and ISL71041M are PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Fast signal propagation and output switching characteristics make these ideal products for existing and new designs.

Features include up to 13.2V operation, 2.9mA operating current, 90µA typical start-up current, adjustable operating frequency to 1MHz and, 1A current drive capability with 35ns rise and 29ns fall times.

The ISL71041M and ISL71043M are available in an 8 LD TDFN package and the ISL71043M is also available in an 8 LD SOIC package. Both packages are specified across the extended temperature range of -55°C to +125°C.

Applications

- Current mode switching power supplies
- Isolated buck and flyback regulators
- Boost regulators
- Direction and speed control in motors
- Control of high current FET drivers

Features

- 1A MOSFET gate driver
- 90µA typical start-up current, 125µA maximum
- 35ns propagation delay current sense to output
- Fast transient response with Peak Current mode control
- 9V to 13.2V operation
- Adjustable switching frequency to 1MHz
- 35ns rise time and 29ns fall time with 1nF output load
- Trimmed timing capacitor discharge current for accurate dead time/maximum duty cycle control
- 1.5MHz bandwidth error amplifier
- Tight tolerance voltage reference over line, load, and temperature
- ±3% current limit threshold
- Ni/Pd/Au-Ag lead finish (Sn-free, Pb-free)
- TID Radiation Lot Acceptance Testing (LDR: ≤10mrad(Si)/s)
    - ISL71041M30RTZ: 30krad(Si)
    - ISL71041M50RTZ: 50krad(Si)
- SEE Characterization
    - No DSEE for VDD = 14.7V and 43MeV•cm^2/mg
    - SET only lasted one PWM pulse

Table 1. Key Differences Between Family of Parts

Part Number	Rising UVLO (V)	Maximum Duty Cycle (%)	Packages Available
ISL71041M	7.0	50	8 Ld TDFN
ISL71043M	8.4	100	8 Ld TDFN, 8 Ld SOIC

Contents

1. Overview

1.1 Typical Application Schematics

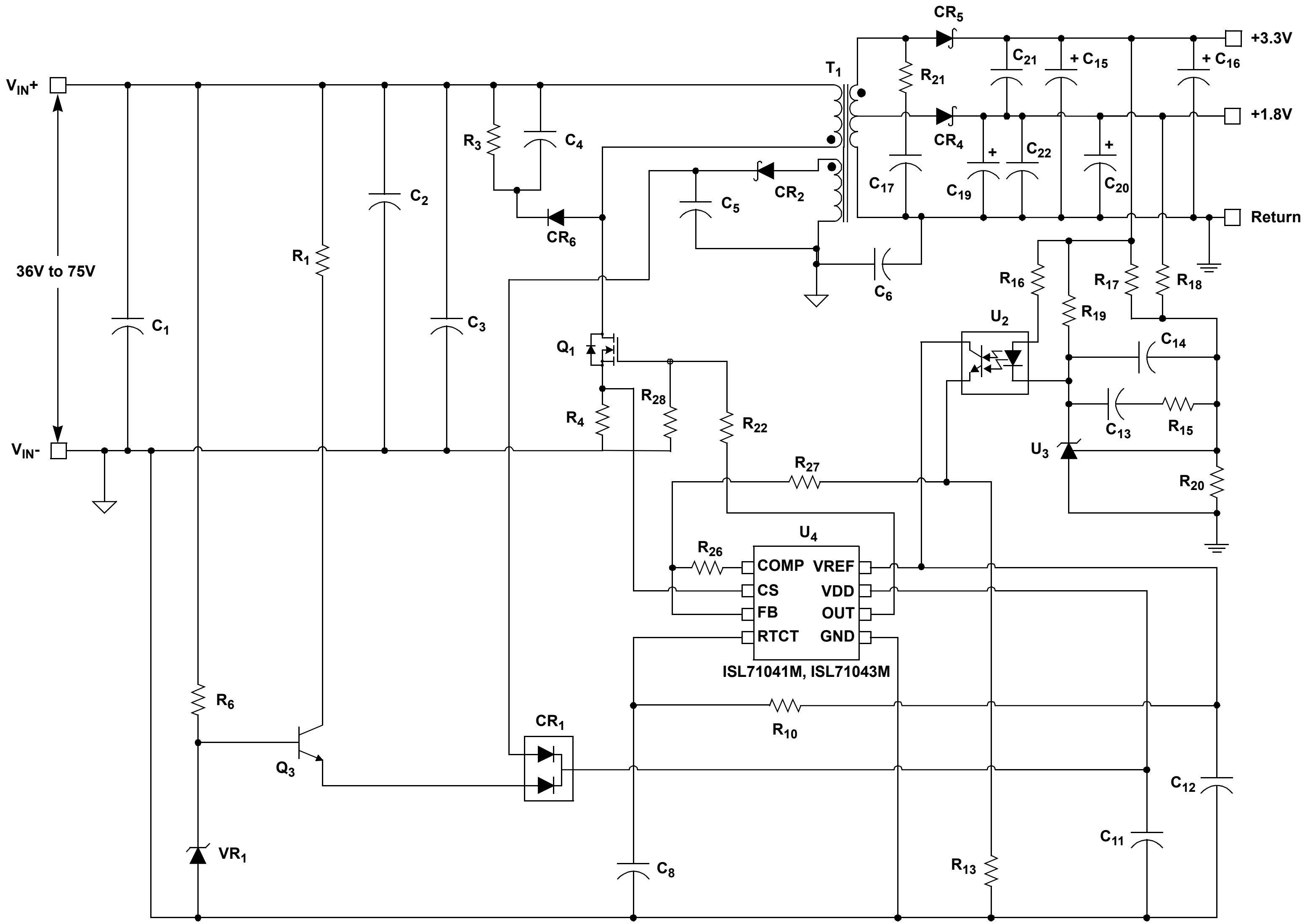


Figure 1. 48V Input Dual Output Flyback

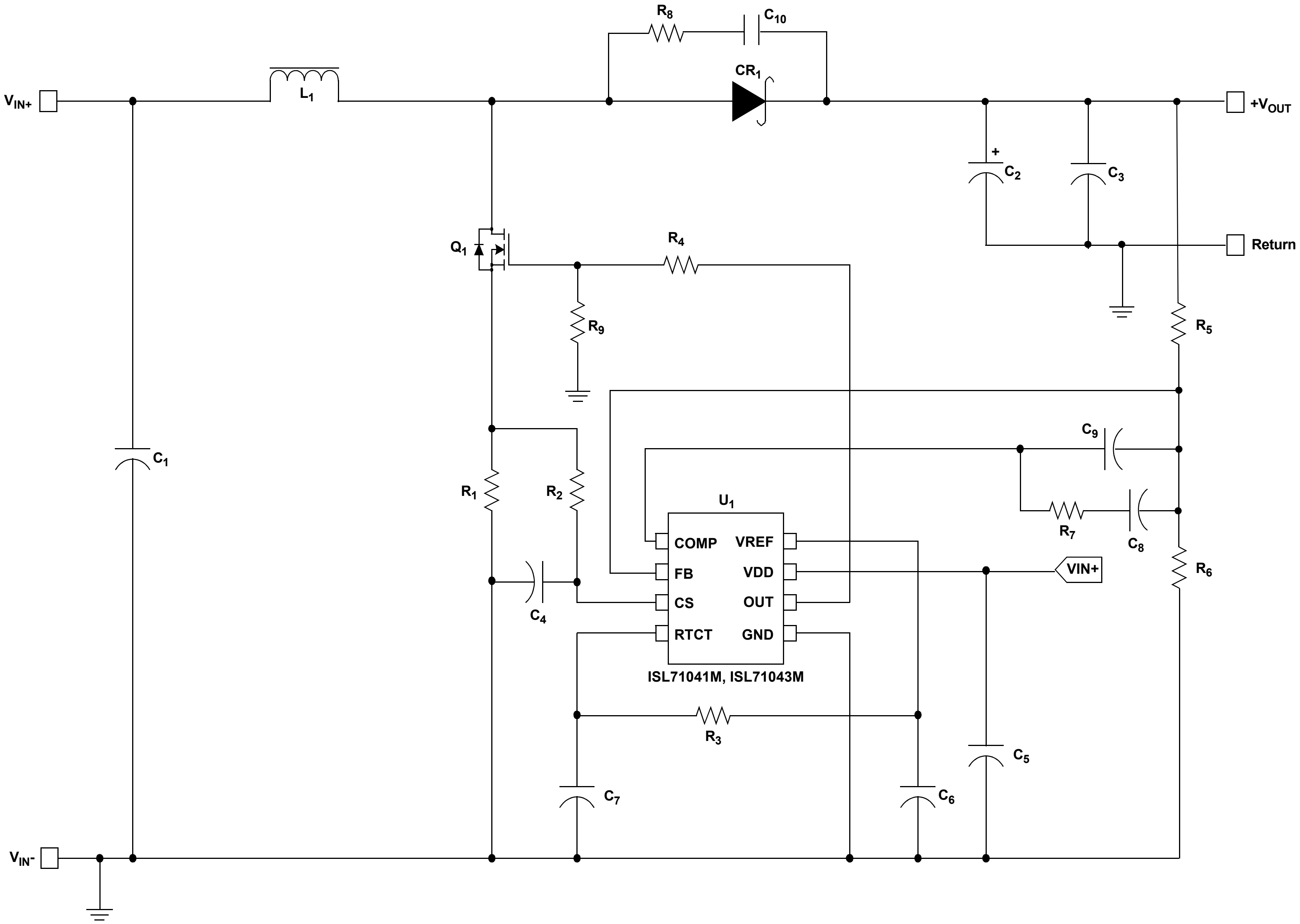


Figure 2. Boost Converter

1.2 Functional Block Diagram

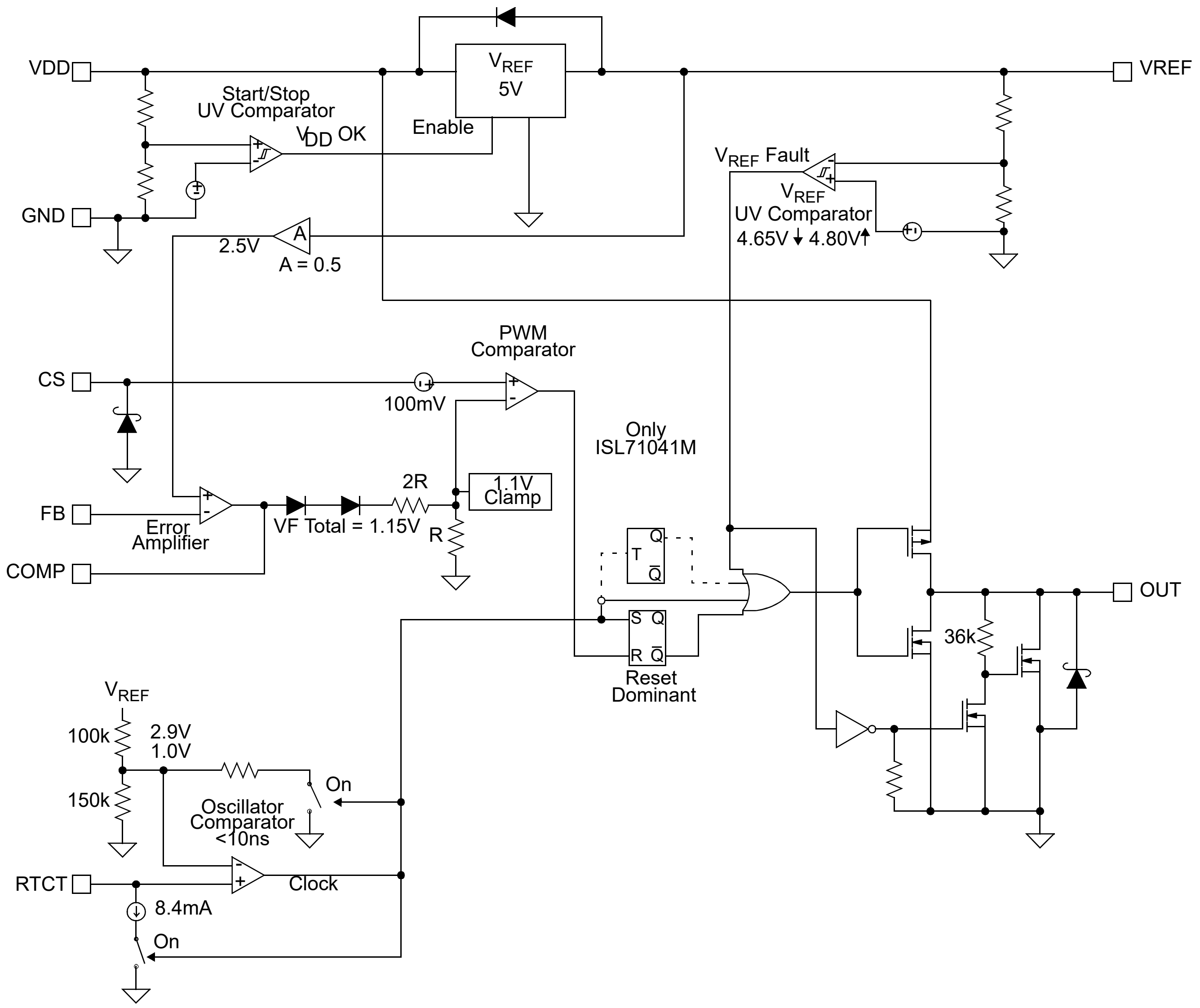
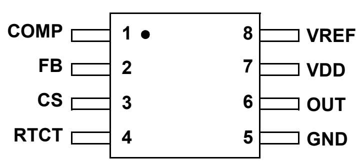


Figure 3. Block Diagram

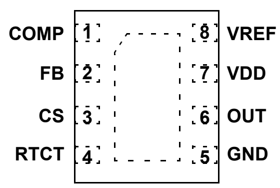
2. Pin Information

2.1 Pin Assignments

8 Ld NSOIC
Top View



8 Ld TDFN
Top View



2.2 Pin Descriptions

Pin #	Pin Name	Description
1	COMP	The output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.
2	FB	The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The noninverting input of the error amplifier is internally tied to a reference voltage.
3	CS	The current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.
4	RTCT	The oscillator timing control pin. Set the operational frequency and maximum duty cycle by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 1.0MHz. The charge time, t_C, the discharge time, t_D, the RTCT oscillator frequency, f, and the maximum duty cycle, D_{MAX}, can be approximated using Equation 1 through Equation 4: (EQ. 1) $t_C \approx 0.56 \times RT \times CT$ (EQ. 2) $t_D \approx 30 \times 10^{-9} + \frac{1.8 \times CT}{0.008 - \frac{3.125}{RT}}$ (EQ. 3) $f = 1/(t_C + t_D)$ (EQ. 4) $D = t_C \times f$ The equations have increased error at higher frequencies due to propagation delays. Figure 4 can be used as a guideline in selecting the capacitor and resistor values required for a given oscillator frequency for the ISL71041M and ISL71043M. Use the spreadsheet calculator tool on the product page to estimate the switching frequency from typical bench test data.
5	GND	GND is the power and small signal reference ground for all functions.
6	OUT	The drive output to the power switching device. This high current output is able to drive the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.
7	VDD	The power connection for the device. The total supply current depends on the load applied to OUT. The total I_{DD} current is the sum of the operating current and the average output current. Use the operating frequency, f, and the MOSFET gate charge, Qg, to calculate the average output current using Equation 5: (EQ. 5) $I_{OUT} = Qg \times f$ To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.
8	VREF	The 5.00V reference voltage output. ±2% tolerance over line, load, and operating temperature. The recommended bypass to GND capacitor is in the range 0.1µF to 0.22µF. A typical value of 0.15µF can be used.
-	EPAD	Applicable to TDFN package only. The exposed pad should be connected externally to GND. Put as many vias as possible in this pad connecting to other PCB layers to improve heat dissipation.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V_{DD}	GND - 0.3	+30.0	V
V_{DD} [1]	GND - 0.3	+14.7	V
OUT	GND - 0.3	V_{DD} + 0.3	V
Signal Pins	-	6.0	V
Peak Current on OUT	-	1	A
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	1.5	kV
Machine Model (Tested per JESD22-A115C)	-	200	V
Charged Device Model (Tested per JS-002-2014)	-	1	kV
Latch-Up (Tested per JESD-78E; Class 2, Level A) at 125°C	-	100	mA

1. Tested in a heavy ion environment at LET = 43MeV•cm^2/mg at +125°C (TC) for SEB.

3.2 Outgas Specifications

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Loss[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirement soft total mass loss <1% and collected volatile condensible material of <0.1%.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld SOIC Package	θ_{JA}[1]	Junction to ambient	105	°C/W
		θ_{JC}[2]	Junction to case	50	
	8 Ld 4x4 TDFN Package	θ_{JA}[3]	Junction to ambient	41	
		θ_{JC}[4]	Junction to case	2.5	

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
2. For θ_{JC}, the case temperature location is the package top center.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
4. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V_{DD}	9	13.2	V
Temperature	-55	+125	°C

3.5 Electrical Specifications

Recommended operating conditions unless otherwise noted. V_{DD} = 13.2V, R_T = 10kΩ, C_T = 3.3nF, T_A = -55°C to +125°C. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Undervoltage Lockout						
Start Threshold	$UVLO\_V_{START}$	ISL71041M	**6.5**	7.0	**7.5**	V
Start Threshold		ISL71043M	**8.0**	8.4	**9.0**	V
Stop Threshold	$UVLO\_V_{STOP}$	ISL71041M	**6.1**	6.7	**6.9**	V
Stop Threshold		ISL71043M	**7.3**	7.6	**8.0**	V
Hysteresis	UVLO_Hyst	ISL71041M	-	0.4	-	V
Hysteresis		ISL71043M	-	0.8	-	V
Start-Up Current, I_{DD}	I_{DDSu}	V_{DD} < Start Threshold	-	90	**125**	µA
Operating Current, I_{DD}	I_{DDOp}		-	2.9	**4.0**	mA
Operating Supply Current, I_D	IDO_{p_LOAD}	Includes 1nF GATE loading	-	4.7	**5.5**	mA
	I_{DDq}	[2]	-	2.9	**4.0**	mA
Reference Voltage						
Overall Accuracy	V_{REF}	Over line (V_{DD} = 9V to 13.2V), load of 1mA and 10mA	**4.925**	5.0	**5.050**	V
Long Term Stability [3]	V_{REF_ST}	T_A = +125°C, 1000 hours	-	5	-	mV
Current Limit, Sourcing	I_{SOURCE}		**-20**	-40	-	mA
Current Limit, Sinking	I_{SINK}		**5**	20	-	mA
Current Sense						
Input Bias Current	CS_I_{BIAS}	V_{CS} = 1V	**-1.0**	-	**1.0**	µA
Input Signal, Maximum	VMAX_IN		**0.97**	1.00	**1.03**	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	COMP_Gain	0 < V_{CS} < 910mV, V_{FB} = 0V	**2.75**	2.82	**3.15**	V/V
CS to OUT Delay	TPCStoOUT		-	35	**60**	ns
Error Amplifier						
Open Loop Voltage Gain	AVOL		-	90	-	dB
Unity Gain Bandwidth	UGB		-	1.5	-	MHz
Reference Voltage, V_{REF}	EA_V_{REF}	$V_{FB} = V_{COMP}$	**2.475**	2.5	**2.530**	V
FB Input Bias Current, FBI_{IB}	FB_I_{BIAS}	V_{FB} = 0V	**-1.5**	-0.2	**1.5**	µA
COMP Sink Current	$COMP\_I_{OL}$	V_{COMP} = 1.5V, V_{FB} = 2.7V	**1.0**	5	-	mA
COMP Source Current	$COMP\_I_{OH}$	V_{COMP} = 1.5V, V_{FB} = 2.3V	**-0.4**	-0.5	-	mA
COMP V_{OH}	$COMP\_V_{OH}$	V_{FB} = 2.3V	**4.80**	-	**V_{REF}**	V

Recommended operating conditions unless otherwise noted. V_{DD} = 13.2V, R_T = 10kΩ, C_T = 3.3nF, T_A = -55°C to +125°C. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
COMP V_{OL}	COMP_V_{OL}	V_{FB} = 2.7V	**0.4**	-	**1.0**	V
Power Supply Rejection Ratio	PSRR	Frequency = 120Hz, V_{DD} = 9V to 13.2V	-	80	-	dB
Oscillator						
Frequency Accuracy	Freq_V_{MAX}	Initial, T_A = +25°C	48	51	54	kHz
Frequency Variation with V_{DD}	Freq_PSRR	T_A= +25°C, $(f_{13.2V} - f_{9V})/f_{12V}$	-1.0	0.2	1.0	%
Temperature Stability[3]			-	5	-	%
Amplitude, Peak-to-Peak	RTCTVpp	Static Test	-	1.75	-	V
RTCT Valley Voltage	$RTCTV_{DIS}$	Static Test	-	1.0	-	V
Discharge Current	$RTCTI_{DIS}$	RTCT = 2.0V	**6.5**	7.8	**8.5**	mA
Output						
Gate V_{OH}[4]	V_{OH}	V_{DD} to OUT, I_{OUT} = -100mA	-	0.5	**1.0**	V
Gate V_{OL}[4]	V_{OL}	OUT to GND, I_{OUT} = 100mA	-	0.5	**1.0**	V
Gate V_{OH}[4]	V_{OH}	V_{DD} to OUT, I_{OUT} = -8mA	-	40	**80**	mV
Gate V_{OL}[4]	V_{OL}	OUT to GND, I_{OUT} = 8mA	-	40	**80**	mV
Peak Output Current[3]	I_{OPK}	C_{OUT} = 1nF	-	1.0	-	A
Rise Time	OUT_RT	C_{OUT} = 1nF	-	35	**60**	ns
Fall Time	OUT_FT	C_{OUT} = 1nF	-	29	**40**	ns
Output Off State Leakage	IDoff	V_{DD} = 5V	-	-	**50**	µA
PWM						
Maximum Duty Cycle	MAX_Duty	COMP = V_{REF} (ISL71041M)	**47**	48	**50**	%
		COMP = V_{REF} (ISL71043M)	**94**	96	-	
Minimum Duty Cycle	MIN_Duty	COMP = GND	-		**0**	%

1. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
3. Compliance to limits is assured by characterization and design.
4. See ISL71041M Radiation Acceptance Test Limits for the ISL71043M test limits for this specification.

3.5.1 ISL71041M Radiation Acceptance Test Limits

ISL71041M LDR acceptance testing is held to the same electrical specifications as the Electrical Specifications, except for the expanded limits below. Typical values of key parameters after 50krad(Si) are shown in Table 4.

Recommended operating conditions unless otherwise noted. V_{DD} = 13.2V, R_T = 10kΩ, C_T = 3.3nF. Typical values are at T_A = +25°C. **Boldface limits apply over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s**

Parameter	Symbol	Test Conditions	Min[1])	Typ	Max[1]	Unit
Output						
Gate V_{OH}	V_{OH}	V_{DD} to OUT, I_{OUT} = -100mA		0.8	**2.0**	V
Gate V_{OL}	V_{OL}	OUT to GND, I_{OUT} = 100mA		0.5	**2.0**	V
Gate V_{OH}	V_{OH}	V_{DD} to OUT, I_{OUT} = -8mA		50	**160**	mV
Gate V_{OL}	V_{OL}	OUT to GND, I_{OUT} = 8mA		40	**160**	mV

1. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Curves

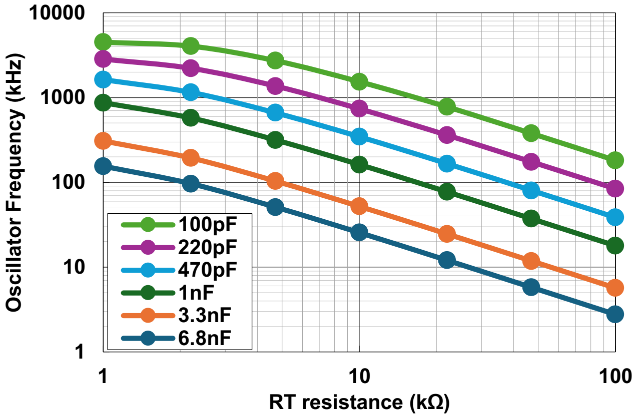


Figure 4. Oscillator Frequency versus RT and CT values

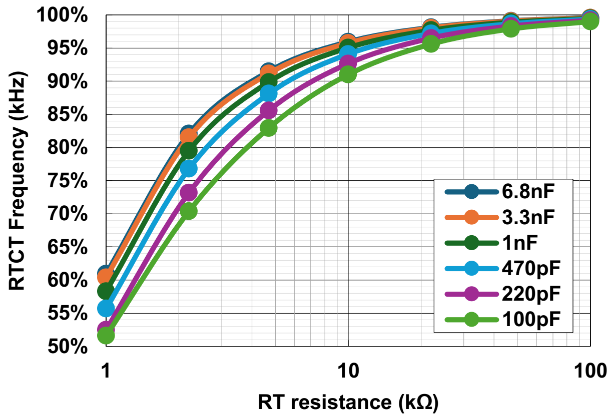


Figure 5. Maximum Oscillator Duty Cycle versus RT and CT values

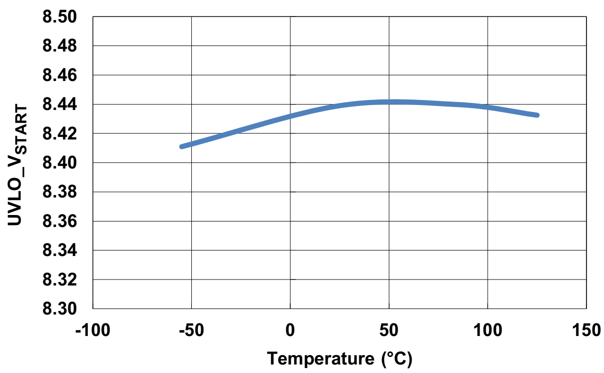


Figure 6. Start Threshold Over Temperature

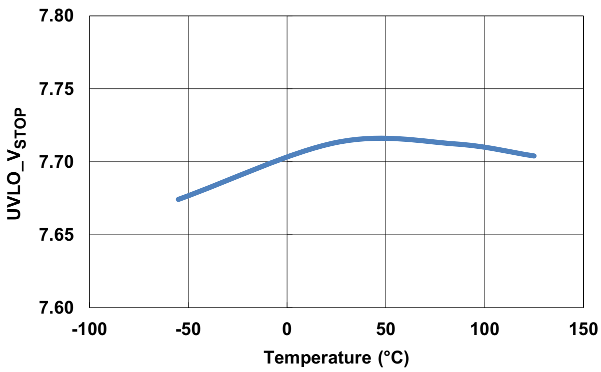


Figure 7. Stop Threshold Over Temperature

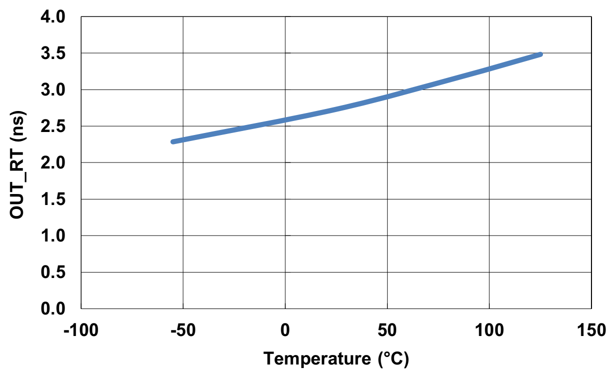


Figure 8. Rise Time Over Temperature

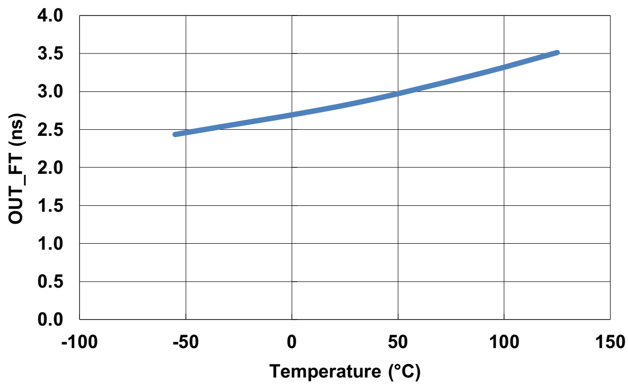


Figure 9. Fall Time Over Temperature

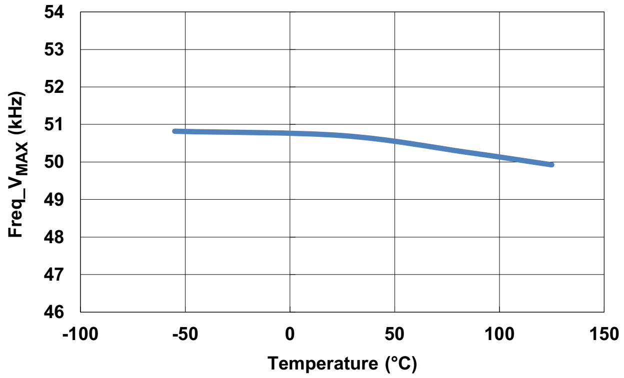


Figure 10. Frequency Accuracy Over Temperature

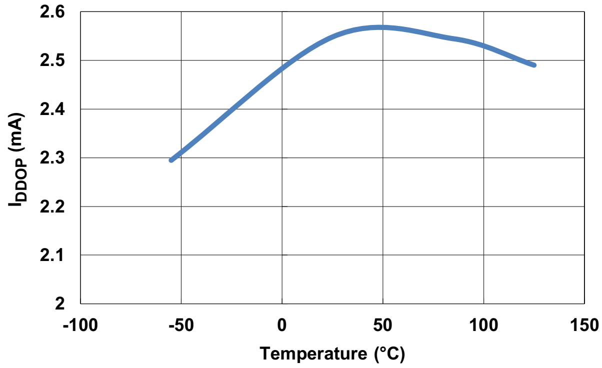


Figure 11. Operating Current Over Temperature

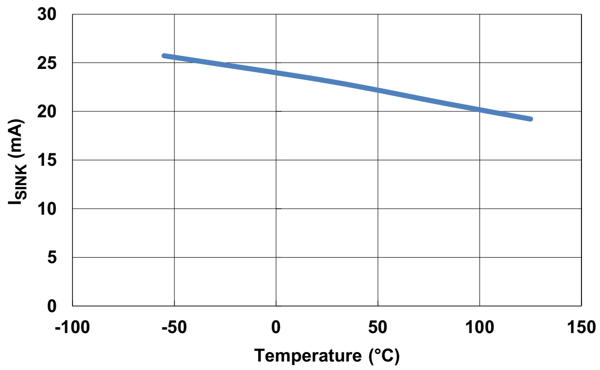


Figure 12. Current Limit, Sinking Over Temperature

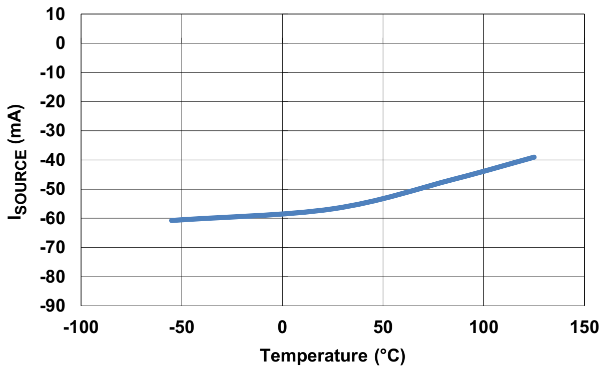


Figure 13. Current Limit, Sourcing Over Temperature

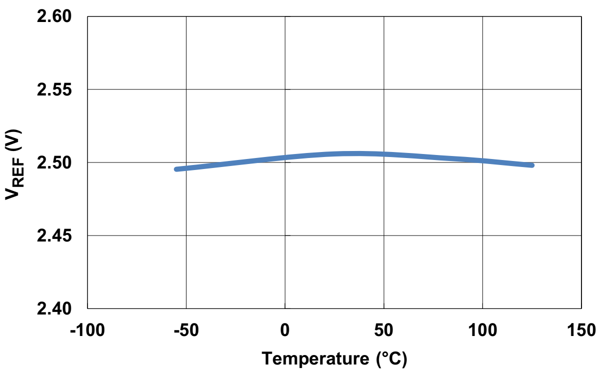


Figure 14. Reference Voltage Over Temperature

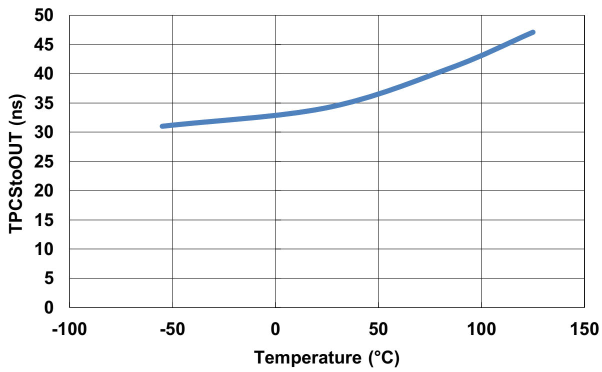


Figure 15. CS to Out Delay Over Temperature

5. Functional Description

5.1 Features

The ISL71041M and ISL71043M current mode PWM makes them an ideal choice for low-cost flyback and forward topology applications.

5.2 Oscillator

The ISL71041M and ISL71043M devices have a sawtooth oscillator with a programmable frequency range to 1MHz that can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin (see Figure 4 for the resistor and capacitance required for a given frequency).

5.3 Soft-Start Operation

Soft-start must be implemented externally. Figure 16 shows one method that clamps the voltage on COMP.

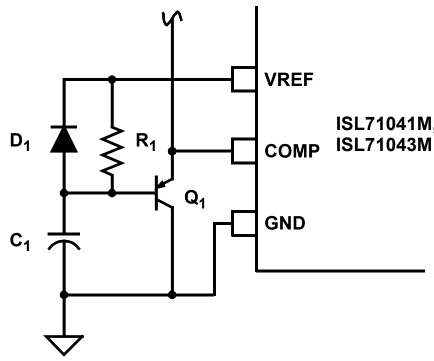


Figure 16. Soft-Start

The COMP pin is clamped to the voltage on capacitor C_1 plus a base-emitter junction by transistor Q_1. C_1 is charged from VREF through resistor R_1 and the base current of Q_1. At power-up, C_1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C_1 charges, the voltage on COMP increases and the duty cycle increases in proportion to the voltage on C_1. When COMP reaches the steady-state operating point, the control loop takes over and soft-start is complete. C_1 continues to charge up to V_{REF} and no longer affects COMP. During power-down, diode D_1 quickly discharges C_1 so that the soft-start circuit is properly initialized before the next power-on sequence.

5.4 Gate Drive

The ISL71041M and ISL71043M devices are capable of sourcing and sinking 1A peak current. An optional external resistor can be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET to limit the peak current through the IC. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

5.5 Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation can be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation can be accomplished by adding an external ramp to the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

The small signal current-mode model[1] shows that the naturally-sampled modulator gain, Fm, without slope compensation is calculated in Equation 6:

(EQ. 6) $$Fm = \frac{1}{S_n t_{SW}}$$

where S_n is the slope of the sawtooth signal and t_{SW} is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 7:

(EQ. 7) $$Fm = \frac{1}{(S_n + S_e)t_{SW}} = \frac{1}{m_c S_n t_{SW}}$$

where S_e is the slope of the external ramp and becomes Equation 8:

(EQ. 8) $$m_c = 1 + \frac{S_e}{S_n}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole is critically damped if the Q-factor is set to 1, over-damped for Q < 1, and under-damped for Q > 1. An under-damped condition can result in current loop instability.

(EQ. 9) $$Q = \frac{1}{\pi(m_c(1 - D) - 0.5)}$$

where D is the percent of on-time during a switching cycle. Setting Q = 1 and solving for S_e yields Equation 10:

(EQ. 10) $$S_e = S_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1 - D} - 1\right)$$

Because S_n and S_e are the on-time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON}.

(EQ. 11) $$V_e = V_n\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1 - D} - 1\right) \quad V$$

where V_n is the change in the current feedback signal (ΔI) during the on-time and V_e is the voltage that must be added by the external ramp.

For a flyback converter, V_n can be solved in terms of input voltage, current transducer components, and primary inductance, yielding Equation 12:

(EQ. 12) $$V_e = \frac{D \cdot t_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p}\left(\left(\frac{1}{\pi} + 0.5\right)\frac{1}{1 - D} - 1\right) \quad V$$

where R_{CS} is the current sense resistor, t_{SW} is the switching period, L_p is the primary inductance, V_{IN} is the minimum input voltage, and D is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is Equation 13:

(EQ. 13) $$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P}\left(I_O + \frac{(1 - D) \cdot V_O \cdot t_{sw}}{2L_s}\right) \quad V$$

1. Ridley, R., *A New Continuous-Time Model for Current Mode Control*, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance, and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Because the peak current limit threshold is 1V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold as shown in Equation 14:

(EQ. 14) $$V_e + V_{CS} = 1V$$

Substituting Equation 12 and Equation 13 into Equation 14 and solving for R_{CS} yields Equation 15:

(EQ. 15) $$R_{CS} = \frac{1}{\frac{D \cdot T_{sw} \cdot V_{IN}}{L_p} \cdot \left(\frac{\frac{1}{\pi}+0.5}{1-D} - 1\right) + \frac{N_s}{N_p} \cdot \left(I_O + \frac{(1-D) \cdot V_O \cdot t_{sw}}{2L_s}\right)}$$

Add slope compensation in the ISL71041M and ISL71043M devices using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 17.

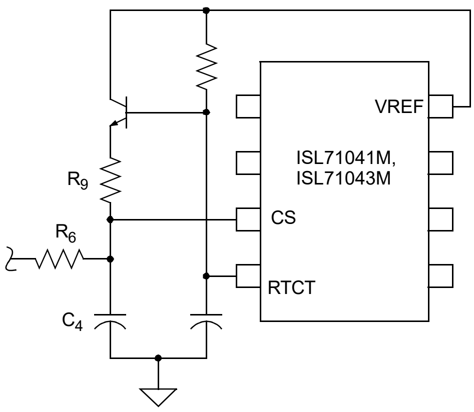


Figure 17. Slope Compensation

Assuming the designer has selected values for the RC filter (R_6 and C_4) placed on the CS pin, the value of R_9 required to add the appropriate external ramp can be found by superposition.

(EQ. 16) $$V_e = \frac{2.05D \cdot R_6}{R_6 + R_9} \quad V$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R_9 yields Equation 17:

(EQ. 17) $$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega$$

The value of R_{CS} determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by R_6 and R_9 makes this necessary.

(EQ. 18) $$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS}$$

Example:

V_{IN} = 12V, V_O = 48V, L_s = 800µH, Ns/Np = 10, Lp = 8.0µH, I_O = 200mA, switching frequency, f_{SW} = 200kHz

duty cycle, D = 28.6%, R_6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equation 15.

R_{CS} = 295mΩ

Determine the amount of voltage, V_e, that must be added to the current feedback signal using Equation 12.

V_e = 92.4mV

Use Equation 17 to solve for the summing resistor, R_9, from CT to CS.

R_9 = 2.67kΩ

Determine the new value of R_{CS} (R'_{CS}) using Equation 18.

R'_{CS} = 350mΩ

Additional slope compensation may be considered for design margin. The previous discussion determines the minimum external ramp that is required. The buffer transistor that creates the external ramp from RTCT should have a sufficiently high gain (>200) to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and reduces the oscillator frequency.

5.6 Fault Conditions

A Fault condition occurs if V_{REF} falls below 4.65V. When a Fault is detected, OUT is disabled. When V_{REF} exceeds 4.80V, the Fault condition clears and OUT is enabled.

5.7 Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be used. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. Bypass VDD directly to GND with good high frequency capacitors.

6. Radiation Tolerance

The ISL71041M and ISL71043M are radiation tolerant devices for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. The response of these devices to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) have been measured, characterized, and reported in the following actions. The TID performance of the ISL71043MBZ, ISL71043MRTZ and the ISL71041MRTZ are not guaranteed through radiation acceptance testing. The ISL71041M30RTZ is radiation lot acceptance tested (RLAT) to 30krad(Si), and the ISL71041M50RTZ is RLAT to 50krad(Si). The SEE characterized performance is not guaranteed.

6.1 Total Ionizing Dose (TID) Testing

6.1.1 Introduction

These tests were conducted to determine the sensitivity of the parts to the total dose environment. Test downpoints for the ISL71041M were 0krad(Si), 10krad(Si), 20krad(Si), 30krad(Si), 40krad(Si), and 50krad(Si).Test downpoints for the ISL71043M were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). Total dose testing was performed using a Hopewell Designs N40 panoramic irradiator. Irradiations were performed at 0.00875 rad(Si)/s. A PbAl box was used to shield the test figure and devices under test against low energy secondary gamma radiation. The characterization matrix for the ISL71041M consisted of 7 samples irradiated under bias and 7 samples irradiated with all pins grounded. The characterization matrix for the ISL71043M consisted of 24 samples irradiated under bias and 12 samples irradiated with all pins grounded. Four control units for each part were used to ensure repeatable data. Two different wafers for each part were used. The bias configuration is shown in Figure 18.

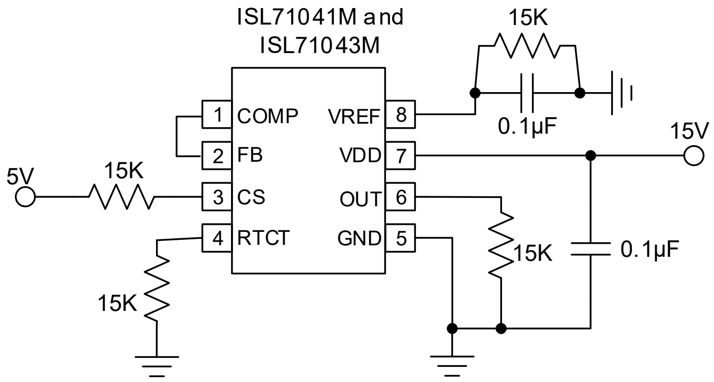


Figure 18. Irradiation Bias Configuration

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE), with data logging at each downpoint (including anneal). Downpoint electrical testing was performed at room temperature.

6.1.2 Results

Table 2 and Table 3 summarize the attributes data. Bin 1 indicates a device that passes all device specification limits.

Table 2. ISL71041M Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Downpoint	Bin1	Rejects
8.75	Figure 18	7	Pre-rad	7	0
			10krad(Si)	7	0
			20krad(Si)	7	0
			30krad(Si)	7	0
			40krad(Si)	7	0
			50krad(Si)	7	0
8.75	Grounded	7	Pre-rad	7	0
			10krad(Si)	7	0
			20krad(Si)	7	0
			30krad(Si)	7	0
			40krad(Si)	7	0
			50krad(Si)	7	0

Table 3. ISL71043M Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Downpoint	Bin1	Rejects
8.75	Figure 18	24	Pre-rad	24	0
			10krad(Si)	24	0
			20krad(Si)	24	0
			30krad(Si)	24	0
8.75	Grounded	12	Pre-rad	12	0
			10krad(Si)	12	0
			20krad(Si)	12	0
			30krad(Si)	12	0

Figure 19 through Figure 24 show data for key parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions. All parts showed excellent stability over irradiation.

6.1.3 Typical Radiation Performance

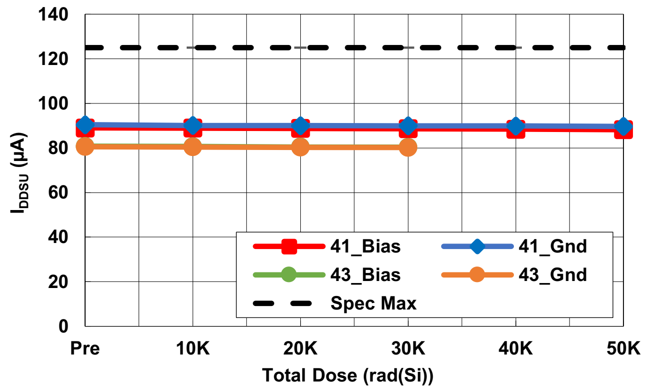


Figure 19. Start-Up Current vs TID

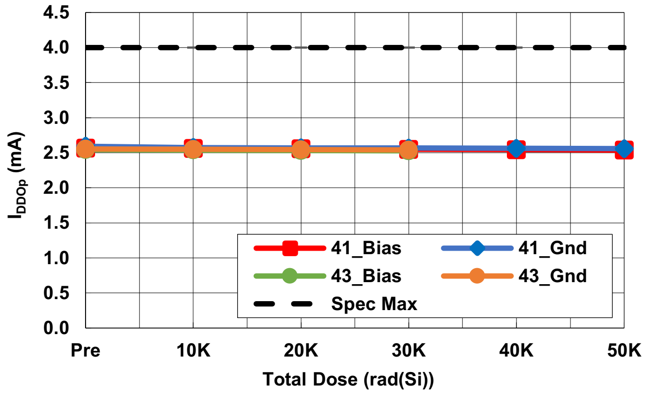


Figure 20. Operating Current vs TID

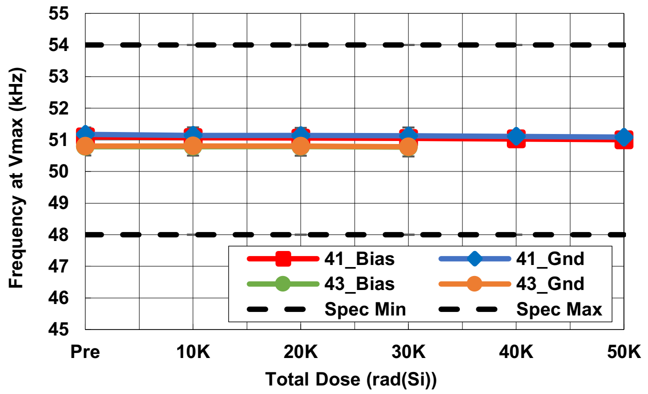


Figure 21. Frequency Accuracy vs TID

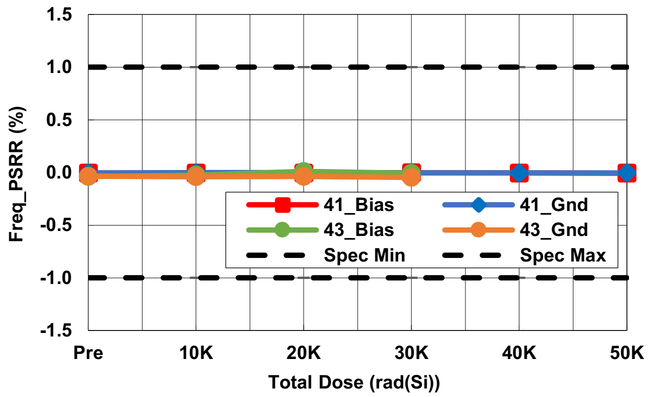


Figure 22. Frequency Variation with V_{DD} vs TID

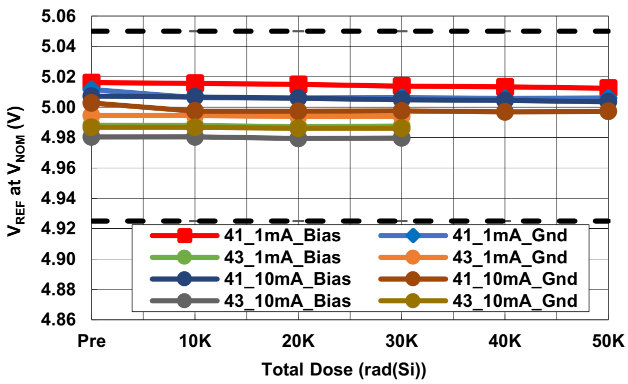


Figure 23. Reference Voltage Accuracy vs TID

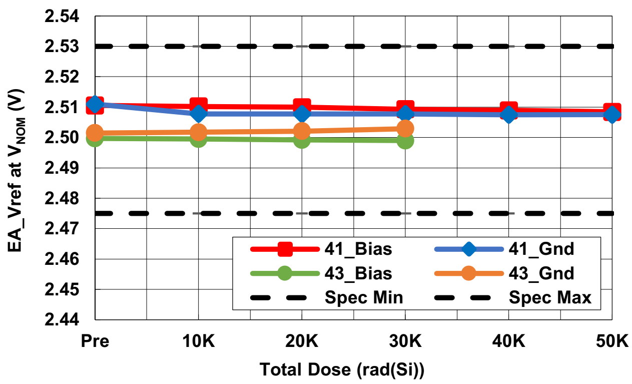


Figure 24. Error Amplifier Reference Voltage vs TID

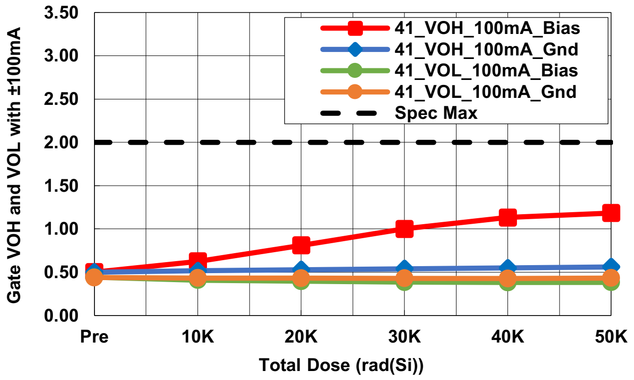


Figure 25. 100mA Gate Drive vs TID

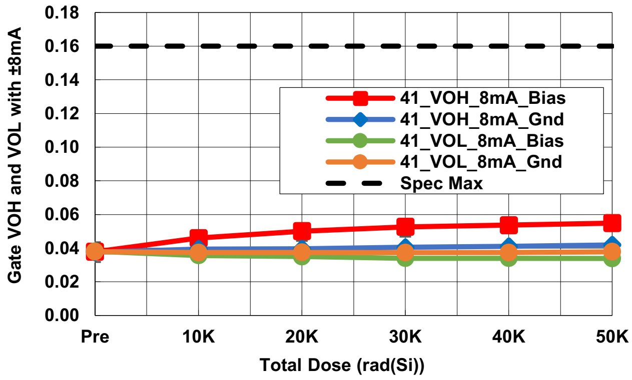


Figure 26. 8mA Gate Drive vs TID

6.1.4 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters is presented in Figure 19 through Figure 24. No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive.

Table 4. ISL71041M Response of Key Parameters vs TID

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	40krad(Si)	50krad(Si)	Unit
Start-Up Current	I_{DDSu}	-	Bias	89.016	88.940	88.789	88.618	88.449	88.185	µA
			GND	90.447	90.059	90.020	89.939	89.866	89.655	µA
Operating Current	I_{DDOp}	9V	Bias	2.523	2.515	2.511	2.505	2.499	2.492	mA
			GND	2.547	2.528	2.525	2.523	2.518	2.514	mA
		12V	Bias	2.568	2.560	2.556	2.550	2.544	2.537	mA
			GND	2.592	2.574	2.570	2.568	2.564	2.559	mA
		13.2V	Bias	2.579	2.571	2.567	2.561	2.555	2.548	mA
			GND	2.604	2.585	2.582	2.579	2.575	2.570	mA
Frequency Accuracy	Freq	13.2V	Bias	51.093	51.068	51.053	51.046	51.032	51.004	kHz
			GND	51.172	51.141	51.134	51.124	51.113	51.086	kHz
Frequency Variation with VDD	Freq_ PSRR	-	Bias	-0.005	-0.006	-0.005	-0.003	-0.004	-0.006	%
			GND	-0.005	-0.002	-0.001	-0.005	-0.005	-0.003	%
Voltage Reference	V_{REF}	1mA	Bias	5.016	5.016	5.015	5.014	5.013	5.012	V
			GND	5.012	5.006	5.006	5.006	5.006	5.006	V
		10mA	Bias	5.007	5.007	5.006	5.005	5.004	5.004	V
			GND	5.003	4.997	4.997	4.997	4.997	4.997	V
Error Amp Reference	EA_ VREF	12V	Bias	2.511	2.510	2.510	2.509	2.509	2.508	V
			GND	2.511	2.508	2.508	2.508	2.507	2.508	V
Gate V_{OH}	V_{OH}	-100mA	Bias	0.501	0.625	0.810	1.001	1.132	1.183	V
			GND	0.500	0.517	0.530	0.540	0.548	0.561	V
		-8mA	Bias	0.038	0.046	0.050	0.053	0.054	0.055	V
			GND	0.038	0.039	0.040	0.040	0.041	0.042	V

Table 4. ISL71041M Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	40krad(Si)	50krad(Si)	Unit
Gate V_{OL}	V_{OL}	100mA	Bias	0.442	0.409	0.396	0.386	0.382	0.383	V
			GND	0.439	0.432	0.431	0.429	0.428	0.434	V
		8mA	Bias	0.038	0.036	0.035	0.034	0.034	0.034	V
			GND	0.038	0.037	0.037	0.037	0.037	0.038	V

Table 5. ISL71043M Response of Key Parameters vs TID (0, 10, 20, 30krad(Si))

Parameter	Symbol	Condition	Bias	0krad(Si)	10krad(Si)	20krad(Si)	30krad(Si)	Unit
Start-Up Current	I_{DDSu}	13.2V	Biased	80.799	80.614	80.451	80.350	µA
			Grounded	80.546	80.406	80.282	80.212	µA
Operating Current	I_{DDOp}	9V	Biased	2.555	2.548	2.543	2.539	mA
			Grounded	2.565	2.560	2.556	2.552	mA
		12V	Biased	2.543	2.536	2.531	2.527	mA
			Grounded	2.554	2.548	2.544	2.540	mA
		13.2V	Biased	3.249	3.249	3.246	3.232	mA
			Grounded	3.263	3.259	3.263	3.243	mA
Frequency	Freq	13.2V	Biased	50.783	50.787	50.787	50.770	kHz
			Grounded	50.803	50.805	50.802	50.782	kHz
Frequency Accurracy	Freq_PSRR		Biased	-0.039	-0.025	0.010	-0.007	%
			Grounded	-0.035	-0.042	-0.039	-0.047	%
Voltage Reference	V_{REF}	1mA	Biased	4.988	4.988	4.987	4.988	V
			Grounded	4.994	4.994	4.993	4.994	V
		10mA	Biased	4.980	4.980	4.979	4.979	V
			Grounded	4.987	4.987	4.986	4.986	V
Error Amp Reference	EA_V_{REF}	12V	Biased	2.500	2.499	2.499	2.499	V
			Grounded	2.501	2.502	2.502	2.502	V

6.2 Single-Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. SEE testing was performed on the ISL71043M only and the results extend to include the ISL71041M because the differences between the parts are so slight. Any differences between the parts were determined to be benign in previous testing. The following is a summary of the ISL71043M SEE testing.

6.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility on April 4, 2019. The overall test setup includes the test jig containing four evaluation boards mounted and wired through a 20ft cable to the data room. The end of the 20ft cable in the data room was connected to a switchboard. The switchboard was wired to the power supplies and monitoring equipment/scopes. The signals from the switchboard were connected to two LeCroy oscilloscopes, one set to capture transients due to pulse-width change and the other to capture on period change. The switchboard at the end of the 20ft cabling was found to require termination to keep the noise on the waveforms to a minimum. OUT and RTCT was terminated with a series combination of 1000pF and 51Ω and the VOUT and VREF signals with a 10nF capacitor to ground.

6.2.2 SEE Test Setup

The SEB/L evaluation board was wired up in the open loop configuration as shown in Figure 27. The biasing used for the SEB/L test runs was V_{DD} = 14.7V. The SET board was wired up in the closed loop configuration shown in Figure 28. The biasing for the SET test runs was V_{DD} = 14.7V.

A SET occurs when a perturbation is detected. This can be a change in pulse-width, which can cause missing pulses. Scope 1 was set to trigger to pulse-width variations of around the nominal value. Measurements on Scope 1 are CH1 = OUT, CH2 = VOUT, CH3 = RTCT, CH4 = VREF, and TRIG = OUT PW. Scope 2 is set to trigger to missing pulse events. This setting triggers when two rising edges deviate from the nominal period by ±20%. Measurements on Scope 2 are CH1 = OUT, CH2 = VOUT, CH3 = RTCT, CH4 = VREF, and TRIG = OUT period.

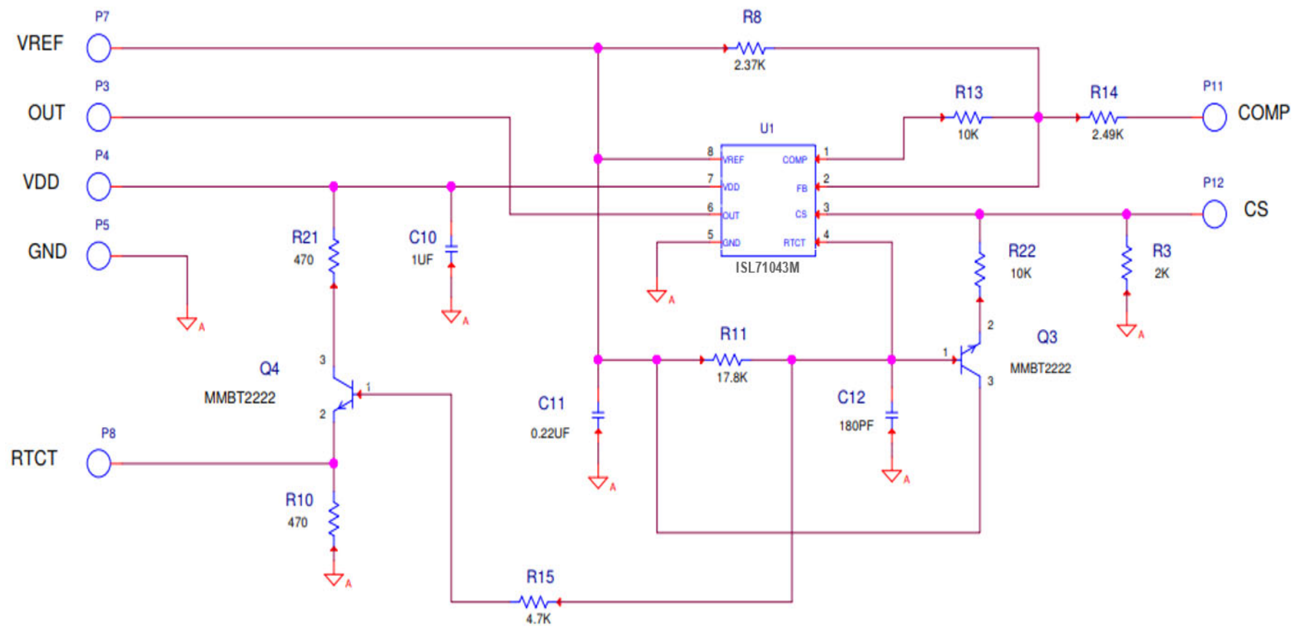


Figure 27. SEB/L Evaluation Board Schematic

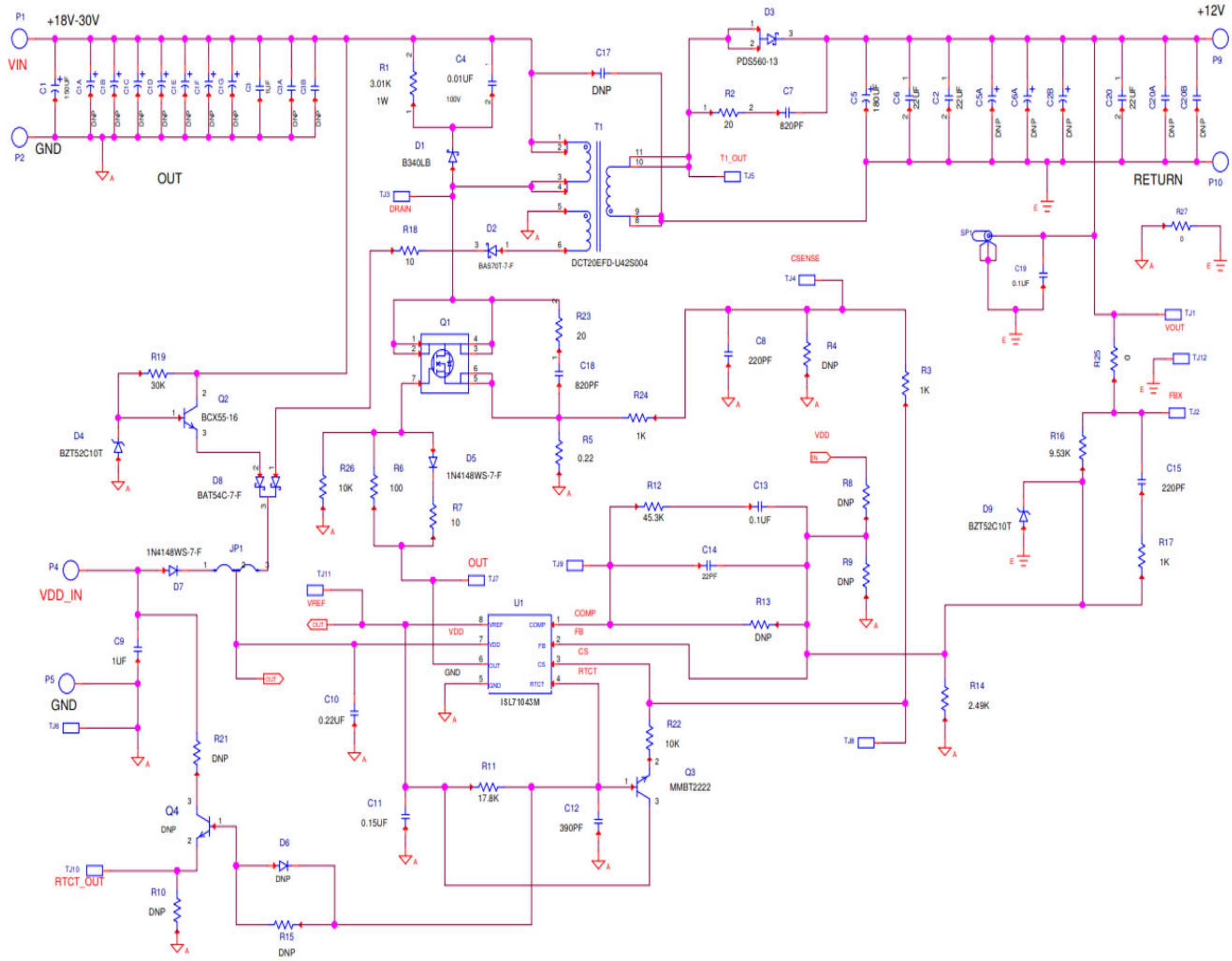


Figure 28. Schematic of SET Evaluation Board

6.2.3 Single Event Burnout and Latch-Up (SEB/L) Results

No SEB was observed for the device LET of 43MeV•cm^2/mg (+125°C) and V_{DD} = 14.7V. No SEL events were observed for the device at LET value of 43MeV•cm^2/mg (+125°C, VREF Cap = 0.22µF). A destructive event occurs when the supply current of the device increases greater than 5%.

6.2.4 SET Results

The device is sensitive to soft errors with a LET of 43MeV•cm^2/mg. No soft error was observed, which caused more than one PWM output pulse dropout at LET value of 43MeV•cm^2/mg. Extreme pulse-width waveforms are shown in Figure 29 through Figure 32.

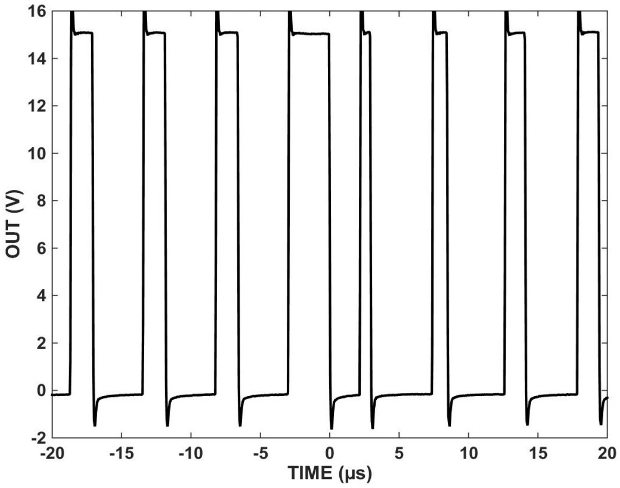


Figure 29. Extreme SET captures from DUT2 with 43MeV·cm^2/mg on the OUT signal with a ±20% pulse-width trigger, maximum pulse-width high

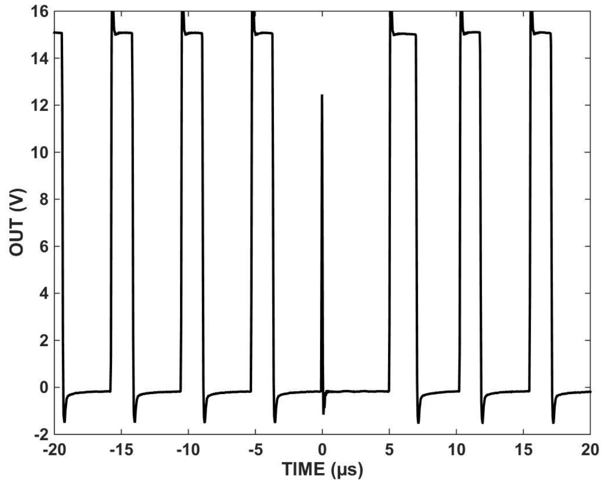


Figure 30. Extreme SET captures from DUT2 with 43MeV·cm^2/mg on the OUT signal with a ±20% pulse-width trigger, maximum pulse-width low

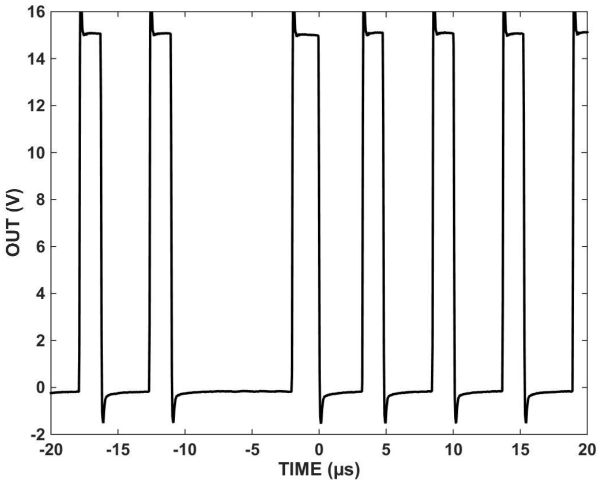


Figure 31. Extreme SET captures from DUT2 with 43MeV·cm^2/mg on the OUT signal with a ±20% pulse-width trigger, minimum pulse-width high

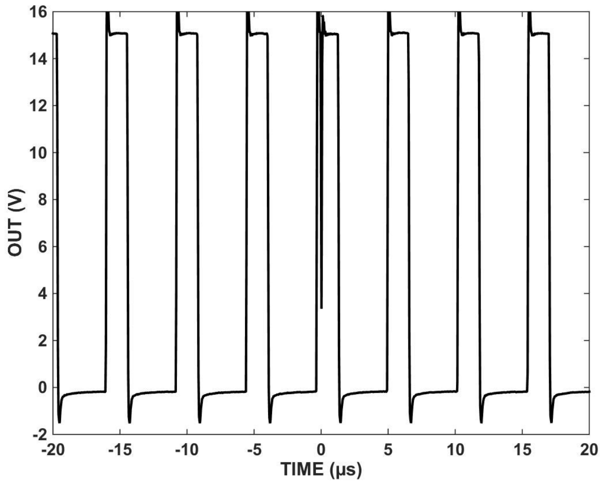


Figure 32. Extreme SET captures from DUT2 with 43MeV·cm^2/mg on the OUT signal with a ±20% pulse-width trigger, minimum pulse-width low

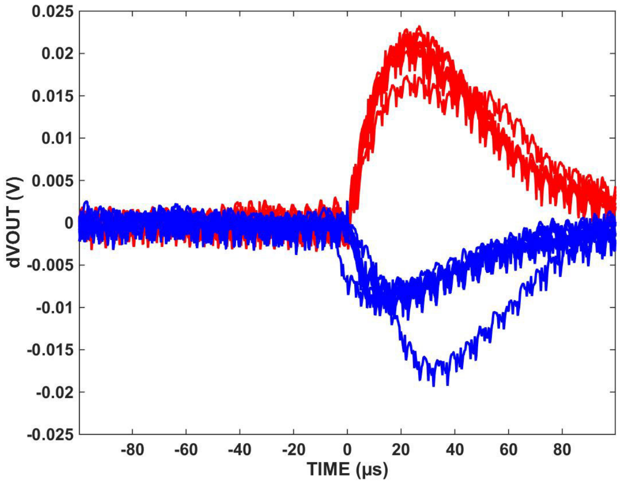


Figure 33. Composite of Ten Greatest Positive and Negative V_{OUT} Transients

6.2.5 Conclusion

The device is sensitive to soft errors with a LET of 43MeV•cm^2/mg. No soft error was observed which caused more than one missing PWM output pulse at LET value of 43MeV•cm^2/mg.

Test[1]	Missed Pulses (Typical)	Missed Pulses (Maximum)	Temp	LET (MeV•cm^2/mg)	Remarks
SEB/L[2][3][4]	-	-	+125	43	No destructive single event burnouts or latch-up events occurred at V_{DD} = 14.7V at 43MeV·cm^2/mg and 0° incidence at a fluence of 4x10^7 particles/cm^2
SET	-	1	+25	43	

1. SEE tests performed at a switching frequency of 200kHz, RT = 17.8k, CT = 390pF. SEB/L tests are done in a standalone open loop configuration and the SET tests are done in a closed loop configuration.
2. SEB occurs if an increase in the I_{DD} of greater than 5% is measured after exposure to the beam. A 0.22µF capacitor was connected from the VREF pin to GND for the purpose of bypass.
3. SEL results: No latch-up conditions were observed, a SEL is categorized by an increase in the I_{DD} current greater than 5% during exposure. A 0.22µF capacitor was used from VREF pin to GND for bypass.
4. The recommended highest operating V_{DD} for the device is 13.2V, which is below the single event breakdown survival voltage of 14.7V for normal incidence LET = 43MeV·cm^2/mg.

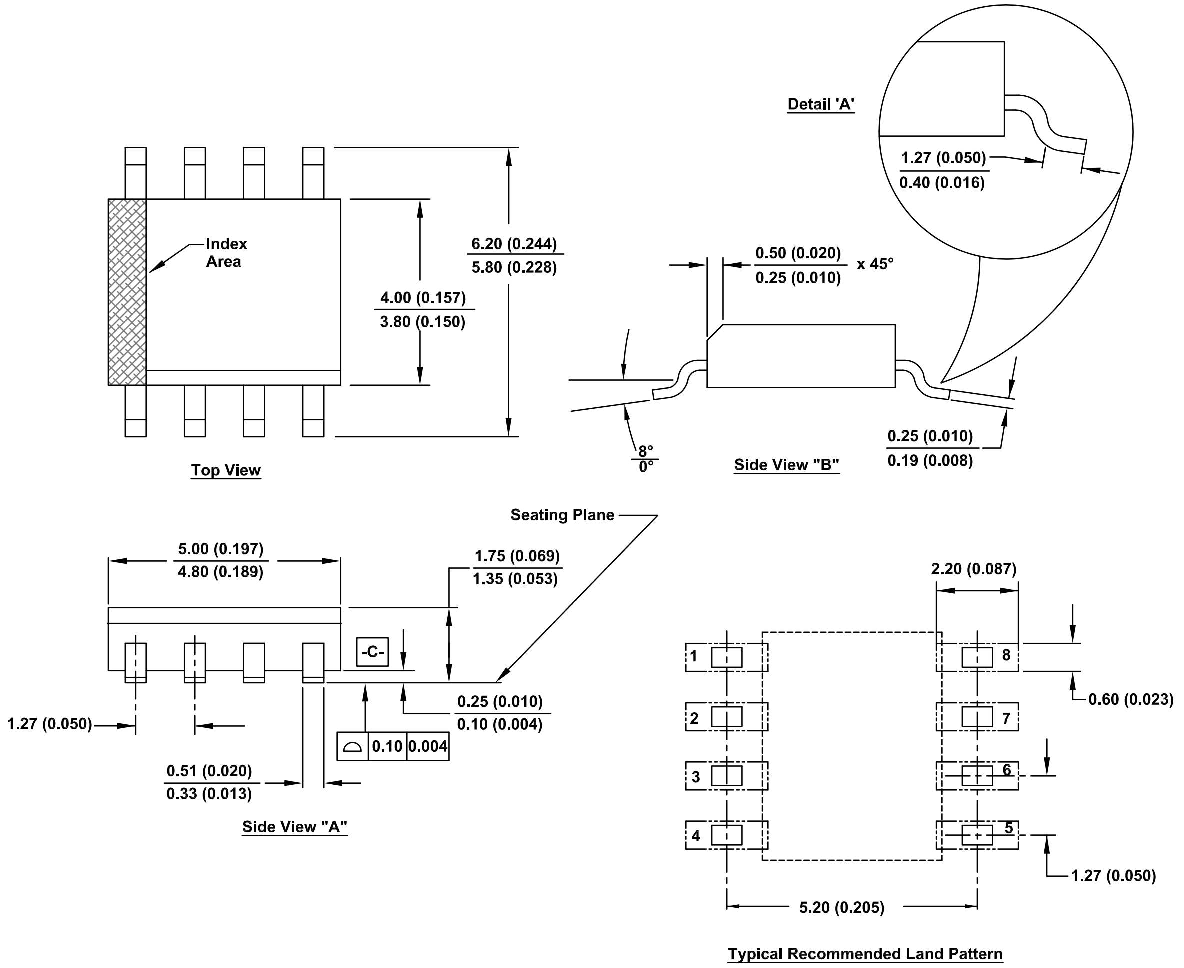
7. Package Outline Drawings

For the most recent package outline drawing, see M8.15.

M8.15

8 Lead Narrow Body Small Outline Plastic Package

Rev 7, 9/2023

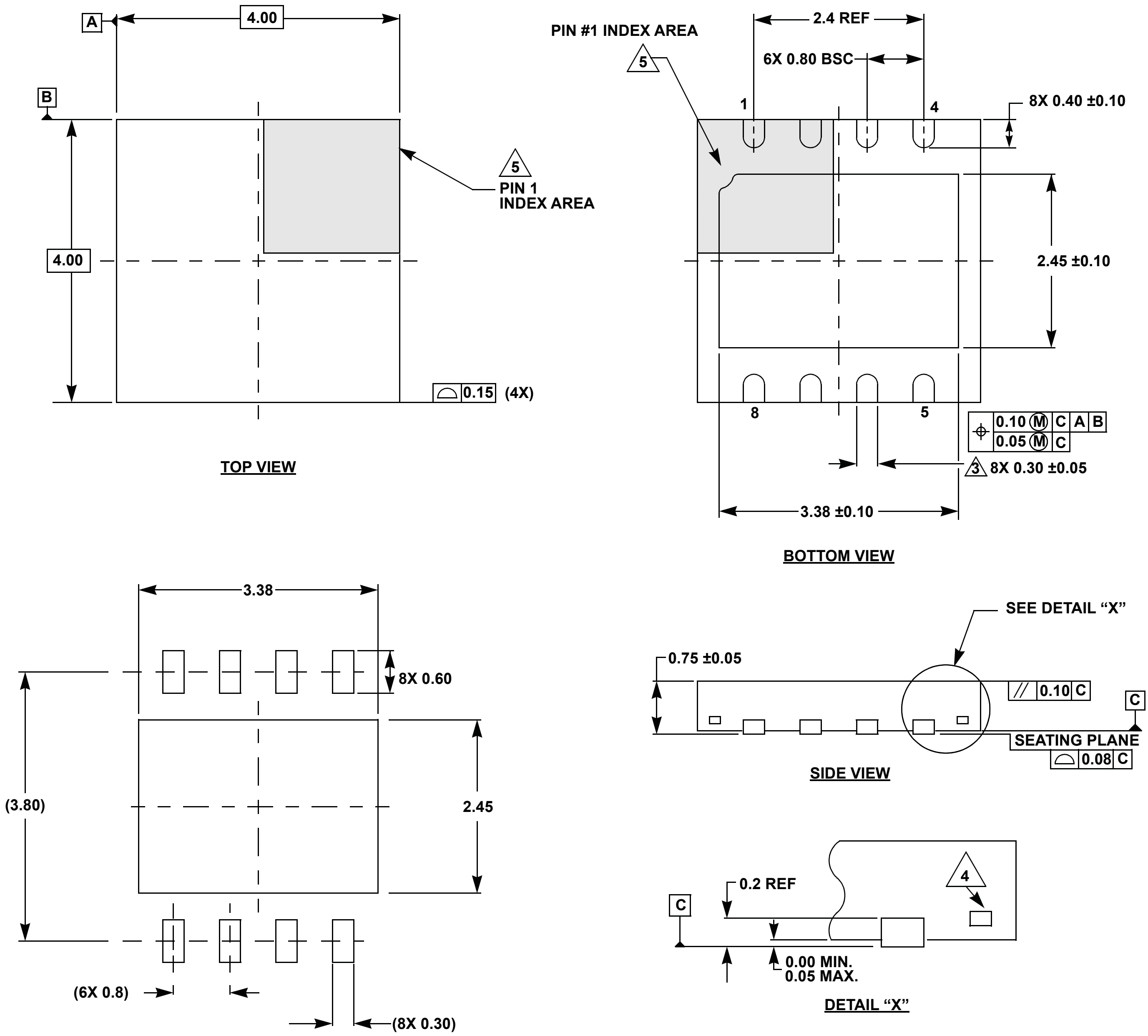


Notes:

1. Dimensioniong and tolerancing conform to ASME Y14.5M-1994.
2. Package length does not include mold flash, protrusion or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
7. Controlling dimension: MILLIMETER. Converted inch dimension are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

For the most recent package outline drawing, see L8.4x4B.

L8.4x4B
8 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)
Rev 0, 05/16



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
4. Tiebar shown (if present) is a non-functional feature, and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

8. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	TID Data Pack Included	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp Range
ISL71043MBZ	71043 MBZ	N/A	No	8 Ld NSOIC	M8.15	Tube	-55 to +125°C
ISL71043MBZ-T		N/A	No			Reel, 1k	
ISL71043MBZ-T7A		N/A	No			Reel, 250	
ISL71043MRTZ	710 43MRTZ	N/A	No	8 Ld TDFN	L8.4x4B	Tube	
ISL71043MRTZ-T		N/A	No			Reel, 1k	
ISL71043MRTZ-T7A		N/A	No			Reel, 250	
ISL71041MRTZ	710 41MRTZ	N/A	No	8 Ld TDFN	L8.4x4B	Tube	
ISL71041MRTZ-T		N/A	No			Reel, 1k	
ISL71041MRTZ-T7A		N/A	No			Reel, 250	
ISL71041M30RTZ	710 41MRTZ	30krad(Si)	Yes	8 Ld TDFN	L8.4x4B	Tube	
ISL71041M30RTZ-T						Reel, 1k	
ISL71041M30RTZ-T7A						Reel, 250	
ISL71041M50RTZ	710 41MRTZ	50krad(Si)	Yes	8 Ld TDFN	L8.4x4B	Tube	
ISL71041M50RTZ-T						Reel, 1k	
ISL71041M50RTZ-T7A						Reel, 250	
ISL71043MEVAL1Z	Flyback Power Supply Evaluation Board using the ISL71043M and ISL71040M.						

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71043M and ISL71041M device pages. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

9. Revision History

Rev.	Date	Description
5.04	Jan 31, 2025	Updated Features bullets. Added references to ISL71041M30 and ISL71041M50 throughout. Edited oscillator frequency equations. Updated Figure 4 and added Figure 5. Updated Table 3. Updated Figures 17, 24, and 25. Updated Table 4. Removed Table 6. Updated Ordering Information table.
5.03	Sep 29, 2023	Updated M8.15 POD to the latest revision (corrected typo).

Rev.	Date	Description
5.02	Aug 11, 2023	Applied the latest template throughout. Updated Features bullets. Updated block diagram. Added Maximum Duty Cycle minimum specification. Added ISL71043M Radiation Acceptance Test Limits section. Added Table 6. Updated Tables 4 and 5. Updated Figures 18 through 23. Added Figures 24 and 25. Removed Reference section as reference is now a footnote on the applicable page.
5.01	Feb 23, 2023	Added EPAD description to the Pin Descriptions table. Removed Related Literature section. Updated ordering information table formatting. Updated POD M8.15 to the latest revision, changes are as follows: ▪ Added the coplanarity spec into the drawing.
5.00	Sep 30, 2020	Added ISL71041 throughout
4.00	Nov 19, 2019	Updated V_{OH} and V_{OL} limits on page 9.
3.00	Oct 18, 2019	Added TDFN package information throughout document.
2.00	Jun 14, 2019	Applied new formatting throughout. Updated the rise and fall time bullet in the Features section. Updated the Reference Voltage Overall Accuracy minimum (from 4.9 to 4.925) and maximum (from 5.1 to 5.050) specifications Updated the Error Amplifier Reference Voltage minimum (from 2.4 to 2.475) and maximum (from 2.6 to 2.530) specifications Updated Table 2 (13.2V condition only). Updated Single-Event Effects Testing sections.
1.00	Jan 21, 2019	Initial release

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