ISL71841SEH

Radiation Hardened 30V 32-Channel Analog Multiplexer

The ISL71841SEH is a radiation hardened, 32-channel high ESD protected multiplexer fabricated using the Renesas proprietary P6SOI (Silicon On Insulator) process technology to mitigate single event effects. It operates with a dual supply voltage ranging from ±10.8V to ±16.5V. It has a 5-bit address plus an enable pin that can be driven with adjustable logic thresholds to conveniently select one of 32 available channels. An inactive channel is separated from an active channel by a high impedance, which inhibits any interaction between them.

The ISL71841SEH's low r_{ON} allows for improved signal integrity and reduced power losses. The ISL71841SEH is also designed for cold sparing, making it excellent for high reliability applications that have redundancy requirements. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without loading signal sources. The ISL71841SEH also incorporates input analog overvoltage protection, which disables the switch to protect downstream devices.

The ISL71841SEH is available in a 48 Ld CQFP, 44 Ld CLCC, or die form and operates across the extended temperature range of -55°C to +125°C.

A 16-channel version in a 28 Ld CDFP is also available. Refer to the ISL71840SEH datasheet for more information. For a list of differences between the ISL71841SEH and ISL71840SEH, see Table 1 on page 3.

Features

- DLA SMD #5962-15220
- Fabricated using P6SOI process technology
- Provides latch-up immunity
- ESD protection 8kV (HBM)
- Rail-to-rail operation
- Overvoltage protection
- Low r_{ON}. . . . . <500Ω (typical)
- Flexible split rail operation
  - Positive supply above GND (V+) . . . . . +10.8V to +16.5V
  - Negative supply below GND (V-) . . . . . -10.8V to -16.5V
- Adjustable logic threshold control with VREF pin
- Cold sparing capable (from ground). . . . . ±25V
- Analog overvoltage range (from ground). . . . . ±35V
- Off switch leakage . . . . . 100nA (maximum)
- Transition times (t_R, t_F) . . . . . 500ns (typical)
- Break-before-make switching
- Grounded metal lid (internally connected)
- Operating temperature range. . . . . -55°C to +125°C
- Radiation tolerance
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . 100krad(Si) (Note 1)
  - SEB LET_{TH} . . . . . 86.4MeV•cm^2/mg

NOTE:

1. Product capability established by initial characterization. All subsequent lots are assurance tested to 50krad (0.01rad(Si)/s) wafer-by-wafer.

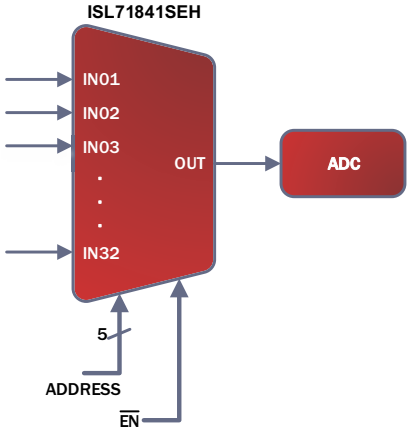

FIGURE 1. TYPICAL APPLICATION

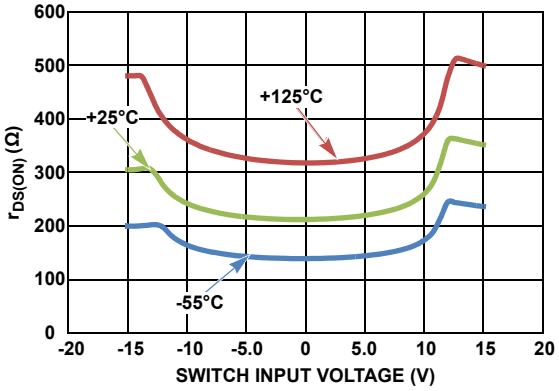

FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY ACROSS SWITCH INPUT COMMON-MODE VOLTAGE AT +25°C

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Ordering Information

SMD ORDERING NUMBER (Note 4)	PART NUMBER	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION	PKG. DWG. #	TEMP RANGE
5962R1522001VXC	ISL71841SEHVF (Note 2)	HDR to 100krad(Si), LDR to 100krad(Si)	48 LD CQFP (RoHS Compliant)	R48.A	-55 to +125°C
5962R1522001VYA	ISL71841SEHVL (Note 3)		44 LD CLCC	J44.A	
5962R1522001V9A	ISL71841SEHVX (Note 5)		Die (RoHS Compliant)	N/A	
N/A	ISL71841SEHF/PROTO (Notes 2, 6)	N/A	48 LD CQFP (RoHS Compliant)	R48.A	
N/A	ISL71841SEHL/PROTO (Notes 3, 6)		44 LD CLCC	J44.A	
N/A	ISL71841SEHX/SAMPLE (Notes 5, 6)		Die (RoHS Compliant)	N/A	
N/A	ISL71841SEHEV1Z (Note 7)	Evaluation Board			

NOTES:

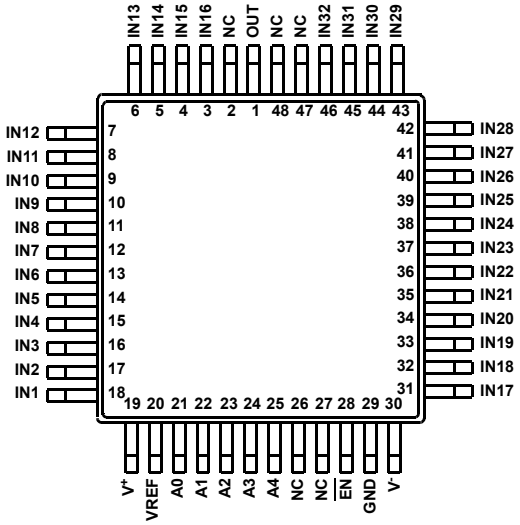
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. These Hermetic Packaged products are intended for SnPb soldering and may be shipped with terminations precoated with SnPb solder compatible with SnPb soldering operations only.
4. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
5. Die product tested at TA = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications (±15V)" and "Electrical Specifications (±12V)".
6. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
7. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

TABLE 1. TABLE OF DIFFERENCES

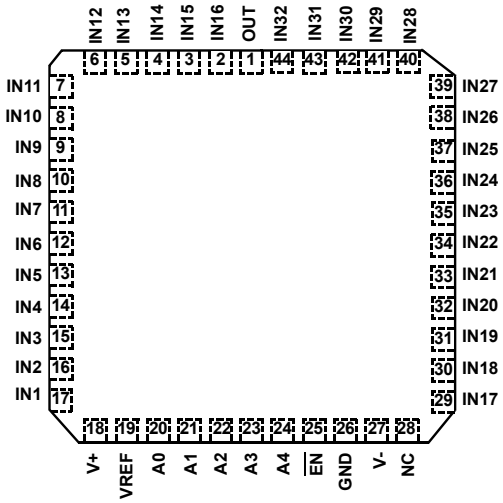
SPECIFICATION	ISL71840SEH	ISL71841SEH
Number of Channels	16	32
Supply Current (I+/I-)	350µA (maximum)	400µA (maximum)
Output Leakage (+125°C)	60nA (maximum)	120nA (maximum)

Pin Configurations

ISL71841SEH
(48 LD CQFP)
TOP VIEW

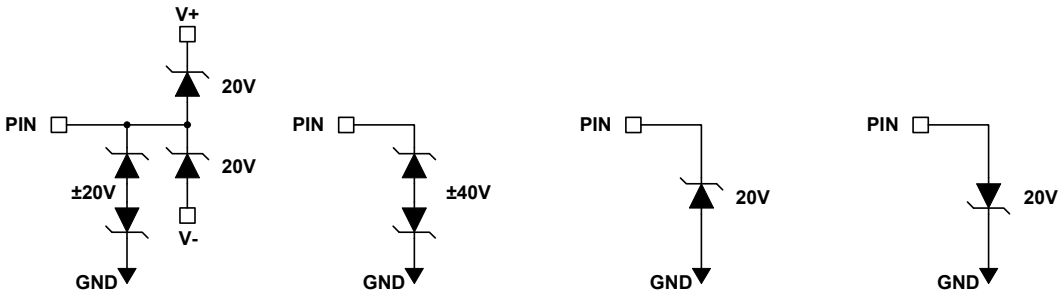


ISL71841SEH
(44 LD CLCC)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER 48 LD CQFP	PIN NUMBER 44 LD CLCC	DESCRIPTION
NC	2, 26, 27, 47, 48	28	Not connected, no internal connection
OUT	1	1	Output for multiplexer (see Circuit 1 in Figure 3)
V^+	19	18	Positive power supply (see Circuit 3 in Figure 3)
V^-	30	27	Negative power supply (see Circuit 4 in Figure 3)
INx	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46	2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44	Inputs for multiplexer (see Circuit 2 in Figure 3)
Ax	21, 22, 23, 24, 25	20, 21, 22, 23, 24	Address lines for multiplexer (see Circuit 3 in Figure 3)
$\overline{EN}$	28	25	Enable control for multiplexer (active low, see Circuit 3 in Figure 3)
VREF	20	19	Reference voltage used to set logic thresholds (see Circuit 3 in Figure 3)
GND	29	26	Ground
LID	NA	NA	Package lid is internally connected to GND (Pin 29 on CQFP, Pin 26 on CLCC)



CIRCUIT 1 CIRCUIT 2 CIRCUIT 3 CIRCUIT 4

FIGURE 3. ESD Circuits

Absolute Maximum Ratings

Positive Supply Voltage above GND (V^+) (Note 10) . . . . . +20V
Negative Supply Voltage below GND (V^-) (Note 10) . . . . . -20V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 10) 40V
Analog Input Voltage (INx)
From GND (Note 10) . . . . . ±35V
Digital Input Voltage Range ($\overline{EN}$, Ax) . . . . . GND - 0.3V to +16.5V
VREF to GND (Note 10) . . . . . +16.5V
ESD Tolerance
Human Body Model (Tested per MIL-STD-883 TM 3015) 8kV
Charged Device Model (Tested per JESD22-C101D) 250V
Machine Model (Tested per JESD22-A115-A) 250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld CQFP (Notes 8, 9)	50	2
44 Ld CLCC (Notes 8, 9)	31	3

Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Positive Supply Voltage Above GND (V^+) . . . . . +10.8V to +16.5V
Negative Supply Voltage Below GND (V^-) . . . . . -10.8V to -16.5V
Supply Voltage Differential (V^+ to V^-) . . . . . 21.6V to 33V
VREF to GND . . . . . 4.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

8. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379 for details.
9. For θ_{JC}, the "case temp" location is the center of the package underside.
10. Tested in a heavy ion environment at LET = 86.3MeV • cm^2/mg at +125°C.

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Analog Input Signal Range	V_S		V^-	-	V^+	V
Channel ON-Resistance	r_{ON}	V± = ±15.0V, ±16.5V, $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA, V_{IN} = +5V, -5V	-	-	**500**	Ω
		V± = ±15.0V, ±16.5V, $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA, V_{IN} = V^+, V^-	-	-	**700**	Ω
r_{ON} Match Between Channels	Δr_{ON}	V_{IN} = +5V, -5V; $V_{\overline{EN}}$ = 0V, I_{OUT} = -1mA	-	10	**20**	Ω
ON-Resistance Flatness	$R_{FLAT(ON)}$	V_{IN} = +5V, -5V, $V_{\overline{EN}}$ = 0V,	-	-	**25**	Ω
Switch Off Leakage	$I_{S(OFF)}$	V_{IN} = V^+ - 5V, V± = ±16.5V All unused inputs are tied to V^- + 5V	-10	-	10	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V^- + 5V, V± = ±16.5V All other inputs = V^+ - 5V T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-100	-	100	nA
Switch Off Leakage with Device Powered Off	$I_{S(OFF)\ POWER\ OFF}$	V_{IN} = +25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, V± = $V_{\overline{EN}}$ = V_A = V_{REF} = 0V T_A = +25°C, V± = 0V	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total Ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total Ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Switch Off Leakage with Device Powered OPEN	$I_{S(OFF)}$ POWER OPEN	V_{IN} = +25V, $V_{\overline{EN}}$ = V_A = V_{REF} = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-10	-	80	nA
		Post radiation	-100	-	100	nA
		V_{IN} = -25V, $V_{\overline{EN}}$ = V_A = V_{REF} = 0V V± = OPEN, T_A = +25°C	-10	-	10	nA
		T_A = -55°C, +125°C	-80	-	10	nA
		Post radiation	-100	-	100	nA
Switch On Leakage Current into the Drain (Overvoltage)	$I_{D(ON)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-	**10**	nA
		Post radiation	**-10**	-	**10**	nA
		V_{IN} = -35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-	**10**	nA
		Post radiation	**-10**	-	**10**	nA
Switch On Leakage Current into the Source (Overvoltage)	$I_{S(ON)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**1**	250	**500**	µA
		Post radiation	**1**	-	**500**	µA
		V_{IN} = -35V, V_{OUT} = 0V, $V_{\overline{EN}}$ = 0V, All unused switch inputs = GND, V± = ±16.5V	**-10**	-5.5	**-1**	µA
		Post radiation	**-10**	-	**-1**	µA
Switch Off Leakage Current into the Source (Overvoltage)	$I_{S(OFF)\ OVERVOLT}$	V_{IN} = +35V, V_{OUT} = 0V, T_A = +25°C, -55°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-80	-	80	nA
		Post radiation	-750	-	750	nA
		V_{IN} = -35V, V_{OUT} = 0V, T_A = +25°C All unused switch inputs = GND, V± = ±16.5V	-10	-	10	nA
		T_A = -55°C	-2	-	2	µA
		T_A = +125°C	-20	-	20	nA
		Post radiation	-750	-	750	nA
Switch Off Leakage	$I_{D(OFF)}$	V_{OUT} = V^+ - 5V, all inputs = V^- + 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-80	-	80	nA
		V_{OUT} = V^- + 5V, all inputs = V^+ - 5V V± = ±16.5V, T_A = +25°C, -55°C	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-80	-	80	nA

Electrical Specifications (±15V)

V^+ = 15V, V^- = -15V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Switch Off Leakage Current into the Drain (Overvoltage)	$I_{D(OFF)\ OVERVOLT}$	V_{OUT} = 0V, V_{IN} = +35V, V± = ±16.5V All unused inputs are tied to GND	-10	-	10	nA
		Post radiation	-500	-	500	nA
		V_{OUT} = 0V, V_{IN} = -35V, V± = ±16.5V All unused inputs are tied to GND	-10	-	10	nA
		Post radiation	-500	-	500	nA
Switch On Leakage Current into the Source/Drain	$I_{D(ON)}$	V_{IN} = V_{OUT} = V^+ - 5V, $V_{\overline{EN}}$ = 0V, T_A = +25°C, -55°C, All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	0	-	120	nA
		Post radiation	-100	-	100	nA
		V_{IN} = V_{OUT} = V^- + 5V, $V_{\overline{EN}}$ = 0V, T_A = +25°C, -55°C, All unused inputs = V^- + 5V, V± = ±16.5V	-10	-	10	nA
		T_A = +125°C	-120	-	0	nA
		Post radiation	-100	-	100	nA
Logic Input High/Low Voltage	$V_{AH/L}$, $V_{ENH/L}$	V_{REF} = 5.0V	**1.2**	-	**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V_A = $V_{\overline{EN}}$ = 4.0V V^+= 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V_A = $V_{\overline{EN}}$ = 0.8V V^+ = 16.5V, V^- = -16.5V	**-100**	-	**100**	nA
Quiescent Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**-400**	-	-	µA
Standby Supply Current	I+	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	-	-	**400**	µA
	I-	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**-400**	-	-	µA
Quiescent Supply Current Into V_{REF}	I_{REF}	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 0.8V, V± = ±15.0V, ±16.5V	**10**	-	**35**	µA
Standby Current Into V_{REF}	$I_{REF(STBY)}$	V_{REF} = 5.5V, V_{IN} = 0V, V_A = 0.8V, $V_{\overline{EN}}$ = 4.0V, V± = ±15.0V, ±16.5V	**10**	-	**35**	µA
DYNAMIC						
Transition Time	t_{ALH}	Figures 5, 6	-	0.5	**800**	ns
Transition Time	t_{AHL}	Figures 5, 6	-	0.5	**800**	ns
Break-Before-Make Delay	t_{BBM}	Figures 9, 10 T_A = -55°C, +25°C, +125°C	5	50	200	ns
		Post radiation	5	-	400	ns
Enable Turn-On Time	t_{ENABLE}	Figures 7, 8 T_A = -55°C, +25°C, +125°C	-	0.5	600	ns
		Post radiation	-	-	800	ns
Disable Turn-Off Time	$t_{DISABLE}$	Figures 7, 8 T_A = -55°C, +25°C, +125°C	-	0.5	600	ns
		Post radiation	-	-	800	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, (Figure 7)	-	2	5	pC

Electrical Specifications (±15V)

$V^+ = 15V$, $V^- = -15V$, $V_{AH} = 4.0V$, $V_{AL} = 0.8V$, $V_{REF} = V_{\overline{EN}} = 5.0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Off Isolation	V_{ISO}	$V_{\overline{EN}} = 4V$, $R_L = 1k\Omega$, f = 200kHz, $C_L = 7pF$, $V_{RMS} = 3V$	75	-	-	dB
Crosstalk	V_{CT}	$V_{\overline{EN}} = 0.8V$, $R_L = 1k\Omega$, f = 200kHz, $C_L = 7pF$, $V_{RMS} = 3V$	47	-	-	dB
Digital Input Capacitance	C_A	f = 1MHz, $V^+ = V^- = 0V$	-	-	**7**	pF
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz, $V^+ = V^- = 0V$	-	-	**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz, $V^+ = V^- = 0V$	-	-	**50**	pF

Electrical Specifications (±12V)

$V^+ = 12V$, $V^- = -12V$, $V_{AH} = 4.0V$, $V_{AL} = 0.8V$, $V_{REF} = V_{\overline{EN}} = 5.0V$, $T_A = +25°C$, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Analog Input Signal Range	V_S		V^-		V^+	V
Channel ON-Resistance	r_{ON}	V± = ±10.8V, ±13.2V $I_{OUT} = -1mA$, $V_{IN} = +5V, -5V$, $V_{\overline{EN}} = 0V$	-	-	**500**	Ω
		V± = ±10.8V, ±13.2V $I_{OUT} = -1mA$, $V_{IN} = V^+, V^-$, $V_{\overline{EN}} = 0V$	-	-	**700**	Ω
r_{ON} Match Between Channels	Δr_{ON}	$V_{IN} = +5V, -5V$; $I_{OUT} = -1mA$, $V_{\overline{EN}} = 0V$	-	10	**20**	Ω
ON-Resistance Flatness	$R_{FLAT(ON)}$	$V_{IN} = +5V, -5V$, V± = ±13.2V, $V_{\overline{EN}} = 0V$	-	-	**25**	Ω
		$V_{IN} = +5V, -5V$, V± = ±10.8V, $V_{\overline{EN}} = 0V$, $T_A = +25°C, -55°C, +125°C$	-	-	30	Ω
		$V_{IN} = +5V, -5V$, V± = ±10.8V, $V_{\overline{EN}} = 0V$, post radiation, $T_A = +25°C$	-	-	40	Ω
Quiescent Supply Current	I+	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 0.8V$, V± = ±10.8V, ±13.2V	-	-	**400**	µA
	I-	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 0.8V$, V± = ±10.8V, ±13.2V	**-400**	-	-	µA
Standby Supply Current	I+	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 4.0V$, V± = ±10.8V, ±13.2V	-	-	**400**	µA
	I-	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 4.0V$, V± = ±10.8V, ±13.2V	**-400**	-	-	µA
Quiescent Supply Current Into V_{REF}	I_{REF}	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 0.8V$, V± = ±10.8V, ±13.2V	-	-	**35**	µA
Standby Current Into V_{REF}	$I_{REF(STBY)}$	$V_{REF} = 5.5V$, $V_{IN} = 0V$, $V_A = 0.8V$, $V_{\overline{EN}} = 4.0V$, V± = ±10.8V, ±13.2V	-	-	**35**	µA
DYNAMIC						
Transition Time	t_{ALH}	Figures 5, 6	-	0.5	800	ns
Transition Time	t_{AHL}	Figures 5, 6	-	0.5	800	ns
Break-Before-Make Delay	t_{BBM}	Figures 9, 10 $T_A = -55°C, +25°C, +125°C$	5	50	200	ns
		Post radiation	5	-	400	ns
Enable Turn-On Time	t_{ENABLE}	Figures 7, 8 $T_A = -55°C, +25°C, +125°C$	-	0.5	600	ns
		Post radiation	-	-	800	ns

Electrical Specifications (±12V) V^+ = 12V, V^- = -12V, V_{AH} = 4.0V, V_{AL} = 0.8V, V_{REF} = $V_{\overline{EN}}$ = 5.0V, T_A= +25°C, unless otherwise noted.

Boldface limits apply across the operating temperature range, -55°C to +125°C or across a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50 to 300krad(Si)/s or a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Disable Turn-Off Time	$t_{DISABLE}$	Figures 7, 8 T_A = -55°C, +25°C, +125°C	-	0.5	600	ns
		Post radiation	-	-	800	ns

NOTE:

11. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

TABLE 2. TRUTH TABLE

A4	A3	A2	A1	A0	EN	"ON"-CHANNEL
X	X	X	X	X	1	None
0	0	0	0	0	0	1
0	0	0	0	1	0	2
0	0	0	1	0	0	3
0	0	0	1	1	0	4
0	0	1	0	0	0	5
0	0	1	0	1	0	6
0	0	1	1	0	0	7
0	0	1	1	1	0	8
0	1	0	0	0	0	9
0	1	0	0	1	0	10
0	1	0	1	0	0	11
0	1	0	1	1	0	12
0	1	1	0	0	0	13
0	1	1	0	1	0	14
0	1	1	1	0	0	15
0	1	1	1	1	0	16
1	0	0	0	0	0	17
1	0	0	0	1	0	18
1	0	0	1	0	0	19
1	0	0	1	1	0	20
1	0	1	0	0	0	21
1	0	1	0	1	0	22
1	0	1	1	0	0	23
1	0	1	1	1	0	24
1	1	0	0	0	0	25
1	1	0	0	1	0	26
1	1	0	1	0	0	27
1	1	0	1	1	0	28
1	1	1	0	0	0	29
1	1	1	0	1	0	30

TABLE 2. TRUTH TABLE (Continued)

A4	A3	A2	A1	A0	EN	"ON"-CHANNEL
1	1	1	1	0	0	31
1	1	1	1	1	0	32

NOTE: X = Don't care, "1" = Logic High, "0" = Logic Low

Block Diagram

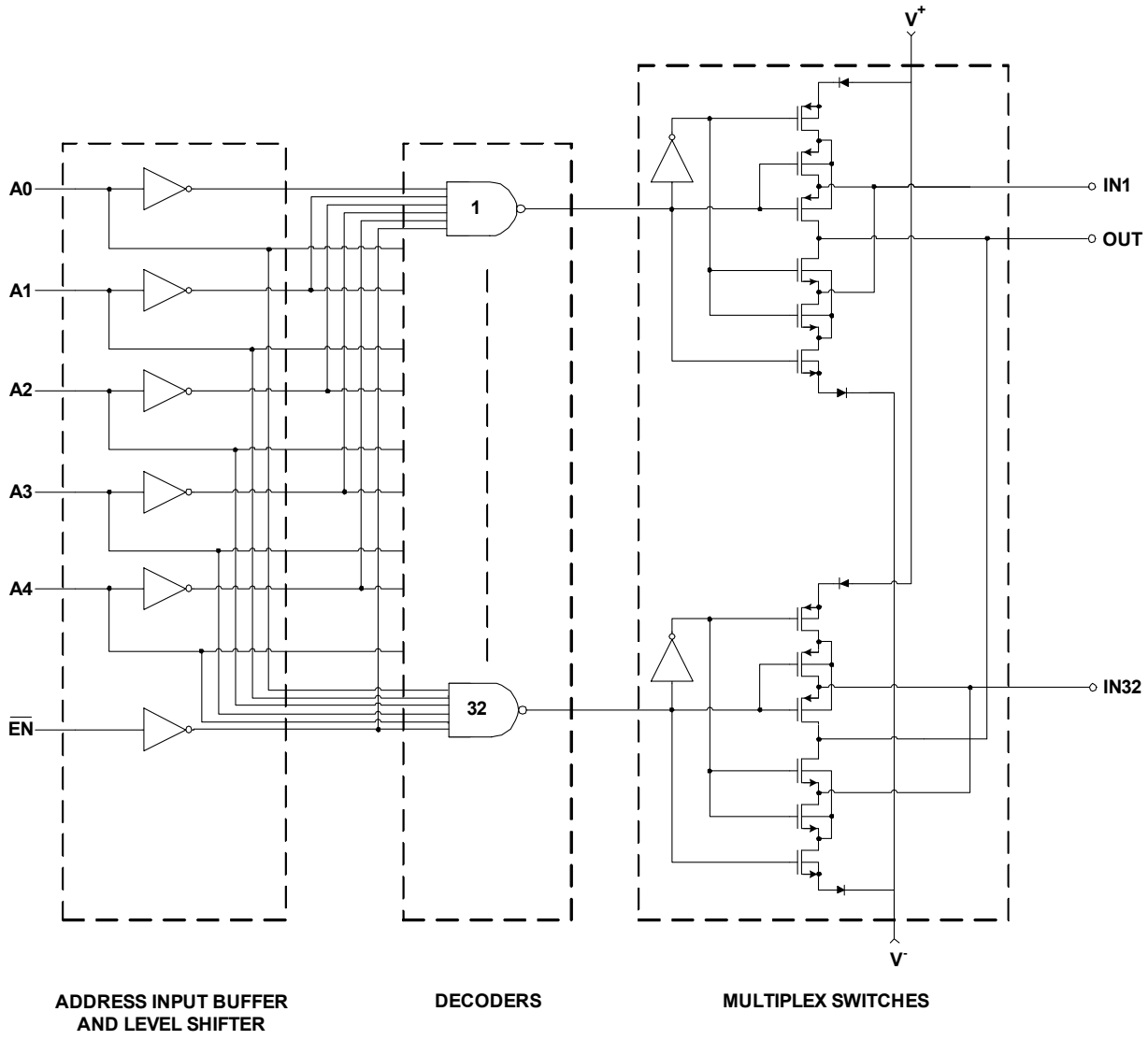


FIGURE 4. BLOCK DIAGRAM

Timing Diagrams

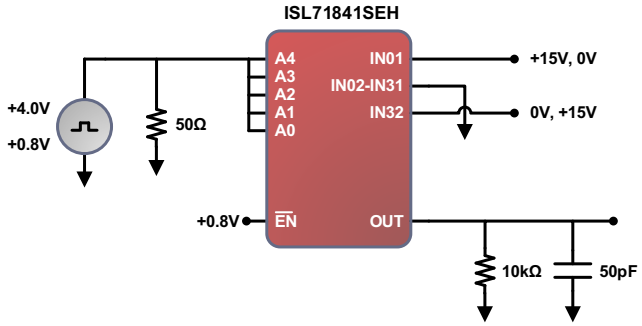


FIGURE 5. ADDRESS TIME TO OUTPUT TEST CIRCUIT

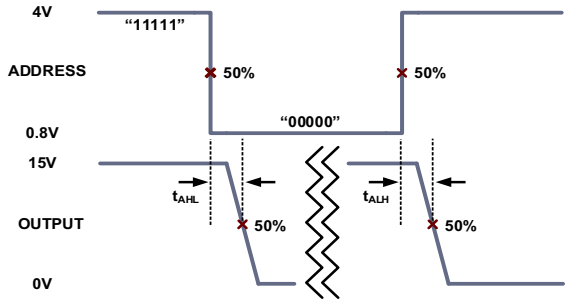


FIGURE 6. ADDRESS TIME TO OUTPUT DIAGRAM

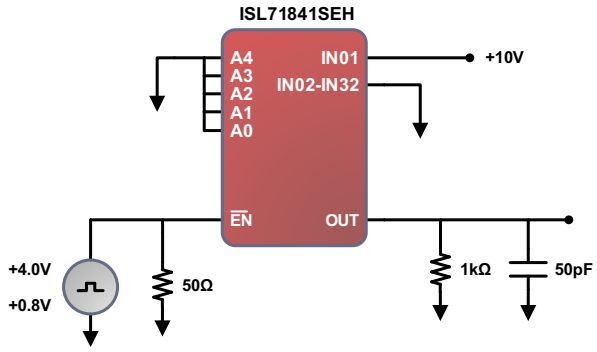


FIGURE 7. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

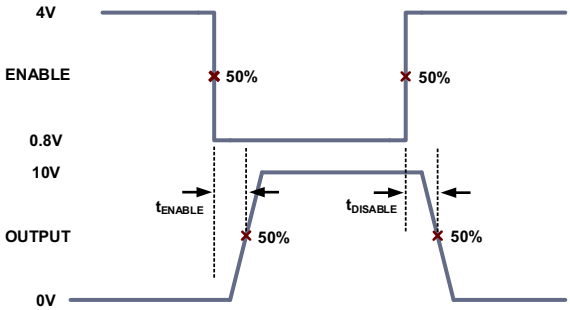


FIGURE 8. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

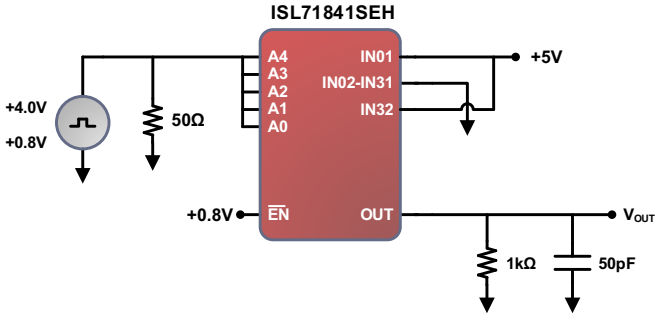


FIGURE 9. BREAK-BEFORE-MAKE TEST CIRCUIT

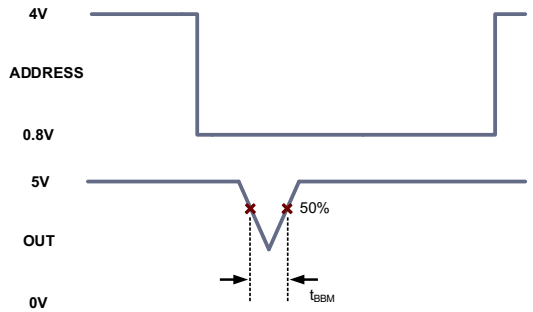


FIGURE 10. BREAK-BEFORE-MAKE DIAGRAM

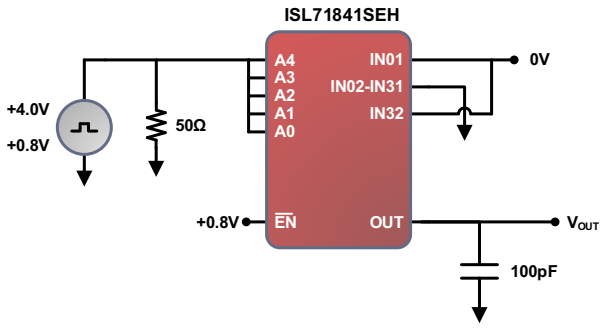


FIGURE 11. CHARGE INJECTION TEST CIRCUIT

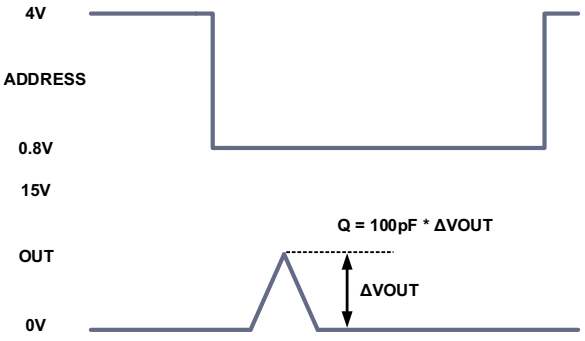


FIGURE 12. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified.

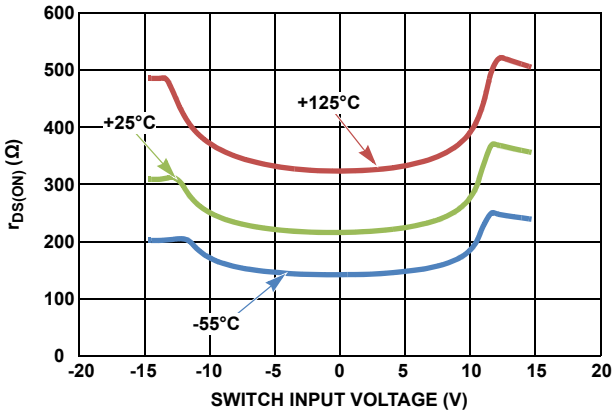


FIGURE 13. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 14.5V$)

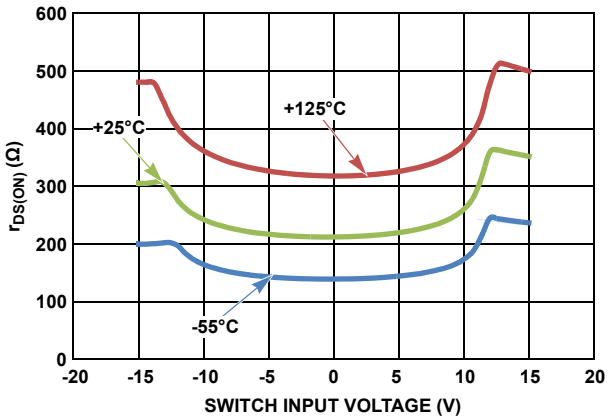


FIGURE 14. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 15.0V$)

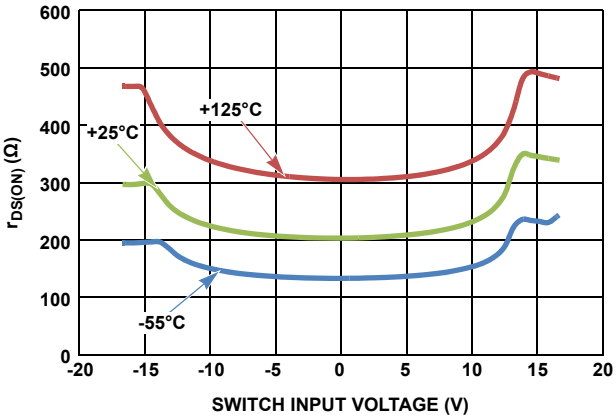


FIGURE 15. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 16.5V$)

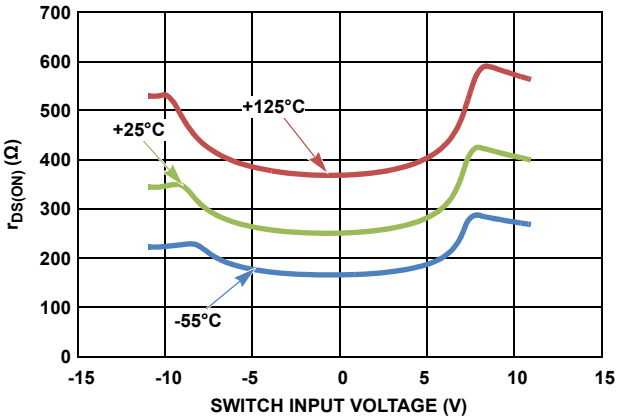


FIGURE 16. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 10.8V$)

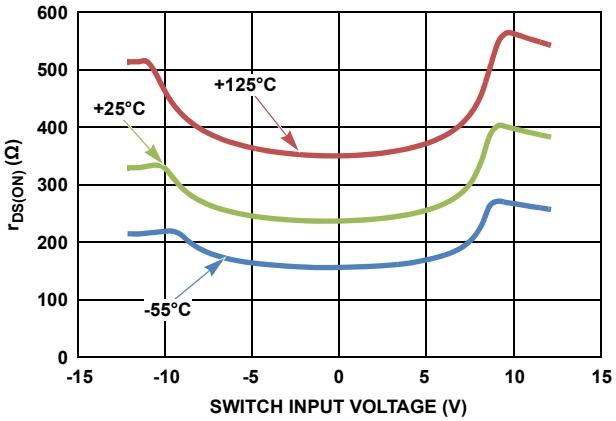


FIGURE 17. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 12.0V$)

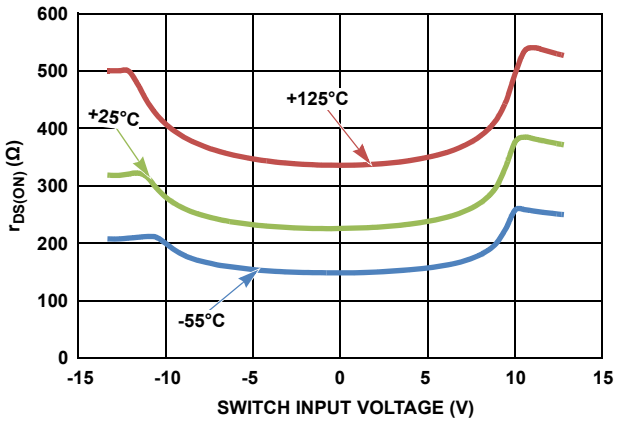


FIGURE 18. $r_{DS(ON)}$ vs V_{CM} ($V\pm = 13.2V$)

Typical Performance Curves

$V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Continued)

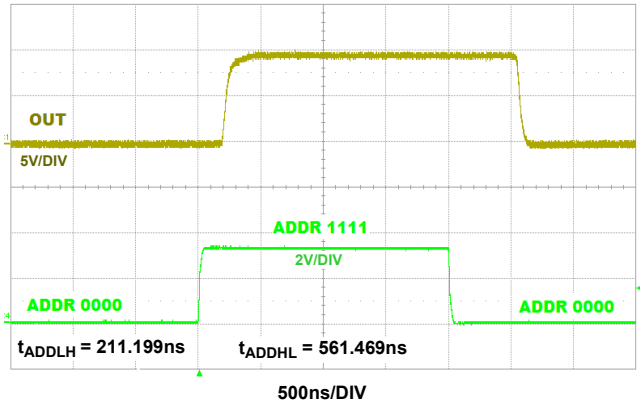


FIGURE 19. TYPICAL ADDRESS TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

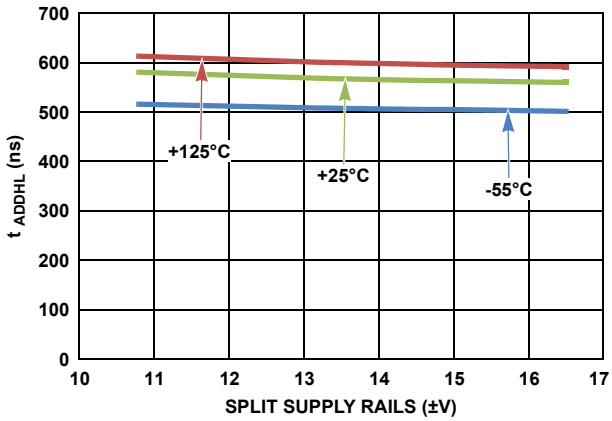


FIGURE 20. ADDRESS TO OUTPUT DELAY (HIGH TO LOW)

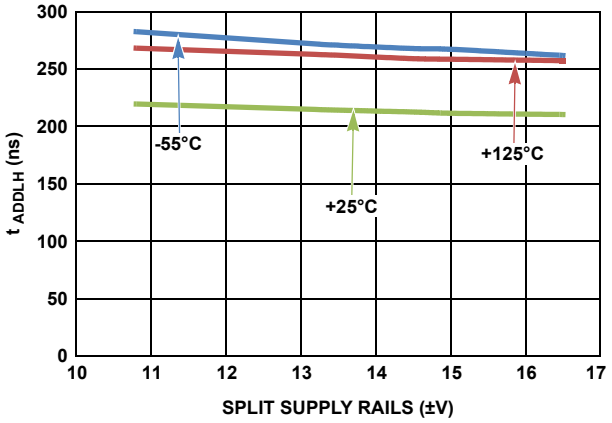


FIGURE 21. ADDRESS TO OUTPUT DELAY (LOW TO HIGH)

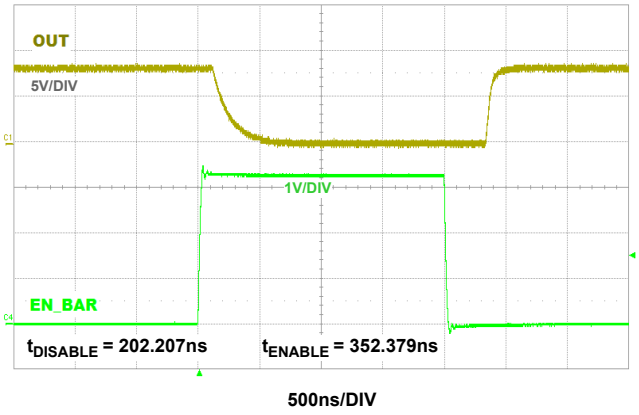


FIGURE 22. TYPICAL ENABLE TO OUTPUT DELAY ($V\pm = \pm15V$, $+25°C$)

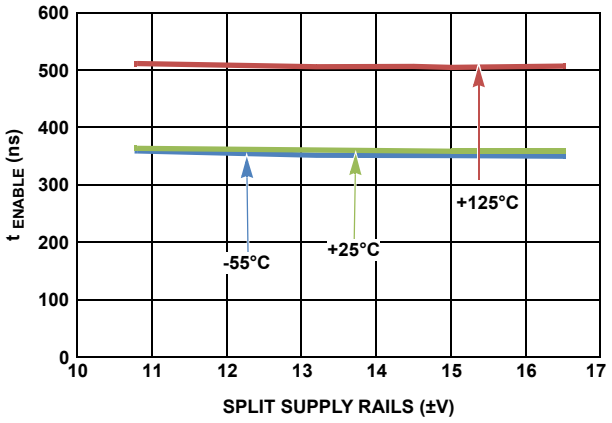


FIGURE 23. ENABLE TO OUTPUT DELAY (LOW TO HIGH)

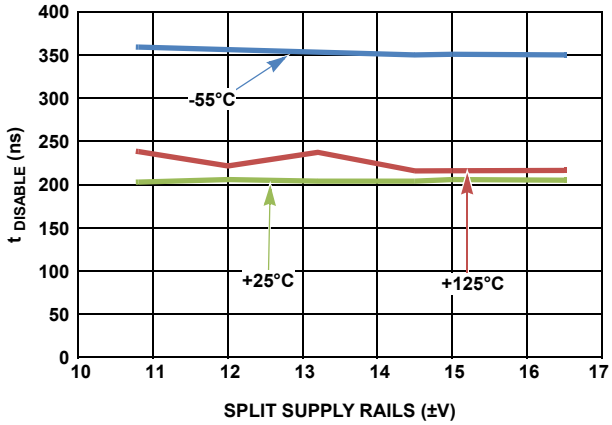


FIGURE 24. DISABLE TO OUTPUT DELAY (LOW TO HIGH)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Continued)

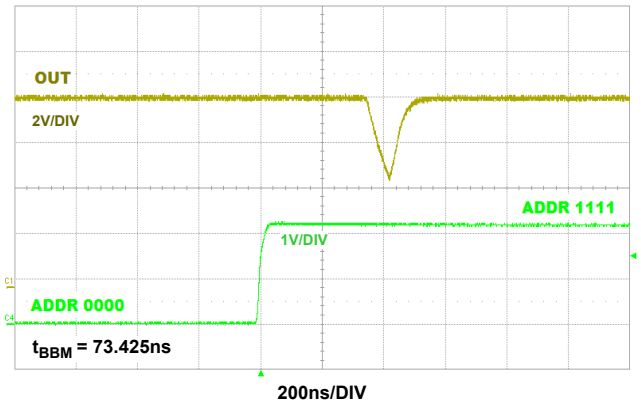


FIGURE 25. TYPICAL BREAK-BEFORE-MAKE DELAY (V± = 15V, +25°C)

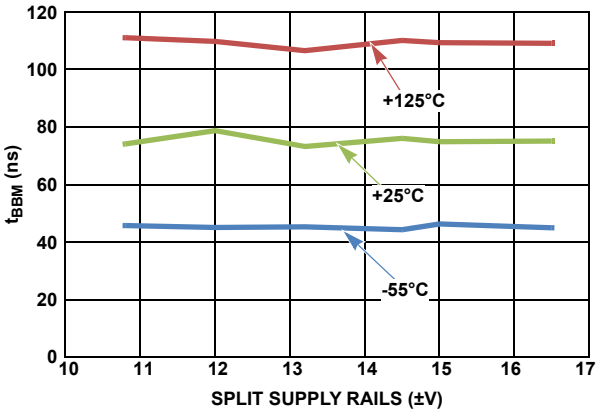


FIGURE 26. BREAK-BEFORE-MAKE DELAY

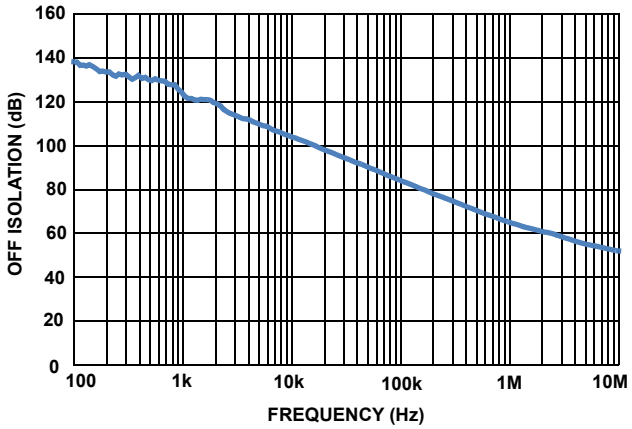


FIGURE 27. OFF ISOLATION (V± = ±15V, R_L = 1kΩ, +25°C)

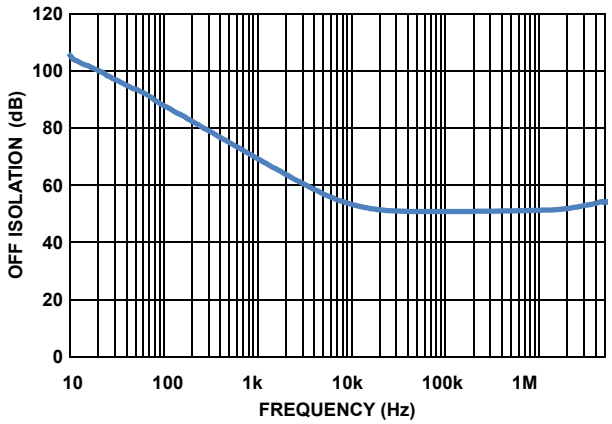


FIGURE 28. OFF ISOLATION (V± = ±15V, R_L = OPEN, +25°C)

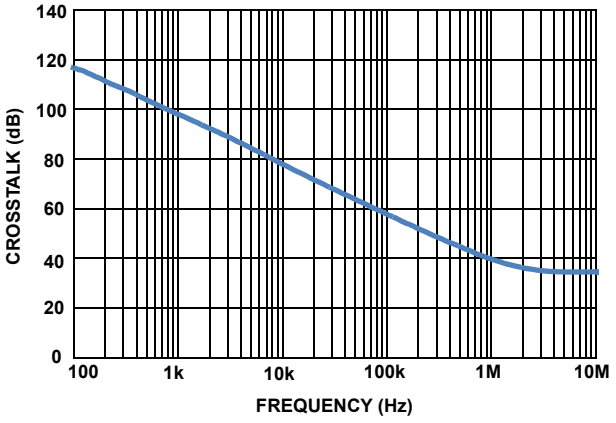


FIGURE 29. CROSSTALK (V± = ±15V, R_L = 1kΩ, +25°C)

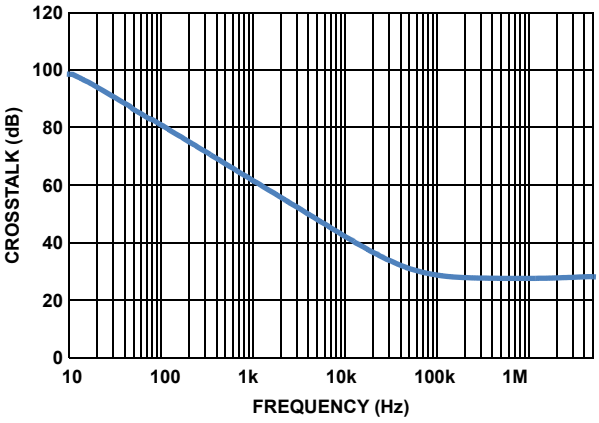


FIGURE 30. CROSSTALK (V± = ±15V, R_L = OPEN, +25°C)

Typical Performance Curves $V\pm = \pm15V$, $V_{CM} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Continued)

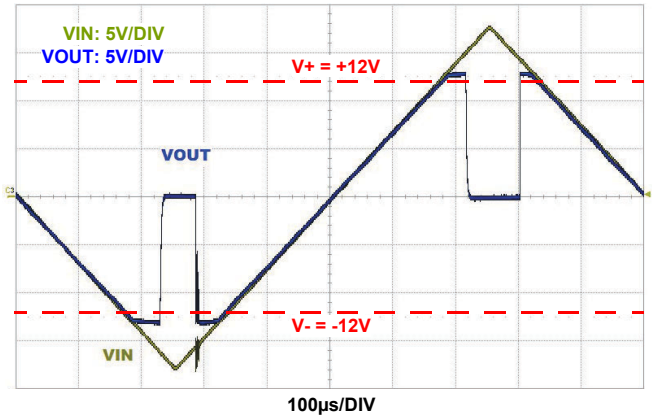


FIGURE 31. OVERVOLTAGE/UNDERVOLTAGE PROTECTION (+25°C)

Post High Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits, nor are they guaranteed.

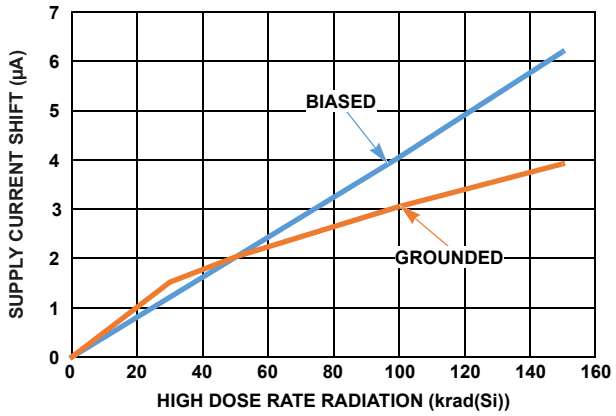


FIGURE 32. I_{CC} SUPPLY CURRENT SHIFT vs HDR RADIATION

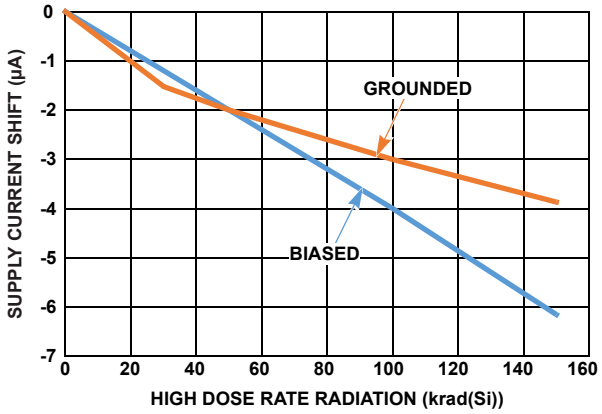


FIGURE 33. I_{EE} SUPPLY CURRENT SHIFT vs HDR RADIATION

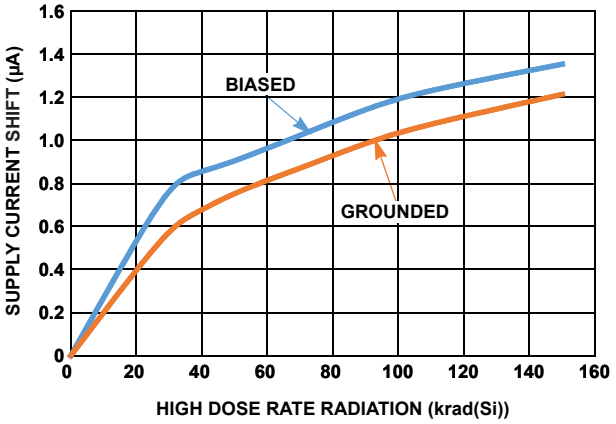


FIGURE 34. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

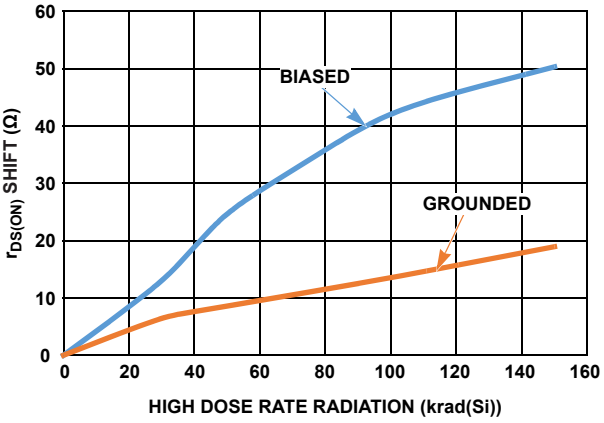


FIGURE 35. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs HDR RADIATION

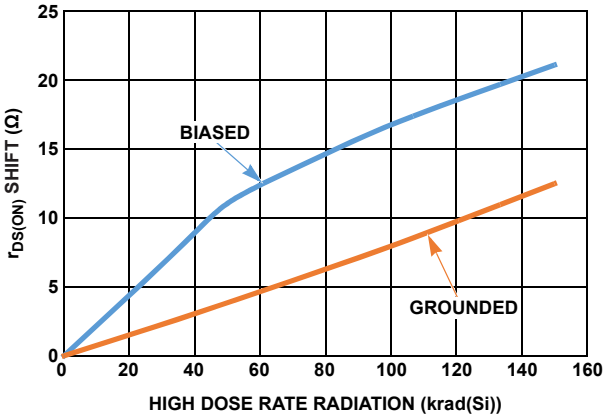


FIGURE 36. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

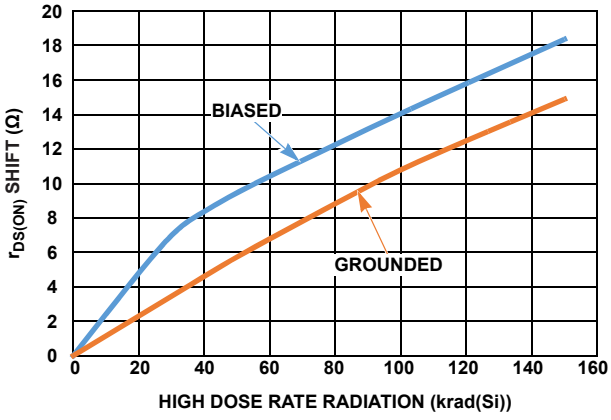


FIGURE 37. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics ($V\pm$ = ±15V)

Unless otherwise specified, $V\pm$ = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

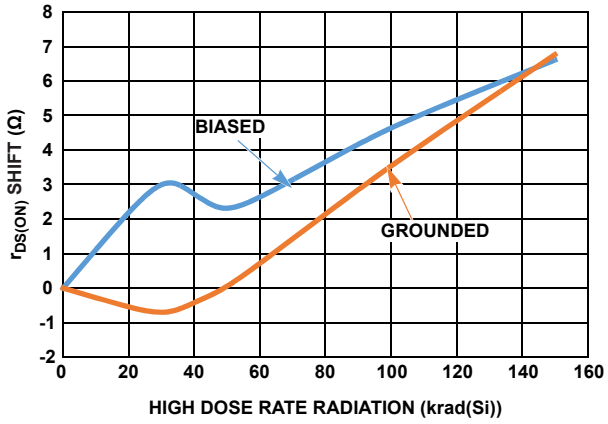


FIGURE 38. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

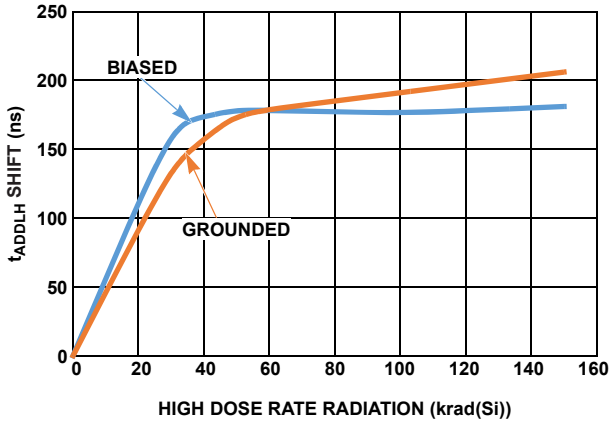


FIGURE 39. t_{ADD} SHIFT (LOW TO HIGH) vs HDR RADIATION

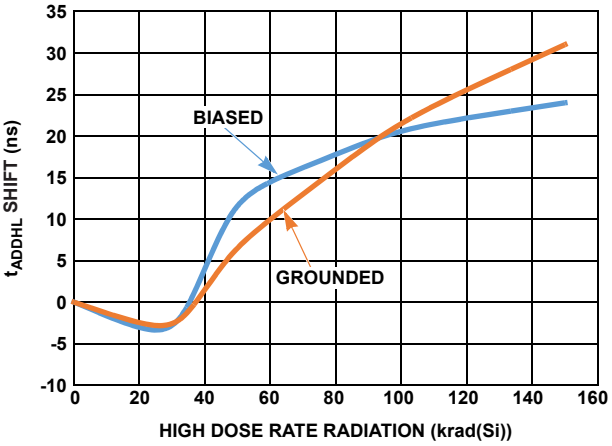


FIGURE 40. t_{ADD} SHIFT (HIGH TO LOW) vs HDR RADIATION

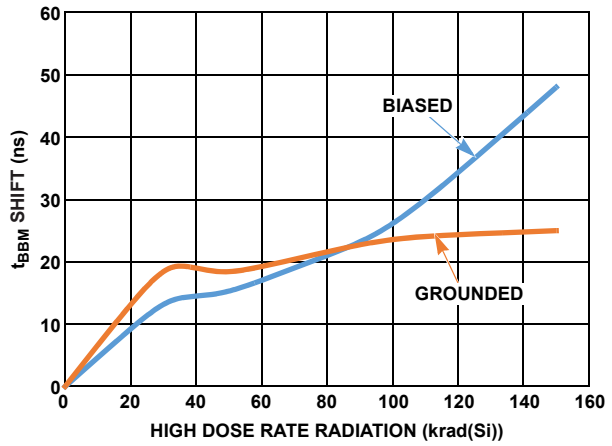


FIGURE 41. t_{BBM} SHIFT vs HDR RADIATION

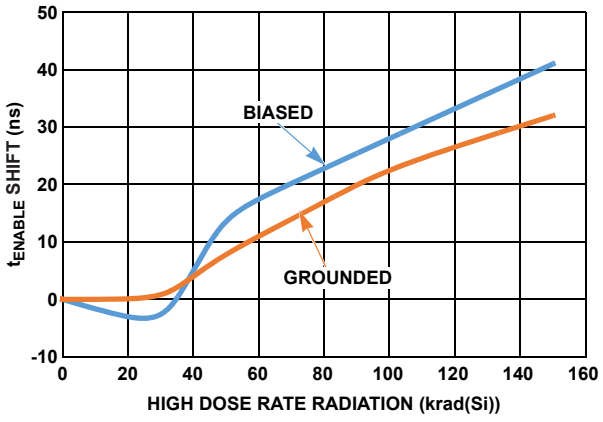


FIGURE 42. t_{ENABLE} SHIFT vs HDR RADIATION

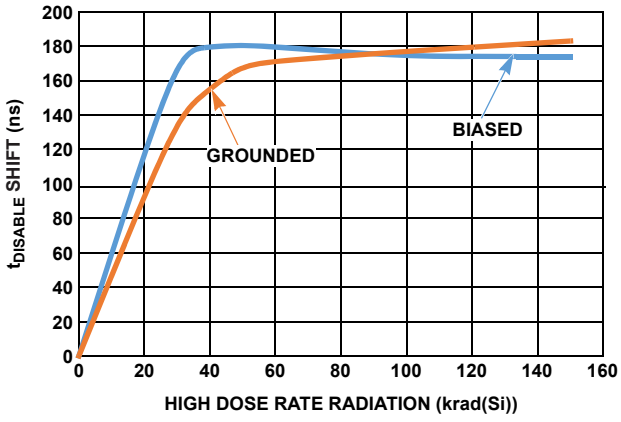


FIGURE 43. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits, nor are they guaranteed.

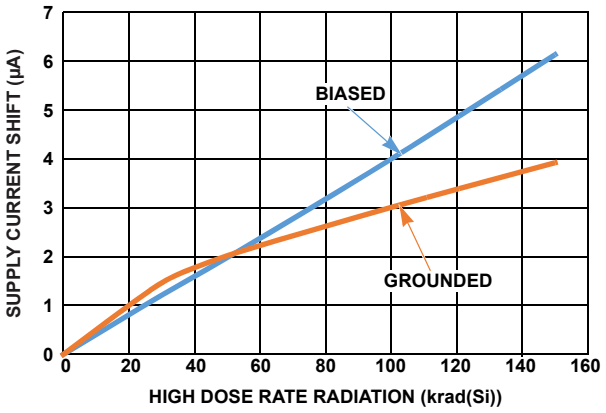


FIGURE 44. I_{CC} SUPPLY CURRENT SHIFT vs HDR RADIATION

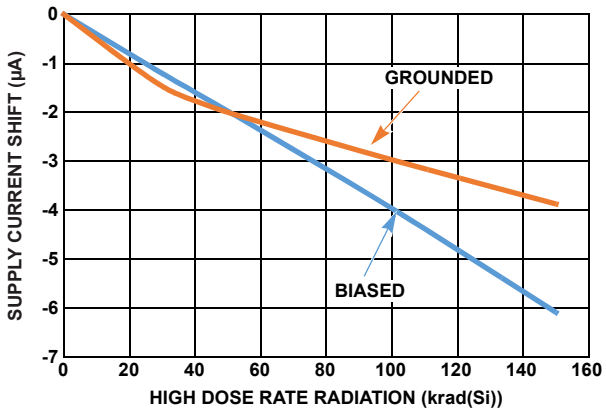


FIGURE 45. I_{EE} SUPPLY CURRENT SHIFT vs HDR RADIATION

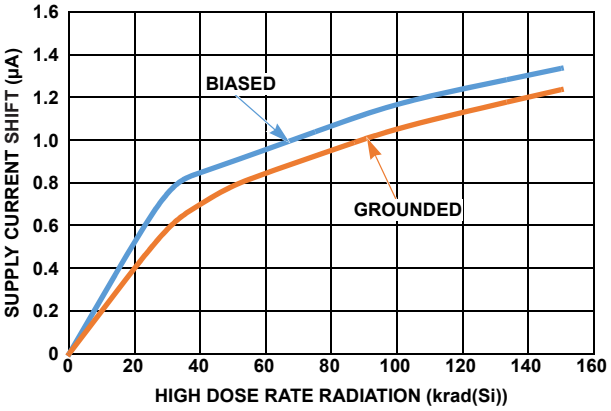


FIGURE 46. I_{REF} SUPPLY CURRENT SHIFT vs HDR RADIATION

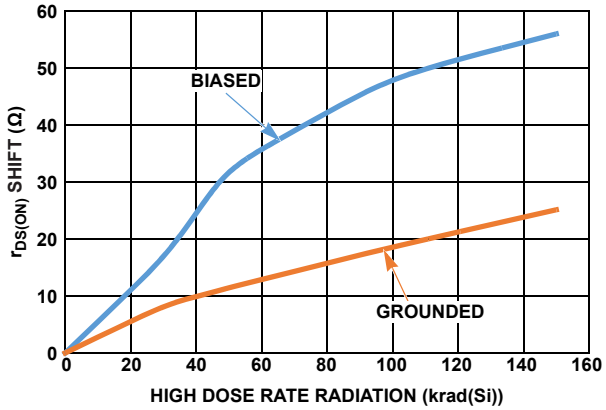


FIGURE 47. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs HDR RADIATION

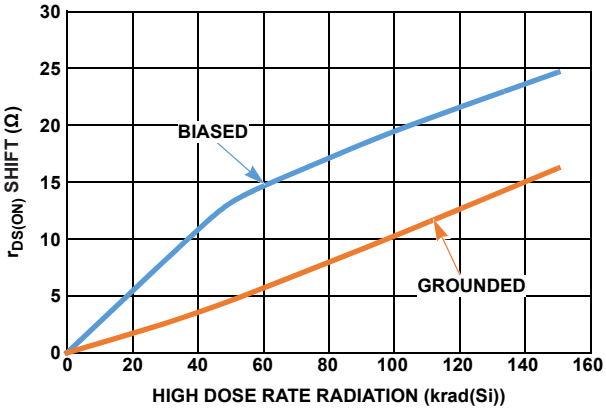


FIGURE 48. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs HDR RADIATION

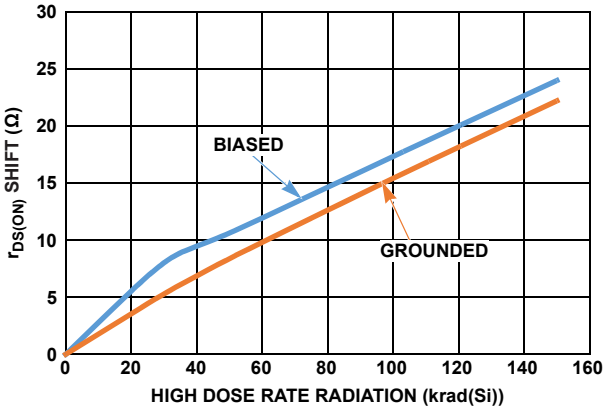


FIGURE 49. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs HDR RADIATION

Post High Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

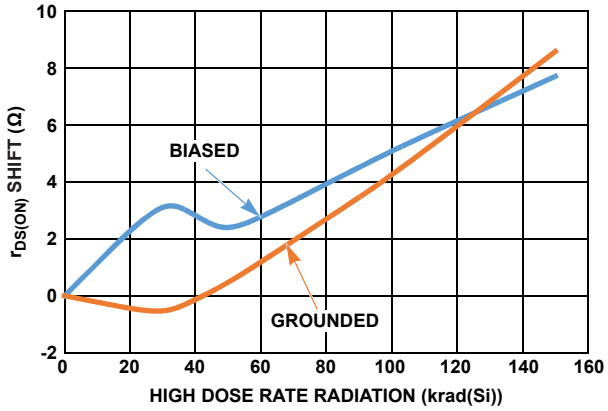


FIGURE 50. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs HDR RADIATION

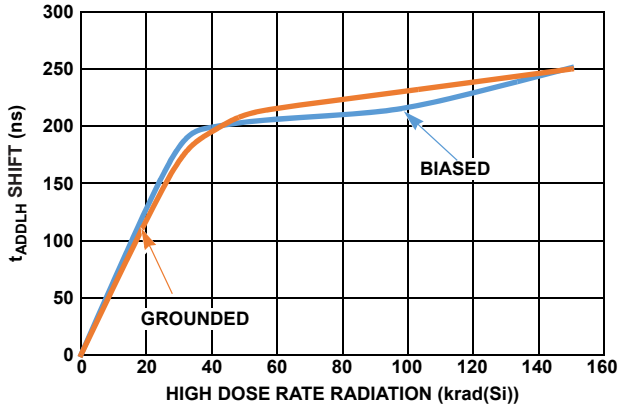


FIGURE 51. t_{ADD} SHIFT (LOW TO HIGH) vs HDR RADIATION

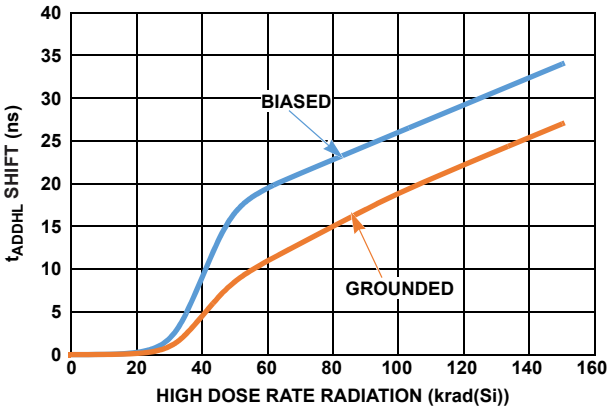


FIGURE 52. t_{ADD} SHIFT (HIGH TO LOW) vs HDR RADIATION

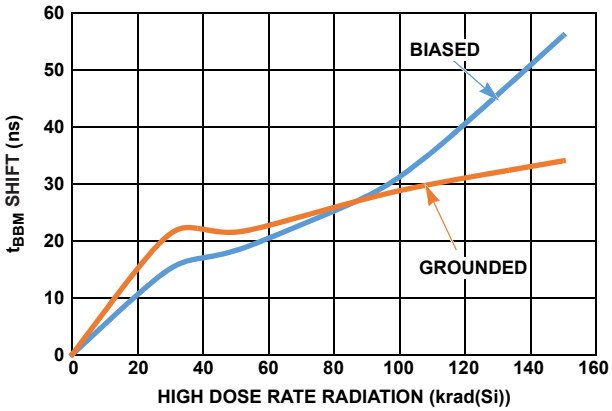


FIGURE 53. t_{BBM} SHIFT vs HDR RADIATION

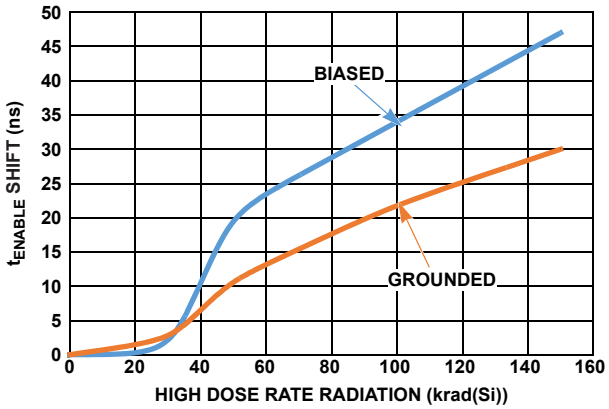


FIGURE 54. t_{ENABLE} SHIFT vs HDR RADIATION

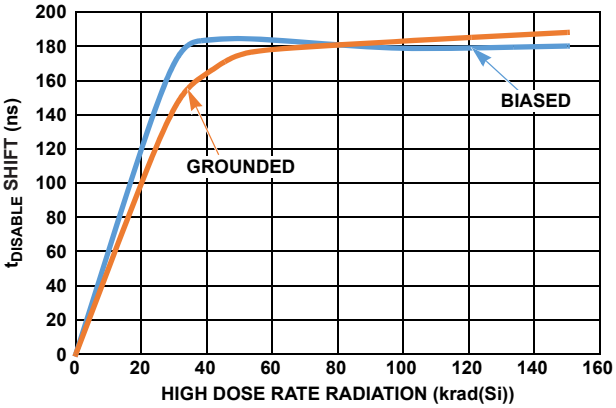


FIGURE 55. $t_{DISABLE}$ SHIFT vs HDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

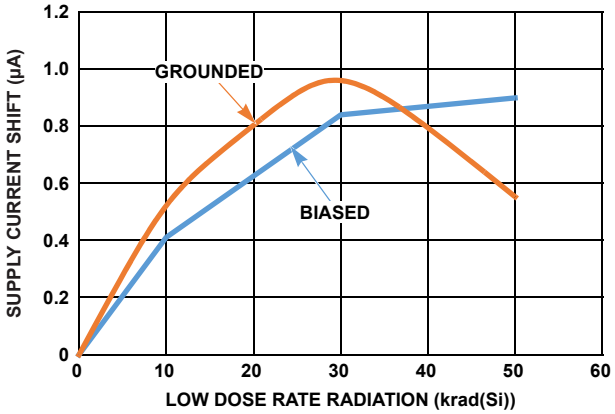


FIGURE 56. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

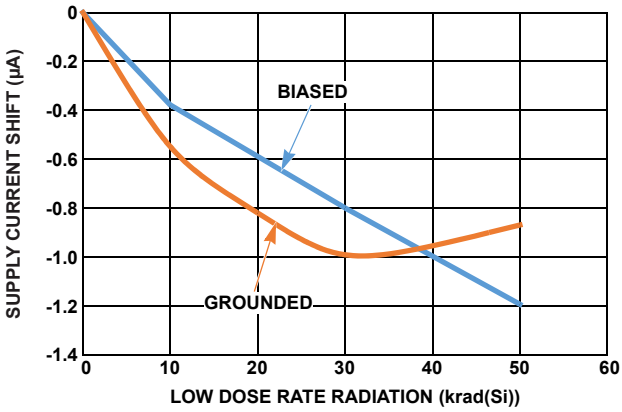


FIGURE 57. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

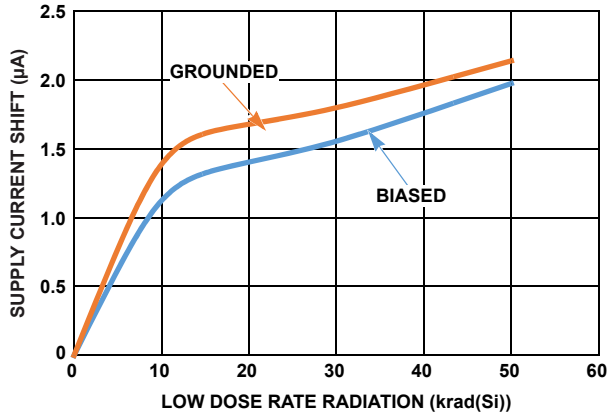


FIGURE 58. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

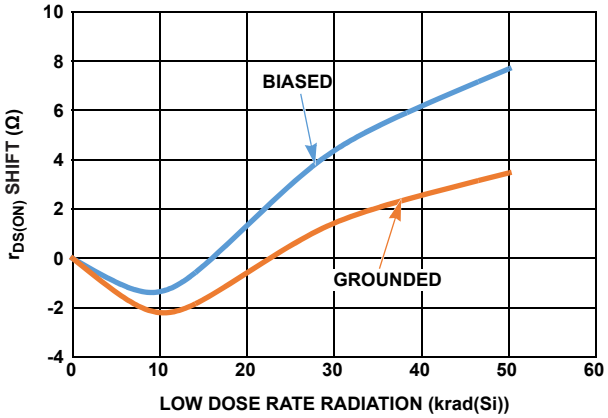


FIGURE 59. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

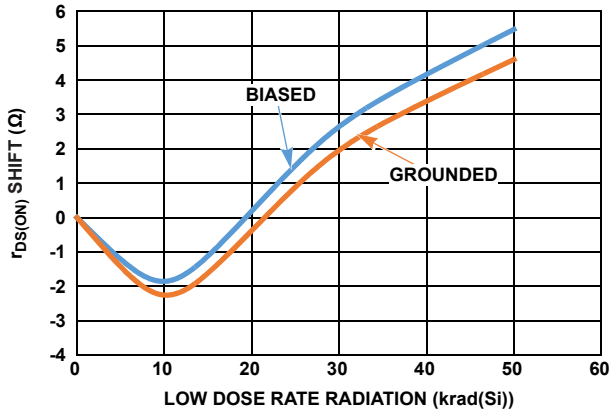


FIGURE 60. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

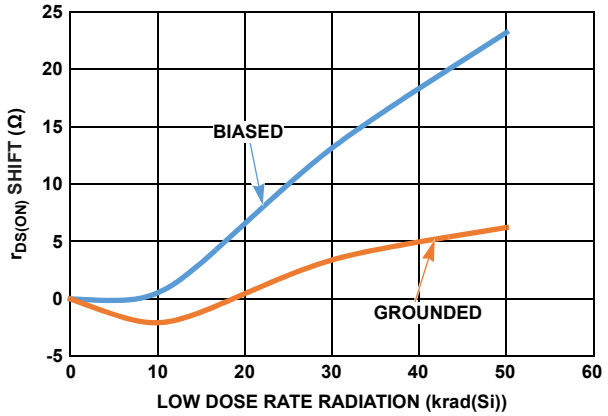


FIGURE 61. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±15V)

Unless otherwise specified, V± = ±15V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

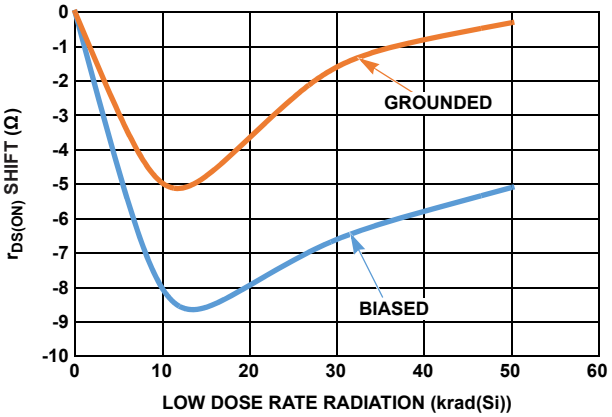


FIGURE 62. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

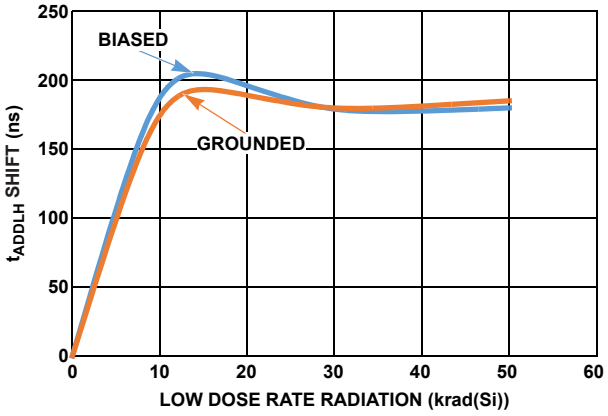


FIGURE 63. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

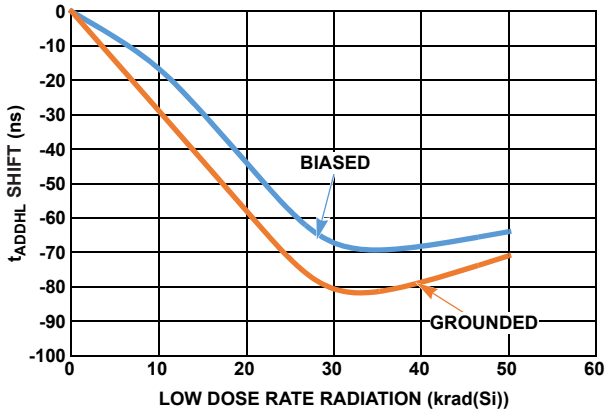


FIGURE 64. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

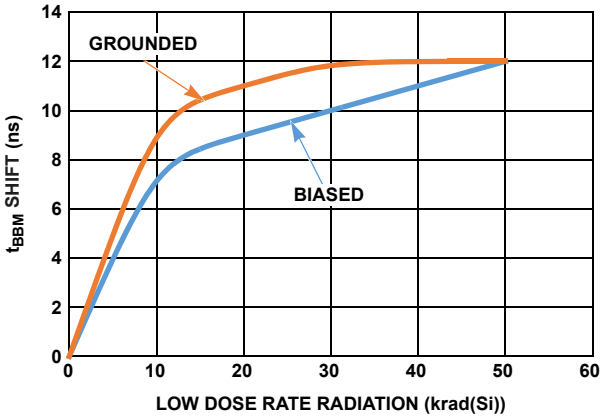


FIGURE 65. t_{BBM} SHIFT vs LDR RADIATION

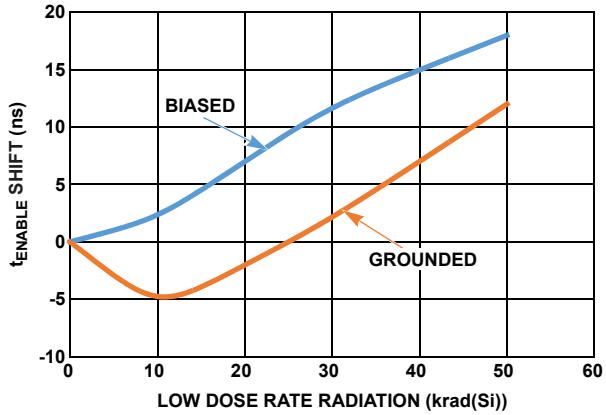


FIGURE 66. t_{ENABLE} SHIFT vs LDR RADIATION

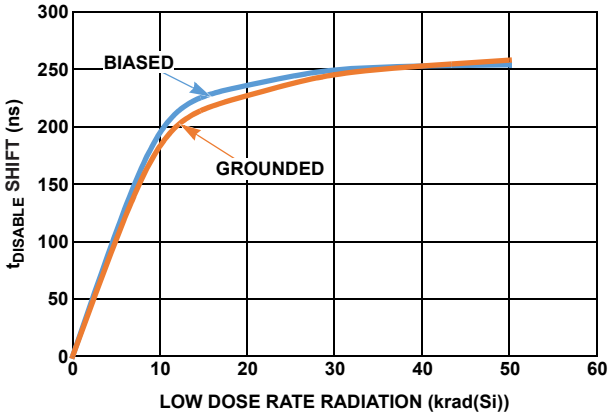


FIGURE 67. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics ($V\pm$ = ±12V)

Unless otherwise specified, $V\pm$ = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed.

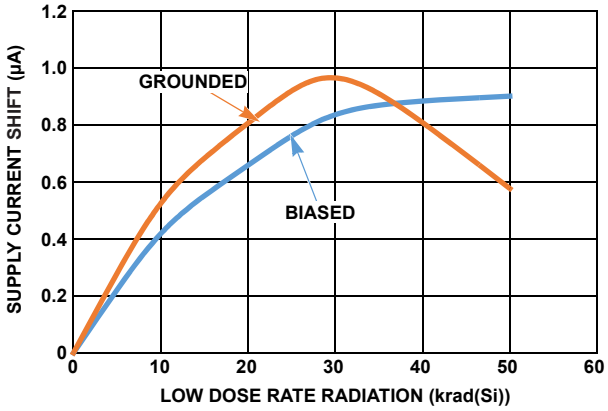


FIGURE 68. I_{CC} SUPPLY CURRENT SHIFT vs LDR RADIATION

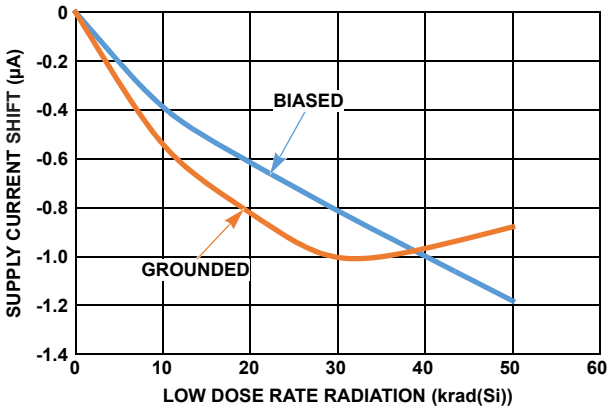


FIGURE 69. I_{EE} SUPPLY CURRENT SHIFT vs LDR RADIATION

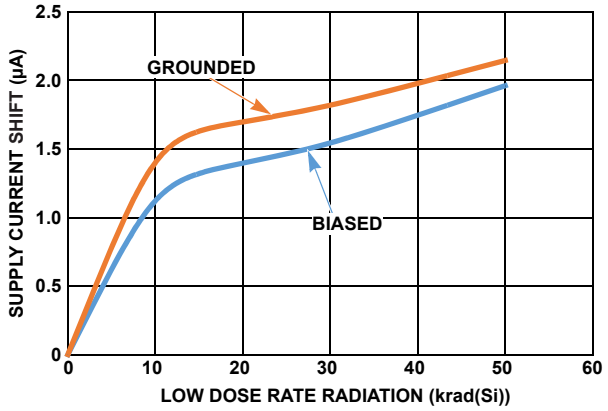


FIGURE 70. I_{REF} SUPPLY CURRENT SHIFT vs LDR RADIATION

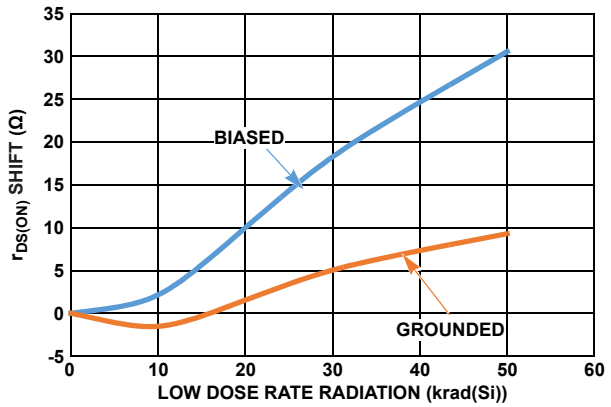


FIGURE 71. $r_{DS(ON)}$ SHIFT (V_{IN} = V^+) vs LDR RADIATION

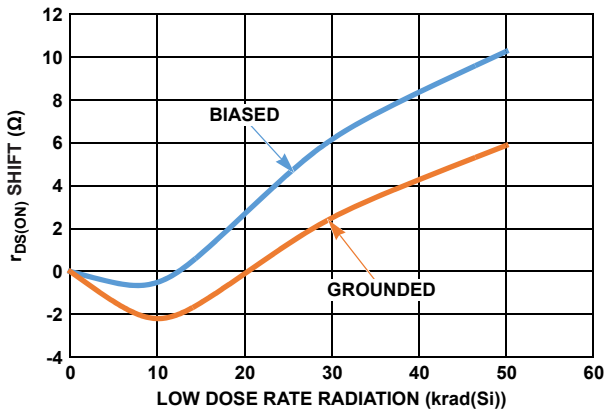


FIGURE 72. $r_{DS(ON)}$ SHIFT (V_{IN} = +5V) vs LDR RADIATION

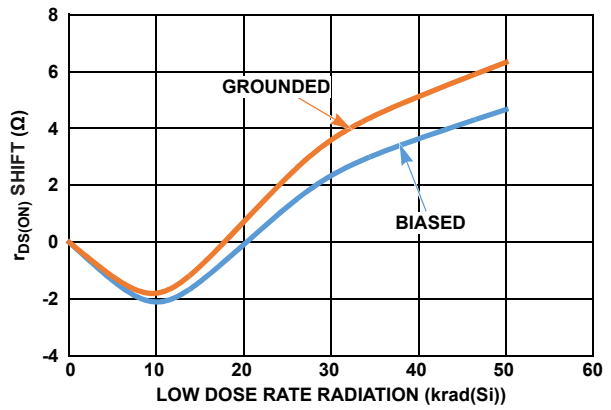


FIGURE 73. $r_{DS(ON)}$ SHIFT (V_{IN} = -5V) vs LDR RADIATION

Post Low Dose Rate Radiation Characteristics (V± = ±12V)

Unless otherwise specified, V± = ±12V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits, nor are they guaranteed. **(Continued)**

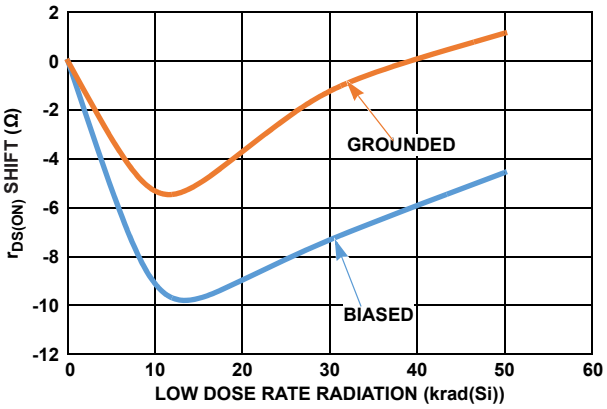


FIGURE 74. $r_{DS(ON)}$ SHIFT (V_{IN} = V^-) vs LDR RADIATION

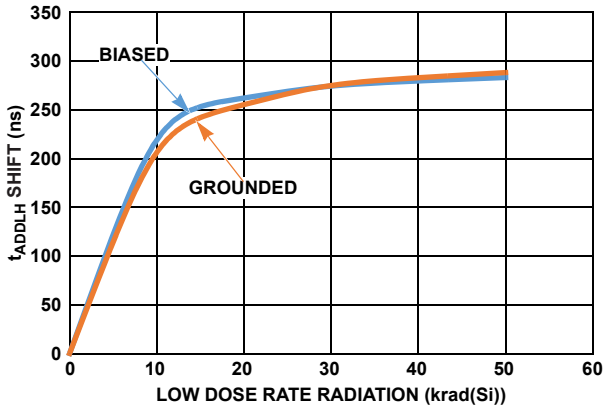


FIGURE 75. t_{ADD} SHIFT (LOW TO HIGH) vs LDR RADIATION

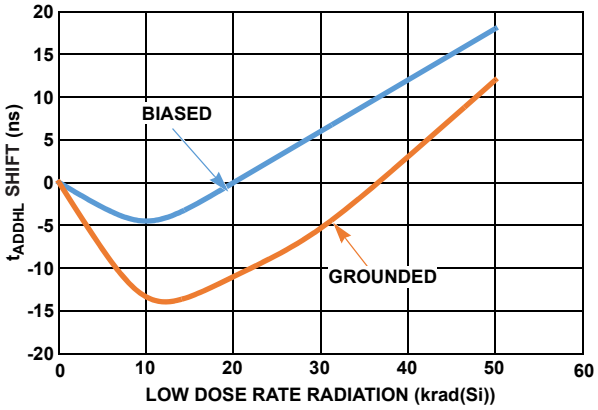


FIGURE 76. t_{ADD} SHIFT (HIGH TO LOW) vs LDR RADIATION

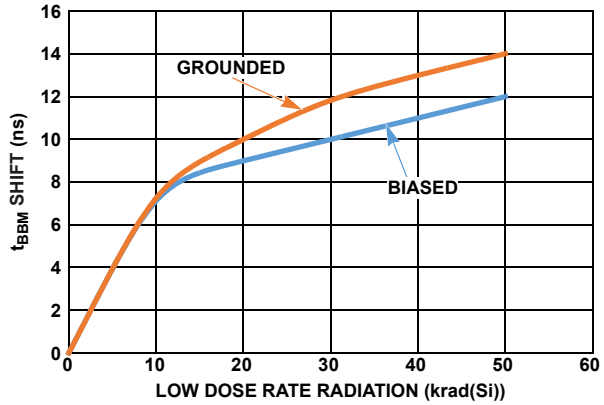


FIGURE 77. t_{BBM} SHIFT vs LDR RADIATION

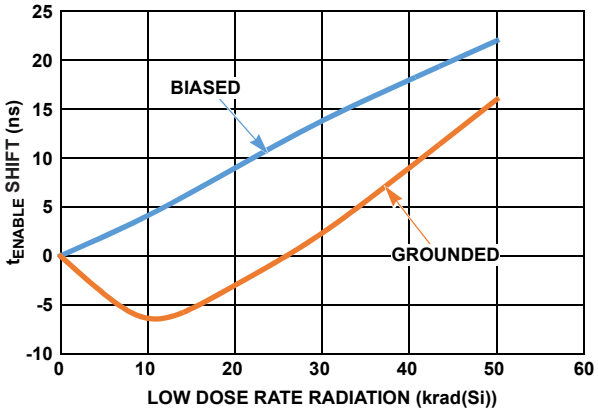


FIGURE 78. t_{ENABLE} SHIFT vs LDR RADIATION

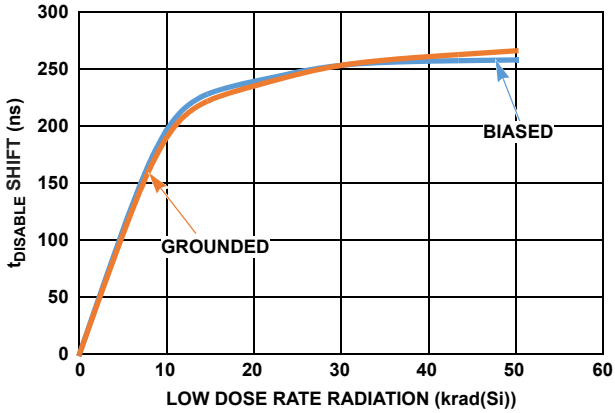


FIGURE 79. $t_{DISABLE}$ SHIFT vs LDR RADIATION

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+, V^-, and VREF; however, it is recommended that all supplies power up relatively close to each other.

Overvoltage Protection

The ISL71841SEH has overvoltage protection on both the input and the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition (3V to 4V past the rail), the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71841SEH. The range for VREF is between 4.5V and 5.5V with a nominal voltage of 5V. The address pins and enable are compared against roughly 30% of V_{REF} voltage (refer to Figure 80). With 5.0V on V_{REF}, the switching point is set to around 1.4V. This switching point allows for both 5V and 3.3V logic control.

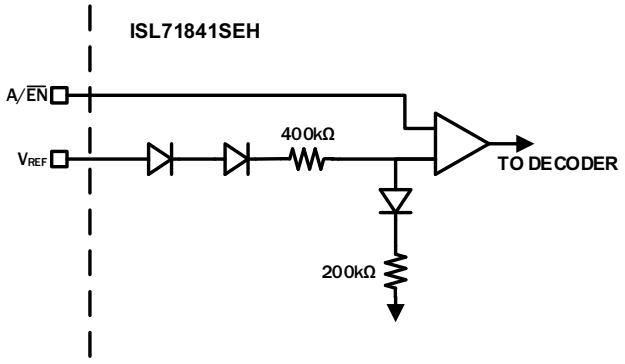


FIGURE 80. SIMPLIFIED V_{REF} CIRCUITRY

Considerations for Redundant Applications

When using the ISL71841SEH in a cold sparing application, it is recommended to keep the ground pin connected to system ground at all times. All supply pins (V+, V-, and VREF) should either be grounded or floating together.

If the supply pins are floating, it is recommended to place a high value bleed resistor (~1MΩ) in parallel with the decoupling capacitors on each supply pin to ensure that the supply voltage is discharged in a predictable manner. Figures 81 and 82 illustrate the recommended cold sparing setup for both shorted or floating supplies.

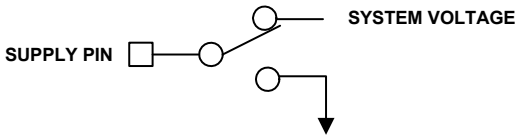


FIGURE 81. COLD SPARING SETUP WITH SUPPLIES SHORTED

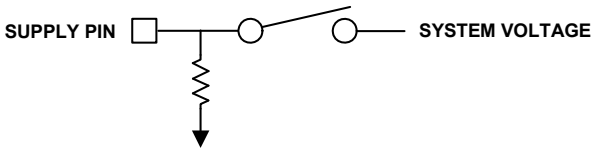


FIGURE 82. COLD SPARING SETUP WITH SUPPLIES FLOATING

ISL71841SEH vs ISL71840SEH

The ISL71840SEH, a 16-channel version of the ISL71841SEH, is available in a 28 Ld CDFP. The parts' performance specifications are very similar. Apart from the apparent increase in channel density, the ISL71841SEH has slightly higher output leakage compared to the ISL71840SEH because it has more channels connected to the output. The supply current for the ISL71841SEH is also slightly higher compared to the ISL71840SEH. Refer to Table 1 on page 3 for a comparison of the two devices.

Die Characteristics

Die Dimensions

5000µm x 4080µm (197 mils x 161 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: 12kÅ Silicon Nitride on 3kÅ Oxide

TOP METALLIZATION

Type: 300Å TiN on 2.8µm AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

$1.6x10^5$ A/cm^2

TRANSISTOR COUNT

10752

Weight of Packaged Device

48 Ld CQFP: 1.54 grams (typical)
44 Ld CLCC: 2.02 grams (typical)

Lid Characteristics

Finish: Gold
Potential: Grounded, tied to package GND pin
In 48 Ld CQFP: Pin 29
In 44 Ld CLCC: Pin 26

Metalization Mask Layout

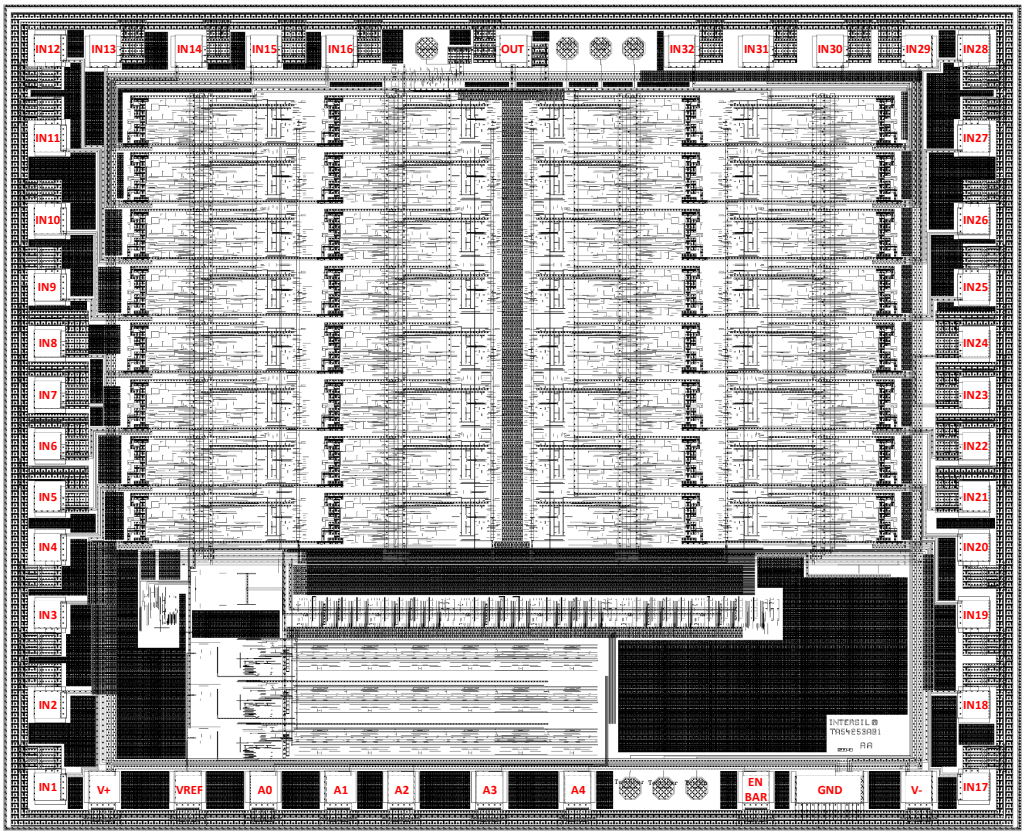


TABLE 3. ISL71840SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN28	P42	122	122	2232.2	1776.05
2	IN29	P43	122	122	1956.5	1772.2
3	IN30	P44	122	122	1529.15	1772.2
4	IN31	P45	122	122	1171.85	1772.2
5	IN32	P46	122	122	816.35	1772.2
9	OUT	P1	122	122	7.2	1773.25
11	IN16	P3	122	122.05	-829.525	1772.2
12	IN15	P4	122	122	-1192.2	1772.2
13	IN14	P5	122	122	-1553.65	1772.2
14	IN13	P6	122	122	-1965.35	1772.2
15	IN12	P7	122	122	-2232.2	1775.55
16	IN11	P8	122	122	-2232.2	1343.55
17	IN10	P9	122	122	-2232.2	944.5
18	IN9	P10	122	122	-2232.2	626.15
19	IN8	P11	122	122	-2232.2	354.4
20	IN7	P12	122	122.05	-2232.2	108.275
21	IN6	P13	122	122	-2232.2	-138.75
22	IN5	P14	122	122	-2232.2	-391.8
23	IN4	P15	122	122	-2232.2	-622.95
24	IN3	P16	122	122	-2232.2	-948.55
25	IN2	P17	122	122	-2232.2	-1379.95
26	IN1	P18	122	122	-2232.2	-1775.95
27	V^+	P19	122	122	-1970.75	-1789.2
28	VREF	P20	122	122	-1558.65	-1789.2
29	A0	P21	122	122	-1196.8	-1789.2
30	A1	P22	122	122	-835.6	-1789.2
31	A2	P23	122	122	-533	-1789.2
32	A3	P24	122	122	-109.45	-1789.2
33	A4	P25	122	122	313.95	-1789.2
37	EN_B	P28	122	122	1171.9	-1789.2
38	GND	P29, P29	320	122	1525.85	-1789.1
39	V^-	P30	122	122	1955.7	-1789.2
40	IN17	P31	122	122	2232.2	-1774.95
41	IN18	P32	122	122	2232.2	-1380.25
42	IN19	P33	122	122	2232.2	-947.45
43	IN20	P34	122	122	2232.2	-624.75
44	IN21	P35	122	122	2232.2	-391.95
45	IN22	P36	122	122	2232.2	-139.05
46	IN23	P37	122	122.05	2232.2	107.525
47	IN24	P38	122	122	2232.2	353.6
48	IN25	P39	122	122	2232.2	626.9
49	IN26	P40	122	122	2232.2	943.9
50	IN27	P41	122	122	2232.2	1342.7

NOTE: Origin of coordinates is the center of the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 10, 2023	8.00	Removed Related Literature section. Updated Ordering Information table and notes. In ABS MAX RATINGS Section on page 5 changed Digital Input Voltage Range ($\overline{EN}$, Ax) from GND to V+, to GND - 0.3V to +16.5V. Updates to the Electrical Specifications (±15V) table are as follows: • On page 5, for parameters Channel On-Resistance, r_{ON} Match Between Channels, and ON-Resistance Flatness, added $V_{\overline{EN}}$ = 0V to the Test Conditions. • On page 6, for parameter Switch Off Leakage with Device Powered OFF changed it to Switch Off Leakage with Device Powered OPEN. • On page 6, added new parameter Switch On Leakage Current into the Drain (Overvoltage) specification. • On page 6, for parameter Switch On Leakage Current into the Source (Overvoltage), updated the limits values and units to µA. • On page 6, for parameter Switch Off Leakage Current into the Source (Overvoltage), added a new T_A = -55°C" specification. • On page 7, for parameter Switch On Leakage Current into the Source/Drain, added $V_{\overline{EN}}$ = 0V to the Test Conditions. • Changed the I+, I- Quiescent & Standby Supply Current parameters to VREF = 5.5V, VIN = 0V, VA = 0.8V. • Changed parameter nomenclature for Supply Current Into V_{REF} to Quiescent Supply Current Into V_{REF}. • Added new specification parameter Standby Current Into V_{REF}. Updates to the Electrical Specifications (±12V) table on page 8 are as follows: • For parameters Channel On-Resistance, r_{ON} Match Between Channels, and ON-Resistance Flatness, added $V_{\overline{EN}}$ = 0V to the Test Conditions. • Changed the I+, I- Quiescent & Standby Supply Current parameters to VREF = 5.5V, VIN = 0V, VA = 0.8V. • Changed parameter nomenclature for Supply Current Into V_{REF} to Quiescent Supply Current Into V_{REF}. • Added new specification parameter Standby Current Into V_{REF}.
Feb 23, 2018	7.00	Added "Considerations for Redundant Applications" on page 24. Removed About Intersil and updated disclaimer.
Nov 30, 2017	6.00	Added ESD circuit images in Figure 3 on page 4.
Jun 22, 2017	5.00	Ordering Information table on page 3, added Notes 5 and 6. In "Pin Descriptions" on page 4, added pin 28 to NC for the CLCC package.
Jun 3, 2016	4.00	Updated Ordering information table on page 3 by updating first column and updating Note 4. Updated bolding in Electrical Specification table and added test conditions to the Break-Before-Make Delay, Enable Turn-On Time and Disable Turn-Off Time specifications. Changed from "V_S" to "V±" in the titles of the Typical Performance, Post High and Post Low Dose Rate Radiation Characteristics curve tables. Changed units from mA to µA for Figures 32, 33, 34, 44, 45, 46, 56, 57, 58, 68, 69, 70.
Apr 15, 2016	3.00	Added ISL71841SEHVL and ISL71841SEHL/PROTO details to the Ordering Information table on page 3 and added the applicable packaging information throughout datasheet. Updated the heading for the Low Dose Rate Radiation Characteristics (Vs = ±15V) table on page 20 in third sentence changed from "high" to "low". Updated the heading for the Low Dose Rate Radiation Characteristics (Vs = ±12V) table on page 22 in third sentence changed from "high" to "low".
Dec 11, 2015	2.00	Updated Y-axis labels on Figures 32 through 79. Updated crosstalk and off Isolation MIN in Electrical Spec table on page 8 from -75 to 75 (off isolation) and -47 to 47 (crosstalk). Changed all instances of V_{DD} to V^+ and V_{SS} to V^-.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
Sep 29, 2015	1.00	Updated Related Literature on page 1. Updated testing information for ESD tolerances, HBM, CDM and MM in “Absolute Maximum Ratings” on page 5. From: Human Body Model (Tested per MIL-PRF-883 3015.7) Charged Device Model (Tested per MIL-PRF-883 3015.7) Machine Model (Tested per MIL-PRF-883 3015.7) To: Human Body Model (Tested per MIL-STD-883 TM 3015) Charged Device Model (Tested per JESD22-C101D) Machine Model (Tested per JESD22-A115-A) Updated crosstalk and off Isolation MIN in Electrical Spec table on page 8 from -90 to -75 (off isolation) and -47 (crosstalk). Added Figures 27, 29 and 31 and updated the figure titles for Figures 28 and 30 on page 14. Updated top metalization thickness and composition in “Die Characteristics” on page 25. Added Table 3 on page 26.
Jun 11, 2015	0.00	Initial release

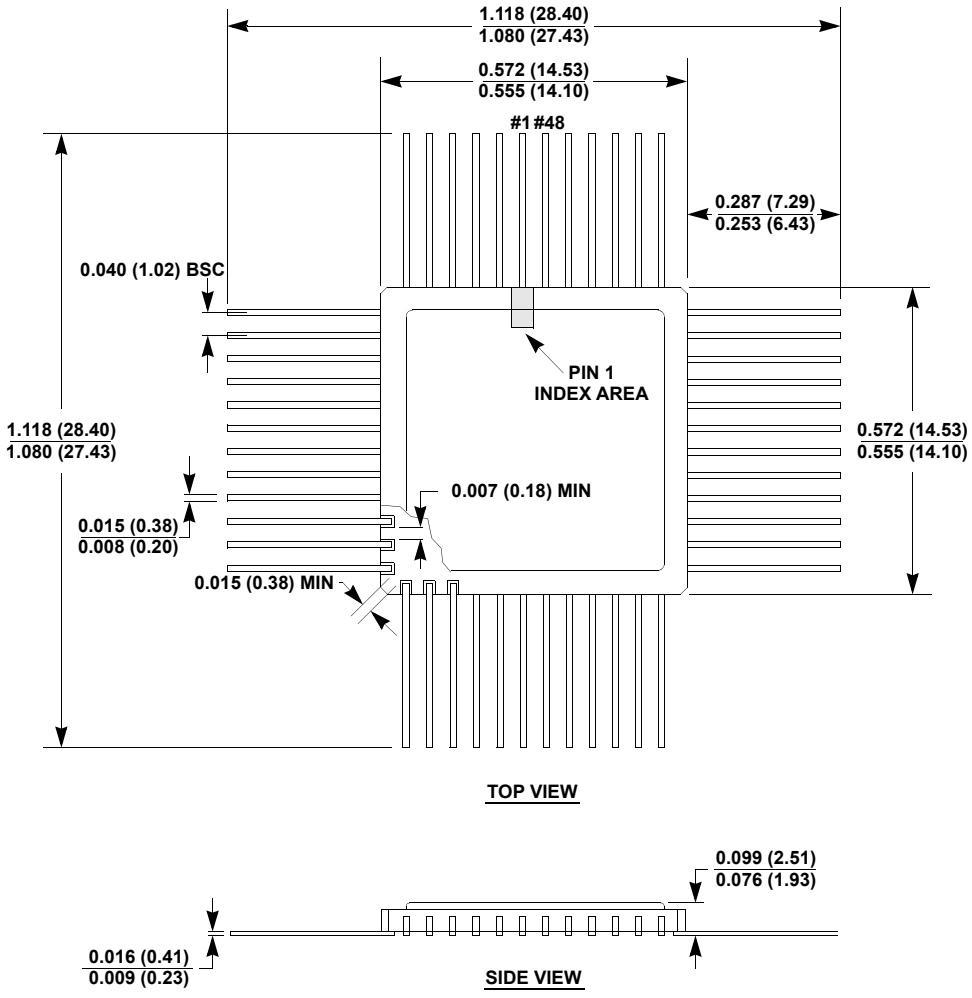
Package Outline Drawings

For the most recent package outline drawing, see R48.A.

R48.A

48 CERAMIC QUAD FLATPACK PACKAGE (CQFP)

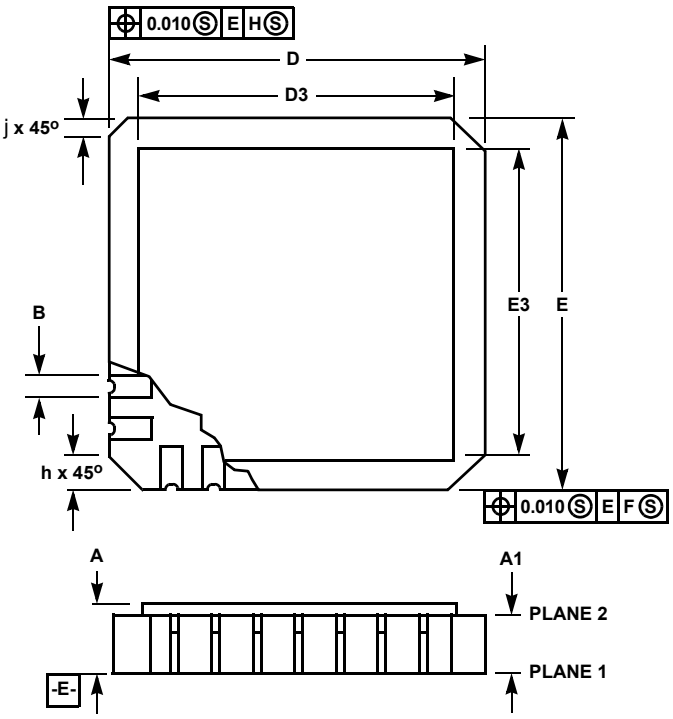
Rev 3, 10/12

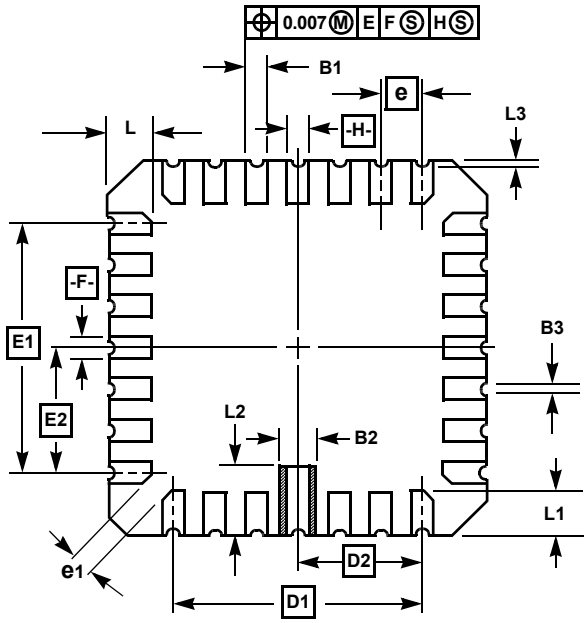


NOTE:

1. **All dimensions are in inches (millimeters).**

For the most recent package outline drawing, see J44.A.





J44.A MIL-STD-1835 CQCC1-N44 (C-5)
44 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.120	1.63	3.05	6, 7
A1	0.054	0.088	1.37	2.24	-
B	0.033	0.039	0.84	0.99	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.662	16.26	16.81	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	-	0.662	-	16.81	2
E	0.640	0.662	16.26	16.81	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	-	0.662	-	16.81	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

Rev. 0 5/18/94

NOTES:

12. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
13. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
14. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
15. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
16. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
17. Chip carriers shall be constructed of a minimum of two ceramic layers.
18. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
19. Dimensioning and tolerancing per ANSI Y14.5M-1982.
20. Controlling dimension: INCH.

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